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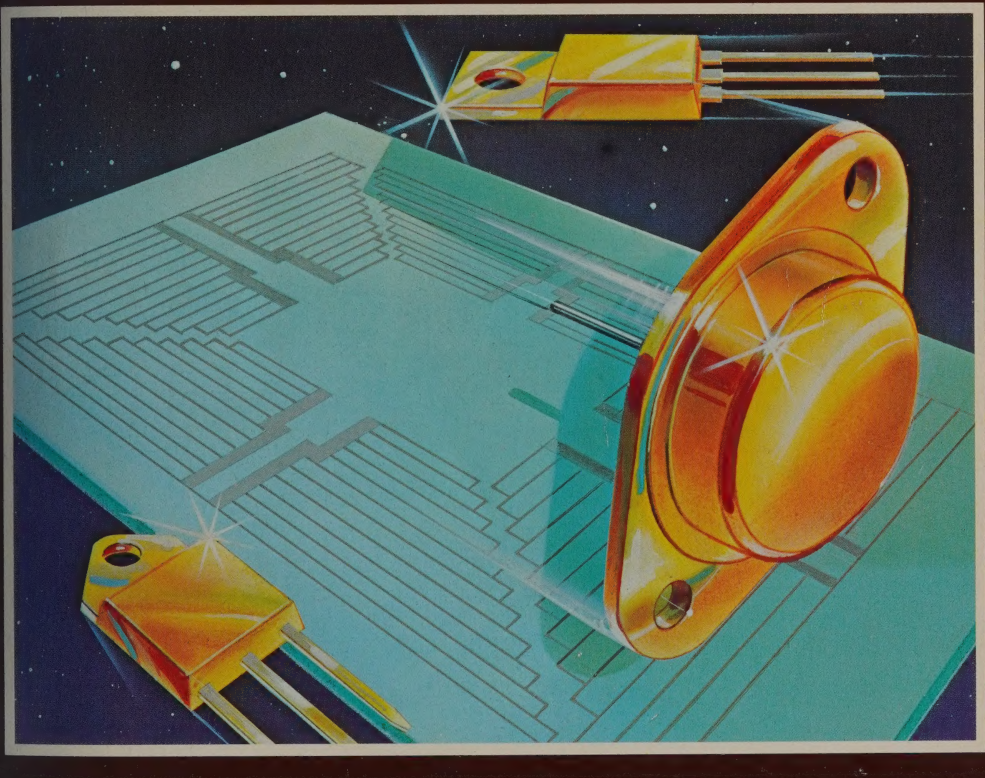
MOTOROLA INC.



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MOTOROLA

POWER DEVICE DATA

Prepared by
Technical Information Center

This book presents technical data for Motorola's broad line of silicon power transistors, thyristors, and triggers. Complete specifications are provided in the form of data sheets and accompanying selection guides provide a quick comparison of characteristics to simplify the task of choosing the best device for a circuit. In addition, separate selector guides for power MOSFETs, power rectifiers, as well as voltage regulator and reference diodes offer a quick technical overview of Motorola's power discrete device lines for power supply and power circuit designs.

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Fourth Edition

Printed in U.S.A.

MOTOROLA POWER TRANSISTORS IN BRIEF

Wide Range of Transistor Specifications

Bipolar transistors, NPNs and PNPs, single and multiple (Darlington) transistor structures, metal and plastic packages, Motorola's inventory of more than 1100 standard (off-the-shelf) power transistors covers the widest range of specifications for virtually every potential applications requirement.

Current Range — 0.5 to 300 Amperes
Voltage Range — 25 to 1500 Volts
Power Dissipation Range — 5 to 500 Watts.

Darlingtons

Consisting of two transistors, up to two resistors, and (up to) two diodes on a single chip, Darlington transistors achieve gain figures up to 20,000 in a single package. Rapid line expansion, and the resulting widespread implementation make Motorola Darlingtons highly cost-effective in a fast growing number of applications.

Chips, Chips, Chips!

Designing a hybrid? Motorola's total repertoire of power transistors is available . . UNENCAPSULATED: Check with your Motorola Sales representative for price and delivery.

Specials Unlimited

Need a unique transistor with specifications not available off-the-shelf? Chances are Motorola can produce it quickly and inexpensively. Routine use of four major power processes and more than two decades of experience in the pioneering of new structures and geometries provide the insight and capability to meet any required specification within the limits of today's technology.

POWER TRANSISTORS

Index and Cross Reference

The table on the subsequent pages contains an Alphanumeric index of Silicon power transistors currently manufactured and available to the industry.

The column headed "Similar" lists units with characteristics that might represent suitable replacements. In cases where such a replacement is contemplated, the Motorola device data sheet should be carefully compared with one for the device being replaced to determine any variations that could affect circuit performance.

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*Consult factory if a direct replacement is necessary.
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2N6051JTXV	2N6051JTXV		1-50
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2N6052JAN	2N6052JAN		1-50
2N6052JTX	2N6052JTX		1-50
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2N6277JTX	2N6277JTX		1-50
2N6277JTXV	2N6277JTXV		1-50
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2N6283JTX	2N6283JTX		1-50
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2N6284JTX	2N6284JTX		1-50
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MJ4381		MJE13005	1-881
MJ4400		MJE13004	1-881
MJ4401		MJE13005	1-881
MJ4502	MJ4502		1-463
MJ4645	MJ4645		1-465
MJ4646	MJ4646		1-465
MJ4647	MJ4647		1-465
MJ6502	MJ6502		1-467
MJ6503	MJ6503		1-467
MJ6700	MJ6700		1-473
MJ8100	MJ8100		1-475
MJ8500	MJ8500		1-477
MJ8501	MJ8501		1-477
MJ8502	MJ8502		1-483
MJ8503	MJ8503		1-483
MJ8504	MJ8504		1-489
MJ8505	MJ8505		1-489
MJ10000	MJ10000		1-495
MJ10001	MJ10001		1-495
MJ10002	MJ10002		1-501
MJ10003	MJ10003		1-501
MJ10004	MJ10004		1-507
MJ10005	MJ10005		1-507
MJ10006	MJ10006		1-513
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MJ10009	MJ10009		1-519
MJ10011	MJ10011		1-525
MJ10012	MJ10012		1-527
MJ10013	MJ10013		1-531
MJ10014	MJ10014		1-531
MJ10015	MJ10015		1-537
MJ10016	MJ10016		1-537
MJ10020	MJ10020		1-542
MJ10021	MJ10021		1-542
MJ10022	MJ10022		1-548
MJ10023	MJ10023		1-548
MJ10024	MJ10024		1-554
MJ10025	MJ10025		1-554
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MJ10052	MJ10052		1-596
MJ10100	MJ10100		1-604
MJ10101	MJ10101		1-612
MJ10102	MJ10102		1-612
MJ10200	MJ10200		1-620
MJ10201	MJ10201		1-628
MJ10202	MJ10202		1-628
MJ11011	MJ11011		1-636
MJ11012	MJ11012		1-636
MJ11013	MJ11013		1-636
MJ11014	MJ11014		1-636
MJ11015	MJ11015		1-636
MJ11016	MJ11016		1-636
MJ11017	MJ11017		1-638
MJ11018	MJ11018		1-638
MJ11019	MJ11019		1-638
MJ11020	MJ11020		1-638
MJ11021	MJ11021		1-638
MJ11022	MJ11022		1-638
MJ11028	MJ11028		1-642
MJ11029	MJ11029		1-642
MJ11030	MJ11030		1-642
MJ11031	MJ11031		1-642
MJ11032	MJ11032		1-642
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MJ12004	MJ12004		1-651
MJ12005	MJ12005		1-657
MJ12010	MJ12010		1-659
MJ12020	MJ12020		1-661
MJ12021	MJ12021		1-661
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MJ13014	MJ13014		1-671
MJ13015	MJ13015		1-671
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MJ13019		MJ13331	1-701
MJ13070	MJ13070		1-677
MJ13071	MJ13071		1-677
MJ13080	MJ13080		1-683
MJ13081	MJ13081		1-683
MJ13090	MJ13090		1-689
MJ13091	MJ13091		1-689
MJ13100	MJ13100		1-695
MJ13101	MJ13101		1-695
MJ13330	MJ13330		1-701
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MJ15011	MJ15011		1-723
MJ15012	MJ15012		1-723
MJ15015	MJ15015		1-65
MJ15016	MJ15016		1-65
MJ15022	MJ15022		1-725
MJ15023	MJ15023		1-728
MJ15024	MJ15024		1-725
MJ15025	MJ15025		1-728
MJ15026	MJ15026		1-731
MJ15027	MJ15027		1-731
MJ16002	MJ16002		1-735
MJ16002A	MJ16002A		1-743
MJ16004	MJ16004		1-735
MJ16006	MJ16006		1-750
MJ16006A	MJ16006A		1-758
MJ16008	MJ16008		1-750
MJ16010	MJ16010		1-765
MJ16010A	MJ16010A		1-773
MJ16012	MJ16012		1-765
MJ16014	MJ16014		1-781
MJ16016	MJ16016		1-781
MJ16018	MJ16018		1-789
MJE29		TIP29*	1-955
MJE29A		TIP29A*	1-955
MJE29B		TIP29B*	1-955
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MJE30		TIP30*	1-955
MJE30A		TIP30A*	1-955
MJE30B		TIP30B*	1-955
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MJE31		TIP31*	1-957
MJE31A		TIP31A*	1-957
MJE31B		TIP31B*	1-957
MJE31C		TIP31C*	1-957
MJE32		TIP32*	1-957
MJE32A		TIP32A*	1-957
MJE32B		TIP32B*	1-957
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MJE104		2N5976	1-207
MJE105	MJE105		1-795
MJE105K		TIP42A	1-967
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MJE171	MJE171		1-797
MJE172	MJE172		1-797
MJE180	MJE180		1-797
MJE181	MJE181		1-797
MJE182	MJE182		1-797
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MJE204		2N5979	1-210
MJE205	MJE205		1-805
MJE205K		TIP41A	1-967
MJE210	MJE210		1-801
MJE220		MJE181*	1-797
MJE221		MJE181*	1-797
MJE222		MJE181*	1-797
MJE223		MJE182*	1-797
MJE224		MJE182*	1-797
MJE225		MJE182*	1-797
MJE230		MJE171*	1-797
MJE231		MJE171*	1-797
MJE232		MJE171*	1-797
MJE233		MJE172*	1-797
MJE234		MJE172*	1-797
MJE235		MJE172*	1-797
MJE240	MJE240		1-807
MJE241	MJE241		1-807
MJE242	MJE242		1-807
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MJE244	MJE244		1-807
MJE250	MJE250		1-807
MJE251	MJE251		1-807
MJE252	MJE252		1-807
MJE253	MJE253		1-807
MJE254	MJE254		1-807
MJE270	MJE270		1-42
MJE271	MJE271		1-42
MJE340	MJE340		1-811
MJE340K		TIP48	1-971
MJE341	MJE341		1-813
MJE341K		TIP47	1-971
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MJE484		2N5192	1-146
MJE488		2N5191	1-146
MJE492		2N5193	1-150
MJE493		2N5194	1-150
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MJE520	MJE520		1-821
MJE520K		TIP31	1-957
MJE521	MJE521		1-42
MJE521K		TIP31	1-957
MJE700	MJE700		1-823
MJE700T	MJE700T		1-823
MJE701	MJE701		1-823
MJE701T	MJE701T		1-823
MJE702	MJE702		1-823
MJE702T	MJE702T		1-823
MJE703	MJE703		1-823
MJE703T	MJE703T		1-823
MJE710	MJE710		1-42
MJE711	MJE711		1-42
MJE712	MJE712		1-42
MJE720	MJE720		1-42
MJE721	MJE721		1-42
MJE722	MJE722		1-42
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MJE800T	MJE800T		1-823
MJE801	MJE801		1-823
MJE801T	MJE801T		1-823
MJE802	MJE802		1-823
MJE802T	MJE802T		1-823
MJE803	MJE803		1-823
MJE803T	MJE803T		1-823
MJE1090	MJE1090		1-43
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MJE1092	MJE1092		1-43
MJE1093	MJE1093		1-43
MJE1100	MJE1100		1-43
MJE1101	MJE1101		1-43
MJE1102	MJE1102		1-43
MJE1103	MJE1103		1-43
MJE1290	MJE1290		1-827
MJE1291	MJE1291		1-827
MJE1660	MJE1660		1-827
MJE1661	MJE1661		1-827
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MJE2481		TIP31A	1-957
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MJE2490		TIP32	1-241
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MJE2521		TIP31A	1-957
MJE2522		TIP31	1-957
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MJE2801	MJE2801		1-831
MJE2801K		MJE2801T	1-831
MJE2801T	MJE2801T		1-831
MJE2901	MJE2901		1-831
MJE2901K		MJE2901T	1-831
MJE2901T	MJE2901T		1-831
MJE2955	MJE2955		1-833
MJE2955K		MJE2955T	1-833
MJE2955T	MJE2955T		1-833
MJE3055	MJE3055		1-833
MJE3055K		MJE3055T	1-833
MJE3055T	MJE3055T		1-833
MJE3300	MJE3300		1-835
MJE3301	MJE3301		1-835
MJE3302	MJE3302		1-835
MJE3310	MJE3310		1-835
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MJE4340	MJE4340		1-839
MJE4341	MJE4341		1-839
MJE4342	MJE4342		1-839
MJE4343	MJE4343		1-839
MJE4350	MJE4350		1-839
MJE4351	MJE4351		1-839
MJE4352	MJE4352		1-839
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MJE5741	MJE5741		1-851
MJE5742	MJE5742		1-851
MJE5850	MJE5850		1-855
MJE5851	MJE5851		1-855
MJE5852	MJE5852		1-855
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SDT13302		2N6547	1-319
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SVT6061		MJ10004	1-507
SVT6062		MJ10005	1-507
SVT6251		MJ10006	1-513
SVT6252		MJ10006	1-513
SVT6253		MJ10007	1-513
SVT6546		MJ13090	1-689
SVT6547		MJ13090	1-689
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SVT7521		2N6543	1-309
SVT7522		MJ13335	1-707
SVT7523		2N6308	1-274
SVT7524		2N6543	1-309
SVT7525		MJ13334	1-707
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*Consult factory if a direct replacement is necessary.
**To be introduced. Contact factory for Data Sheet.

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*Consult factory if a direct replacement is necessary.
**To be introduced. Contact factory for Data Sheet.

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*Consult factory if a direct replacement is necessary.
**To be introduced. Contact factory for Data Sheet.

POWER TRANSISTORS
Selector Guide

The selector guides on the subsequent pages offer a quick "first-selection" capability for devices that fit specific applications categories.

Because designers have different application prerequisite, the devices are categorized in three ways:

1. by package
2. by major product category
3. by major applications

In each case, pertinent electrical characteristics are supplied to permit rapid comparison of potentially suitable devices.

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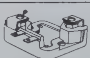
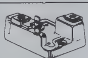
SELECTION BY PACKAGE

Motorola power transistors are available in a wide variety of metal and plastic packages to match thermal, electrical and cost requirements. The following table compares the basic packages from the standpoint of current, voltage and power capabilities. The devices available in the various packages are tabulated on the succeeding pages.

Package		I_C Range (Amps)	V_{CE} Range (Volts)	P_D (Watts)	Page
	TO-204AA (TO-3) Case 1 Case 11	2.5-60	40-1500	36-300	35
	TO-204AE Case 197	2.5-60	40-1500	36-300	35
	TO-205AA (TO-5) Case 31	3.0	40-800	6.0	38
	TO-205AD (TO-39) Case 79	0.5-5.0	40-400	5-10	39
	TO-210AA (TO-59) Case 160	7.0-10	60-100	60	40
	TO-213AA (TO-66) Case 80	1-10	40-325	20-90	41
	TO-225AA (TO-126) Case 77	0.3-5.0	25-400	12.5-40	42
	TO-225AB Case 90	5-15	40-100	65-100	43
	Case 152	0.5-2.0	30-300	10	43
	TO-202AC Case 306	0.1-3.0	30-350	6.25-12.5	44
	TO-218AC Case 340	5.0-25	40-800	80-150	45
	TO-220AB Case 221A	0.5-15	30-800	15-125	46
	MO-040AA CASE 346	50-200	200-850	500	48
	CASE 353	25-100	250-850	250	48

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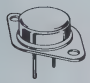
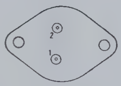
Switchmode Power Transistors (<200 Volts) 54

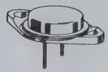
TO-204AA (Formerly TO-3)/TO-204AE (Type)



CASE 11-01, 11-3 — 40 mil pins
CASE 1-04, 1-05 — 40 mil pins
MODIFIED TO-3

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR





CASE 197-01 — 60 mil pins

I_C Cont	$V_{CEO(sus)}$	Device Type		h_{FE}	@ I_C	Resistive Switching			f_T MHz	P_D (Case) Watts
						t_s µs	t_f µs	@ I_C		
Amps Max	Volts Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
2.5	700	MJ8500		7.5 min	0.5	4	2	1		125
	800	MJ8501		7.5 min	0 5	4	2	1		125
	1300*	BU204		2 min	2		0.75 typ	2	4 typ	36
	1400*	MJ205					1	2		110
	1500*	BU205 MJ12002		2 min 1.11 min	 2	2	0.75 typ 1	2 2	4 typ 4 typ	36 75
3	250	2N5838		8/40	3	1 typ	0.4 typ	3	5	100
	275	2N5839		10/50	2	1 typ	0.4 typ	3	5	100
	350	2N5840		10/50	2	1 typ	0 4 typ	3	5	100
3.5	325	2N3902		30/90	1	1 2 typ	0.1 typ	1	2.8	100
4	1500*	MJ12003		2.5 min	3		1	3		100
5	120	2N4347		15/60	2					100
	200	MJ410		30/90	1				2 5	100
	250	MJ3029		30 min	0.4		1	3		125
	300	MJ411 2N6542		30/90 7/35	1 3	 4	 0 8	 3	2 5. 6	100 100
	325	MJ3030		3.75 min	3		1	3		125
	400	2N6543 MJ13070		7/35 8 min	3 3	4 1.5	0 8 0 5	3 3	6	100 125
	450	MJ13071 MJ16002 MJ16004 2N6834		8 min 5 min 7 min 10/30	3 5 5 3	1.5 3 2.7 2 7	0.5 0.3 0.35 0.35	3 3 3 3	 15	125 125 125 125
	500	MJ16002A		5.0 min	5.0	3.0	0 3	3.0		125
	700	MJ8502		7.5 min	1	4	2	2.5		150
	800	MJ8503		7.5 min	1	4	2	2.5		150
	850*	MJ12020		5.0 min	5 0		0 13 typ	3 0	15	125
	1300*	BU207		2.25 min	4 5		0.6 typ	4.5	4 typ	60
	1500*	BU208 BU208D† MJ12004		2.25 min 2.25 min 2.5 min	4 5 4.5 4 5		0.6 typ 0.6 typ 1	4 5 4 5 4 5	4 typ 4 typ 4	60 60 100
6	100	2N5758	2N6226	25/100	3	0.7 typ	0.5 typ	3	1	150
	120	2N5759	2N6227	20/80	3	0 7 typ	0.5 typ	3	1	150
	140	2N5760	2N6228	15/60	3	0.7 typ	0.5 typ	3	1	150
	250	MJ15011	MJ15012	20/100	2					200
7.0	300	MJ3041		250 min	2.5					175
	350	MJ3042		250 min	2 5					175

(continued)

$|h_{fe}|$ @ 1 MHz
*$V_{(BR)CEX}$ or $V_{(BR)CES}$
†D Suffix on this device signifies internal C-E Diode

1.2

TO-204AA (FORMERLY TO-3)/TO-204AE (Type) (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
7.5	60	2N3445		20/60	5	2	0.35	5	10	115
		2N3447		40/120	5	2	0.35	5	10	115
	80	2N3446		20/60	5	2	0.35	5	10	115
		2N3448		40/120	5	2	0.35	5	10	115
8	60	MJ1000	MJ900	1k min	3					90
		2N6055	2N6053	750/18k	4	1.5 typ	1.5 typ	4	4#	100
	80	MJ1001	MJ901	1k min	3					90
		2N6056	2N6054	750/18k	4	1.5 typ	1.5 typ	4	4#	100
	120	MJ4247	MJ4237	40 min	3	0.4 typ	0.18 typ	5	20	90
	150	MJ4248	MJ4238	40 min	3	0.4 typ	0.18 typ	5	20	90
	250	2N6306		15/75	3	1.6	0.4	3	5	125
			MJ6502	15 min	2	2	0.5	4		125
	300	2N6307		15/75	3	1.6	0.4	3	5	125
		2N6544		7/35	5	4	1	5	6	125
	350	2N6308		12/60	3	1.6	0.4	5	5	125
	400	2N6545		7/35	5	4	1	5	6	125
			MJ6503	15 min	2	2	0.5	4		125
		MJ13080		8 min	5	1.5	0.5	5		150
	450	MJ13081		8 min	5	1.5	0.5	5		150
		MJ16006		5 min	8	2.5	0.25	5		150
		MJ16008		7 min	8	2.2	0.25	5		150
		2N6835		10/30	5	2.5	0.25	5	10	150
	500	MJ16006A		5.0 min	8.0	3.0	0.4	5.0		150
	850*	MJ12021		5.0 min	8.0		0.1 typ	5.0		150
	1400*	MJ10011		20 min	4		1	4		80
	1500*	MJ12005		5 min	5		1	5		100
10	40	2N6383	2N6648	1k/20k	5				20#	100
	60	2N3713	2N3789	15 min	3	0.3 typ	0.4 typ	5	4	150
		2N3715	2N3791	30 min	3	0.3 typ	0.4 typ	5	4	150
		2N5877	2N5875	20/100	4	1	0.8	4	4	150
		2N6384	2N6649	1k/20k	5				20#	100
		MJ3000	MJ2500	1k min	5					150
	80	2N3714	2N3790	15 min	3	0.3 typ	0.4 typ	5	4	150
		2N3716	2N3792	30 min	3	0.3 typ	0.4 typ	5	4	150
		2N5878	2N5876	20/100	4	1	0.8	4	4	150
		2N6385	2N6650	1k/20k	5				20#	100
		MJ3001	MJ2501	1k min	5					150
	100	2N5632	2N6229	25/100	5	0.9 typ	0.9 typ	5	1	150
	120	2N5633	2N6230	20/80	5	0.9 typ	0.9 typ	5	1	150
	140	2N5634	2N6231	15/60	5	0.9 typ	0.9 typ	5	1	150
		2N3442		20/70	4					117
	250	MJ15011	MJ15012	20/100	2					200
	325	MJ413		20/80	0.5				2.5	125
		MJ423		30/90	1				2.5	125
		MJ431		15/35	2.5				2 5	125
	350	MJ13014		8/20	5	2	0.5	5		150
		MJ10002		3/300	5	2.5	1	5	10#	150
		MJ10006		30/300	5	1.5	0.5	5	10#	150
	400	MJ10003		30/300	5	2.5	1	5	10#	150
		MJ10007		30/300	5	1.5	0.5	5	10#	150
		MJ10012		100/2k	6	15	15	6		175
		MJ13015		8/20	5	2	0.5	5		150
	450	SDT13304		10/40	5	1.6 typ	0.35 typ	5	15 typ	125*
	500	SDT13305		10/40	5	1.6 typ	0.35 typ	5	15 typ	125*
	550	MJ10013		10/250	10	2.5	0.8	10		175
	600	MJ10014		10/250	10	2.5	0.8	10		175
	700	MJ8504		7.5 min	1.5	4	2	5		175
	800	MJ8505		7.5 min	1.5	4	2	5		175
		MJ16018		7.0 min	5.0	2.0 typ	0.9 typ	5.0		150
	950*	MJ12010		4.2 min	5		1	5		100
12	40	2N6569	2N6594	15/200	4	5	1.5	2	1.5 to 15	100
	60	2N6057	2N6050	750/18k	6	1.6 typ	1.5 typ	6	4#	150
	80	2N6058	2N6051	750/18k	6	1.6 typ	1.5 typ	6	4#	150
	100	2N6059	2N6052	750/18k	6	1.6 typ	1.5 typ	6	4#	150
15	60	2N3055	MJ2955	20/70	4	0.7 typ	0.3 typ	4	2.5	115
		2N3055A	MJ2955A	20/70	4				0.8	115
		2N6576		2k/20k	4	2	7	10	10-200#	120
		2N5881	2N5879	20/100	6	1	0.8	6	4	160

*$V_{(BR)CEX}$ # $|h_{fe}|$ @ 1 MHz

(continued)

TO-204AA (FORMERLY TO-3)/TO-204AE (Type) (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
15	80	2N5882	2N5880	20/100	6	1	0.8	6	4	160
	90	2N6577		2k/20k	4	2	7	10	10-200#	120
	120	MJ15015	MJ15016	20/70	4				1	180
		2N6578		2k/20k	4	2	7	10	10-200#	120
	140	MJ15001	MJ15002	25/150	4				2	200
	150	MJ11018	MJ11017	100 min	15				3#	175
	200	2N6249		10/50	10	3.5	1	10	2.5	175
		MJ11020	MJ11019	100 min	15				3#	175
	250	MJ11022	MJ11021	100 min	15				3#	175
	275	2N6250		8/50	10	3.5	1	10	2.5	175
	300	2N6546		6/30	10	4	0.7	10	6 to 24	175
		2N6676		8 min	15	2.5	0.5	15	3	175
	350	2N6251		6/50	10	3.5	1	10	2.5	175
		2N6677		8 min	15	2.5	0.5	15	3	175
	400	2N6547		6/30	10	4	0.7	10	6 to 24	175
		2N6678		8 min	15	2.5	0.5	15	3	175
		MJ13090		8 min	10	2.5	0.5	10		175
	450	MJ13091		8 min	10	2.5	0.5	10		175
		MJ16010		5 min	15	1.2 typ	0.2 typ	10		175
		MJ16012		7 min	15	0.9 typ	0.15 typ	10		175
		2N6836		10/30	10	3.0	0.35	10	10	175
	500	MJ16010A		5.0 min	15	3.0	0.4	10		175
	850*	MJ12022		5.0 min	15		0.1 typ	10		175
16	60	MJ4033	MJ4030	1k/	10					150
	80	MJ4034	MJ4031	1k/	10					150
	100	2N5629	2N6029	25/100	8	1.2 typ	1.2 typ	8	1	200
		MJ4035	MJ4032	1k/	10					150
	120	2N5630	2N6030	20/80	8	1.2 typ	1.2 typ	8	1	200
	140	2N3773	2N6609	15/60	8	1.1 typ	1.5 typ	8	4	150
		2N5631	2N6031	15/60	8	1.2 typ	1.2 typ	8	1	200
	200	MJ15022	MJ15023	15/60	8				5	250
		MJ15026	MJ15027	6 min	16				15	250
	250	MJ15024	MJ15025	15/60	8				5	250
20	40	2N6257		15/75	8				2	150
	60	2N3772		15/60	10				2	150
		2N6282	2N6285	750/18k	10	2.5 typ	2.5 typ	10	4#	160
	75	2N5039		20/100	10	1.5	0.5	10	60	140
	80	2N5303	2N5745	15/60	10	2	1	10	2	200
		2N6283	2N6286	750/18k	10	2.5 typ	2.5 typ	10	4#	160
	90	2N5038		20/100	12	1.5	0.5	12	60	140
	100	2N6284	2N6287	750/18K	10	2.5 typ	2.5 typ	10	4#	160
	140	MJ15003	MJ15004	25/150	5				2	250
	200	MJ13330		8/40	10	3.5	0.7	10	5 to 40	175
	250	MJ13331		8/40	10	3.5	0.7	10	5 to 40	175
	350	MJ10000		40/400	10	3	1.8	10	10#	175
		MJ10004		40/400	10	1.5	0.5	10	10#	175
		MJ13332		10/60	5	4	0.7	10		175
	400	MJ10001		40/400	10	3	1.8	10	10#	175
		MJ10005		40/400	10	1.5	0.5	10	10#	175
		MJ13100		8 min	15	3.5	0.5	15		175
		MJ13333		10/60	5	4	0.7	10		175
	450	MJ10008		30/300	10	2	0.6	10	8#	175
		MJ13101		8 min	15	3.5	0.5	15		175
		MJ13334		10/60	5	4	0.7	10		175
		MJ16014		5 min	20	2.7	0.35	20		250
		MJ16016		7 min	20	2.2	0.25	20		250
		2N6837		10/30	15	2.5	0.25	15	15	250
	500	MJ10009		30/300	10	2	0.6	10	8#	175
		MJ13335		10/60	5	4	0.7	10		175
	750	MJ10024		50/600	20	5	1.8	10		250
	850	MJ10025		50/600	20	5	1.8	10		250

*$V_{(BR)CEX}$ # $|h_{fe}|$ @ 1 MHz

(continued)

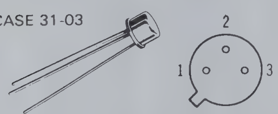
TO-204AA (FORMERLY TO-3)/TO-204AE (Type) (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
25	60	2N5885	2N5883	20/100	10	1	0.8	10	4	200
	80	2N5886	2N5884	20/100	10	1	0.8	10	4	200
			2N6436	30/120	10	1	0.25	10	40	200
	100	2N6338		30/120	10	1	0.25	10	40	200
			2N6437	30/120	10	1	0.25	10	40	200
	120	2N6339		30/120	10	1	0.25	10	40	200
			2N6438	30/120	10	1	0.25	10	40	200
	140	2N6340		30/120	10	1	0.25	10	40	200
	150	2N6341		30/120	10	1	0.25	10	40	200
30	40	2N3771		15/60	15				2	150
		2N5301	2N4398	15/60	15	2	1	10	2	200
	60	2N5302	2N4399	15/60	15	2	1	10	2	200
		MJ11012	MJ11011	1k min	20				4#	200
		2N6326	2N6329	6/30	30				3	200
	80	2N6327	2N6330	6/30	30				3	200
	90	MJ11014	MJ11013	1k min	20				4#	200
	100	2N6328	2N6331	6/30	30				3	200
		MJ802	MJ4502	25/100	7.5				2	200
	120	MJ11016	MJ11015	1k min	20				4#	200
40	350	MJ10022●		50/600	10	2.5	0.9	20		250
	400	MJ10023●		50/600	10	2.5	0.9	20		250
50	60	2N5685●	2N5683●	15/60	25	0.5 typ	0.3 typ	25	2	300
		MJ11028●	MJ11029●	400 min	50					300
	80	2N5686●	2N5684●	15/60	25	0.5 typ	0.3 typ	25	2	300
			2N6377●	30/120	20	0.8	0.25	20	30	250
	90	MJ11030	MJ11031	400 min	50					300
	100	2N6274●	2N6378●	30/120	20	0.8	0.25	20	30	250
	120	2N6275●	2N6379●	30/120	20	0.8	0.25	20	30	250
		MJ11032●	MJ11033●	400 min	50					300
	140	2N6276●		30/120	20	0.8	0.25	20	30	250
	150	2N6277●		30/120	20	0.8	0.25	20	30	250
	400	MJ10015●		10 min	40	2.5	1.0	20		250
	500	MJ10016●		10 min	40	2.5	1.0	20		250
60	60	MJ14000●	MJ14001●	15/100	50					300
	80	MJ14002●	MJ14003●	15/100	50					300
	200	MJ10020●		75 min	15	3.5	0.5	30		250
	250	MJ10021●		75 min	15	3.5	0.5	30		250

● Modified TO-3, 60 mil pins # $|h_{fe}|$ @ 1MHz

TO-205AA (TO-5) Package

CASE 31-03



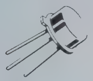
STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
3	40		2N3719	25/180	1	0.4*		1	60	6
			2N3867	40/200	1.5	0.4*		1.5	60	6
	60		2N3720	25/180	1	0.4*		1	60	6
			2N3868	30/150	1.5	0.4*		1.5	60	6
	80		2N6303	30/150	1.5	0.4*		1.5	60	6

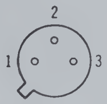
* t_{off}

TO-205AD (TO-39) Package

CASE 79-02



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(Pin 3 connected to case)

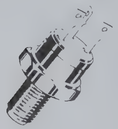


I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.5	**200**		**MJ4645**	20 min	0 5	0 72*		0 05	40	5
	300		**MJ4646**	20 min	0 5	0.72*		0.05	40	5
	400		**MJ4647**	20 min	0 5	0 72*		0.05	30	5
4	**60**	**2N4877**		20/100	4	1.5	0 5	4	4	10
5	**60**		**MJ8100**	25/180	2	1	0 15	2	30	10
	80	**2N5336**	**2N6190**	30/120	2	2	0 2	2	30	6
		2N5337	**2N6191**	60/240	2	2	0 2	2	30	6
	100	**2N5338**	**2N6192**	30/120	2	2	0 2	2	30	10
		2N5339	**2N6193**	60/240	2	2	0 2	2	30	6

* t_{off}

TO-210AA (TO-59) Package

CASE 160-03

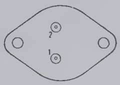


STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
7	60		**MJ6700**	25/180	2	1	0.15	2	30	60
	80	**2N5346**		30/120	2	2	0.2	2	30	60
		2N5347		60/240	2	2	0.2	2	30	60
	100	**2N5348**		30/120	2	2	0.2	2	30	60
		2N5349		60/240	2	2	0.2	2	30	60
10	80		**2N6186**	30/120	2	2	0.2	2	30	60
			2N6187	60/240	2	2	0.2	2	30	60
	100		**2N6188**	30/120	2	2	0.2	2	30	60
			2N6189	60/240	2	2	0.2	2	30	60

TO213AA (TO-66) Package

CASE 80-02



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

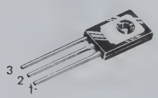
I_C Cont	$V_{CEO(sus)}$	Device Type		h_{FE}	@ I_C	Resistive Switching			f_T MHz	P_D (Case) Watts
						t_s µs	t_f µs	@ I_C		
Amps Max	Volts Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
1	40		**2N4898**	20/100	0.5	0.6 typ	0.3 typ	0.5	3	25
	60		**2N4899**	20/100	0.5	0.6 typ	0.3 typ	0.5	3	25
	80	**2N4912**	**2N4900**	20/100	0.5	0.6 typ	0.3 typ	0.5	3	25
	175	**2N3583**	**2N6420**	40/200	0.5	2 typ	0.23 typ	0.5	10	35
	225	**2N3738**	**2N6424**	40/200	0.1	3 typ	0.3 typ	0.1	10	20
	250		**2N5344**	25/100	0.5	0.6	0.1	0.5	60	40
	300	**2N3739**	**2N6425**	40/200	0.1	3 typ	0.3 typ	0.1	10	20
			2N5345	25/100	0.5	0.6	0.1	0.5	60	40
2	125	**2N5050**		25/100	0.75	3.5	1.2	0.75	10	40
	150	**2N5051**		25/100	0.75	3.5	1.2	0.75	10	40
	200	**2N5052**		25/100	0.75	3.5	1.2	0.75	10	40
	225		**2N6211**	10/100	1	2.5	0.6	1	20	35
	250	**2N3584**	**2N6421**	25/100	1	4	3	1	10	35
	300		**2N6212**	10/100	1	2.5	0.6	1	20	35
		2N3585	**2N6422**	25/100	1	4	3	1	10	35
		2N4240	**2N6423**	30/150	0.75	6	3	0.75	15	35
	350		**2N6213**	10/100	1	2.5	0.6	1	20	35
3	140	**2N3441**		25/100	0.5				0.2	25
4	60		**2N3740,A**	30/100	0.25	1.3 typ	0.27 typ	0.25	4	25
		2N3054,A	**2N6049**	25/100	0.5	1 typ	0.3 typ	0.5	3	75
		2N3766		40/160	0.5	0.9 typ	0.09 typ	0.5	10	20
		2N6294	**2N6296**	750/18k	2	0.9 typ	0.7 typ	2	4#	50
	80		**2N3741,A**	30/100	0.25	1.3 typ	0.27 typ	0.25	4	25
		2N3767		40/160	0.5	0.9 typ	0.09 typ	0.5	10	20
		2N6295	**2N6297**	750/18k	2	0.9 typ	0.7 typ	2	4	50
5	40	**2N4231A**	**2N6312**	25/100	1.5	0.5 typ	0.2 typ	1.5	4	75
	60	**2N4232A**	**2N6313**	25/100	1.5	0.5 typ	0.2 typ	1.5	4	75
	80	**2N4233A**	**2N6314**	25/100	1.5	0.5 typ	0.2 typ	1.5	4	75
	225	**2N6233**		25/125	1	3.5	0.5	1	20	50
	275	**2N6234**		25/125	1	3.5	0.5	1	20	50
	325	**2N6235**		25/125	1	3.5	0.5	1	20	50
7	60	**2N6315**	**2N6317**	20/100	2.5	1	0.8	2.5	4	90
	80	**2N5427**		30/120	2	2	0.2	2	30	40
		2N5428		60/240	2	2	0.2	2	30	40
		2N6316	**2N6318**	20/100	2.5	1	0.8	2.5	4	90
	100	**2N5429**		30/120	2	2	0.2	2	30	40
		2N5430		60/240	2	2	0.2	2	30	40
	250	**2N6078**		12/70	1.2	2.8	0.3	1.2	1	45
	275	**2N6077**		12/70	1.2	2.8	0.3	1.2	1	45
8	60	**2N6300**	**2N6298**	750/18k	4	1.5 typ	1.5 typ	4	4#	75
	80	**2N6301**	**2N6299**	750/18k	4	1.5 typ	1.5 typ	4	4#	75
	120	**MJ3247**	**MJ3237**	40 min	3	0.4 typ	0.18 typ	5	20	75
	150	**MJ3248**	**MJ3238**	40 min	3	0.4 typ	0.18 typ	5	20	75
10	80	**2N6495**		10/60	10	0.15 typ	0.05 typ	10	25	70

$|h_{fe}|$ @ 1MHz

1.2

TO-225AA Package (Formerly TO-126)

CASE 77-04
PLASTIC



STYLE 3
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.3	250	MJE3440		40/160	0.02				15	15
	350	MJE3439		40/160	0.02				15	15
0.5	150	MJE341		25/200	0.05				15	20.8
	200	MJE344		30/300	0.05				15	20.8
	250	2N5655		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
	300	MJE340	MJE350	30/240	0.05					20.8
		2N5656		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
	350	2N5657		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
1	40	2N4921	2N4918	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
	60	2N4922	2N4919	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
	80	2N4923	2N4920	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
1.5	40	MJE720	MJE710	8 min	1					20
	60	MJE721	MJE711	8 min	1					20
	80	MJE722	MJE712	8 min	1					20
	300	MJE13002●		5/25	1	4	0.7	1	5	40
	400	MJE13003●		5/25	1	4	0.7	1	5	40
2	100	MJE270	MJE271	1.5k min	0.12				6	15
3	30	MJE520	MJE370	25 min	1					25
	40	MJE180	MJE170	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	60	MJE181	MJE171	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	80	MJE182	MJE172	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
4	40	MJE3300●	MJE3310●	1k min	1				20	15
		2N5190	2N5193	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		MJE521	MJE371	40 min	1					40
		2N6037	2N6034	750/18k	2	1.7 typ	1.2 typ	2	25	40
	60	MJE3301●	MJE3311●	1k min	1				20#	15
		2N5191	2N5194	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		MJE800	MJE700	750 min	1.5				1#	40
		MJE801	MJE701	750 min	2				1#	40
		2N6038	2N6035	750/18k	2	1.7 typ	1.2 typ	2	25	40
	80	MJE3302●	MJE3312●	1k min	1				20#	15
		2N5192	2N5195	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		MJE802	MJE702	750 min	1.5				1#	40
		MJE803	MJE703	750 min	2				1#	40
		2N6039	2N6036	750/18k	2	1.7 typ	1.2 typ	2	25	40
	100	MJE243	MJE253	40/120	0.2	0.7 typ	0.08 typ	0.2	40	15
5	25	MJE200	MJE210	45/180	2	0.13 typ	0.035 typ	2	65	15

● Case 77 (Style 3)   # $|h_{fe}|$ @ 1MHz

TO-225AB Package (Formerly TO-127)

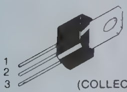
CASE 90-05
PLASTIC

STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
5	40	2N5977	2N5974	20/120	2.5	0.45 typ	0.18 typ	2.5	2	75
	50	MJE205	MJE105	25/100	2					65
	60	MJE1100 MJE1101 2N5978	MJE1090 MJE1091 2N5975	750 min 750 min 25/100	3A 4A 2.5	 0.55 typ	 0.18 typ	 2.5	1 1 2	70 70 75
	80	MJE1102 MJE1103 2N5979	MJE1092 MJE1093 2N5976	750 min 750 min 20/120	3A 4A 2.5	 0.45 typ	 0.18 typ	 2.5	1 1 2	70 70 75
8	60	MJE6043	MJE6040	1k/20k	4	1.5 typ	1.5 typ	4	4#	75
	80	MJE6044	MJE6041	1k/20k	4	1.5 typ	1.5 typ	4	4#	75
	100	MJE6045	MJE6042	1k/20k	4	1.5 typ	1.5 typ	4	4#	75
10	60	MJE2801 MJE3055	MJE2901 MJE2955	25/100 20/70	3 4				 2	90 90
12	40	2N5989	2N5986	20/120	6	0.5 typ	0.25 typ	6	2	100
	60	2N5990	2N5987	20/120	6	0.5 typ	0.25 typ	6	2	100
	80	2N5991	2N5988	20/120	6	0.5 typ	0.25 typ	6	2	100
15	40	MJE1660	MJE1290	20/100	5				3	90
	60	MJE1661	MJE1291	20/100	5				3	90

$|h_{fe}|$ @ 1 MHz

CASE 152



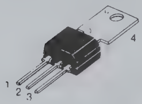
STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

(COLLECTOR CONNECTED TO TAB)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.5	65	MPS-U31		10 min	0.1					10
	300	MPS-U10	MPS-U60	30 min	0.030				60	10
0.8	40	MPS-U02	MPS-U52	30 min	0.5				150	10
1	120	MPS-U03		40 min	0.010				100	10
	180	MPS-U04		40 min	0.010				100	10
2	30	MPS-U01	MPS-U51	50 min	1				50	10
	40	MPS-U01A MPS-U45	MPS-U51A MPS-U95	50 min 4k min	1 1				50 100	10 10
	60	MPS-U05	MPS-U55	60 min	0.25				50	10
	80	MPS-U06	MPS-U56	60 min	0.25				50	10
	100	MPS-U07	MPS-U57	30 min	0.25				50	10

TO-202AC Package

CASE 306-04



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

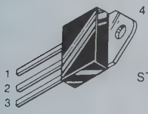
STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.1	250	D40N1		30/90	0.02				50-80	6.25
		D40N2		60/180	0.02				50-80	6.25
	300	D40N3		30/90	0.02				50-80	6.25
		D40N4		60/180	0.02				50-80	6.25
0.5	30	D40C1		10k/60k	0.2	0.35 typ	0.8 typ	1	75 typ	6.25
		D40C2		40k min	0.2	0.35 typ	0.8 typ	1	75 typ	6.25
	40	D40C4		10k/60k	0.2	0.35 typ	0.8 typ	1	75 typ	6.25
		D40C5		40k min	0.2	0.35 typ	0.8 typ	1	75 typ	6.25
	120	D40P1		40 min	0.08	2.5		0.08	50	6.25
	150	2N6591		40/200	0.1				35	10
	180	D40P3		40 min	0.08	2.5		0.08	50	6.25
	200	2N6592		30/200	0.1				35	10
	225	D40P5		40 min	0.08	2.5		0.08	50	6.25
	250	2N6557		40/180	0.03				45	10
		MDS20		40/250	0.03				60	10
		2N6593		30/200	0.1				35	10
	300	2N6558		40/180	0.03				45	10
			MDS60	30 min	0.03				60	10
		MDS21		40/250	0.03				60	10
	350	2N6559		40/180	0.03				45	10
1	30	D40D1	D41D1	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
		D40D2	D41D2	20 min	1	0.2 typ	0.05 typ	1	200 typ	10
	45	D40D4	D41D4	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
		D40D5	D41D5	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
	60	2N6551	2N6554	25 min	0.5				75	10
		D40D7	D41D7	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
		D40D8	D41D8	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
	75	D40D10	D41D10	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
		D40D11	D41D11	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
		D40D13	D41D13	50/150	0.1	0.2 typ	0.05 typ	1	200 typ	10
		D40D14	D41D14	50/150	0.1	0.2 typ	0.05 typ	1	200 typ	10
	80	2N6552	2N6555	25 min	0.5				75	10
	100	2N6553	2N6556	25 min	0.5				75	10
2	30	D40E1	D41E1	10 min	1	0.4 typ	0.17 typ	1	230 typ	8
		D40K1	D41K1	1k min	1.5				75 typ	10
		D40K3	D41K3	1k min	1				75 typ	10
	40	2N6548		5k min	1				100	10
		2N6549		3k min	1				100	10
	50	D40K2	D41K2	1k min	1.5				75 typ	10
		D40K4	D41K4	1k min	1				75 typ	10
	60	D40E5	D41E5	10 min	1	0.4 typ	0.17 typ	1	230 typ	8
	80	D40E7	D41E7	10 min	1	0.4 typ	0.17 typ	1	230 typ	8
3	40	MDS26†	MDS76†	30 min	1				50	12.5
	60	MDS27†	MDS77†	30 min	1				50	12.5

† Style 3.

TO-218AC Package

CASE 340-01
PLASTIC



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

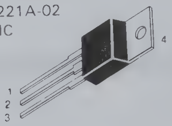
I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	t_f μs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
5	450	MJH16002		5.0 min	5	3.0	0.30	3.0		100
		MJH16004		7.0 min	5	2.7	0.35	3.0		100
	500	MJH16002A		5.0 min	5	3.0	0.30	3.0		100
8	450	MJH16006		5.0 min	8	2.5	0.25	5.0		125
		MJH16008		7.0 min	8	2.2	0.25	5.0		125
	500	MJH16008A		5.0 min	8	2.5	0.25	5.0		125
10	40	TIP33	TIP34	20 min	3				3.0	80
	60	TIP33A	TIP34A	20 min	3				3.0	80
		TIP140	TIP145	500 min	10	2.5 typ	2.5 typ	5.0	4.0#	125
	80	TIP33B	TIP34B	20 min	3				3.0	80
		TIP141	TIP146	500 min	10	2.5 typ	2.5 typ	5.0	4.0#	125
	100	TIP33C	TIP34C	20 min	3				3.0	80
		TIP142	TIP147	500 min	10	2.5 typ	2.5 typ	5.0	4.0#	125
	800	MJH16018		7.0 min	5	2.0 typ	0.5 typ	5.0		150
15	60	TIP3055	TIP2955	5 min	10				2.5	80
	150	MJH11018*	MJH11017*	400/15K	10				3.0#	150
	200	MJH11020*	MJH11019*	400/15K	10				3.0#	150
	250	MJH11022*	MJH11021*	400/15K	10				3.0#	150
	450	MJH16010		5.0 min	15	1.2	0.2	10		150
		MJH16012		7.0 min	15	.9	0.15	10		150
	500	MJH16010A		5.0 min	15	3.0	0.4	10		150
16	100	MJE4340	MJE4350	15 min	8.0	1.2 typ	1.2 typ	8.0	1.0	125
	120	MJE4341	MJE4351	15 min	8.0	1.2 typ	1.2 typ	8.0	1.0	125
	140	MJE4342	MJE4352	15 min	8.0	1.2 typ	1.2 typ	8.0	1.0	125
	160	MJE4343	MJE4353	15 min	8.0	1.2 typ	1.2 typ	8.0	1.0	125
20	60	MJH6282*	MJH6285*	750/18K	10				4.0#	125
	80	MJH6283*	MJH6286*	750/18K	10				4.0#	125
	100	MJH6284*	MJH6287*	750/18K	10				4.0#	125
25	40	TIP35	TIP36	10/75	15	0.6 typ	0.3 typ	10	3.0	125
	60	TIP35A	TIP36A	10/75	15	0.6 typ	0.3 typ	10	3.0	125
	80	TIP35B	TIP36B	10/75	15	0.6 typ	0.3 typ	10	3.0	125
	100	TIP35C	TIP36C	10/75	15	0.6 typ	0.3 typ	10	3.0	125

$|h_{fe}|$ @ 1 MHz
*To be introduced

1.2

TO-220AB Package

CASE 221A-02
PLASTIC



STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.5	40	TIP61	TIP62	15/100	0.5	0.9 typ	0.4 typ	0.5	3	15
	60	TIP61A	TIP62A	15/100	0.5	0.9 typ	0.4 typ	0.5	3	15
	80	TIP61B	TIP62B	15/100	0.5	0.9 typ	0.4 typ	0.5	3	15
	100	TIP61C	TIP62C	15/100	0.5	0.9 typ	0.4 typ	0.5	3	15
	350	MJE2360T		15 min	0.1				10 typ	30
		MJE2361T		40 min	0.1				10 typ	30
1	40	TIP29	TIP30	15/75	1	0.6 typ	0.3 typ	1	3	30
	60	TIP29A	TIP30A	15/75	1	0.6 typ	0.3 typ	1	3	30
	80	TIP29B	TIP30B	15/75	1	0.6 typ	0.3 typ	1	3	30
	100	TIP29C	TIP30C	15/75	1	0.6 typ	0.3 typ	1	3	30
	120	TIP29D	TIP30D	15/75	1	0.6 typ	0.3 typ	1	3	30
	140	TIP29E	TIP30E	15/75	1	0.6 typ	0.3 typ	1	3	30
	160	TIP29F	TIP30F	15/75	1	0.6 typ	0.3 typ	1	3	30
	250	TIP47		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	300	TIP48	MJE5730	30/150	0.3	2 typ	0.18 typ	0.3	10	40
	350	TIP49	MJE5731	30/150	0.3	2 typ	0.18 typ	0.3	10	40
	400	TIP50	MJE5732	30/150	0.3	2 typ	0.18 typ	0.3	10	40
2	60	TIP110	TIP115	500 min	2	1.7 typ	1.3 typ	2	25#	50
	80	TIP111	TIP116	500 min	2	1.7 typ	1.3 typ	2	25#	50
	100	TIP112	TIP117	500 min	2	1.7 typ	1.3 typ	2	25#	50
2.5	700	MJE8500		7.5 min	0.5	4	2	1		65
	750	MJE12007		1.1 min	2		1.0	2	4 typ	65
	800	MJE8501		7.5 min	0.5	4	2	1		65
3	40	TIP31	TIP32	25 min	1	0.6 typ	0.3 typ	1	3	40
	60	TIP31A	TIP32A	25 min	1	0.6 typ	0.3 typ	1	3	40
	80	TIP31B	TIP32B	25 min	1	0.6 typ	0.3 typ	1	3	40
	100	TIP31C	TIP32C	25 min	1	0.6 typ	0.3 typ	1	3	40
	120	TIP31D	TIP32D	25 min	1	0.6 typ	0.3 typ	1	3	40
	140	TIP31E	TIP32E	25 min	1	0.6 typ	0.3 typ	1	3	40
	160	TIP31F	TIP32F	25 min	1	0.6 typ	0.3 typ	1	3	40
4	45	2N6121	2N6124	25/100	1.5	0.4 typ	0.3 typ	1.5	2.5	40
	60	2N6122	2N6125	25/100	1.5	0.4 typ	0.3 typ	1.5	2.5	40
		MJE800T	MJE700T	750 min	1.5				1#	40
		MJE801T	MJE701T	750 min	2				1#	40
	80	2N6123	2N6126	20/80	1.5	0.4 typ	0.3 typ	1.5	2.5	40
		MJE802T	MJE702T	750 min	1.5				1#	40
		MJE803T	MJE703T	750 min	2				1#	40
	100	FT317	FT417	20 min	3	0.8 typ	0.5 typ	4	20	40
	120	FT317A	FT417A	20 min	3	0.8 typ	0.5 typ	4	20	40
	140	FT317B	FT417B	20 min	3	0.8 typ	0.5 typ	4	20	40
	300	MJE13004		6/30	3	3	0.7	3	4	60
	400	MJE13005		6/30	3	3	0.7	3	4	60
5	60	TIP120	TIP125	1k min	3	1.5 typ	1.5 typ	3	4#	65
	80	TIP121	TIP126	1k min	3	1.5 typ	1.5 typ	3	4#	65
	100	TIP122	TIP127	1k min	3	1.5 typ	1.5 typ	4	4#	75
	250	2N6497		10/75	2.5	1.8	0.8	2.5	5	80
	300	2N6498		10/75	2.5	1.8	0.8	2.5	5	80
	350	2N6499		10/75	2.5	1.8	0.8	2.5	5	80
	400	MJE13070		8 min	3	1.5	0.5	3		80
	450	MJE13071		8 min	3	1.5	0.5	3		80
		MJE16002		5 min	5	3	0.3	3		80
		MJE16004		7 min	5	2.7	0.35	3		80
	700	MJE8502		7.5 min	1	4	2	2.5		80
	800	MJE8503		7.5 min	1	4	2	2.5		80

* t_{off} # $|h_{fe}|$ @ 1 MHz

(continued)

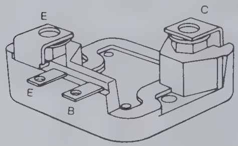
TO-220AB PACKAGE (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
6	40	TIP41	TIP42	15/75	3	0.4 typ	0.15 typ	3	3	65
	60	TIP41A	TIP42A	15/75	3	0.4 typ	0.15 typ	3	3	65
	80	TIP41B	TIP42B	15/75	3	0.4 typ	0.15 typ	3	3	65
	100	TIP41C	TIP42C	15/75	3	0.4 typ	0 15 typ	3	3	65
	120	MJE5180	MJE5170	15/75	3				3	65
		TIP41D	TIP42D	15/75	3	0.4 typ	0.15 typ	3	3	65
	140	MJE5181	MJE5171	15/75	3				3	65
		TIP41E	TIP42E	15/75	3	0.4 typ	0.15 typ	3	3	65
	160	MJE5182	MJE5172	15/75	3				3	65
		TIP41F	TIP42F	15/75	3	0 4 typ	0.15 typ	3	3	65
7	30	2N6288	2N6111	30/150	3	0 4 typ	0.15 typ	3	4	40
	40	2N6129	2N6132	20/100	2.5	0.4 typ	0.15 typ	3	2.5	50
	50	2N6290	2N6109	30/150	2 5	0 4 typ	0.15 typ	3	4	40
	60	2N6130	2N6133	20/100	2.5	0.4 typ	0 15 typ	3	2.5	50
	70	2N6292	2N6107	30/150	3	0.4 typ	0 15 typ	3	4	40
	80	2N6131	2N6134	20/100	2.5	0.4 typ	0.15 typ	3	2.5	50
	150	BU407		30 min	1.5		0 75	5	10	60
	200	BU406		30 min	1.5		0.75	5	10	60
8	40	2N6386	2N6666	1k/20k	3				20#	65
	60	2N6043	2N6040	1k/10k	4	1.5 typ	1.5 typ	3	4#	75
		TIP100	TIP105	1k/20k	3	1.5 typ	1.5 typ	3	4#	80
	80	2N6044	2N6041	1k/10k	4	1.5 typ	1.5 typ	3	4#	75
		TIP101	TIP106	1k/20k	3	1.5 typ	1.5 typ	3	4#	80
	100	2N6045	2N6042	1k/10k	3	1.5 typ	1.5 typ	3	4#	75
		TIP102	TIP107	1k/20k	3	1.5 typ	1.5 typ	3	4#	80
	120	MJE15028	MJE15029	20 min	4				30	50
	150	MJE15030	MJE15031	20 min	4				30	50
		BU807		100 min	5	0.55 typ	0.2 typ	5		60
	200	BU806		100 min	5	0.55 typ	0.2 typ	5		60
	300	MJE13006		5/30	5	3	0.7	5	4	80
		MJE5740		200 min	4	8 typ	2 typ	6		80
			MJE5850	15 min	2	2	0 5	4		80
	350	MJE5741		200 min	4	8 typ	2 typ	6		80
			MJE5851	15 min	2	2	0.5	4		80
	400	MJE5742		200 min	4	8 typ	2 typ	6		80
		MJE13007		5/30	5	3	0 7	5	4	80
			MJE5852	15 min	2	2	0.5	4		80
10	30	D44H1	D45H1	20 min	4					50
		D44H2	D45H2	40 min	4					50
	40	D44E1	D45E1	1000 min	5	2.0 typ	0.5 typ	10		50
	45	D44H4	D45H4	20 min	4					50
		D44H5	D45H5	40 min	4					50
	60	D44E2	D45E2	1000 min	5	2 0 typ	0.5 typ	10		50
		D44H7	D45H7	20 min	4					50
		D44H8	D45H8	40 min	4					50
			D45H9	40 min	4					50
		TIP140T	TIP145T	500 min	10	2 5 typ	2 5 typ	5	4.0#	125
		MJE2801T	MJE2901T	25/100	3					75
		MJE3055T	MJE2955T	20/70	4					75
		2N6387	2N6667	1k/20k	5				20#	65
		SE9300	SE9400	1k min	4				1#	70
	80	D44E3	D45E3	1000 min	5	2.0 typ	0 5 typ	10		50
		TIP141T	TIP146T	500 min	10	2 5 typ	2 5 typ	5	4.0#	125
			D45H12	40 min	4					50
		2N6388	2N6668	1k/20k	5				20#	65
		D44H10	D45H10	20 min	4	0 5 typ	0.14 typ	5	50 typ	50
		D44H11	D45H11	40 min	4	0.5 typ	0.14 typ	5	50 typ	50
		SE9301	SE9401	1k min	4				1#	70
	100	TIP142T	TIP147T	500 min	10	2 5 typ	2 5 typ	5	4.0#	125
		SE9302	SE9402	1k min	4				1#	70
12	300	MJE13008		6/30	8	3	0 7	8	4	100
	400	MJE13009		6/30	8	3	0.7	8	4	100
15	30	D44VH1	D45VH1	20 min	4	0.7	0.09	8	50 typ	83
	40	2N6486	2N6489	20/150	5	0.6 typ	0.3 typ	5	5	75
	45	D44VH4	D45VH4	20 min	4	0 5	0.09	8	50 typ	83
	60	2N6487	2N6490	20/150	5	0.6 typ	0.3 typ	5	5	75
		D44VH7	D45VH7	20 min	4	0 5	0 09	8	50 typ	83
	80	2N6488	2N6491	20/150	5	0 6 typ	0 3 typ	5	5	75
		D44VH10	D45VH10	20 min	4	0 5	0.09	8	50 typ	83

* t_{off} # $|h_{fe}|$ @ 1 MHz

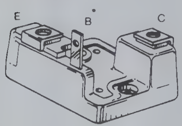
MO-040AA

CASE 346-01
HIGH CURRENT PACKAGE



I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amps	t_s µs Max	t_f µs Max	@ I_C Amps	P_D (Case) Watts @ 25°C
50	850	**MJ10050**		40 min	50	100	35	50	500
		MJ10051		40 min		10	5		
	750	**MJ10052**		40 min	50	10	5	50	
100	450	**MJ10100**		60 min	100	25	10	100	
		MJ10101		60 min		3.75	1.25		
	350	**MJ10102**		60 min	100	3.75	1.25	100	
200	250	**MJ10200**		90 min	200	20	8	200	
		MJ10201		90 min		4	1.0		
	200	**MJ10202**		90 min	200	4	1	200	

CASE 353-01
MEDIUM CURRENT PACKAGE



I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amps	t_s µs Max	t_f µs Max	@ I_C Amps	P_D (Case) Watts @ 25°C
25	850	**MJ10041**		25 min	25	10	5	25	250
		MJ10042		35 min	25	100	35	25	
50	450	**MJ10044**		50 min	50	3.8	1.3	50	
		MJ10045		50 min	50	25	10	50	
100	250	**MJ10047**		75 min	100	4.0	1.0	100	
		MJ10048		75 min	100	20	8	100	

Military Specified Power Transistors

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN/#	Device Type PNP/#	h_{FE} Min/Max	Resistive Switching @ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	@ I_C Amps	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
1	300	2N3739J,/402A TX,TXV		40/200	0.1	3.5*		0.5	10	20	TO-213AA/80
3	40		2N3867J,/350A TX,TXV	40/200	1.5	0.5	0.1	1.5	60	10	TO-205AA/31
			2N3867SJ,350A TX,TXV	40/200	1.5	0.5	0.1	1.5	60	10	TO-205AD/79
	60		2N3868J,/350A TX,TXV	30/150	1.5	0.5	0.1	1.5	60	10	TO-205AA/31
			2N3868SJ,/350A TX,TXV	30/150	1.5	.055	.035	1.5	60	5	TO-205AD/79
4	60		2N3740J,/441A TX,TXV	30/100	0.25	1*		1	5	25	TO-213AA/80
		2N3766J,/518 TX,TXV		40/160	0.5	2.5*		0.5	10	25	TO-213AA/80
	80		2N3741J,/441A TX,TXV	30/100	0.25	1*		1	5	25	TO-213AA/80
		2N3767J,/518 TX,TXV		40/160	0.5	2.5*		0.5	10	25	TO-213AA/80
8	60	2N6300J,/540** TX,TXV	2N6298J,/540** TX,TXV	750/18k	4	8*		4	25	75	TO-213AA/80
	80	2N6301J,/540** TX,TXV	2N6299J,/540** TX,TXV	750/18k	4	8*		4	25	75	TO-213AA/80
	250	2N6306J,/498		15/75	3	3*		3	5	125	TO-204/1
	350	2N6308J,/498		12/60	3	3*		3	5	125	TO-204/1
10	40	2N6383J,/523** TX,TXV	2N6648J,527 TX,TXV	1k/20k	5	10*		5	20	100	TO-204/1
			2N6648J,/527** TX,TXV	1k/20k	5	10*		5	50	85	TO-204/1
	60	2N3715J,408B TX,TXV	2N3791J,/379B TX,TXV	30/120	3	2*		5	4	150	TO-204/1
		2N6384J,/523** TX,TXV		1k/20k	5	10*		5	20	100	TO-204/1
			2N6649J,/527 TX,TXV	1k/20k	5	10*		5	50	85	TO-204/1
	80	2N3716J,/408B TX,TXV	2N3792J,/379B TX,TXV	30/120	3	2*		5	4	150	TO-204/1
		2N6385J,/523** TX,TXV		1k/20k	5	10*		5	20	100	TO-204/1
			2N6650J,/527** TX,TXV	1k/20k	5	10*		5	50	85	TO-204/1

MIL-S-19500 Detailed Spec. shown by Device Type

$|h_{fe}|$ @ 1 MHz

* t_{off}

** Consult Factory for qualification status.

(continued)

MILITARY SPECIFIED POWER TRANSISTORS (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN/#	Device Type PNP/#	h_{FE} Min/Max	Resistive Switching @ I_C Amp	t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
12	80	2N6058J,/502** TX,TXV	2N6051J,/501** TX,TXV	1k/18k	6	10*		5	10	150	TO-204/1
	100	2N6059J,/502** TX,TXV	2N6052J,/501** TX,TXV	1k/18k	6	10*		5	10	150	TO-204/1
15	300	2N6546J,/525 TX		12/60	5	4.7*		10	6	175	TO-204/1
	400	2N6547J,/525 TX		12/60	5	4.7*		10	6	175	TO-204/1
20	75	2N5039J,/439 TX,TXV**		30/150	2	2*		10	60	140	TO-204/1
	80	2N5303J,/456A TX,TXV	2N5745J,433 TX,TXV	15/60	10	3*		10	2	200	TO-204/1
		2N6283J,/504** TX,TXV	2N6286J,/505** TX,TXV	1250/18k	10	10*		10	8	175	TO-204/1
	90	2N5038J/439 TX,TXV**		50/200	2	2*		12	60	140	TO-204/1
	100	2N6284J,/504** TX,TXV	2N6287J,/505 TX,TXV	1250/18k	10	10*		10	8	175	TO-204/1
25	100	2N6338J,/509 TX,TXV**		30/120	10	1		10	40	200	TO-204/1
			2N6437J,/508 TX,TXV**	30/120	10	1		10	40	200	TO-204/1
	120		2N6438J,/509 TX,TXV**	30/120	10	1		10	40	200	TO-204/1
	150	2N6341J,/509 TX,TXV**		30/120	1-	1		10	40	200	TO-204/1
30	60	2N5302J,/456A TX,TXV	2N4399J,/433 TX,TXV	15/60	15	3*		10	2	200	TO-204/1
50	60	2N5685J,/464 TX,TXV	2N5683J,/466 TX,TXV	15/60	25	3*		25	2	300	TO-204/197 MOD
	80	2N5686J,/464 TX,TXV	2N5684J,/466 TX,TXV	15/60	25	3*		25	2	300	TO-204/197 MOD
	100	2N6274J,/514 TX,TXV**	2N6378J,/515 TX,TXV**	30/120	20	1.05*		20	30	250	TO-204/197 MOD
	120		2N6379J,/515 TX,TXV**	30/120	20	1.05*		20	30	250	TO-204/197 MOD
	150	2N6277J,/514 TX,TXV**		30/120	20	1.05*		20	30	250	TO-204/197

MIL-S-19500 Detailed Spec. shown by Device Type

$|h_{fe}|$ @ 1 MHz

* t_{off}

** Consult Factory for qualification status.

Power Darlingtons

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	$\|h_{fe}\|$ @ 1 MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
0.5	30	D40C1		10k/60k	0.2	0.35 typ	0.8 typ	1	75 typ	10	TO-202/306
		D40C2		40k min	0.2	0.35 typ	0.8 typ	1	75 typ	6.25	
	40	D40C4		10k/60k	0.2	0.35 typ	0.8 typ	1	75 typ	10	TO-202/306
		D40C5		40k min	0.2	0.35 typ	0.8 typ	1	75 typ	6.25	
2	30	D40K1	D41K1	1k min	1.5				75 typ	10	TO-202/306
			D41K3	1k min	1.5				75 typ	10	
	40	2N6548		5k min	1				100	10	TO-202/306
		2N6549		3k min	1				100	10	TO-202/306
		MPS-U45	MPS-U95	4k min	1				100	10	/152
	60	TIP110	TIP115	1k min	1	2 typ	1 typ	1	25	50	TO-220/221A
	80	TIP111	TIP116	1k min	1	2 typ	1 typ	1	25	50	TO-220/221A
	100	TIP112	TIP117	1k min	1	2 typ	1 typ	1	25	50	TO-220/221A
		MJE270	MJE271	1.5k min	0.12				6	25	TO-225AA/77
4	40	MJE3300	MJE3310	1k min	1				20	15	TO-225AA/77R
		2N6037	2N6034	750/1k	2	1.7 typ	1.2 typ	2	25	40	TO-225AA/77
	60	MJE3301	MJE3311	1k min	1				20	15	TO-225AA/77R
		MJE800	MJE700	750 min	1.5				1	40	TO-225AA/77
		MJE800T	MJE700T	750 min	1.5				1	40	TO-220/221A
		MJE801	MJE701	750 min	2				1	40	TO-225AA/77
		MJE801T	MJE701T	750 min	2				1	40	TO-220/221A
		2N6038	2N6035	750/18k	2	1.7 typ	1.2 typ	2	25	40	TO-225AA/77
		2N6294	2N6296	750/18k	2	0.9 typ	0.7 typ	2	4	50	TO-213AA/80
	80	MJE3302	MJE3312	1k min	1				20	15	TO-225AA/77R
		MJE802	MJE702	750 min	1.5				1	40	TO-225AA/77
		MJE802T	MJE702T	750 min	1.5				1	40	TO-220/221A
		MJE803	MJE703	750 min	2				1	40	TO-225AA/77
		MJE803T	MJE703T	750 min	2				1	40	TO-220/221A
		2N6039	2N6036	750/18k	2	1.7 typ	1.2 typ	2	25	40	TO-225AA/77
		2N6295	2N6297	750/18k	2	0.9 typ	0.7 typ	2	4	50	TO-213AA/80
5	60	MJE1100	MJE1090	750 min	3A				1	70	TO-225AB/90
		MJE1101	MJE1091	750 min	4A				1	70	TO-225AB/90
		TIP120	TIP125	1k min	3	1.5 typ	1.5 typ	3	4	65	TO-220/221A
	80	MJE1102	MJE1092	750 min	3A				1	70	TO-225AB/90
		MJE1103	MJE1102	750 min	4A				1	70	TO-225AB/90
		TIP121	TIP126	1k min	3	1.5 typ	1.5 typ	3	4	65	TO-220/221A
	100	TIP122	TIP127	1k min	3	1.5 typ	1.5 typ	3	4	65	TO-220/221A
7	300	MJ3041		250 min	2.5					100	TO-204/1
	350	MJ3042		250 min	2.5					100	TO-204/1
8	40	2N6386	2N6666	1k/20k	3				20	65	TO-220/221A
	60	MJ1000	MJ900	1k min	3					90	TO-204/11
		TIP100	TIP105	1k/20k	3	1.5 typ	1.5 typ	3	4	80	TO-220/221A
		2N6043	2N6040	1k/10k	4	1.5 typ	1.5 typ	3	4	75	TO-220/221A
		2N6300	2N6298	750k/18k	4	1.5 typ	1.5 typ	4	4	75	TO-213AA/80
		2N6055	2N6053	750k/18k	4	1.5 typ	1.5 typ	4	4	100	TO-204/11
		MJE6043	MJE6040	1k/20k	4	1.5 typ	1.5 typ	4	2	75	TO-225AB/90
	80	MJ1001	MJ901	1k min	3					90	TO-204/11
		TIP101	TIP106	1k/20k	3	1.5 typ	1.5 typ	3	4	80	TO-220/221A
		2N6044	2N6041	1k/10k	4	1.5 typ	1.5 typ	3	4	75	TO-220/221A
		2N6301	2N6299	750k/18k	4	1.5 typ	1.5 typ	4	4	75	TO-213AA/80
		2N6056	2N6054	750k/18k	4	1.5 typ	1.5 typ	4	4	100	TO-204/11
		MJE6044	MJE6041	1k/20k	4	1.5 typ	1.5 typ	4	2	75	TO-225AB/90
	100	MJE6045	MJE6042	1k/20k	4	1.5 typ	1.5 typ	4	2	75	TO-225AB/90
		TIP102	TIP107	1k/20k	3	1.5 typ	1.5 typ	3	4	80	TO-220/221A
		2N6045	2N6042	1k/10k	4	1.5 typ	1.5 typ	3	4	75	TO-220/221A
	150	BU807		100 min	5	0.55 typ	0.2 typ	5		60	TO-220/221A
	200	BU806		100 min	5	0.55 typ	0.2 typ	5		60	TO-220/221A
	300	MJE5740		200/400	4	8 typ	2 typ	6		80	TO-220/221A
	350	MJE5741		200/400	4	8 typ	2 typ	6		80	TO-220/221A
	400	MJE5742		200/400	4	8 typ	2 typ	6		80	TO-220/221A
	1400*	MJE10011		20 min	4			1	4	80	TO-204/1
10	40	2N6383	2N6648	1k/20k	5				20	100	TO-204/11
		D44E1	D45E1	1000 min	5	2.0 typ	0.5 typ	10		50	TO-220/221A
	60	MJ3000	MJ2500	1k min	5					150	TO-204/1
		2N6387	2N6667	1k/20k	5				20	65	TO-220/221A
		2N6384	2N6649	1k/20k	5				20	100	TO-204/11
		D44E2	D45E2	1000 min	5	2.0 typ	0.5 typ	10		50	TO-220/221A
		TIP140	TIP145	500 min	10	2.5 typ	2.5 typ	5	4	125	TO-218/340
		TIP140T	TIP145T	500 min	10	2.5 typ	2.5 typ	5	4	125	TO-220/221A

POWER DARLINGTONS (continued)

1.2

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	t_f μs Max	@ I_C Amp	$\|h_{fe}\|$ @ 1 MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
10	80	2N6388	2N6668	1k/20k	5				20	65	TO-220/221A
		2N6385	2N6650	1k/20k	5				20	100	TO-204/11
		D44E3	D45E3	1000 min	5	2.0 typ	0.5 typ	10		50	TO-220/221A
		TIP141	TIP146	500 min	10	2.5 typ	2.5 typ	5	4	125	TO-218/340
		TIP141T	TIP146T	500 min	10	2.5 typ	2.5 typ	5	4	125	TO-220/221A
	100	TIP142	TIP147	500 min	10	2.5 typ	2.5 typ	5	4	125	TO-218/340
		TIP142T	TIP147T	500 min	10	2.5 typ	2.5 typ	5	4	125	TO-220/221A
	350	MJ10002		30/300	5	2.5	1	5	10	150	TO-204/1
		MJ10006●		30/300	5	1.5	0.5	5	10	150	TO-204/1
	400	MJ10003		30/300	5	2.5	1	5	10	150	TO-204/1
		MJ10007●		30/300	5	1.5	0.5	5	10	150	TO-204/1
		MJ10012		100/2k	6	15	15	6		175	TO-204/1
	550	MJ10013●		10/250	10	2.5	0.8	10		175	TO-204/1
	600	MJ10014●		10/250	10	2.5	0.8	10		175	TO-204/1
12	60	2N6057	2N6050	750/18k	6	1.6 typ	1.5 typ	6	4	150	TO-204/1
	80	2N6058	2N6051	750/18k	6	1.6 typ	1.5 typ	6	4	150	TO-204/1
	100	2N6059	2N6052	750/18k	6	1.6 typ	1.5 typ	6		150	TO-204/11
15	60	2N6576		2k/20k	4	2	7	10	10/200	120	TO-204/11
	90	2N6577		2k/20k	4	2	7	10	10/200	120	TO-204/11
	120	2N6578		2k/20k	4	2	7	10	10/200	120	TO-204/11
	150	MJ11018	MJ11017	100 min	15				3#	175	TO-204/1
		MJH11018	MJH11017	100 min	15				3	150	TO-218/340
	200	MJ11020	MJ11019	100 min	15				3#	175	TO-204/1
		MJH11020	MJH11019	100 min	15				3	150	TO-218/340
	250	MJ11022	MJ11021	100 min	15				3#	175	TO-204/1
		MJH11022	MJH11021	100 min	15				3	150	TO-218/340
16	60	MJ4033	MJ4030	1k min	10					150	TO-204/1
	80	MJ4034	MJ4031	1k min	10					150	TO-204/1
	100	MJ4035	MJ4032	1k min	10					150	TO-204/1
20	60	2N6282	2N6285	750/18k	10	2.5 typ	2.5 typ	10	4	160	TO-204/1
		MJH6282	MJH6285	750/18K	10	2.5 typ	2.5 typ	10	4	125	TO-218/340
	80	2N6283	2N6286	750/18k	10	2.5 typ	2.5 typ	10	4	160	TO-204/1
		MJH6283	MJH6286	750/18K	10	2.5 typ	2.5 typ	10	4	125	TO-218/340
	100	2N6284	2N6287	750/18k	10	2.5 typ	2.5 typ	10	4	160	TO-204/1
		MJH6284	MJH6287	750/18K	10	2.5 typ	2.5 typ	10	4	125	TO-218/340
	350	MJ10000		40/400	10	3	1.8	10	10	175	TO-204/1
		MJ10004●		40/400	10	1.5	0.5		10	175	TO-204/1
	400	MJ10001		40/400	10	3	1.8	10	10	175	TO-204/1
		MJ10005●		40/400	10	1.5	0.5		10	175	TO-204/1
	450	MJ10008●		30/300	10	2	0.6	10	8	175	TO-204/1
	500	MJ10009●		30/300	10	2	0.6	10	8	175	TO-204/1
	750	MJ10024		50/600	20	5	1.8	10		250	TO-204/1
	850	MJ10025		50/600	20	5	1.8	10		250	TO-204/1
25	850	MJ10041●		25 min	25	10	5	25		250	— /353
		MJ10042		35 min	25	100	35	25		250	— /353
30	60	MJ11012	MJ11011	1k min	20				4	200	TO-204/1
	90	MJ11014	MJ11013	1k min	20				4	200	TO-204/1
	120	MJ11016	MJ11015	1k min	20				4	200	TO-204/1
40	350	MJ10022●		50/600	10	2.5	0.9	20		250	TO-204 Mod/197
	400	MJ10023●		50/600	10	2.5	0.9	20		250	TO-204 Mod/197
50	60	MJ11028	MJ11029	400 min	50					300	TO-204 Mod/197
	90	MJ11030	MJ11031	400 min	50					300	TO-204 Mod/197
	120	MJ11032	MJ11033	400 min	50					300	TO-204 Mod/197
	400	MJ10015●		10 min	40	2.5	0.5	20	10	250	TO-204 Mod/197
	450	MJ10044●		50 min	50	3.8	1.3	50		250	— /353
		MJ10045		50 min	50	2.5	10	50		250	— /353
	500	MJ10016●		10 min	40	2.5	0.5	20	10	250	TO-204 Mod/197
	850	MJ10050		40 min	50	100	35	50		500	MO-040/346
		MJ10051●		40 min	50	10	5	50		500	MO-040/346
60	200	MJ10020●		75/1k min	15	3.5	0.5	30		250	TO-204 Mod/197
	250	MJ10021●		75/1k min	15	3.5	0.5	30		250	TO-204 Mod/197
100	250	MJ10047●		75 min	100	4.0	1.0	100		250	— /353
		MJ10048●		75 min	100	20	8.0	100		250	— /353
	450	MJ10100		60 min	100	25	10	100		500	MO-040/346
		MJ10101●		60 min	100	3.75	1.25	100		500	MO-040/346
200	250	MJ10200		90 min	200	20	8	200		500	MO-040/346
		MJ10201●		90 min	200	4	1	200		500	MO-040/346

● Darlington with speed-up diode.

Power Switching Transistors

$V_{CEO} < 200V$
(See next page for 200 Volts and greater.)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
2	120	2N5050		25/100	0.75	3.5	1.2	0.75	10	40	TO-213AA/80
	150	2N5051		25/100	0.75	3.5	1.2	0.75	10	40	TO-213AA/80
3	40		2N3719	25/180	2	0.4*		1	60	6	TO-205AA/31
			2N3867	40/200	2	0.4*		1	60	6	TO-205AA/31
	60		2N3720	25/180	2	0.4*		1	60	6	TO-205AA/31
			2N3868	30/150	2	0.4*		1	60	6	TO-205AA/31
	80		2N6303	30/150	2	0.4*		1	60	6	TO-205AA/31
4	60	2N4877		20/100	4	1.5	0.5	4	30	10	TO 205AD/79
5	60		MJ8100	25/180	2	1	0.15	2	30	10	TO-205AD/79
	80	2N5337	2N6191	60/240	2	2	0.2	2	30	10	TO-205AD/79
	100	2N5339	2N6193	60/240	2	2	0.2	2	30	10	TO-205AD/79
7	60	2N6315	2N6317	20/100	2.5	1	0.8	2.5	4	90	TO-213AA/80
	80	2N5428		60/240	2	2	0.2	2	30	60	TO-213AA/80
		2N5347	2N6187	60/240	2	2	0.2	2	30	60	TO-210AA/160
		2N6316	2N6318	20/100	2.5	1	0.8	2.5	4	90	TO-213AA/80
	100	2N5430		60/240	2	2	0.2	2	30	60	TO-213AA/80
		2N5349	2N6189	60/240	2	2	0.2	2	30	60	TO-210AA/160
7.5	60	2N3447		40/120	5	2	0.35	5	10	115	TO-204/11
	80	2N3448		40/120	5	2	0.35	5	10	115	TO-204/11
8	120	MJ3247	MJ3237	40 min	3	0.4 typ	0.18 typ	5	20	75	TO-213AA/80
		MJ4247	MJ4237	40 min	3	0.4 typ	0.18 typ	5	20	90	TO-204/11
		MJE15028	MJE15029	20 min	4	0.4 typ	0.18 typ	5	30	50	TO-220/221A
	150	MJ3248	MJ3238	40 min	3	0.4 typ	0.18 typ	5	20	75	TO-213AA/80
		MJ4248	MJ4238	40 min	3	0.4 typ	0.18 typ	5	20	90	TO-204/11
		MJE15030	MJE15031	20 min	4	0.4 typ	0.18 typ	5	30	50	TO-220/221A
10	60		MJ6700	25/180	2	1	0.15	2	30	60	TO-210AA/160
		2N5877	2N5875	20/100	4	1	0.8	4	4	150	TO-204/11
	80	2N5878	2N5876	20/100	4	1	0.8	4	4	150	TO-204/11
15	60	2N5881	2N5879	20/100	6	1	0.8	6	4	160	TO-204/11
	80	2N5882	2N5880	20/100	6	1	0.8	6	4	160	TO-204/11
20	75	2N5039		20/100	10	1.5	0.5	10	60	140	TO-204/1
	80	2N5303	2N5745	15/60	10	2	1	10	2	200	TO-204/11
	90	2N5038		20/100	12	1.5	0.5	12	60	140	TO-204/1
25	60	2N5885	2N5883	20/100	10	1	0.8	10	4	200	TO-204/11
	80	2N5886	2N5884	20/100	10	1	0.8	10	4	200	TO-204/11
			2N6436	30/120	10	1	0.25	10	40	200	TO-204/1
	100	2N6338		30/120	10	1	0.25	10	40	200	TO-204/1
			2N6437	30/120	10	1	0.25	10	40	200	TO-204/1
	120	2N6339		30/120	10	1	0.25	10	40	200	TO-204/1
			2N6438	30/120	10	1	0.25	10	40	200	TO-204/1
	140	2N6340		30/120	10	1	0.25	10	40	200	TO-204/1
	150	2N6341		30/120	10	1	0.25	10	40	200	TO-204/1
30	40	2N5301	2N4398	15/60	15	2	1	10	2	200	TO-204/11
	60	2N5302	2N4399	15/60	15	2	1	10	2	200	TO-204/11
50	80		2N6377	30/120	20	0.8					TO-204 Mod/197
	100	2N6274	2N6378	30/120	20	0.8	0.25	20	30	250	TO-204 Mod/197
	120	2N6275	2N6379	30/120	20	0.8	0.25	20	30	250	TO-204 Mod/197
	140	2N6276		30/120	20	0.8	0.25	20	30	250	TO-204 Mod/197
	150	2N6277		30/120	20	0.8	0.25	20	30	250	TO-204 Mod/197

* t_{off}

Switchmode Power Transistors

$V_{CEO} \geqslant 200\,V$

Devices are listed in descending order of $V_{CEO(sus)}$, and I_CCont

$V_{CEO(sus)}$ Volts Min	I_C Cont Amps Max	V_{CEV} Volts Min	Device Type NPN unless otherwise noted	h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	Case JEDEC/MOT
						t_s μs Max	t_f μs Max	@ I_C Amp		
850	50	900	MJ10050#★	40 min	50	100	35	50		MO-040/346
		900	MJ10051##★	40 min	50	10	5	50		MO-040/346
	25	900	MJ10041##★	25 min	25	10	5	25		— /353
		900	MJ10042#★	35 min	25	100	35	25		— /353
	20	1200	MJ10025##★	50/600	20	5	1.8	10		TO-204/1
800	10	1400	MJ8505★	7.5 min	1.5	4	2	5		TO-204/1
		1500	MJ16018★	7.0 min	5.0	2.0 typ	0.9 typ	5.0		TO-204/1
		1500	MJH16018★	7.0 min	5.0	2.0 typ	0.9 typ	5.0		TO-218/340
	5	1400	MJ8503★	7.5 min	1	4	2	2.5		TO-204/1
		1400	MJE8503★	7.5 min	1.0	4	2	2.5		TO-220/221A
	2.5	1400	MJ8501★	7.5 min	0.5	4	2	1		TO-204/1
		1400	MJE8501★	7.5 min	0.5	4	2	1		TO-220/221A
750	50	900	MJ10052##★	40 min	50	10	5	50		MO-040/346
	20	1000	MJ10024##★	50/600	20	5	1.8	10		TO-204/1
	8	1500	MJ12005	5 min	5		1	5	4 typ	TO-204/1
	5	1500	MJ12004★	2.5 min	4.5		1	4.5	4 typ	TO-204/1
	4	1500	MJ12003	2.5 min	3		1	3	4 typ	TO-204/1
	2.5	1500	MJ12002★	1.11 min	2		1	2	4 typ	TO-204/1
		1500	MJE12007★	1.1 min	2		1	2	4 typ	TO-220/221A
700	10	1200	MJ8504★	7.5 min	1.5	4	2	5		TO-204/1
	8	1400	MJ10011#	20 min	4		1	4		TO-204/1
	5	1200	MJ8502★	7.5 min	1	4	2	2.5		TO-204/1
		1200	MJE8502★	7.5 min	1	4	2	2.5		TO-220/221A
		1500	BU208D	2.25 min	4.5		0.6 typ	4.5		TO-204/1
	2.5	1200	MJ8500★	7.5 min	0.5	4	2	1		TO-204/1
		1200	MJE8500★	7.5 min	0.5	4	2	1		TO-220/221A
600	15	700	MJ10014##★	10/250	10	2.5	0.8	10		TO-204/1
550		650	MJ10013##★	10/250	10	2.5	0.8	10		TO-204/1
500	50	750	MJ10016##★	10 min	40	2.5	1	20		TO-204 Mod/197
	20	600	MJ10009##★	30/300	10	2	0.6	10	8**	TO-204/1
		800	MJ13335★	10/60	5	4	0.7	10		TO-204/1
	15	1000	MJ16010A★	5.0 min	15.0	3.0	0.4	10.0		TO-204/1
		1000	MJH16010A★	5.0 min	15.0	3.0	0.4	10.0		TO-218/340
	8	1000	MJ16006A★	5.0 min	15.0	3.0	0.4	10.0		TO-204/1
		1000	MJH16006A★	5.0 min	15.0	3.0	0.4	10.0		TO-218/340
	5	1000	MJ16002A★	5.0 min	15.0	3.0	0.3	3.0		TO-204/1
		1000	MJH16002A★	5.0 min	15.0	3.0	0.3	3.0		TO-218/340
450	100	500	MJ10100#★	60 min	100	25	10	100		MO-040/346
		500	MJ10101##★	60 min	100	3.75	1.25	100		MO-040/346
	50	500	MJ10044##★	50 min	50.0	3.8	1.3	50.0		— /353
		500	MJ10045#★	50 min	50.0	25	10	50.0		— /353
	20	650	MJ10008##★	30/300	10	2	0.6	10	8**	TO-204/1
		750	MJ13101★	8 min	15	3.5	0.5	15		TO-204/1
			MJ13334★	10/60	5	4	0.7	10		TO-204/1
		850	2N6837★	10/30	15	2.5	.25	15	15	TO-204/1
		850	MJ16014★	5 min	20	2.7	0.35	20		TO-204/197
		850	MJ16016★	7 min	20	2.2	0.25	20		TO-204/197
	15	750	MJ13091★	8 min	10	2.5	0.5	10		TO-204/1
		850	2N6836★	10/30	10.0	3.0	0.35	10.0	10	TO-204/1
		850	MJ12022★	5.0 min	15.0		0.1 typ	10.0		TO-204/1
		850	MJ16010★	5 min	15	1.2 typ	0.2 typ	10		TO-204/1
		850	MJ16012★	7 min	15	0.9 typ	0.15 typ	10		TO-204/1
		850	MJH16010★	5.0 min	15.0	1.2	0.2	10.0		TO-218/340
		850	MJH16012★	7.0 min	15.0	0.9	0.15	10.0		TO-218/340
	8	750	MJ13081★	8 min	5	1.5	0.5	5		TO-204/1
		850	2N6835★	7.5/3.0	5.0	2.5	0.25	5.0	10	TO-204/1
		850	MJ12021★	5.0 min	8.0		0.1 typ	8.0		TO-204/1
		850	MJ16006★	5 min	8	2.5	0.25	5		TO-204/1
		850	MJ16008★	7 min	8	2.2	0.25	5		TO-204/1
		850	MJH16006★	5.0 min	8.0	2.5	0.25	5.0		TO-218/340
		850	MJH16008★	7.0 min	8.0	2.2	0.25	5.0		TO-218/340

★Designers Data Sheet characterization
\# Darlington   ## Darlington with speed-up diode   * t_{off} ** $|h_{fe}|$ @ 1MHz

(continued)

SWITCHMODE POWER TRANSISTORS (continued)

$V_{CEO} \geqslant 200V$

$V_{CEO(sus)}$ Volts Min	I_C Cont Amps Max	V_{CEV} Volts Min	Device Type NPN unless otherwise noted	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	Case JEDEC/MOT
450	5	750	MJ13071★	8 min	3	1.5	0.5	3		TO-204/1
		750	MJE13071★	8 min	3	1.5	0.5	3		TO-220/221A
		850	2N6834★	10/30	3.0	2.7	0.35	3.0	15	TO-204/1
		850	MJ12020★	5.0 min	5.0		0.13 typ	3.0		TO-204/1
		850	MJ16002★	5 min	5	3	0.3	3		TO-204/1
		850	MJ16004★	8 min	3	2.7	0.35	3		TO-204/1
		850	MJE16002★	5 min	5	3	0.3	3		TO-220/221A
		850	MJE16004★	7 min	5	2.7	0.35	3		TO-220/221A
		850	MJH16002★	5.0 min	5.0	3.0	0.30	3.0		TO-218/340
		850	MJH16004★	7.0 min	5.0	2.7	0.35	3.0		TO-218/340
400	50	650	MJ10015##★	10 min	40	2.5	1	20		TO-204 Mod/197
	40	600	MJ10023##★	50/600	10	2.5	0.9	20		TO-204 Mod/197
	20	500	MJ10001#★	40/400	10	3	1.8	10	10**	TO-204/1
		500	MJ10005#★	40/400	10	1.5	0.5	10	10**	TO-204/1
		500	MJ13333★	10/60	5	4	0.7	10		TO-204/1
		650	MJ13100★	8 min	15	3.5	0.35	15		TO-204/1
		850	2N6547★	6/30	10	4	0.7	10	6 to 24	TO-204/1
	15	650	MJ13090★	8 min	10	2.5	0.5	10		TO-204/1
		650	2N6678	8 min	15	2.5	0.5	15	3	TO-204/1
	12	700	MJE13009★	6/30	8	3	0.7	8	4**	TO-220/221A
	10	950	MJ12010	4.2 min	5		1	5	6 typ	TO-204/1
		550	MJ10012#	100/2k	6	6	15	15	6	TO-204/1
		500	MJ10003#★	30/300	5	2.5	1	5	10**	TO-204/1
		500	MJ10007##★	30/300	5	1.1	0.25	5	10**	TO-204/1
		450	MJ13015★	8/20	5	2	0.5	5		TO-204/1
	8	850	2N6545★	7/35	5	4	1	5	6	TO-204/1
		800	MJE5742#	200/400	4	8 typ	2 typ	6		TO-220/221A
		700	MJE13007★	6/30	5	3	0.7	5	4	TO-220/221A
		650	MJ13080★	8 min	5	1.5	0.5	5		TO-204/1
		450	MJ6503-PNP★	15 min	2	2	0.5	4		TO-204/1
		450	MJE5852-PNP★	15 min	2	2	0.5	4		TO-220/221A
	5	850	2N6543★	7/35	3	4	0.8	3	6	TO-204/1
		650	MJ13070★	8 min	3	1.5	0.5	3		TO-204/1
		650	MJE13070★	8 min	3	1.5	0.5	3		TO220/221A
	4	700	MJE13005★	6/30	3	3	0.7	3	4	TO-220/221A
	1.5	700	MJE13003★	5/25	1	4	0.7	1	5	TO-225AA/77R
	0.5	400	MJ4647-PNP	20 min	0.5	0.72*		0.05	40	TO-205AD/79
350	100	500	MJ10102##★	60 min	100	3.75	1.25	100		MO-040/346
	40	450	MJ10022##★	50/600	10	2.5	0.9	20		TO-204 Mod/197
	20	450	MJ10000#★	40/400	10	3	1.8	10	10**	TO-204/1
		450	MJ10004##★	40/400	10	1.5	0.5	10	10**	TO-204/1
		450	MJ13332★	10/60	5	4	0.7	10		TO-204/1
350	15	550	2N6677	8 min	15	2.5	0.5	15	3	TO-204/1
		375	2N6251	6/50	10	3.5	1	10	2.5	TO-204/1
	10	450	MJ10002#★	30/300	5	2.5	1	5	10**	TO-204/1
		450	MJ10006##★	30/300	5	1.5	0.5	5	10**	TO-204/1
		400	MJ13014★	8/20	5	2	0.5	5		TO-204/1
	8	700	2N6308	12/60	3	1.6	0.4	5	5	TO-204/1
		700	MJE5741#	200/400	4	8 typ	2 typ	6		TO-220/221A
		400	MJE5851-PNP	15 min	2	2	0.5	4		TO-220/221A
	5	450	2N6499	10/75	2.5	1.8	0.8	2.5	5	TO-220/221A
	3	375	2N5840	10/50	2	3	1.5	2	5	TO-204/1
	2	400	2N6213PNP	10/100	1	2.5	0.6	1	4	TO-213AA/80
325	5	700	MJ3030	3.75 min	3		1	3		TO-204/1
		350	2N6235	25/125	1	3.5	0.5	1	20	TO-213AA/80
300	15	650	2N6546★	6/30	10	4	0.7	10	6 to 24	TO-204/1
	15	450	2N6676	8 min	15	2.5	0.5	15	3	TO-204/1
	12	600	MJE13008★	6/30	8	3	0.7	8	4**	TO-220/221A
	8	650	2N6544★	7/35	5	4	1	5	6	TO-204/1
		600	2N6307	15/75	3	1.6	0.4	3	5	TO-204/1
		600	MJE13006★	6/30	5	3	0.7	5	4	TO-220/221A
		600	MJE5740	200/400	4	8 typ	2 typ	6		TO-220/221A
		350	MJE5850-PNP★	15 min	2	2	0.5	4		TO-220/221A

★Designers Data Sheet characterization
\# Darlington ## Darlington with speed-up diode * t_{off} ** $|h_{fe}|$ @ 1MHz

(continued)

SWITCHMODE POWER TRANSISTORS (continued)

$V_{CEO} \geqslant 200\,V$

$V_{CEO(sus)}$ Volts Min	I_C Cont Amps Max	V_{CEV} Volts Min	Device Type NPN unless otherwise noted	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	t_f μs Max	@ I_C Amp	f_T MHz Min	Case JEDEC/MOT
300	7	275	2N6077	12/70	1.2	2.8	0.3	1.2	7	TO-213AA/80
	5	650	2N6542★	7/35	3	4	0.8	3	6	TO-204/1
		400	2N6498	10/75	2.5	1.8	0.8	2.5	5	TO-220/221A
	4	600	MJE13004★	6/30	3	3	0.7	3	4	TO-220/221A
	2	500	2N3585	25/100	1	4	3	1	10	TO-213AA/80
		500	2N6422-PNP	25/100	1	4	3	1	10	TO-213AA/80
		350	2N6212-PNP	10/100	1	2.5	0.6	1	4	TO-213AA/80
	1.5	600	MJE13002★	5/25	1	4	0.7	1	5	TO-225AA/77R
	1	300	2N5345-PNP	25/100	0.5	0.6	0.1	0.5	60	TO-213AA/80
	0.5	300	MJ4646-PNP	20 min	0.5	0.72*		0.05	40	TO-205AD/79
275	15	300	2N6250	8/50	10	3.5	1	10	2.5	TO-204/1
	7	275	2N6078	12/70	1.2	2.8	0.3	1.2	7	TO-213AA/80
	5	275	2N6234	25/125	1	3.5	0.5	1	20	TO-213AA/80
	3	300	2N5839	10/50	2	3.75	1.5	2	5	TO-204/1
250	200	300	MJ10200#★	90 min	200	20	8	20		MO-040/346
		300	MJ10201##★	90 min	200	4	1	200		MO-040/346
	100	300	MJ10047##★	75 min	100.0	4.0	1.0	100		— /353
		300	MJ10048#★	75 min	100.0	2.0	8	100		— /353
	60	350	MJ10021##★	25 min	30	3.5	0.5	30		TO-204 Mod/197
	20	450	MJ13331★	8/40	10	3.5	0.7	10	5/40	TO-204/1
	15	250	MJ11021#PNP	100 min	15				3#	TO-204/1
		250	MJ11022#	100 min	15				3#	TO-204/1
	8	500	2N6306	15/75	3	1.6	0.4	3	5	TO-204/1
		400	MJ6502-PNP★	15 min	2	2	0.5	4		TO-204/1
	5	500	MJ3029	30 min	0.4		1	3		TO-204/11
		350	2N6497	10/75	2.5	1.8	0.8	2.5	5	TO-220/221A
	3	275	2N5838	10/50	2	3	1.5	3	5	TO-204/11
	2	375	2N3584	25/100	1	4	3	1	10	TO-213AA/80
		375	2N6421-PNP	25/100	1	4	3	1	10	TO-213AA/80
	1	250	2N5344-PNP	25/100	0.5	0.6	0.1	0.5	60	TO-213AA/80
225	2	275	2N6211	10/100	1	2.5	0.6	1	20	TO-213AA/80
200	200	300	MJ10202##★	90 min	200	4	1	200		MO-040/346
	60	300	MJ10020##★	25 min	30	3.5	0.5	30		TO-204 Mod/197
	20	400	MJ13330★	8/40	10	3.5	0.7	10	5/40	TO-204/11
	15	225	2N6249	10/50	10	3.5	1	10	2.5	TO-204/11
		200	MJ11019#PNP	100 min	15				3#	TO-204/1
		200	MJ11020#	100 min	15				3#	TO-204/1
	2	200	2N5052	25/100	0.75	3.5	1.2	0.75	10	TO-213AA/80
	0.5	200	MJ4645-PNP	20 min	0.5	0.72*		0.05	40	TO-205AA/79

★Designers Data Sheet characterization
Darlington   ## Darlington with speed-up diode   * t_{off} ** $|h_{fe}|$ @ 1 MHz

POWER TRANSISTOR

1.3

Data Sheets

The following power transistor data sheets are arranged in alphanumeric sequence except in such instances where a particular data sheet may contain information applying to more than one transistor — e.g. 2N4398, 2N4399, 2N5745. To determine if a particular device type is covered by a data sheet in this section, please refer to the alphanumeric listing of the Index and Cross Reference on page1-2.

2N3054
2N3054A

MOTOROLA

1.3

MEDIUM-POWER NPN SILICON TRANSISTORS

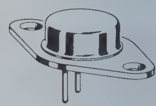
. . . designed for general purpose switching and amplifier applications.

- Excellent Safe Operating Area
- DC Current Gain Specified to 3.0 Amperes
- Complement to PNP Type 2N6049 or 2N4912

4 AMPERE

POWER TRANSISTORS
NPN SILICON

55 VOLTS
25 WATTS – 2N3054
75 WATTS – 2N3054A



*MAXIMUM RATINGS

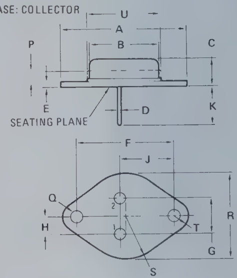
Rating	Symbol	2N3054A	2N3054	Unit
Collector-Emitter Voltage	V_{CEO}	55		Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	60		Vdc
Collector-Base Voltage	V_{CB}	90		Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	4.0 10**		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.43	25 0.143	Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	–65 to +200		°C

*Indicates JEDEC Registered Data
**Addition to JEDEC Registered Data

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N3054A	2N3054	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.33	7.0	°C/W

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

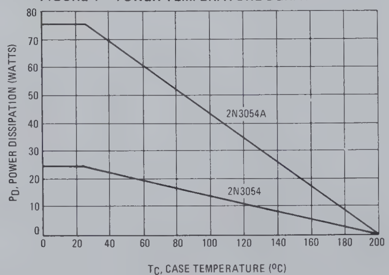


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

FIGURE 1 — POWER-TEMPERATURE DERATING



ELECTRICAL CHARACTERISTICS ($T_C = 25^o$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	55	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, R_{BE} = 100 Ω)	$V_{CER(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 6.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
***ON CHARACTERISTICS** (1)				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	25 5.0	150 –	–
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C =3.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	– –	1.0 6.0	Vdc
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.7	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc)	f_T	3.0	–	MHz
*Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	25	180	–
*Common-Emitter Cutoff Frequency (I_C = 100 mAdc, V_{CE} = 4.0 Vdc)	f_{hfe}	30	–	kHz

*Indicates JEDEC Registered Data
(1) Pulse test: Pulse Width ⩽300 μs, Duty Cycle ⩽2.0%

FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUIT

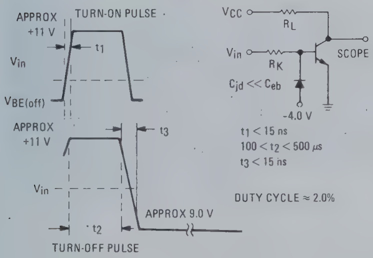


FIGURE 3 – TURN-ON TIME

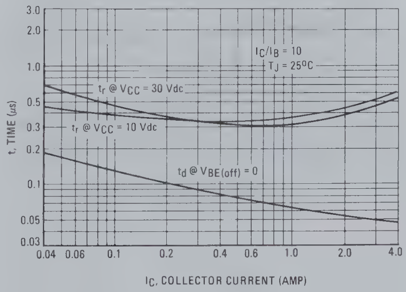


FIGURE 4 – THERMAL RESPONSE

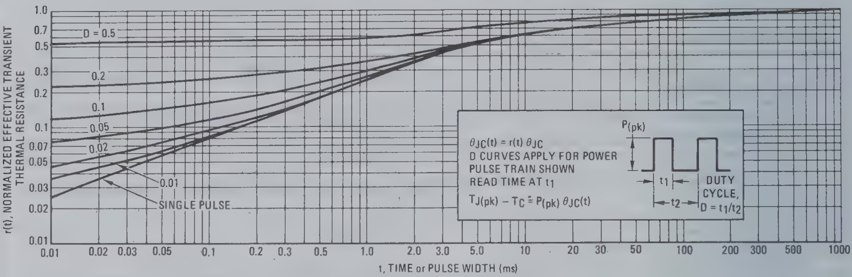
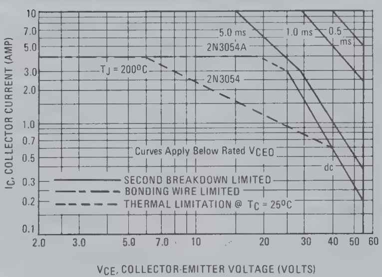


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

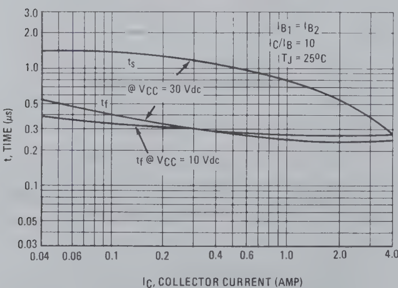


FIGURE 7 – CAPACITANCE

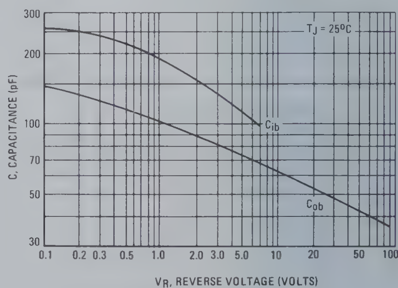


FIGURE 8 – DC CURRENT GAIN

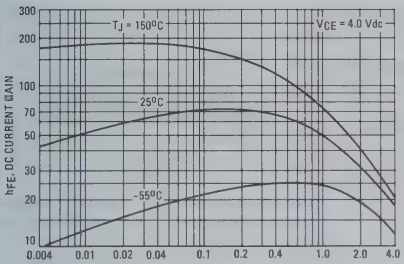


FIGURE 9 – COLLECTOR SATURATION REGION

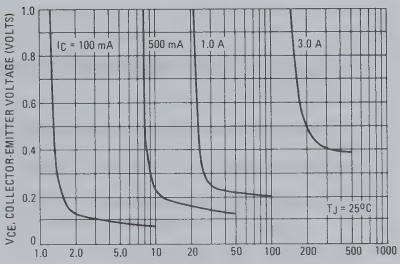


FIGURE 10 – TEMPERATURE COEFFICIENTS

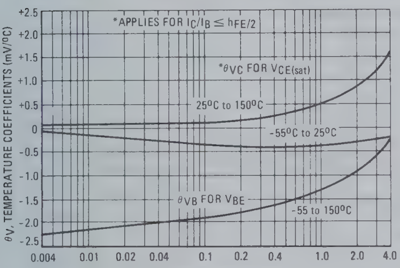


FIGURE 11 – "ON" VOLTAGES

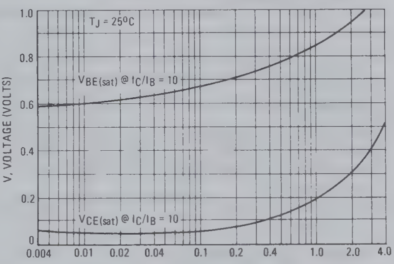


FIGURE 12 – COLLECTOR CUT-OFF REGION

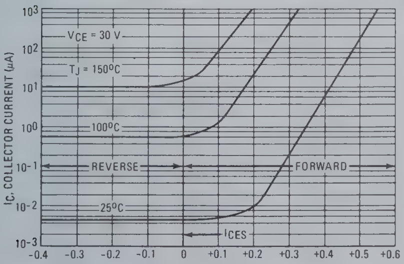
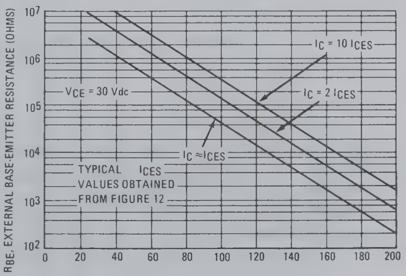


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



NPN 2N3055 PNP MJ2955

MOTOROLA

1.3

COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose switching and amplifier applications.

- DC Current Gain — h_{FE} = 20-70 @ I_C = 4 Adc
- Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4 Adc
- Excellent Safe Operating Area

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON

60 VOLTS
115 WATTS

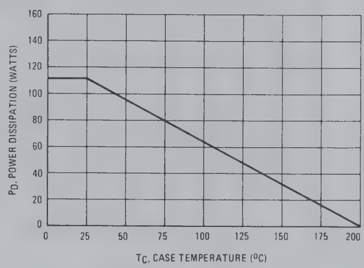
MAXIMUM RATINGS

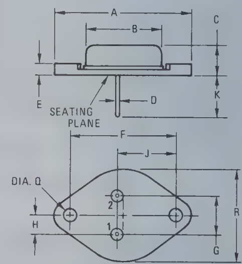
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Emitter Voltage	V_{CER}	70	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	7	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	115 0.657	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	$^oC/W$

FIGURE 1 – POWER DERATING





NOTE:
1. DIM "Q" IS DIA.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

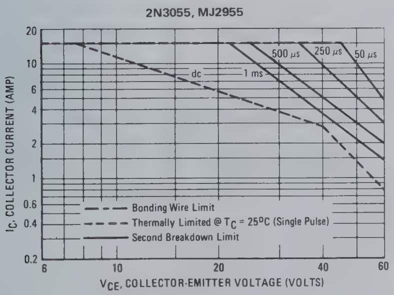
Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	70	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
***ON CHARACTERISTICS (1)**				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	70 –	–
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	–	1.1 3.0	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.5	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s; Nonrepetitive)	$I_{s/b}$	2.87	–	Adc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	–	MHz
*Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	15	120	–
*Small-Signal Current Gain Cutoff Frequency (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	f_{hfe}	10	–	kHz

* Indicates Within JEDEC Registration. (2N3055)
(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2.0%.

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

NPN 2N3055 | PNP MJ2955

FIGURE 3 – DC CURRENT GAIN

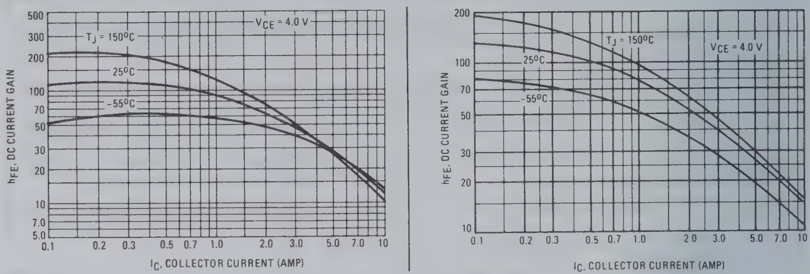


FIGURE 4 – COLLECTOR SATURATION REGION

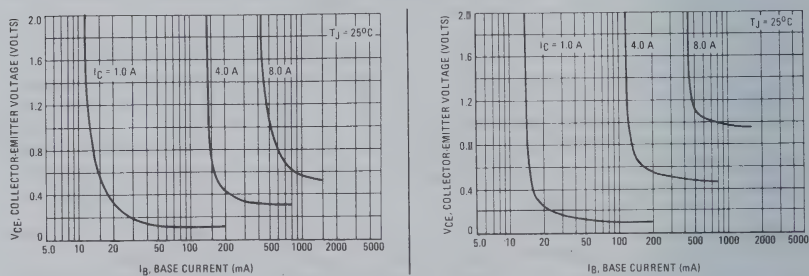
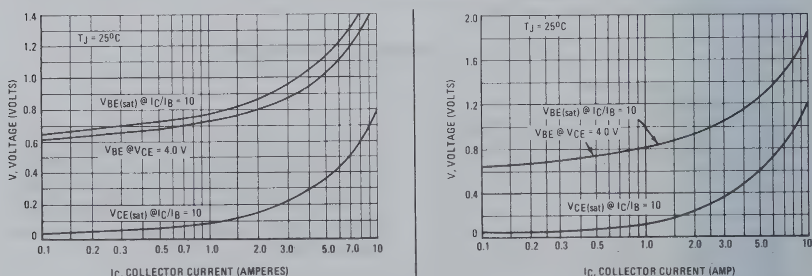


FIGURE 5 – "ON" VOLTAGES



MOTOROLA

NPN
2N3055A · MJ15015
PNP
MJ2955A · MJ15016

1.3

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

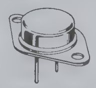
. . . PowerBase complementary transistors designed for high power audio, stepping motor and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc-to-dc converters, inverters, or for inductive loads requiring higher safe operating area than the 2N3055 and MJ2955.

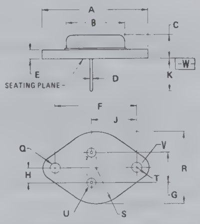
- Current-Gain — Bandwidth-Product @ I_C = 1.0 Adc
  f_T = 0.8 MHz (Min) — NPN
  = 2.2 MHz (Min) — PNP
- Safe Operating Area — Rated to 60 V and 120 V, Respectively

15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60, 120 VOLTS
115, 180 WATTS





STYLE 1.
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.
2. 001-02 OBSOLETE, NEW STANDARD 011-01 .
3. 001-01 OBSOLETE, NEW STANDARD 001-03.
4. DIAMETER V AND SURFACE W ARE DATUMS.
5. POSITIONAL TOLERANCE FOR HOLE Q:
   | ⌖ | ∅ 0.25 (0.010) Ⓜ | W | V Ⓜ |
6. POSITIONAL TOLERANCE FOR LEADS:
   | ⌖ | ∅ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ |

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12 19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

CASE 1-04
TO-204AA

*MAXIMUM RATINGS

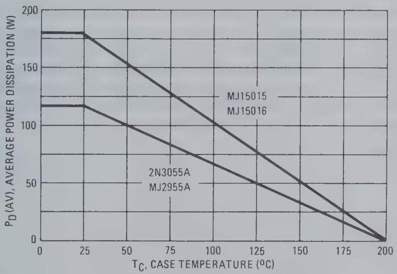
Rating	Symbol	2N3055A MJ2955A	MJ15015 MJ15016	Unit
Collector-Emitter Voltage	V_{CEO}	60	120	Vdc
Collector-Base Voltage	V_{CBO}	100	200	Vdc
Collector-Emitter Voltage Base Reversed Biased	V_{CEV}	100	200	Vdc
Emitter-Base Voltage	V_{EBO}	7.0		Vdc
Collector Current — Continuous	I_C	15		Adc
Base Current	I_B	7.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.65	180 1.03	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.52	0.98	°C/W

*Indicates JEDEC Registered Data (2N3055A)

FIGURE 1 — POWER DERATING



1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
*Collector-Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	2N3055A, MJ2955A MJ15015, MJ15016	$V_{CEO(sus)}$	60 120	– –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, $V_{BE(off)}$ = 0 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 0 Vdc)	2N3055A, MJ2955A MJ15015, MJ15016	I_{CEO}	– –	0.7 0.1	mAdc
*Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	2N3055A, MJ2955A MJ15015, MJ15016	I_{CEV}	– –	5.0 1.0	mAdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3055A, MJ2955A MJ15015, MJ15016	I_{CEV}	– –	30 6.0	mAdc
*Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	2N3055A, MJ2955A MJ15015, MJ15016	I_{EBO}	– –	5.0 0.2	mAdc
***SECOND BREAKDOWN**					
Second Breakdown Collector Current with Base Forward Biased (t = 0.5 s non-repetitive) (V_{CE} = 60 Vdc)	2N3055A, MJ2955A MJ15015, MJ15016	$I_{S/b}$	1.95 3.0	– –	Adc
***ON CHARACTERISTICS (1)**					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	10 20 5.0	70 70 –	–
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc) (I_C = 15 Adc, I_B = 7.0 Adc)		$V_{CE(sat)}$	– – –	1.1 3.0 5.0	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	0.7	1.8	Vdc
***DYNAMIC CHARACTERISTICS**					
Current-Gain—Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)	2N3055A, MJ15015 MJ2955A, MJ15016	f_T	0.8 2.2	6.0 18	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	60	600	pF
***SWITCHING CHARACTERISTICS (2N3055A only)**					
RESISTIVE LOAD					
Delay Time	(V_{CC} = 30 Vdc, I_C = 4.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, t_p = 25 μs Duty Cycle ≤ 2%)	t_d	–	0.5	μs
Rise Time		t_r	–	4.0	μs
Storage Time		t_s	–	3.0	μs
Fall Time		t_f	–	6.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.
*Indicates JEDEC Registered Data (2N3055A)

FIGURE 2 – DC CURRENT GAIN

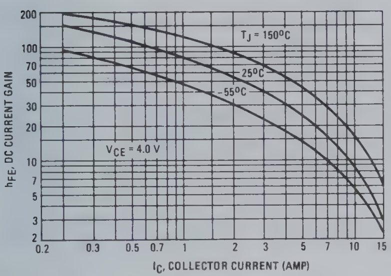


FIGURE 3 – COLLECTOR SATURATION REGION

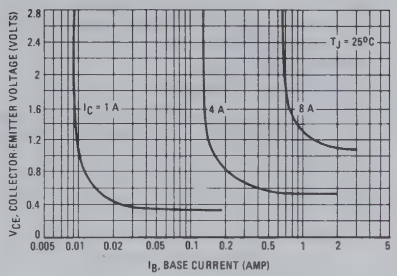


FIGURE 4 – "ON" VOLTAGES

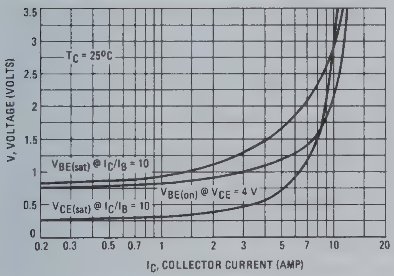


FIGURE 5 – CURRENT-GAIN–BANDWIDTH PRODUCT

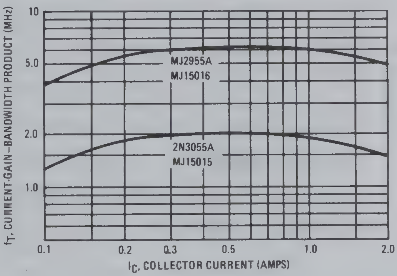


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT
(Circuit shown is for NPN)

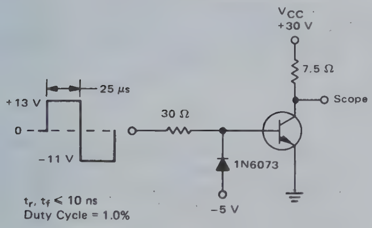
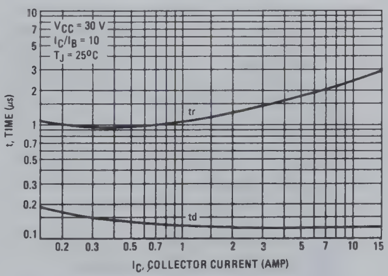


FIGURE 7 – TURN-ON TIME



1.3

FIGURE 8 – TURN-OFF TIMES

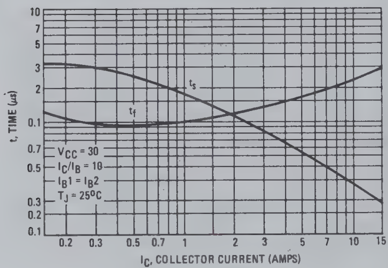
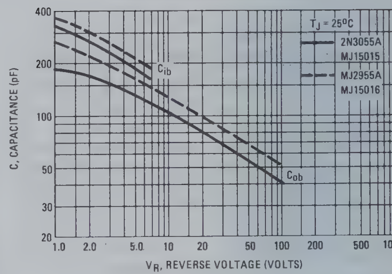


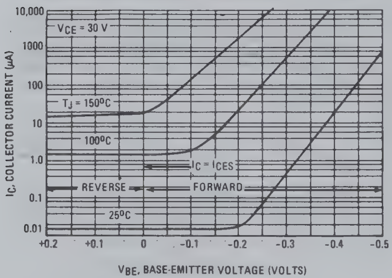
FIGURE 9 – CAPACITANCES



COLLECTOR CUT-OFF REGION

NPN

FIGURE 10 – 2N3055A, MJ15015



PNP

FIGURE 11 – MJ2955A, MJ15016

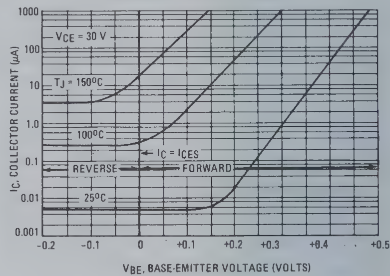


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA
2N3055A, MJ2955A

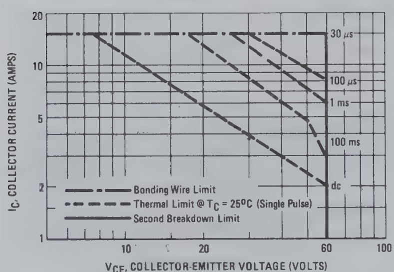
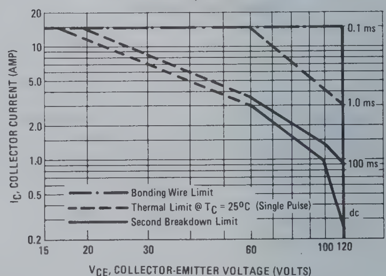


FIGURE 13 – FORWARD BIAS SAFE OPERATING AREA
MJ15015, MJ15016



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe Operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 12 and 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

MOTOROLA

NPN SILICON POWER TRANSISTOR

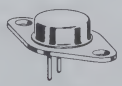
. . . 2N3441 transistor is designed for use in general-purpose switching and linear amplifier applications requiring high breakdown voltages. It is characterized for use as:

- Driver for High Power Outputs
- Series and Shunt Regulators
- Audio and Servo Amplifiers
- Solenoid and Relay Drivers
- Power Switching Circuits

3 AMPERES

NPN SILICON
POWER TRANSISTOR

140 VOLTS
25 WATTS

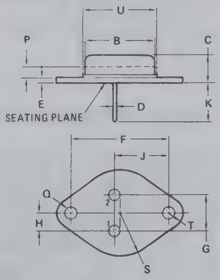


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	140	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector Current — Continuous	I_C	3	Adc
Base Current — Continuous	I_B	2	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	25 0.142	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7	$^oC/W$



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

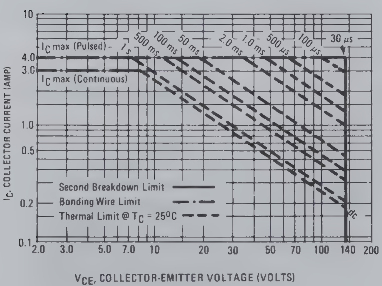
CASE 80-02
TO-66

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Adc, I_B = 0)	I_{CEO}	–	100	mA
Collector Cutoff Current	I_{CEX}			mA
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 V)		–	5.0	
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 V @ 150°C)		–	6.0	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mA
ON CHARACTERISTICS				
DC Current Gain (1)	h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 4.0 V)		25	100	
(I_C = 2.7 Adc, V_{CE} = 4.0 V)		5.0	–	
Collector-Emitter Saturation Voltage (1) (I_C = 2.7 Adc, I_B = 0.9 Adc)	$V_{CE(sat)}$	–	6.0	Vdc
Base-Emitter On Voltage (1) (I_C = 2.7 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	-	6.7	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1 kHz)	h_{fe}	15	75	-
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f_{test} = 0.4 MHz)	$\|h_{fe}\|$	5.0	–	–

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA

2N3442
2N4347

HIGH-POWER INDUSTRIAL TRANSISTORS

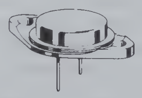
NPN silicon power transistors designed for applications in industrial and commercial equipment including high fidelity audio amplifiers, series and shunt regulators and power switches.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 2.0 Adc — 2N4347
- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 120 Vdc (Min) — 2N4347
  140 Vdc (Min) — 2N3442
- Excellent Second-Breakdown Capability

5.0 AND 10 AMPERE

POWER TRANSISTORS
NPN SILICON

120, 140 VOLTS
100, 117 WATTS



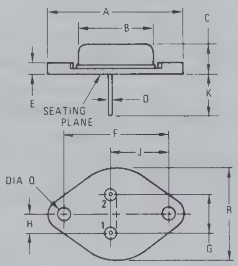
*MAXIMUM RATINGS

Rating	Symbol	2N4347	2N3442	Unit
Collector-Emitter Voltage	V_{CEO}	120	140	Vdc
Collector-Base Voltage	V_{CB}	140	160	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	5.0 10	10 15**	Adc
Base Current — Continuous Peak	I_B	3.0 8.0	7.0 —	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.57	117 0.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N4347	2N3442	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	1.5	°C/W

*Indicates JEDEC Registered Data.
**This data guranteed in addition to JEDEC registered data.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37	–	1.550
B	–	21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	–	1.050

Collector connected to case
CASE 11-01
(TO-3)

1.3

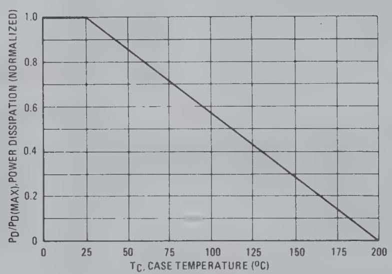
ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	2N4347	$V_{CEO(sus)}$	120	–	Vdc
	2N3442		140	–	
Collector Cutoff Current (V_{CE} = 100 Vdc, I_B = 0)	2N4327	I_{CEO}	–	200	mAdc
(V_{CE} = 140 Vdc, I_B = 0)	2N3422		–	200	
Collector Cutoff Current (V_{CE} = 125 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4347	I_{CEX}	–	2.0	mAdc
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3442		–	5.0	
(V_{CE} = 120 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150^oC$)	2N4347		–	10	
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150^oC$)	2N3442		–	30	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	2N4347, 2N3442	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)	2N4347	h_{FE}	15	60	–
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	2N4347		10	–	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N3442		20	70	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3442		7.5	–	
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)	2N4347	$V_{CE(sat)}$	–	1.0	Vdc
(I_C = 5.0 Adc, I_B = 0.63 Adc)	2N4347		–	2.0	
(I_C = 10 Adc, I_B = 2.0 Adc)	2N3442		–	5.0	
Base-Emitter On Voltage (I_C = 2.0 Adc; V_{CE} = 4.0 Vdc)	2N4347	$V_{BE(on)}$	–	2.0	Vdc
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	2N4347		–	3.0	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3442		–	5.7	
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f_{test} = 50 kHz)	2N4347	f_T	200	–	kHz
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 40 kHz)	2N3442		80	–	
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	2N4347	h_{fe}	40	–	–
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	2N3442		12	72	

*Indicates JEDEC Registered Data

NOTES: 1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
2. $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 1 — POWER DERATING



ACTIVE REGION SAFE OPERATING AREA INFORMATION

FIGURE 2 – 2N3442

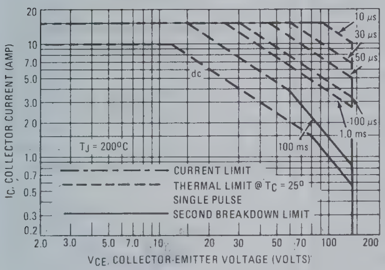
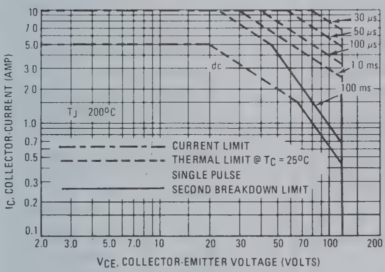


FIGURE 3 – 2N4347



There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 and 3 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 – DC CURRENT GAIN

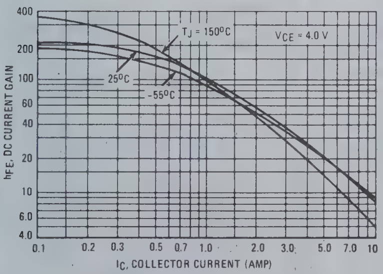
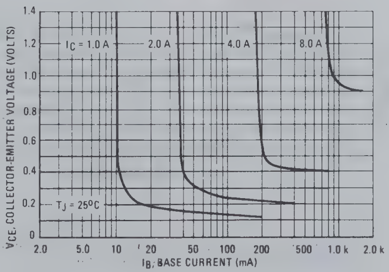


FIGURE 5 – COLLECTOR-SATURATION REGION



2N3445
thru
2N3448

MOTOROLA

1.3

HIGH-SPEED SILICON ANNULAR NPN POWER TRANSISTORS

. . . for switching and amplifier applications

FEATURES

- Fast Switching: Total Switching Time = 1.2 μs (Typ) @ 5.0 A
- High Gain: H_{FE} = 40 to 120 @ 5.0 Amps (2N3447-48)
- Guaranteed DC Safe Area: 1.5 Amps (Min) @ V_{CE} = 40 Vdc
- Low $V_{CE(sat)}$: 1.0 Volt (Typ), 1.5 Volts (Max) @ 5.0 Amps
- Excellent Beta Linearity

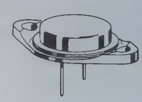
APPLICATIONS

- Specified safe area of this series allows reliable design for inverters, converters, hammer, and servo drivers.
- Fast response makes it ideal for series regulators; high switching speeds enhance its use in switching regulators.
- Wide bandwidth and flat beta hold-up result in exceptional amplifier characteristics.

7.5 AMPERE

POWER TRANSISTORS SILICON NPN

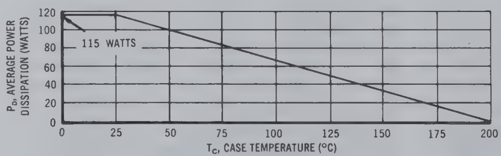
60-80 VOLTS
115 WATTS



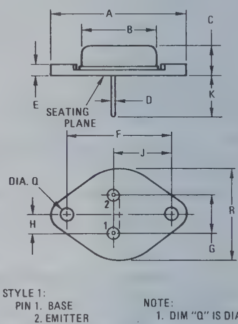
MAXIMUM RATING

Rating	Symbol	2N3445 2N3447	2N3446 2N3448	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0	10	Vdc
Collector Current-Continuous	I_C	7.5		Adc
Base Current - Continuous	I_B	4.0		Adc
Total Device Dissipation	P_D	Figure 1, 2	Figure 1, 3	Watts
Operating Junction Temperature Range	T_J	−65 to +200		°C

FIGURE 1 — POWER DERATING CURVE



These transistors are also subject to safe area curves as indicated by Figures 2, 3. Both limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Emitter-Base Cutoff Current		I_{EBO}				mAdc
(V_{EB} = 6 Vdc)	2N3445, 2N3447		–	–	0.25	
(V_{EB} = 10 Vdc)	2N3446, 2N3448		–	–	0.25	
Collector-Emitter Cutoff Current		I_{CEX}				mAdc
(V_{CE} = 60 Vdc, V_{BE} = –1 Vdc)	2N3445, 2N3447		–	–	0.1	
(V_{CE} = 60 Vdc, V_{BE} = –1 Vdc, T_C = 150°C)	2N3445, 2N3447		–	–	1.0	
(V_{CE} = 80 Vdc, V_{BE} = –1 Vdc)	2N3446, 2N3448		–	–	0.1	
(V_{CE} = 80 Vdc, V_{BE} = –1 Vdc, T_C = 150°C)	2N3446, 2N3448		–	–	1.0	
Collector-Emitter Cutoff Current		I_{CEO}				mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N3445, 2N3447		–	–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N3446, 2N3448		–	–	1.0	
Collector-Base Breakdown Voltage		BV_{CBO}				Vdc
(I_C = 1 mAdc, I_E = 0)	2N3445, 2N3447		80	–	–	
	2N3446, 2N3448		100	–	–	
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$				Vdc
(I_C = 100 mAdc, I_B = 0)	2N3445, 2N3447		60	–	–	
	2N3446, 2N3448		80	–	–	
DC Current Gain		h_{FE}				–
(I_C = 0.5 Adc, V_{CE} = 5 Vdc)	2N3445, 2N3446		20	45	–	
	2N3447, 2N3448		40	85	–	
(I_C = 3 Adc, V_{CE} = 5 Vdc)	2N3445, 2N3446		20	40	60	
(I_C = 5 Adc, V_{CE} = 5 Vdc)	2N3447, 2N3448		40	75	120	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 3 Adc, I_B = 0.3 Adc)	2N3445, 2N3446		–	0.6	1.5	
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3447, 2N3348		–	0.8	1.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 3 Adc, I_B = 0.3 Adc)	2N3445, 2N3446		–	1.0	1.5	
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3447, 2N3338		–	1.0	1.5	
Base-Emitter Voltage		V_{BE}				Vdc
(I_C = 3 Adc, V_{CE} = 5 Vdc)	2N3445, 2N3446		–	1.0	1.5	
(I_C = 5 Adc, V_{CE} = 5 Vdc)	2N3447, 2N3448		–	1.0	1.4	
Small Signal Current Gain		h_{fe}				–
(V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1 KHz)	2N3445, 2N3446		20	–	100	
	2N3447, 2N3448		40	–	200	
(V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 10 MHz)	All Types		1.0	1.6	–	
Common Base Output Capacitance		C_{ob}				pf
(V_{CB} = 10 Vdc, f = 0.1 MHz)	All Types		–	260	400	
Switching Times						μs
(V_{CC} = 25 Vdc, R_L = 5 ohms, I_C = 5 A, I_{B1} = I_{B2} = 0.5 A)						
Delay Time plus Rise Time		$t_d + t_r$	–	0.15	0.35	
Storage Time		t_s	–	0.9	2.0	
Fall Time		t_f	–	0.15	0.35	

SAFE OPERATING AREAS

FIGURE 2 – 2N3445, 2N3447

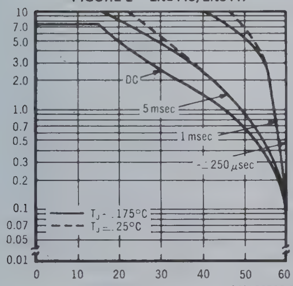
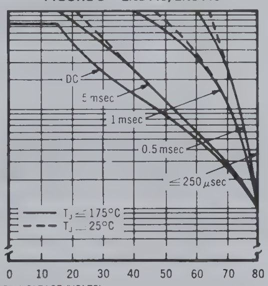


FIGURE 3 – 2N3446, 2N3448



V_{CE}, COLLECTOR-EMITTER VOLTAGE (VOLTS)

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

2N3583 thru 2N3585, 2N4240 NPN
2N6420 thru 2N6423 PNP

MOTOROLA

1.3

COMPLEMENTARY MEDIUM-POWER HIGH VOLTAGE POWER TRANSISTORS

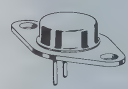
. . . designed for high-speed switching and linear amplifier applications for high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

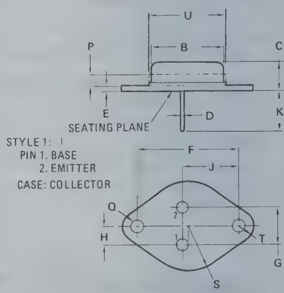
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 175 to 300 Vdc @ I_C = 200 mAdc
- Second Breakdown Collector Current —
  $I_{s/b}$ = 350 mAdc @ V_{CE} = 100 Vdc — NPN
  = 150 mAdc @ V_{CE} = 100 Vdc — PNP
- Usable DC Current Gain to 2.0 Adc

1.0 AND 2.0 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

250-500 VOLTS
35 WATTS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

*MAXIMUM RATINGS

Rating	Symbol	2N3583 2N6420	2N3584 2N6421	2N3585 2N6422	2N4240 2N6423	Unit
Collector-Emitter Voltage	V_{CEO}	175	250	300	300	Vdc
Collector-Base Voltage	V_{CB}	250	375	500	500	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →				Vdc
Collector Current — Continuous	I_C	1.0	← 2.0 →			Adc
— Peak (1)		5.0	← 5.0 →			
Base Current	I_B	← 1.0 →				Adc
Total Power Dissipation @ $T_C = 25^oC$,	P_D	← 35 →				Watts
Derate above 25^oC		← 0.2 →				$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →				^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.0	$^oC/W$

*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	NPN	PNP	Symbol	NPN Min	NPN Max	PNP Min	PNP Max	Unit
***OFF CHARACTERISTICS (1)**								
Collector-Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0) NPN	2N3583	2N6420	$V_{CEO(sus)}$	175	–	175	–	Vdc
	2N3584	2N6421		250	–	250	–	
	2N3585	2N6422		300	–	300	–	
(I_C = 50 mAdc, I_B = 0) PNP	2N4240	2N6423		300	–	300	–	
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	2N3583	2N6420	I_{CEO}	–	10		10	mAdc
	2N3584	2N6421		–	5.0	–	5.0	
	2N3585	2N6422		–	5.0	–	5.0	
	2N4240	2N6423		–	5.0	–	5.0	
Collector Cutoff Current (V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3583	2N6420	I_{CEX}	–	1.0	–	1.0	mAdc
(V_{CE} = 340 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3584	2N6421		–	1.0	–	1.0	
(V_{CE} = 450 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3585	2N6422		–	1.0	–	1.0	
	2N4240	2N6423		–	2.0	–	2.0	
(V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3583	2N6420		–	3.0	–	3.0	
(V_{CE} = 300 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3584	2N6421		–	3.0	–	3.0	
	2N3585	2N6422		–	3.0	–	3.0	
	2N4240	2N6423		–	5.0	–	5.0	
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	2N3583	2N6420	I_{EBO}	–	5.0	–	5.0	mAdc
	2N3584	2N6421			0.5	–	0.5	
	2N3585	2N6422		–	0.5		0.5	
	2N4240	2N6423		–	0.5	–	0.5	
ON CHARACTERISTICS (1)								
DC Current Gain	All	All	h_{FE}					–
(I_C = 0.1 Adc, V_{CE} = 10 Vdc)				40	–	40	–	
*(I_C = 0.5 Adc, V_{CE} = 10 Vdc)	2N3583	2N6420		40	200	40	200	
*(I_C = 0.75 Adc, V_{CE} = 2.0 Vdc)	2N4240	2N6423		10	100	10	100	
(I_C = 0.75 Adc, V_{CE} = 10 Vdc)	2N4240	2N6423		30	150	30	150	
*(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	2N3584	2N6421		8.0	80	8.0	80	
	2N3585	2N6422		8.0	80	8.0	80	
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)	2N3583*	2N6420		10	–	10	–	
	2N3584	2N6421		25	100	25	100	
	2N3585	2N6422		25	100	25	100	
*Collector-Emitter Saturation Voltage (I_C = 0.75 Adc, I_B = 75 mAdc)	2N4240	2N6423	$V_{CE(sat)}$	–	1.0	–	1.0	Vdc
(I_C = 1.0 Adc, I_B = 125 mAdc)	2N3583	2N6420		–	5.0	–	5.0	
	2N3584	2N6421		–	0.75	–	0.75	
	2N3585	2N6422		–	0.75	–	0.75	
*Base-Emitter Saturation Voltage (I_C = 0.75 Adc, I_B = 75 mAdc)	2N4240	2N6423	$V_{BE(sat)}$	–	1.8	–	1.8	Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc)	2N3584	2N6421		–	1.4	-	1.4	
	2N3585	2N6422		–	1.4	–	1.4	
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)	All	All	$V_{BE(on)}$	–	1.4	–	1.4	Vdc

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

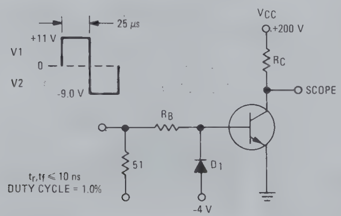
ELECTRICAL CHARACTERISTICS ($T_C = 25^{o}C$ unless otherwise noted.)

Characteristic	NPN	PNP	Symbol	NPN Min	NPN Max	PNP Min	PNP Max	Unit
DYNAMIC CHARACTERISTICS								
*Current Gain – Bandwidth Product[1] (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 5.0 MHz)	2N3583	2N6420	f_T	10	–	10	–	MHz
	2N3584	2N6421						
	2N3585	2N6422						
	2N4240	2N6423		15	–	15	–	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	All		C_{ob}	–	120	–	120	pF
*Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 30 Vdc; f = 1.0 kHz)	2N3583	2N6420	h_{fe}	25	350	25	350	–
***SWITCHING CHARACTERISTICS**								
Rise Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, R_L = 200 Ohms, I_{B1} = 100 mAdc)	2N3584	2N6421	t_r	–	3.0	–	3.0	μs
	2N3585	2N6422						
(V_{CC} = 200 Vdc, I_C = 0.75 Adc, R_L = 267 Ohms, I_{B1} = 75 mAdc)	2N4240	2N6423		–	0.5	–	0.5	
Storage Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, $I_{B1} = I_{B2}$ = 100 mAdc)	2N3584	2N6421	t_s	–	4.0	–	4.0	μs
	2N3585	2N6422						
(V_{CC} = 200 Vdc, I_C = 0.75 Adc, $I_{B1} = I_{B2}$ = 75 mAdc)	2N4240	2N6423		–	6.0	–	6.0	
Fall Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, $I_{B1} = I_{B2}$ = 100 mAdc)	2N3584	2N6421	t_f	–	3.0	–	3.0	μs
	2N3585	2N6422						
(V_{CC} = 200 Vdc, I_C = 0.75 Adc, $I_{B1} = I_{B2}$ = 75 mAdc)	2N4240	2N6423		–	3.0	–	3.0	
Second Breakdown Collector Current (V_{CE} = 100 Vdc)	All	All	$I_{s/b}$	350	–	150	–	mAdc

*Indicates JEDEC Registered Data

(1) $f_T = |h_{fe}| \bullet f_{test}$.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA
FOR t_d and t_r, D1 IS DISCONNECTED AND V_2 = 0.
FOR PNP TEST CIRCUIT, REVERSE DIODE AND VOLTAGE POLARITIES.

NPN
2N3583 thru 2N3585,2N4240

PNP
2N6420 thru 2N6423

FIGURE 2 – TURN-ON TIME

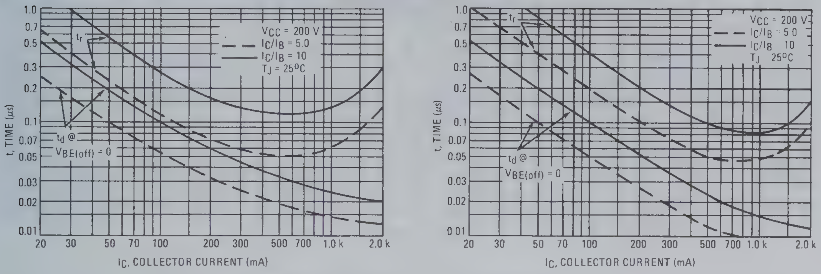


FIGURE 3 – TURN-OFF TIME

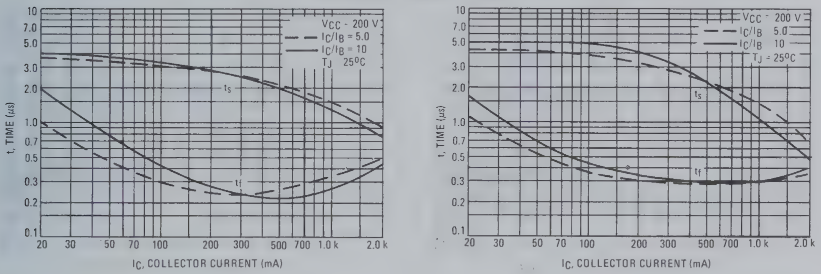


FIGURE 4 – CURRENT-GAIN – BANDWIDTH PRODUCT

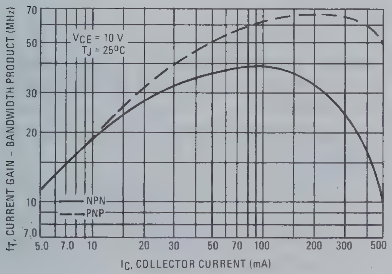
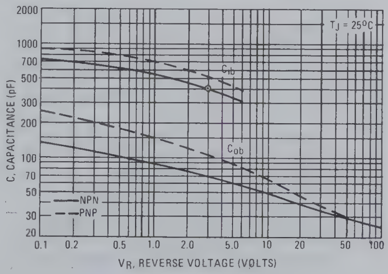
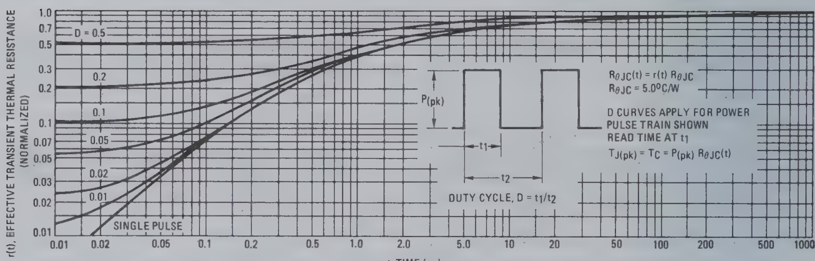


FIGURE 5 – CAPACITANCE



1.3

FIGURE 6 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 7 – 2N3583 thru 2N3585, 2N4240

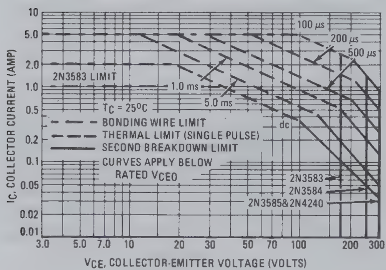


FIGURE 8 – 2N6420 thru 2N6423

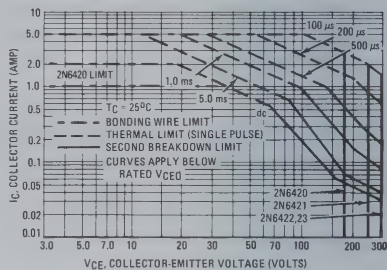
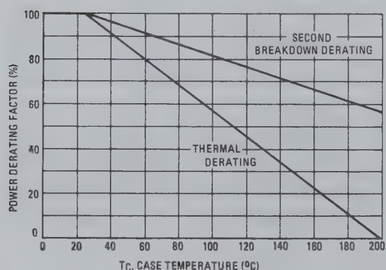


FIGURE 9 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 7 and 8 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 9.

$T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 7 and 8 may be found at any case temperature by using the appropriate curve on Figure 9.

NPN
2N3583 thru 2N3585,2N4240

PNP
2N6420 thru 2N6423

FIGURE 10 – DC CURRENT GAIN

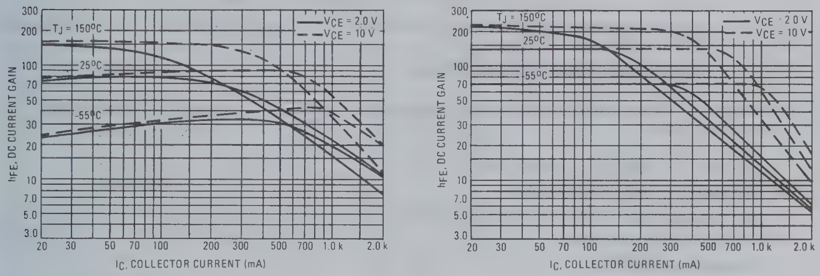


FIGURE 11 – COLLECTOR SATURATION REGION

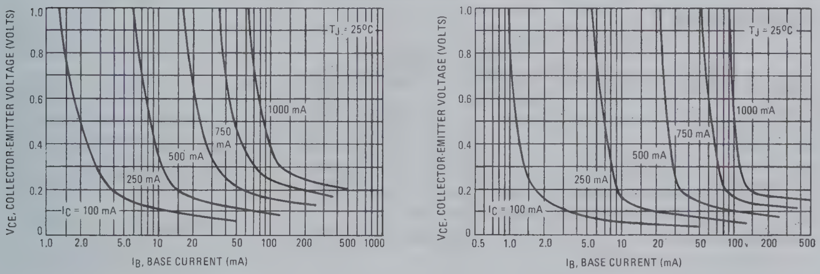
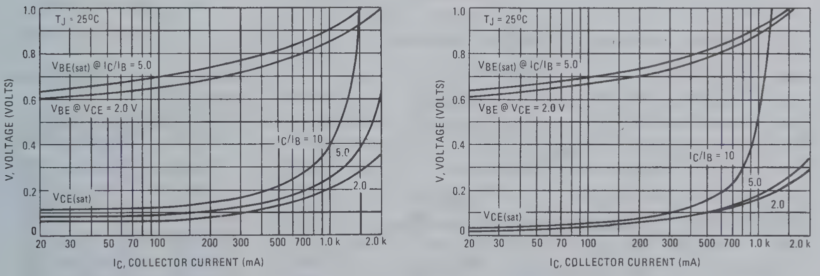


FIGURE 12 – "ON" VOLTAGES



NOTE: DC CURRENT LIMIT FOR 2N3583, 2N6420 is 1.0 Amp.

2N3713 thru 2N3716 NPN

MOTOROLA

1.3

SILICON NPN POWER TRANSISTORS

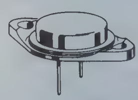
. . . designed for medium-speed switching and amplifier applications. These devices feature:

- Total Switching Time at 3 A typically 1.15 μs
- Gain Ranges Specified at 1 A and 3 A
- Low $V_{CE(sat)}$: typically 0.5V at I_C = 5A and I_B = 0.5A
- Excellent Safe Operating Areas
- Complement to 2N3789-92

10 AMPERE

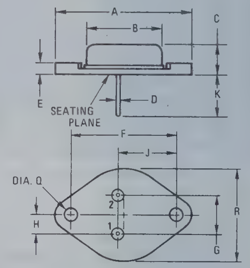
POWER TRANSISTORS
SILICON NPN

60-80 VOLTS
150 WATTS



MAXIMUM RATINGS

Rating	Symbol	2N3713 2N3715	2N3714 2N3716	Unit
Collector-Base Voltage	V_{CB}	80	100	Volts
Collector-Emitter Voltage	V_{CEO}	60	80	Volts
Emitter-Base Voltage	V_{EB}	7.0	7.0	Volts
Collector Current	I_C	10	10	Amps
Base Current	I_B	4.0	4.0	Amps
Power Dissipation	P_D	150	150	Watts
Thermal Resistance	θ_{JC}	1.17	1.17	$^oC/W$
Operating Junction and Storage Temperature Range	T_J and T_{stg}	-65 to +200		^oC



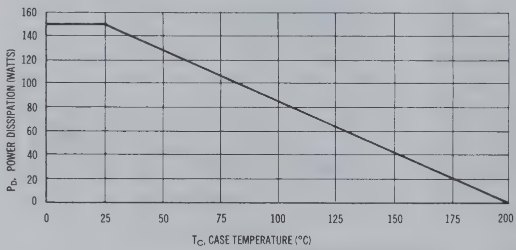
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



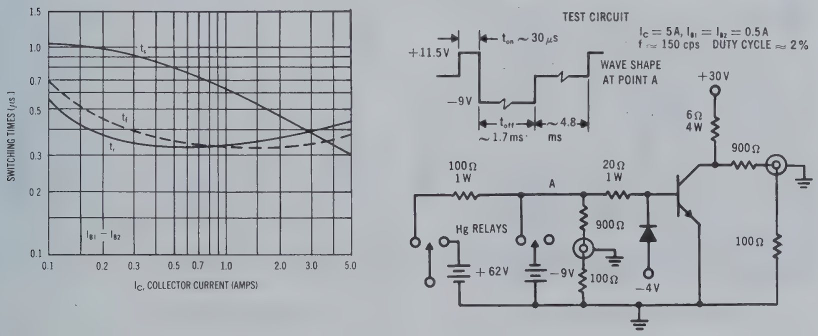
Safe Area Limits are indicated by Figures 12, 13. Both limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Emitter-Base Cutoff Current (V_{EB} = 7 Vdc)	All Types	I_{EBO}	—	5	mAdc
Collector-Emitter Cutoff Current (V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc) (V_{CE} = 100 Vdc, V_{BE} = -1.5 Vdc) (V_{CE} = 60 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C) (V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	 2N3713, 2N3715 2N3714, 2N3716 2N3713, 2N3715 2N3714, 2N3716	I_{CEX}	 — — — —	 1 1 10 10	mAdc
Collector-Emitter Sustaining Voltage* (I_C = 200 mAdc, I_B = 0)	 2N3713, 2N3715 2N3714, 2N3716	$V_{CEO(sus)}$*	 60 80	 — —	Vdc
DC Current Gain* (I_C = 1 Adc, V_{CE} = 2 Vdc) (I_C = 3 Adc, V_{CE} = 2 Vdc)	 2N3713, 2N3714 2N3715, 2N3716 2N3713, 2N3714 2N3715, 2N3716	h_{FE}*	 25 50 15 30	 90 150 — —	—
Collector-Emitter Saturation Voltage* (I_C = 5 Adc, I_B = 0.5 Adc)	 2N3713, 2N3714 2N3715, 2N3716	$V_{CE(sat)}$*	 — —	 1.0 0.8	Vdc
Base-Emitter Saturation Voltage* (I_C = 5 Adc, I_B = 0.5 Adc)	 2N3713, 2N3714 2N3715, 2N3716	$V_{BE(sat)}$*	 — —	 2.0 1.5	Vdc
Base-Emitter Voltage* (I_C = 3 Adc, V_{CE} = 2 Vdc)	All Types	V_{BE}*	—	1.5	Vdc
Small Signal Current Gain (V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1 MHz)	All Types	h_{fe}	4	—	—
Switching Times (Figure 2) (I_C = 5 A, I_{B1} = I_{B2} = 0.5 Adc) Rise Time Storage Time Fall Time		 t_r t_s t_f	Typ 0.45 0.3 0.4		μs

*Use sweep test to prevent overheating

FIGURE 2 – TYPICAL SWITCHING TIMES



1.3

FIGURE 3 – COLLECTOR CURRENT versus BASE CURRENT

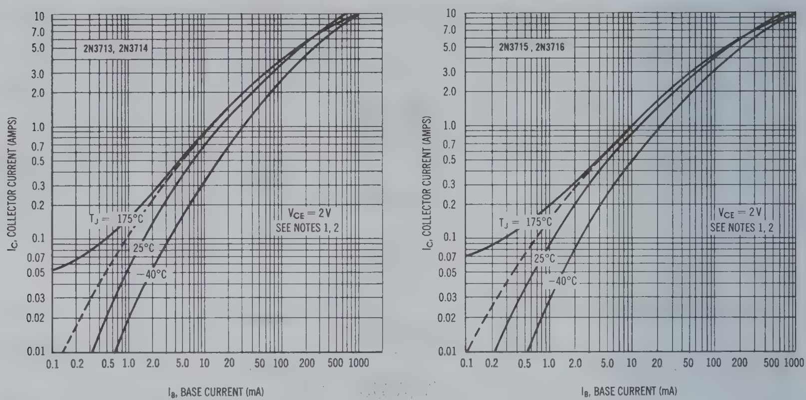


FIGURE 4 – BASE CURRENT-VOLTAGE VARIATIONS

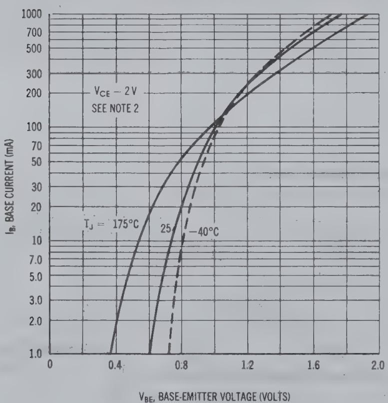
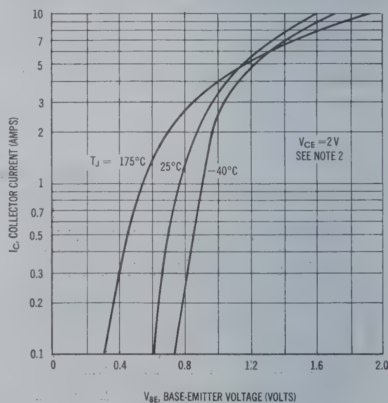


FIGURE 5 – COLLECTOR CURRENT-VOLTAGE VARIATIONS



NOTE 1. Dotted line indicates metered base current plus the I_{CBO} of the transistor at 175°C.

NOTE 2. Pulse test: pulse width ≈ 200 μsec, duty cycle ≈ 1.5%

FIGURE 6 – COLLECTOR-EMITTER SATURATION VOLTAGE VARIATIONS

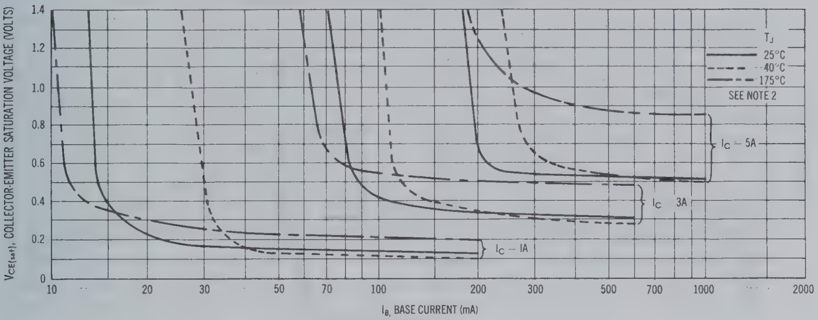


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE VARIATIONS

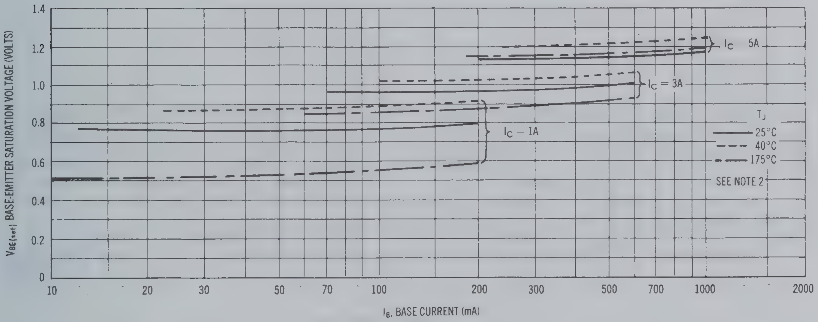


FIGURE 8 – COLLECTOR CURRENT versus BASE-EMITTER VOLTAGE

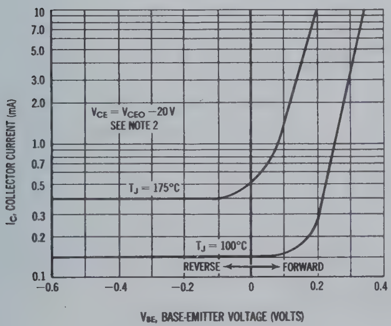


FIGURE 9 – COLLECTOR CURRENT versus BASE-EMITTER RESISTANCE

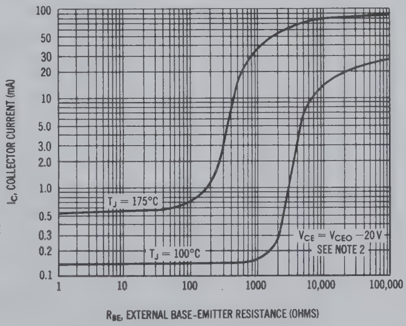


FIGURE 10 – CURRENT GAIN VARIATIONS

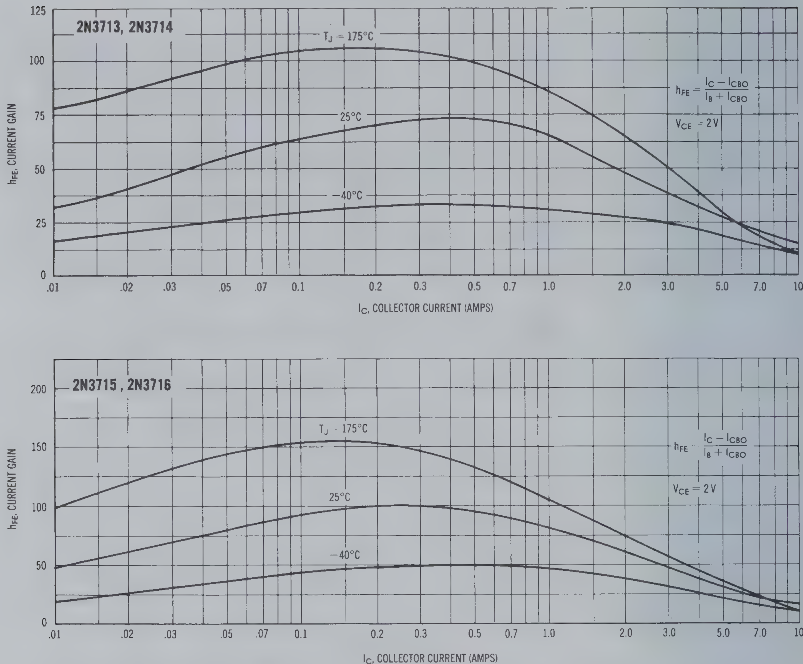
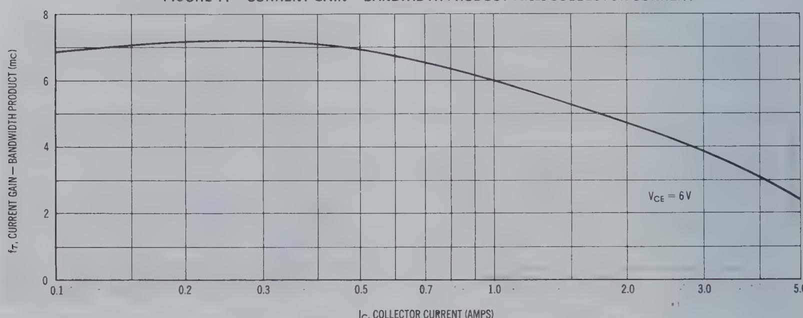


FIGURE 11 – CURRENT GAIN – BANDWIDTH PRODUCT versus COLLECTOR CURRENT



SAFE OPERATING AREAS

FIGURE 12 – 2N3713, 2N3715

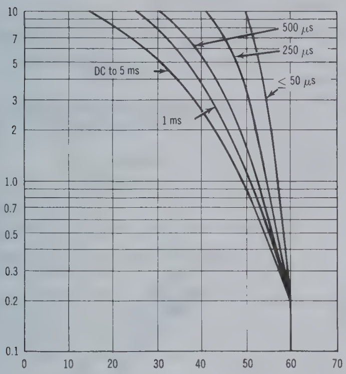
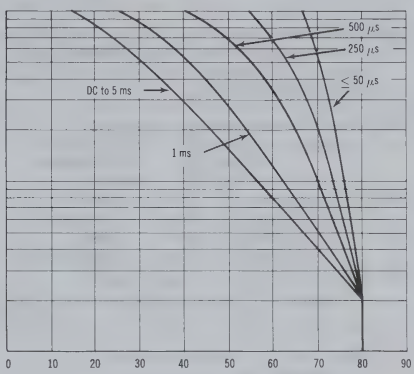


FIGURE 13 – 2N3714, 2N3716



I_C, COLLECTOR CURRENT (AMPS)

V_{CE}, COLLECTOR-EMITTER VOLTAGE (VOLTS)

The Safe Operating Area Curves indicate I_C — V_{CE} limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

2N3719, 2N3720
2N3867, 2N3868
2N6303

MOTOROLA

1.3

SILICON PNP POWER TRANSISTORS

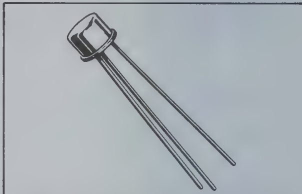
. . . designed for high-speed, medium-current switching and high-frequency amplifier applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc (Min) — 2N3719,2N3867
  = 60 Vdc (Min) — 2N3720,2N3868
  = 80 Vdc (Min) — 2N6303
- DC Current Gain —
  h_{FE} = 25-180 @ I_C = 1.0 Adc — 2N3719,2N3720
  = 40-200 @ I_C = 1.5 Adc — 2N3867
  = 30-150 @ I_C = 1.5 Adc — 2N3868,2N6303
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.75 Vdc @ I_C = 1.0 Adc — 2N3719,2N3720
  = 0.75 Vdc @ I_C = 1.5 Adc — 2N3867,2N3868, 2N6303
- High Current-Gain — Bandwidth Product —
  f_T = 90 MHz (Typ)
- 2N3867 JAN and 2N3868 JAN also Available

3 AMPERE

POWER TRANSISTORS
PNP SILICON

40,60,80 VOLTS
6 WATTS



*MAXIMUM RATINGS

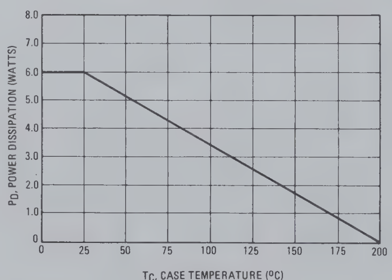
Rating	Symbol	2N3719 2N3867	2N3720 2N3868	2N6303	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}		4.0		Vdc
Collector Current — Continuous Peak	I_C		3.0 10		Adc
Base Current	I_B		0.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		6.0 34.3		Watts mW/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.0 5.71		Watt mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}		-65 to +200		°C

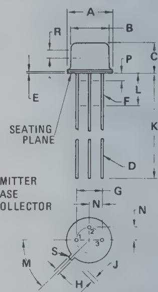
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	29	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	175	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.711	0.864	0.028	0.034
J	0.734	1.14	0.029	0.045
K	38.10	–	1.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	
P	–	1.27	–	0.050
R	2.54	–	0.100	–
S	–	0.179	–	0.007

All JEDEC dimensions and notes apply.

CASE 31-03
TO-5

1.3

*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 20 mAdc, I_B = 0)	2N3867	$V_{CEO(sus)}$	40	–	Vdc
	2N3868		60	–	
	2N6303		80	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	2N3867	BV_{CBO}	40	–	Vdc
	2N3868		60	–	
	2N6303		80	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 2.0 Vdc)		I_{CEX}	–	1.0	μAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0, $T_C = 150^oC$)		I_{CBO}	–	150	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)	2N3867	h_{FE}	50	–	–
	2N3868, 2N6303		35	–	
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N3867		40	200	
	2N3868, 2N6303		30	150	
(I_C = 2.5 Adc, V_{CE} = 3.0 Vdc)	2N3867		25	–	
	2N3868, 2N6303		20	–	
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	2N3867		20	–	
	2N3868, 2N6303				
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)		$V_{CE(sat)}$	–	0.5	Vdc
(I_C = 1.5 Adc, I_B = 150 mAdc)			–	0.75	
(I_C = 2.5 Adc, I_B = 250 mAdc)			–	1.3	
Base-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)		$V_{BE(sat)}$	–	1.0	Vdc
(I_C = 1.5 Adc, I_B = 150 mAdc)			0.9	1.4	
(I_C = 2.5 Adc, I_B = 250 mAdc)			–	2.0	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f_{test} = 20 MHz)		f_T	60	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	120	pF
Input Capacitance (V_{EB} = 3.0 Vdc, I_C = 0, f = 0.1 MHz)		C_{ib}	–	1000	pF
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = 0, I_C = 1.5 Adc, I_{B1} = 150 mAdc)	t_d	–	35	ns
Rise Time		t_r	–	65	ns
Storage Time	(V_{CC} = 30 Vdc, I_C = 1.5 Adc, $I_{B1} = I_{B2}$ = 150 mAdc)	t_s	–	325	ns
Fall Time		t_f	–	75	ns

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.

1.3

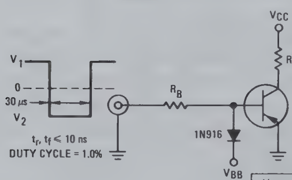
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 20 mAdc, I_B = 0)	2N3719		40	–	
	2N3720		60	–	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 2.0 Vdc)	2N3719		–	10	μAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 2.0 Vdc)	2N3720		–	10	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = 150°C)	2N3719		–	1.0	mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = 150°C)	2N3720		–	1.0	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N3719		–	10	
(V_{CB} = 60 Vdc, I_E = 0)	2N3720		–	10	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 4.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 1.5 Vdc)			20	–	
(I_C = 1.0 Adc, V_{CE} = 1.5 Vdc)			25	180	
(I_C = 1.0 Adc, V_{CE} = 1.5 Vdc, T_C = −40°C)			15	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc, T_C = −40°C to +100°C)			–	0.75	
(I_C = 3.0 Adc, I_B = 300 mAdc, T_C = −40°C to +100°C)			–	1.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc, T_C = −40°C to +100°C)			–	1.5	
(I_C = 3.0 Adc, I_B = 300 mAdc, T_C = −40°C to +100°C)			–	2.3	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2)		f_T			MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 30 MHz)			60	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			–	120	
Input Capacitance		C_{ib}			pF
(V_{EB} = 0.5 Vdc, I_C = 0, f = 0.1 MHz)			–	1000	
SWITCHING CHARACTERISTICS					
Turn-On Time		t_{on}			ns
(V_{CC} = 12 Vdc, $V_{BE(off)}$ = 0, I_C = 1.0 Adc, I_{B1} = 0.1 Adc)			–	100	
Turn-Off Time		t_{off}			ns
(V_{CC} = 12 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc)			–	400	

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%. (2) $f_T = |h_{fe}| \bullet f_{test}$.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



	2N3719 2N3720	2N3867 2N3868 2N6303
V_{CC}	−12 V	−30 V
R_C	12 Ω	19 Ω
R_B	100 Ω	100 Ω
V_1	+8.0 V	13.6 V
V_2	−11 V	−16.4 V
V_{BB}	≈ 3.0 V	≈ 3.0 V

NOTE:
For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.
For t_d and t_r specifications, remove diode and set V_I = 0.

FIGURE 3 – TURN-ON TIME

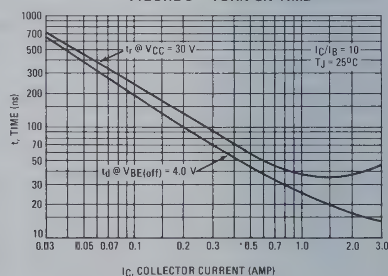


FIGURE 4 — THERMAL RESISTANCE

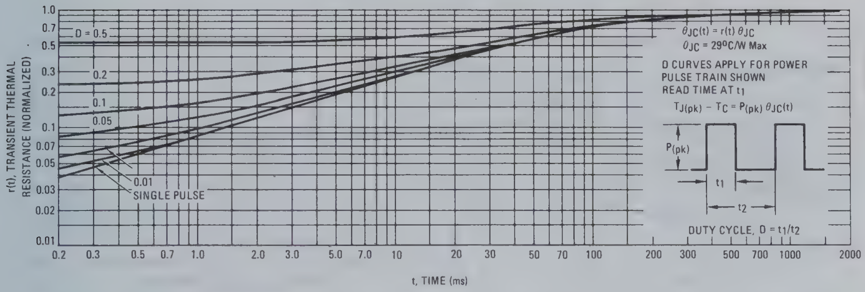
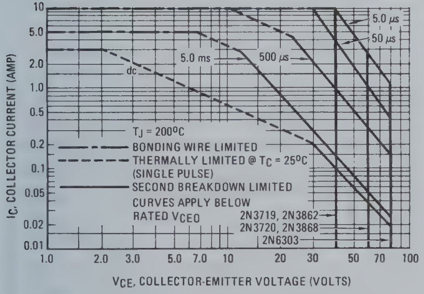


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — TURN-OFF TIME

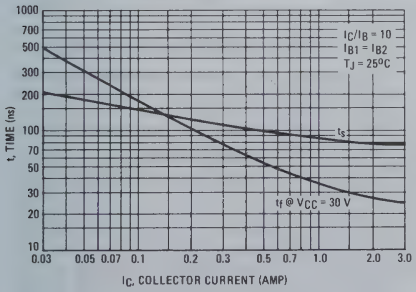


FIGURE 7 — CAPACITANCE

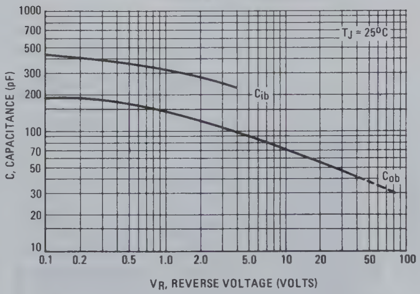


FIGURE 8 – DC CURRENT GAIN

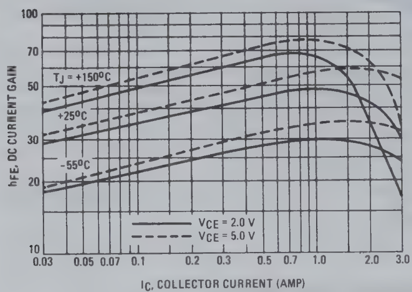


FIGURE 9 – COLLECTOR SATURATION REGION

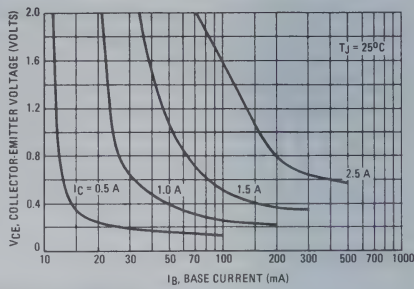


FIGURE 10 – "ON" VOLTAGES

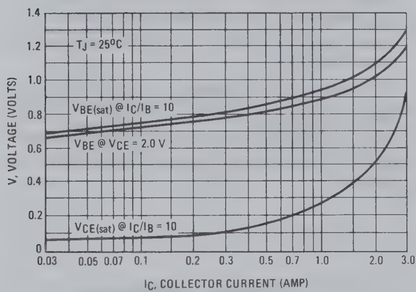


FIGURE 11 – TEMPERATURE COEFFICIENTS

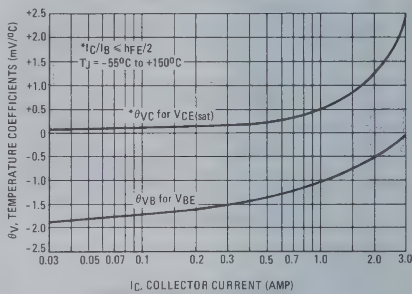


FIGURE 12 – COLLECTOR CUT-OFF REGION

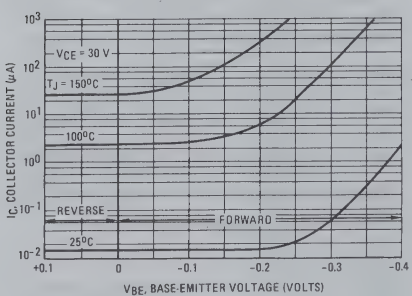
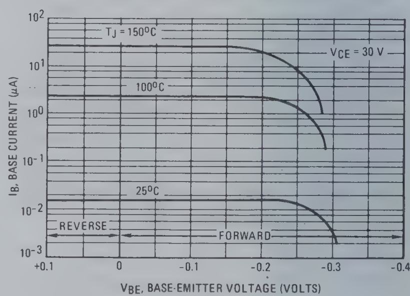


FIGURE 13 – BASE CUT-OFF REGION



2N3738, 2N3739 NPN
2N6424, 2N6425 PNP

MOTOROLA

HIGH VOLTAGE COMPLEMENTARY SILICON POWER TRANSISTORS

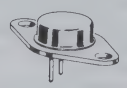
. . . designed for high-speed switching, linear amplifier applications, high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 225 Vdc @ I_C = 5.0 mAdc (2N3738, 2N6424)
  = 300 Vdc @ I_C = 5.0 mAdc (2N3739, 2N6425)
- DC Current Gain —
  h_{FE} = 40-200 @ I_C = 100 mAdc
- Current-Gain — Bandwidth Product —
  f_T = 10 MHz (Min) @ I_C = 100 mAdc
- $I_{S/b}$ Rated to 2.0 Amperes

1.0 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

225, 300 VOLTS
20 WATTS



*MAXIMUM RATINGS

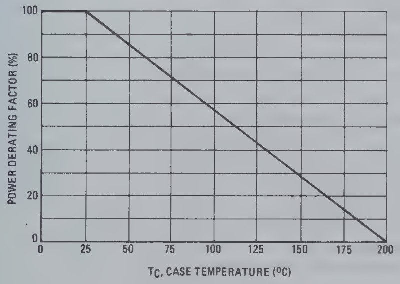
Rating	Symbol	2N3738 2N6424	2N3739 2N6425	Unit
Collector-Emitter Voltage	V_{CEO}	225	300	Vdc
Collector-Base Voltage	V_{CB}	250	325	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak	I_C	1.0 2.0		Adc
Base Current — Continuous — Peak	I_B	0.50 1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.133		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

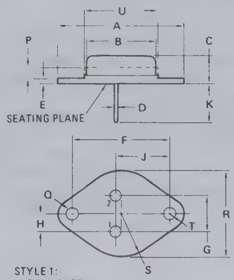
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.5	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

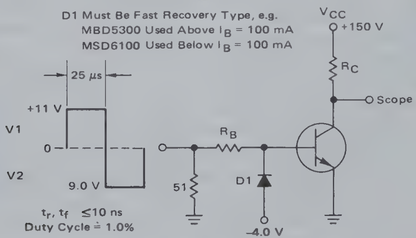
Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 5.0 mAdc, I_B = 0)	2N3738, 2N6424		225	–	
	2N3739, 2N6425		300	–	
Collector-Emitter Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 125 Vdc, I_B = 0)	2N3738, 2N6424		–	0.25	
(V_{CE} = 200 Vdc, I_B = 0)	2N3739, 2N6425		–	0.25	
Collector-Base Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 250 Vdc, I_E = 0)	2N3738, 2N6424		–	0.1	
(V_{CB} = 325 Vdc, I_E = 0)	2N3739, 2N6425		–	0.1	
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3738, 2N6424		–	0.5	
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3739, 2N6425		–	0.5	
(V_{CE} = 125 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N3738, 2N6424		–	1.0	
(V_{CE} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N3739, 2N6425		–	1.0	
Emitter-Base Cutoff Current (V_{EB} = 6.0 Vdc)		I_{EBO}		0.1	mAdc
***ON CHARACTERISTICS**					
DC Current Gain (1)		h_{FE}			–
(I_C = 50 mAdc, V_{CE} = 10 Vdc)			30	–	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)			40	200	
(I_C = 250 mAdc, V_{CE} = 10 Vdc)			25	–	
Collector-Emitter Saturation Voltage (1) (I_C = 250 mAdc, I_B = 25 mAdc)		$V_{CE(sat)}$		2.5	Vdc
Base-Emitter "ON" Voltage (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
SMALL SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	10	–	MHz
*Output Capacitance (V_{CB} = 100 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	20	pF
*Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 20 Vdc, f = 1.0 kHz)		h_{fe}	35	–	–

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

(2) $f_T = |h_{fe}| \bullet$ frequency

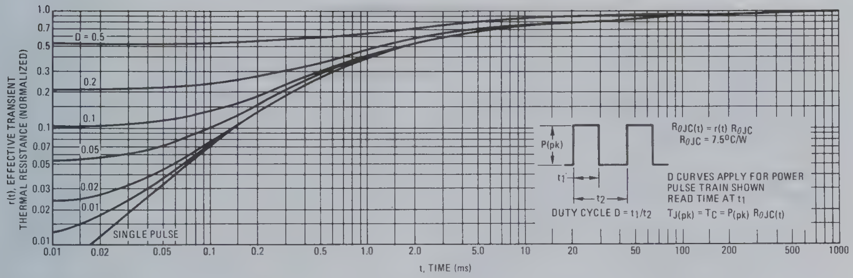
FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



R_B and R_C Varied to Obtain Desired Current Levels

For t_d and t_r, D1 is disconnected and V2 = 0
For PNP test circuit, reverse diode and voltage polarities.

FIGURE 3 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 4 – 2N3738, 2N3739

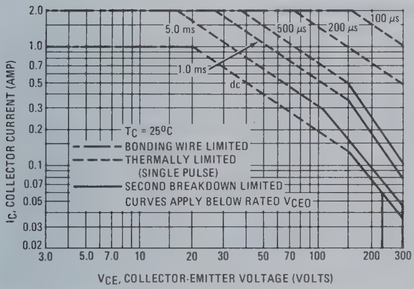
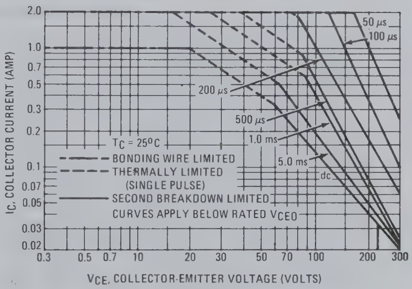


FIGURE 5 – 2N6424, 2N6425



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 4 and 5 is based on $T_C = 25^\circ C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 175^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 4 and 5 may be found at any case temperature by using the appropriate curve on Figure 1.

NPN 2N3738, 2N3739	PNP 2N6424, 2N6425

FIGURE 6 – DC CURRENT GAIN

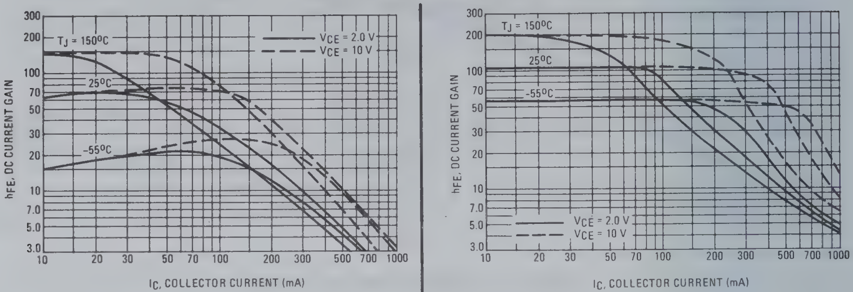


FIGURE 7 – COLLECTOR SATURATION REGION

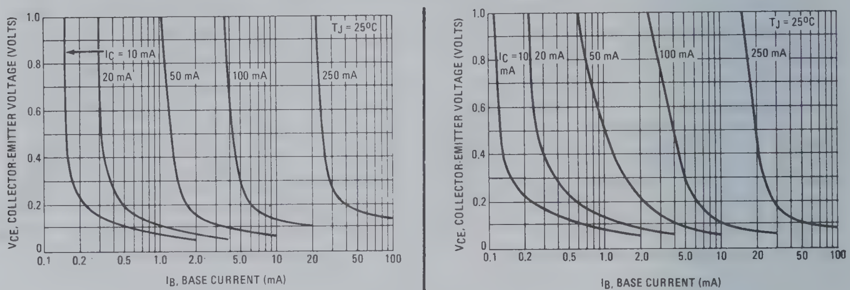
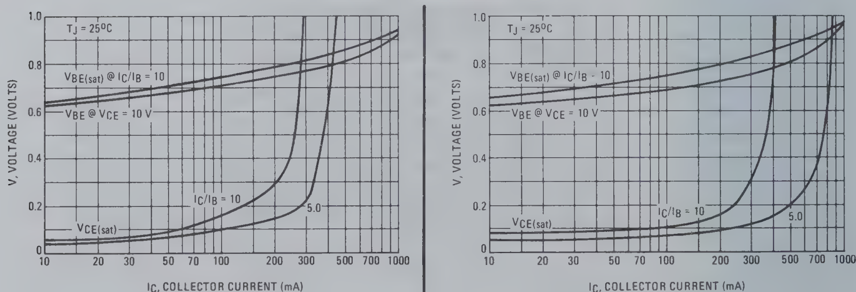


FIGURE 8 – "ON" VOLTAGE



2N3740,A
2N3741,A

MOTOROLA

1.3

MEDIUM-POWER PNP TRANSISTORS

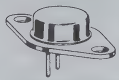
. . . ideal for use as drivers, switches and medium-power amplifier applications. These devices feature:

- Low Saturation Voltage — 0.6 $V_{CE(sat)}$ @ I_C = 1.0 Amp
- High Gain Characteristics — h_{FE}@ I_C = 250 mA: 30–100
- Excellent Safe Area Limits (See Figure 2)
- Low Collector Cutoff Current —
  100 nA (Max) 2N3740A, 2N3741A
- Complementary to NPN 2N3766 (2N3740) and 2N3767 (2N3741)

POWER TRANSISTORS

PNP SILICON

60–80 VOLTS
25 WATTS

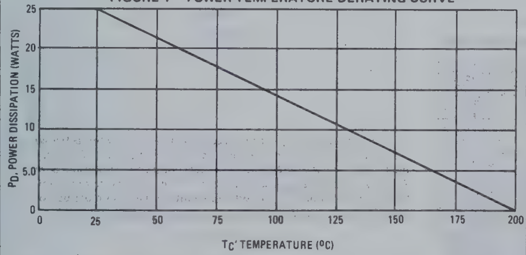


*MAXIMUM RATINGS

Rating	Symbol	2N3740 2N3740A	2N3741 2N3741A	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	7.0	7.0	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Collector Current — Continuous — Peak (Note 1)	I_C	4.0 10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	25 0.143		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

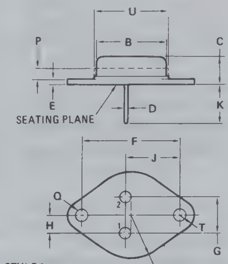
Note 1: See Figure 2

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2.
Both limits are applicable and must be observed.

*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

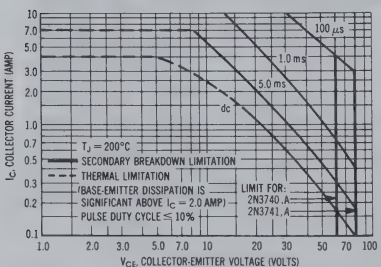
CASE 80-02
(TO-66)

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$ (1)			Vdc
(I_C = 100 mAdc, I_B = 0)	2N3740, 2N3740A		60	–	
	2N3741, 2N3741A		80	–	
Emitter Base Cutoff Current		I_{EBO}			
(V_{EB} = 7.0 Vdc)	2N3740, 2N3741		–	0.5	mAdc
	2N3740A, 2N3741A			100	nAdc
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3740		–	100	µAdc
	2N3740A		–	100	nAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3741		–	100	µAdc
	2N3741A		–	100	nAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3740		–	1.0	mAdc
	2N3740A		–	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3741		–	1.0	mAdc
	2N3741A		–	0.5	
Collector-Emitter Cutoff Current		I_{CEO}			
(V_{CE} = 40 Vdc, I_B = 0)	2N3740		–	1.0	mAdc
	2N3740A		–	1.0	µAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N3741		–	1.0	mAdc
	2N3741A		–	1.0	µAdc
Collector Base Cutoff Current		I_{CBO}			
(V_{CB} = 60 Vdc, I_E = 0)	2N3740		–	100	µAdc
	2N3740A		–	100	nAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N3741		–	100	µAdc
	2N3741A		–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE} (1)			–
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			40	–	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			30	100	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			20	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 125 mAdc)		$V_{CE(sat)}$ (1)	–	0.6	Vdc
Base-Emitter Voltage (I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		V_{BE} (1)	–	1.0	Vdc
TRANSIENT CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	–	MHz
			4.0†	–	
Common Base Output Capacitance (V_{CB} = 10 Vdc, I_C = 0, f = 100 kHz)		C_{ob}	–	100	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

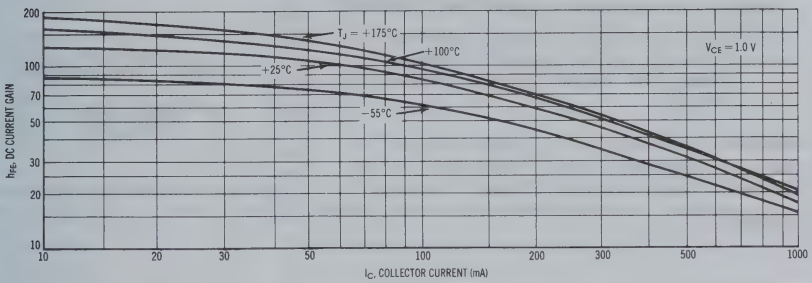
*Indicates JEDEC Registered Data.
†Motorola guarantees this value in addition to the JEDEC registered data shown.
(1) Pulse Test: Pulse Width ≤300 µs, Duty Cycle ≤2.0%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 3 – CURRENT GAIN



SATURATION REGION CHARACTERISTICS

FIGURE 4 – COLLECTOR SATURATION REGION

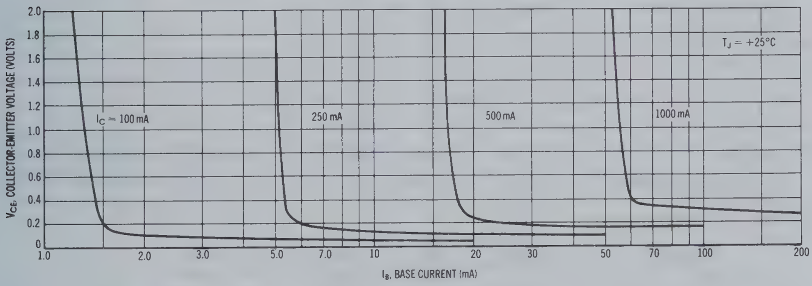


FIGURE 5 – "ON" VOLTAGES

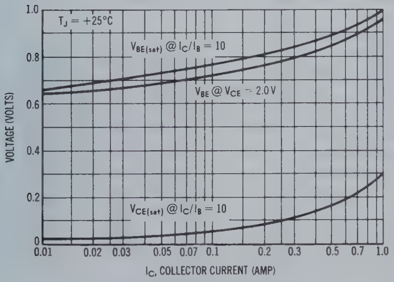
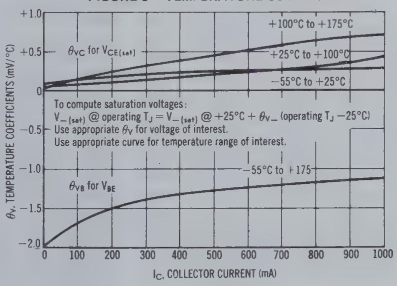


FIGURE 6 – TEMPERATURE COEFFICIENTS



2N3766
2N3767

MOTOROLA

1.3

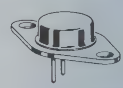
MEDIUM-POWER NPN SILICON TRANSISTORS

. . . for use in driver circuits, switching, and medium-power-amplifiers applications. These high performance devices feature:

- Low Saturation Voltage — 1.0 $V_{CE(sat)}$ @ I_C = 500 mA
- High Gain Characteristics — h_{FE} = 40-160 @ I_C = 500 mA
- Packaged in the Compact, High-Efficiency TO-66 Case
- Complementary to PNP 2N3740 (2N3766) and 2N3741 (2N3767)

4 AMPERE POWER TRANSISTORS

NPN SILICON
60-80 VOLTS
20 WATTS



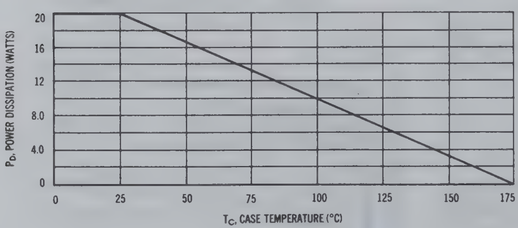
MAXIMUM RATINGS

Rating	Symbol	2N3766	2N3767	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.133		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

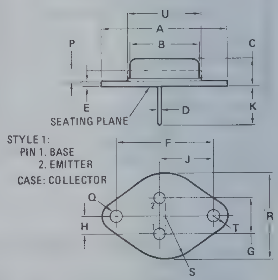
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	7.5	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2. Both limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

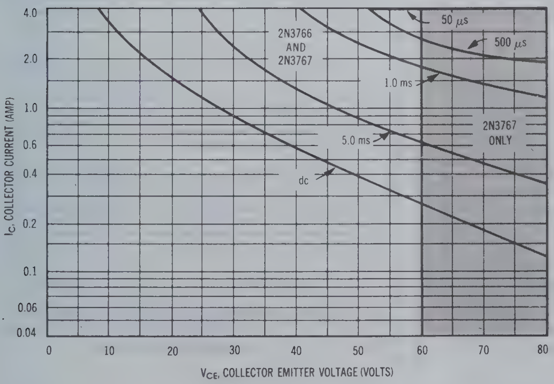
CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Voltage [1] (I_C = 100 mAdc, I_B = 0)	2N3766 2N3767	BV_{CEO}	60 80	— —	Vdc
Emitter-Base Cutoff Current (V_{EB} = 6.0 Vdc)		I_{EBO}	—	0.75	mAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{BE} = 1.5 Vdc) (V_{CE} = 100 Vdc, V_{BE} = 1.5 Vdc) (V_{CE} = 50 Vdc, V_{BE} = 1.5 Vdc, T_C = 150°C) (V_{CE} = 70 Vdc, V_{BE} = 1.5 Vdc, T_C = 150°C)	2N3766 2N3767 2N3766 2N3767	I_{CEX}	— — — —	0.1 0.1 1.0 1.0	mAdc
Collector-Emitter Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	2N3766 2N3767	I_{CEO}	— —	0.7 0.7	mAdc
Collector-Base Cutoff Current (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	2N3766 2N3767	I_{CBO}	— —	0.1 0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc) (I_C = 500 mAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		h_{FE}	30 40 20	— 160 —	—
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc) (I_C = 500 mAdc, I_B = 50 mAdc)		$V_{CE(sat)}$	— —	2.5 1.0	Vdc
Base-Emitter Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		V_{BE}	—	1.5	Vdc
TRANSIENT CHARACTERISTICS					
Current-Gain - Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	10	—	MHz
Common-Base Output Capacitance (V_{CB} = 10 Vdc, I_C = 0 Adc, f = 100 kHz)		C_{ob}	—	50	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	40	—	—

[1] Pulse Test: Pulse Width ≤300μs, Duty Cycle ≤2.0%.

FIGURE 2 — ACTIVE REGION SAFE AREAS



The Safe Operating Area Curves indicate I_C-V_{CE} limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Case temperature and duty cycle of the excursions make no significant change in these safe areas.) The load line may exceed the BV_{CEO} voltage limit only if the collector current has been reduced to 20 mA or less before or at the BV_{CES} limit; then and only then may the load line be extended to the absolute maximum voltage rating of BV_{CBO}. To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

1.3

LARGE SIGNAL CHARACTERISTICS

FIGURE 3 – TRANSCONDUCTANCE

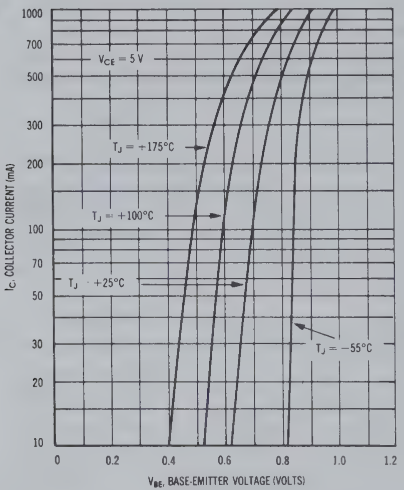
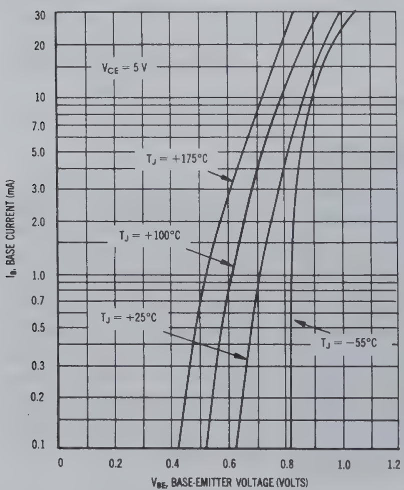


FIGURE 5 – INPUT ADMITTANCE



CUT-OFF CHARACTERISTICS

FIGURE 4 – TRANSCONDUCTANCE

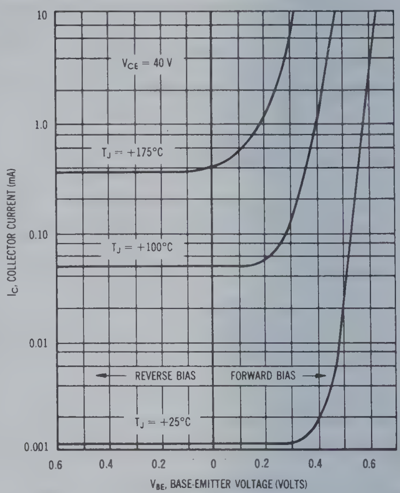


FIGURE 6 – EFFECT OF BASE-EMITTER RESISTANCE

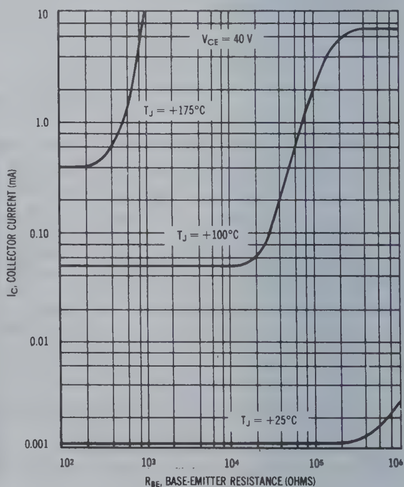


FIGURE 7 – CURRENT GAIN

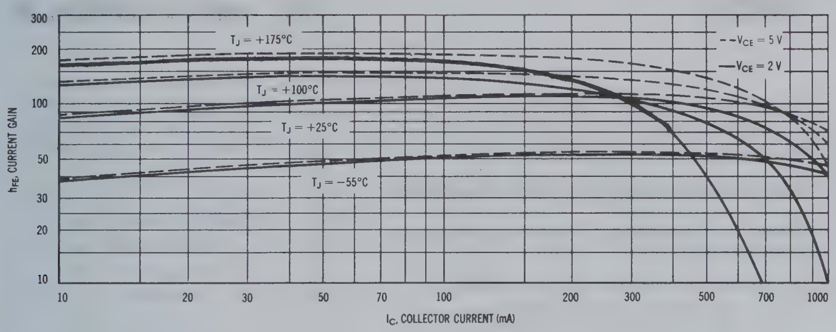


FIGURE 8 – COLLECTOR SATURATION REGION

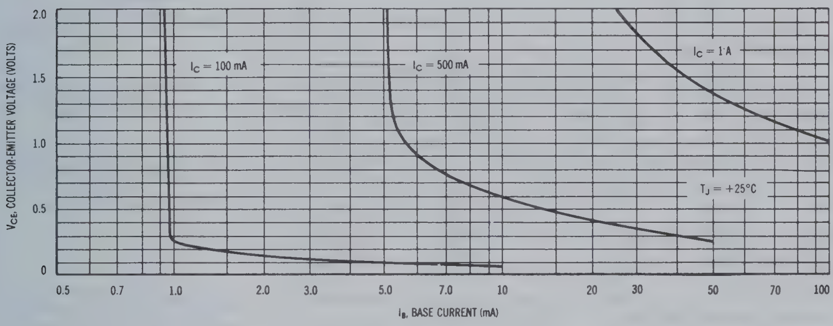


FIGURE 9 – "ON" VOLTAGES

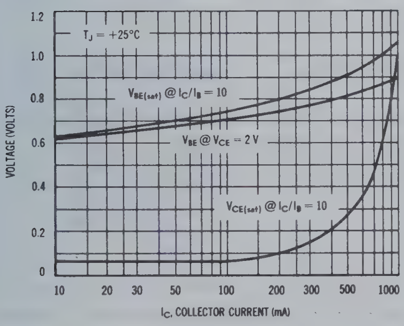
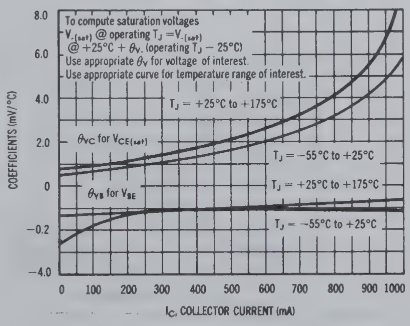


FIGURE 10 – TEMPERATURE COEFFICIENTS



2N3771 2N3772
2N6257

MOTOROLA

1.3

HIGH POWER NPN SILICON POWER TRANSISTORS

. . . designed for linear amplifiers, series pass regulators, and inductive switching applications.

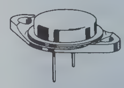
- Forward Biased Second Breakdown Current Capability

  $I_{S/b}$ = 3.75 Adc @ V_{CE} = 40 Vdc – 2N3771
  = 2.5 Adc @ V_{CE} = 60 Vdc – 2N3772
  = 3.75 Adc @ V_{CE} = 40 Vdc – 2N6257

20 and 30 AMPERE

POWER TRANSISTORS
NPN SILICON

40 and 60 VOLTS
150 WATTS



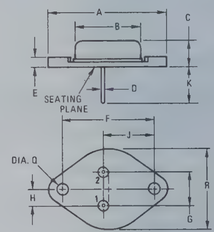
*MAXIMUM RATINGS

Rating	Symbol	2N3771	2N3772	2N6257	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	40	Vdc
Collector-Emitter Voltage	V_{CEX}	50	80	50	Vdc
Collector-Base Voltage	V_{CB}	50	100	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0	7.0	5.0	Vdc
Collector Current – Continuous Peak	I_C	30 30	20 30	20 30	Adc
Base Current – Continuous Peak	I_B	7.5 15	5.0 15	5.0 15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N3771, 2N3772, 2N6257	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data



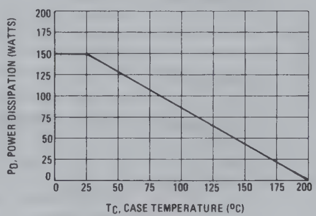
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.

CASE 11-01

FIGURE 1 – POWER DERATING



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (1)	2N3771	$V_{CEO(sus)}$	40	—	Vdc
(I_C = 0.2 Adc, I_B = 0)	2N3772		60	—	
	2N6257		40	—	
Collector-Emitter Sustaining Voltage	2N3771	$V_{CEX(sus)}$	50	—	Vdc
(I_C = 0.2 Adc, $V_{EB(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	2N3772		80	—	
	2N6257		50	—	
Collector-Emitter Sustaining Voltage	2N3771	$V_{CER(sus)}$	45	—	Vdc
(I_C = 0.2 Adc, R_{BE} = 100 Ohms)	2N3772		70	—	
	2N6257		45	—	
*Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N3771		—	10	
(V_{CE} = 50 Vdc, I_B = 0)	2N3772		—	10	
(V_{CE} = 25 Vdc, I_B = 0)	2N6527		—	10	
*Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3771		—	2.0	
(V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3772		—	5.0	
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6257		—	4.0	
(V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3771		—	10	
	2N3772		—	10	
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6527		—	20	
*Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 50 Vdc, I_E = 0)	2N3771		—	2.0	
	2N6257		—	4.0	
(V_{CB} = 100 Vdc, I_E = 0)	2N3772		—	5.0	
*Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)	2N3771		—	5.0	
	2N6257		—	10	
(V_{BE} = 7.0 Vdc, I_C = 0)	2N3772		—	5.0	
***ON CHARACTERISTICS**					
DC Current Gain (1)		h_{FE}			—
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)	2N3771		15	60	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3772		15	60	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	2N6257		15	75	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N3771		5.0	—	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N3772		5.0	—	
	2N6257		5.0	—	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 1.5 Adc)	2N3771		—	2.0	
(I_C = 10 Adc, I_B = 1.0 Adc)	2N3772		—	1.4	
(I_C = 8.0 Adc, I_B = 0.8 Adc)	2N6257		—	1.5	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N3771		—	4.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N3772		—	4.0	
	2N6257		—	4.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)	2N3771		—	2.7	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3772		—	2.2	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	2N6257		—	2.2	
***DYNAMIC CHARACTERISTICS**					
Current-Gain—Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 50 kHz)		f_T	0.2	—	MHz
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	40	—	—
SECOND BREAKDOWN					
Second Breakdown Energy with Base Forward Biased, t = 1.0 s (non-repetitive)		$I_{S/b}$			Adc
(V_{CE} = 40 Vdc)	2N3771		3.75	—	
	2N6257		3.75	—	
(V_{CE} = 60 Vdc)	2N3772		2.5	—	

*Indicates JEDEC Registered Data

(1) Pulse Test: 300 μs, Rep. Rate 60 cps.

FIGURE 2 — THERMAL RESPONSE — 2N3771, 2N3772, 2N6257

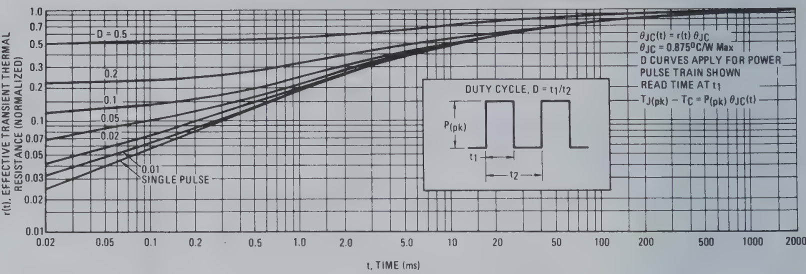
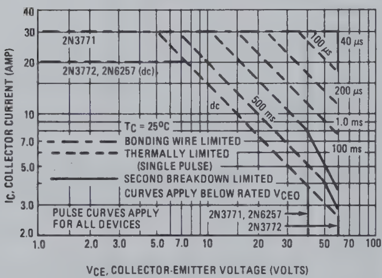


FIGURE 3 — ACTIVE-REGION SAFE OPERATING AREA — 2N3771, 2N3772, 2N6257



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based upon JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3, $T_{J(pk)}$ will be found to be less than $T_{J(max)}$ for pulse widths of 1 ms and less. When using Motorola transistors, it is permissible to increase the pulse power limits until limited by $T_{J(max)}$.

FIGURE 4 — SWITCHING TIME TEST CIRCUIT

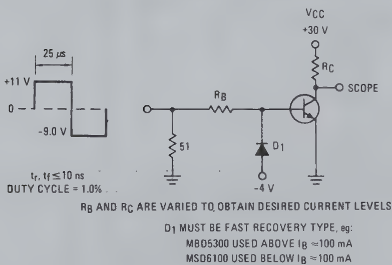


FIGURE 5 — TURN-ON TIME

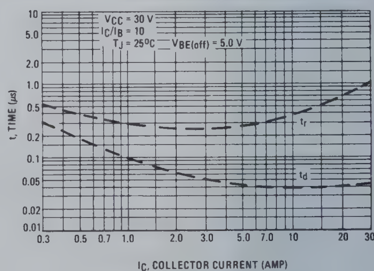


FIGURE 6 — TURN-OFF TIME

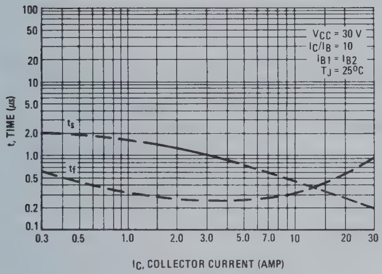


FIGURE 7 — CAPACITANCE

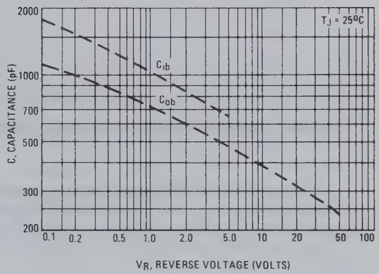


FIGURE 8 — DC CURRENT GAIN

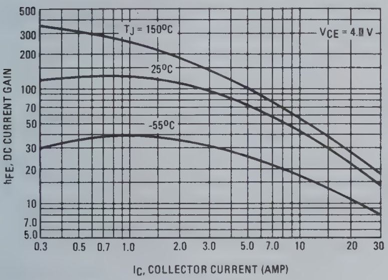
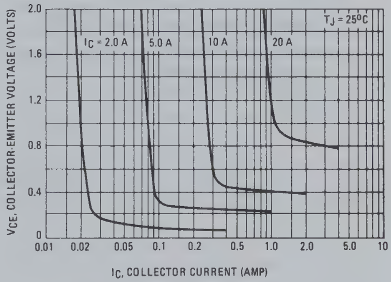


FIGURE 9 — COLLECTOR SATURATION REGION



NPN **2N3773** PNP **2N6609**

MOTOROLA

1.3

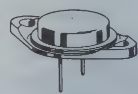
COMPLEMENTARY SILICON POWER TRANSISTORS

The 2N3773 and 2N6609 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc to dc converters or inverters.

- High Safe Operating Area (100% Tested)
  150 W @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{fe} = 15 (Min) @ 8 A, 4 V
  $V_{CE(sat)}$ = 1.4 V (Max) @ I_C = 8 A, I_B = 0.8 A
- For Low Distortion Complementary Designs

16 AMPERE COMPLEMENTARY POWER TRANSISTORS

140 VOLTS
150 WATTS



*MAXIMUM RATINGS

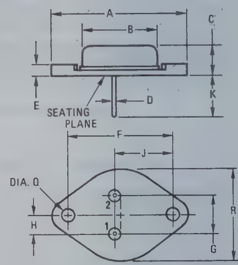
Rating	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	140	Vdc
Collector-Emitter Voltage	V_{CEX}	160	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector Current — Continuous — Peak (1)	I_C	16 30	Adc
Base Current — Continuous — Peak (1)	I_B	4 15	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
*Collector-Emitter Breakdown Voltage (I_C = 0.2 Adc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
*Collector-Emitter Sustaining Voltage (I_C = 0.1 Adc, $V_{BE(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	$V_{CEX(sus)}$	160	–	Vdc
Collector-Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	150	–	Vdc
*Collector Cutoff Current (V_{CE} = 120 Vdc, I_B = 0)	I_{CEO}	–	10	mAdc
*Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 – –	 2 10	mAdc
Collector Cutoff Current (V_{CB} = 140 Vdc, I_E = 0)	I_{CBO}	–	2	mAdc
*Emitter Cutoff Current (V_{BE} = 7 Vdc, I_C = 0)	I_{EBO}	–	5	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain *(I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)	h_{FE}	 15 5	 60 	–
Collector-Emitter Saturation Voltage *(I_C = 8 Adc, I_B = 800 mAdc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 – –	 1.4 4	Vdc
*Base-Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	–	2.2	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common-Emitter Small-Signal, Short-Circuit, Forward Current Transfer Ratio (I_C = 1 A, f = 50 kHz)	$\|h_{fe}\|$	4	–	–
*Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	40	–	–
SECOND BREAKDOWN CHARACTERISTICS				
Second Breakdown Collector Current with Base Forward Biased t = 1 s (non-repetitive), V_{CE} = 100 V, See Figure 12	$I_{S/b}$	1.5	–	Adc

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

*Indicates JEDEC Registered Data

NPN

FIGURE 1 – DC CURRENT GAIN

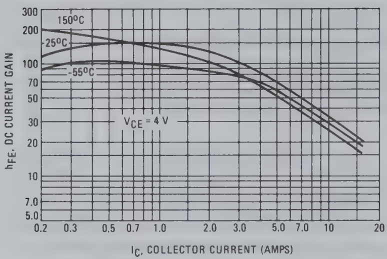


FIGURE 3 – COLLECTOR SATURATION REGION

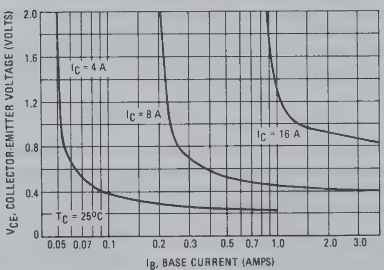
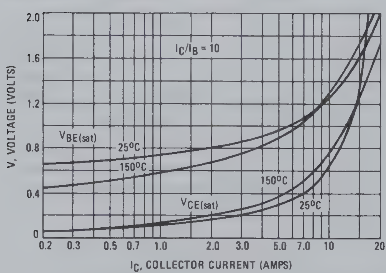


FIGURE 5 – "ON" VOLTAGE



PNP

FIGURE 2 – DC CURRENT GAIN

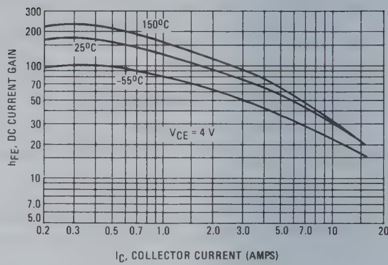


FIGURE 4 – COLLECTOR SATURATION REGION

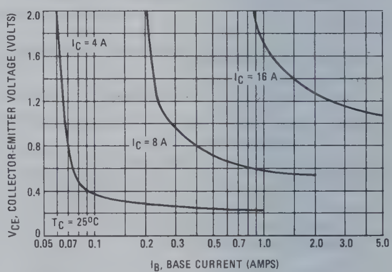


FIGURE 6 – "ON" VOLTAGE

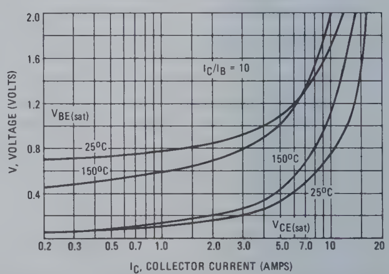
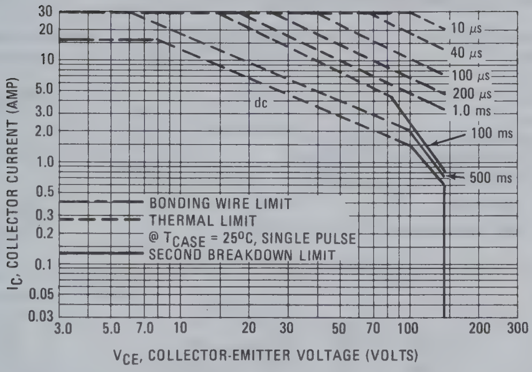


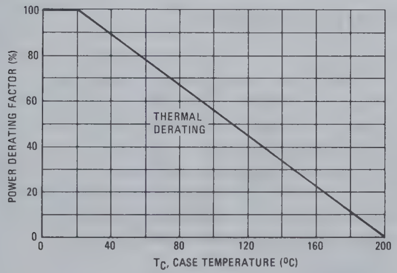
FIGURE 7 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 – POWER DERATING



2N3789 thru 2N3792

MOTOROLA

1.3

SILICON PNP POWER TRANSISTORS

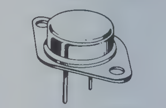
. . . designed for medium-speed switching and amplifier applications. These devices feature:

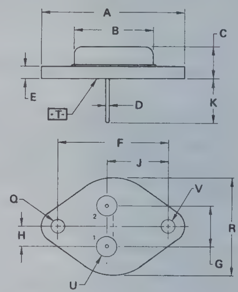
- Total Switching Time @ 3 A ≈ 1 μs (typ)
- Two Gain Ranges:
  h_{FE} (min) = 15 and 30 @ 3 A (2N3789, 2N3790)
  25 and 50 @ 1 A (2N3791, 2N3792)
- Low $V_{CE(sat)}$ = 0.5 V (typ) @ I_C = 4.0 A, I_B = 0.4 A
- Excellent Safe Area Limits
- Complementary NPN types available — 2N3713 thru 2N3716

10 AMPERE

POWER TRANSISTORS
PNP SILICON

60-80 VOLTS
150 WATTS





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅0.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

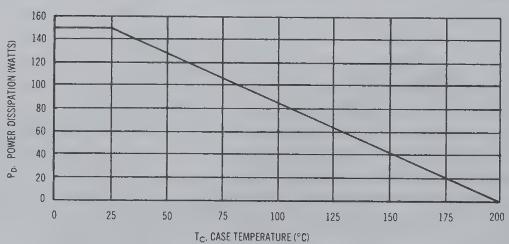
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

MAXIMUM RATINGS

Characteristic	Symbol	2N3789 2N3791	2N3790 2N3792	Unit
Collector-Base Voltage	V_{CB}	60	80	Volts
Collector-Emitter Voltage	V_{CEO}	60	80	Volts
Emitter-Base Voltage	V_{EB}	7.0	7.0	Volts
Collector Current (Continuous)	I_C	10	10	Amps
Base Current (Continuous)	I_B	4.0	4.0	Amps
Power Dissipation	P_D	150	150	Watts
Thermal Resitance	θ_{JC}	1.17	1.17	°C/W
Junction Operating and Storage Temperature Range	T_J, T_{stg}	–65 to +200		°C

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



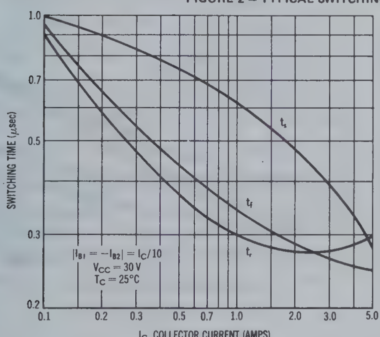
Safe Area Limits are indicated by Figures 15, 16. Both limits are applicable and must be observed.

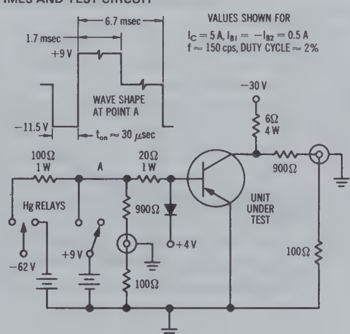
ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector-Emitter Sustaining Voltage*		$V_{CEO(sus)}$*			Vdc
(I_C = 200 mAdc, I_B = 0)	2N3789, 2N3791		60	–	
	2N3790, 2N3792		80	–	
Collector-Emmiter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, V_{BE} = -1.5 Vdc)	2N3789, 2N3791		–	1	
(V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc)	2N3790, 2N3792		–	1	
(V_{CE} = 60 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3789, 2N3791		–	5	
(V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3790, 2N3792		–	5	
Emitter-Base Cutoff Current		I_{EBO}			mAdc
(V_{EB} = 7 Vdc)	All Types		–	5	
DC Current Gain*		h_{FE}*			–
(I_C = 1 Adc, V_{CE} = 2 Vdc)	2N3789, 2N3790		25	90	
	2N3791, 2N3792		50	180	
(I_C = 3 Adc, V_{CE} = 2 Vdc)	2N3789, 2N3790		15	–	
	2N3791, 2N3792		30	–	
Collector-Emitter Saturation Voltage*		$V_{CE(sat)}$*			Vdc
(I_C = 4 Adc, I_B = 0.4 Adc)	2N3789, 2N3790		–	1.0	
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3791, 2N3792		–	1.0	
Base-Emitter On Voltage*		$V_{BE(on)}$*			Vdc
(I_C = 5 A, V_{CE} = 2 Vdc)	2N3789, 2N3790		–	2.0	
	2N3791, 2N3792		–	1.8	
(I_C = 10 Adc, V_{CE} = 4 Vdc)	All Types		–	4.0	
Current Gain – Bandwidth Product		f_T			MHz
(V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1 MHz)	All Types		4	–	

*Sweep Test: 1/2 sine wave cycle @ 60 cps.

FIGURE 2 – TYPICAL SWITCHING TIMES AND TEST CIRCUIT





1.3

FIGURE 3 – CURRENT GAIN VARIATIONS

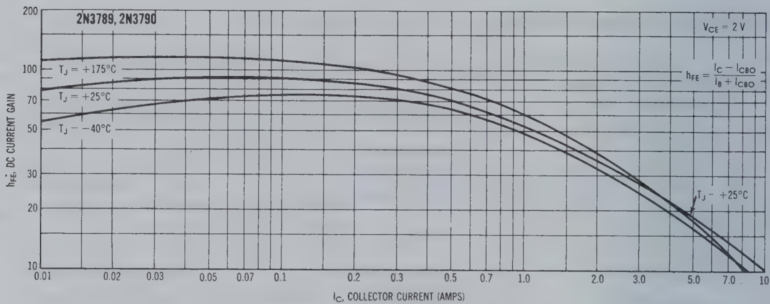


FIGURE 4 – CURRENT GAIN VARIATIONS

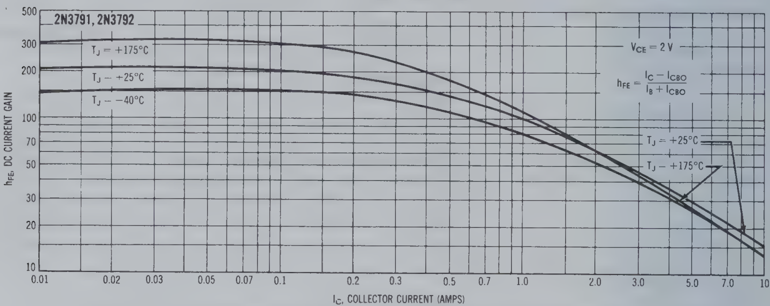


FIGURE 5 – SATURATION VOLTAGES

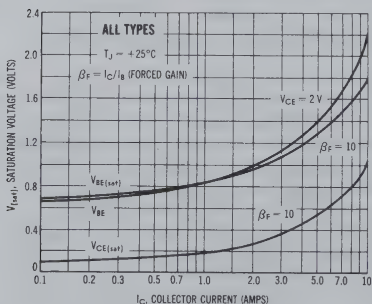
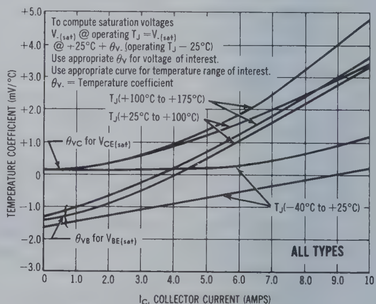


FIGURE 6 – TEMPERATURE COEFFICIENTS



1.3

SAFE OPERATING AREAS

FIGURE 7 – 2N3789, 2N3791

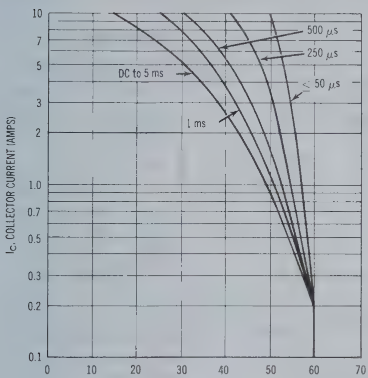
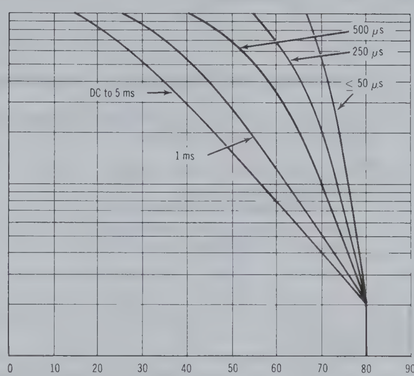


FIGURE 8 – 2N3790, 2N3792



V_{CE}, COLLECTOR-EMITTER VOLTAGE (VOLTS)

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

FIGURE 9 – CUT-OFF REGION TRANSCONDUCTANCE

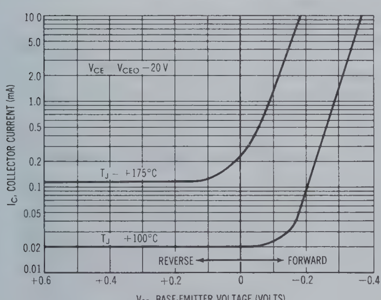
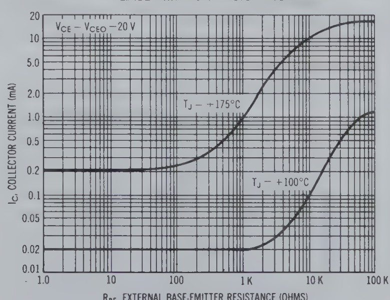


FIGURE 10 – COLLECTOR CUT-OFF CURRENT versus BASE-EMITTER RESISTANCE



2N3902 NPN

MOTOROLA

1.3

HIGH VOLTAGE NPN SILICON TRANSISTORS

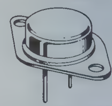
. . . designed for use in high-voltage inverters, converters, switching regulators and line operated amplifiers.

- High Collector-Emitter Voltage — V_{CEX} = 700 Vdc
- Excellent DC Current Gain — h_{FE} = 10 (Min) @ I_C = 2.5 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.8 Vdc (Max) @ I_C = 1.0 Adc

3.5 AMPERE

POWER TRANSISTORS
NPN SILICON

400 VOLTS
100 WATTS



*MAXIMUM RATINGS

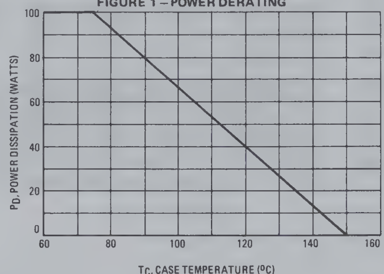
Rating	Symbol	2N3902	Unit
Collector-Emitter Voltage	V_{CEO}	400	Vdc
Collector-Emitter Voltage	V_{CEX}	700	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	3.5	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	100 1.33	Watts W/°C
Operating Junction Temperature Range	T_J	-65 to +150	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

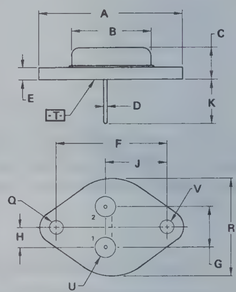
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.75	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	∅.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	∅.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

1.3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0) (See Figure 12)	$V_{CEO(sus)}$	325	–	Vdc
Collector Cutoff Current (V_{CE} = 400 Vdc, I_B = 0)	I_{CEO}	0.25	–	mAdc
Collector Cutoff Current (V_{CE} = 700 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	–	2.5	mAdc
(V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)		–	0.5	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	30	90	–
(I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)		10	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	–	0.8	Vdc
(I_C = 2.5 Adc, I_B - 0.5 Adc)		–	2.5	
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B - 0.1 Adc)	$V_{BE(sat)}$	–	1.5	Vdc
(I_C 2.5 Adc, I_B 0.5 Adc)		–	2.0	
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc)	f_T	2.8	–	MHz

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT

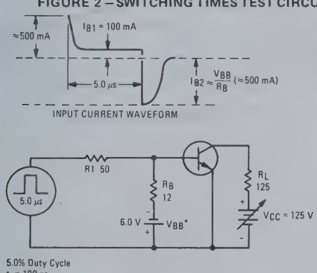


FIGURE 3 — TURN-ON TIME

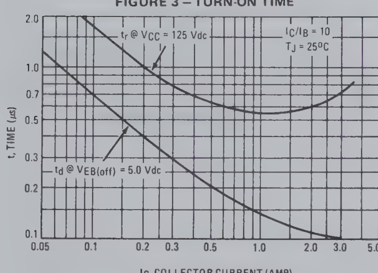


FIGURE 4 — THERMAL RESPONSE

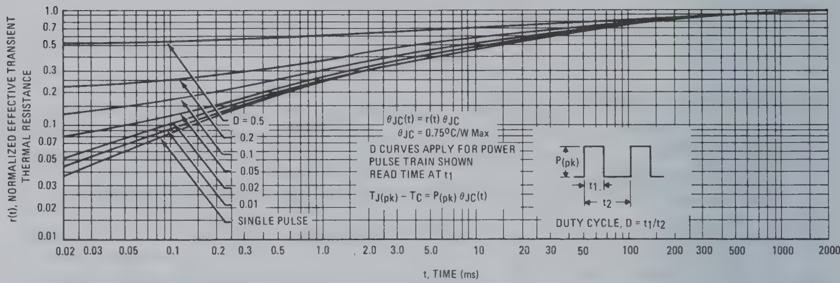
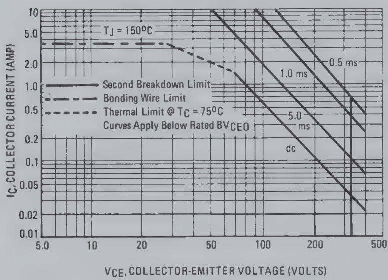


FIGURE 5 — ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 150^{\circ}C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 — TURN-OFF TIME

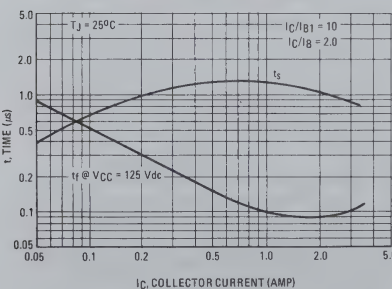


FIGURE 7 — CAPACITANCE

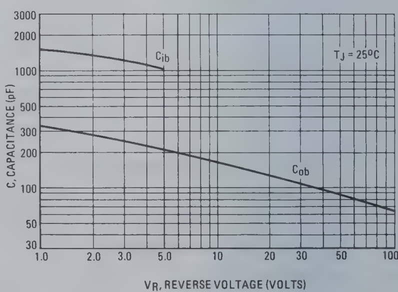


FIGURE 8 – DC CURRENT GAIN

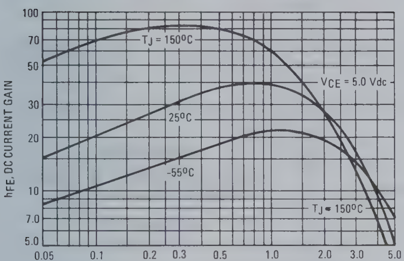


FIGURE 9 – "ON" VOLTAGES

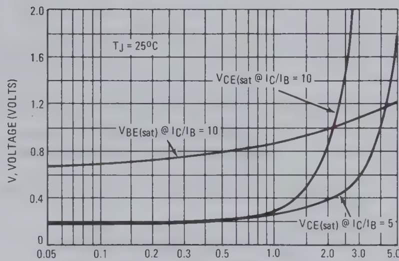


FIGURE 10 – COLLECTOR CUT-OFF REGION

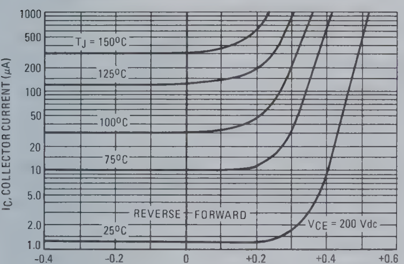


FIGURE 11 – TEMPERATURE COEFFICIENTS

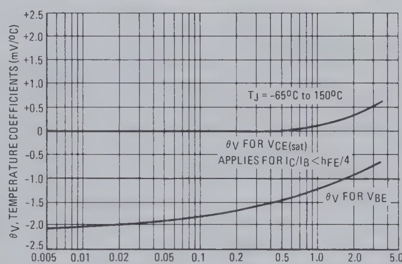
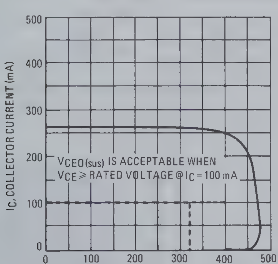
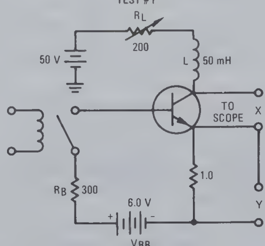


FIGURE 12 – COLLECTOR-EMITTER SUSTAINING VOLTAGE TEST CIRCUITS AND LOAD LINES





2N4231A thru 2N4233A NPN
2N6312 thru 2N6314 PNP

MOTOROLA

COMPLEMENTARY SILICON MEDIUM-POWER TRANSISTORS

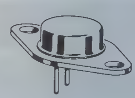
. . . designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 1.5 Adc
- Low Leakage Current — I_{CEX} = 0.1 mAdc (Max)
- Excellent DC Current Gain — h_{FE} = 25-100 @ I_C = 1.5 Adc
- High Current Gain — Bandwidth Product — f_T = 4.0 MHz @ I_C = 0.25 Adc

5.0 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40-60-80 VOLTS
75 WATTS



*MAXIMUM RATINGS

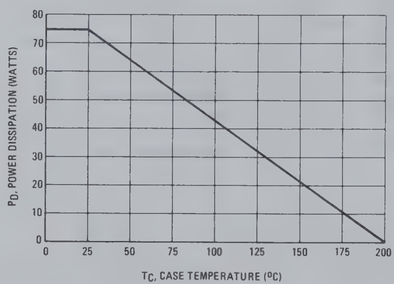
Rating	Symbol	2N4231A 2N6312	2N4232A 2N6313	2N4233A 2N6314	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous / Peak	I_C	← 5.0 → / ← 10 →			Adc
Base Current	I_B	← 2.0 →			Adc
Total Device Dissipation @ T_C = 25°C / Derate above 25°C	P_D	← 75 → / ← 0.43 →			Watts / W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -65 to +200 →			°C

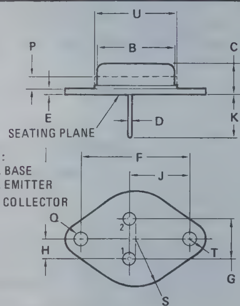
* THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.32	°C/W

*Indicates JEDEC registered data. (All values meet or exceed JEDEC registered data).

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

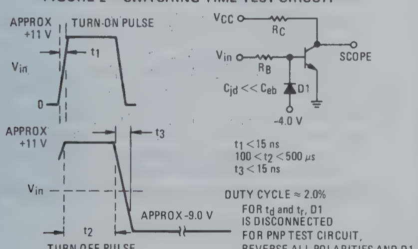
CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N4231A, 2N6312		40	–	
	2N4232A, 2N6313		60	–	
	2N4233A, 2N6314		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N4231A, 2N6312		–	1.0	
(V_{CE} = 50 Vdc, I_B = 0)	2N4232A, 2N6313		–	1.0	
(V_{CE} = 70 Vdc, I_B = 0)	2N4233A, 2N6314		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4231A, 2N6312		–	0.1	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4232A, 2N6313			0.1	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4233A, 2N6314		–	0.1	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150^oC$)	2N4231A, 2N6312		–	1.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150^oC$)	2N4232A, 2N6313		–	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150^oC$)	2N4233A, 2N6314		–	1.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N4231A, 2N6312			0.05	
(V_{CB} = 60 Vdc, I_E = 0)	2N4232A, 2N6313			0.05	
(V_{CB} = 80 Vdc, I_E = 0)	2N4233A, 2N6314		–	0.05	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
*(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			40	–	
*(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			25	100	
*(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)			10	–	
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
*Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			–	0.7	
(I_C = 3.0 Adc, I_B = 0.3 Adc)			–	2.0	
(I_C = 5.0 Adc, I_B = 1.25 Adc)			–	4.0	
*Base-Emitter On Voltage (1) (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.4	Vdc
***DYNAMIC CHARACTERISTICS**					
Current-Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}		300	pF
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–

*Indicates JEDEC registered data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



FOR CURVES OF FIGURES 3 AND 6, R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

FIGURE 3 – TURN "ON" TIME

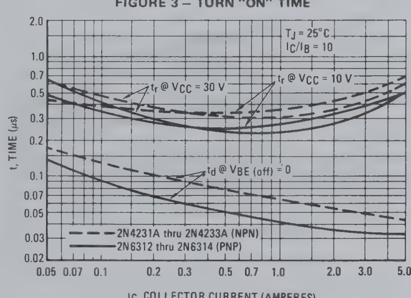


FIGURE 4 — THERMAL RESPONSE

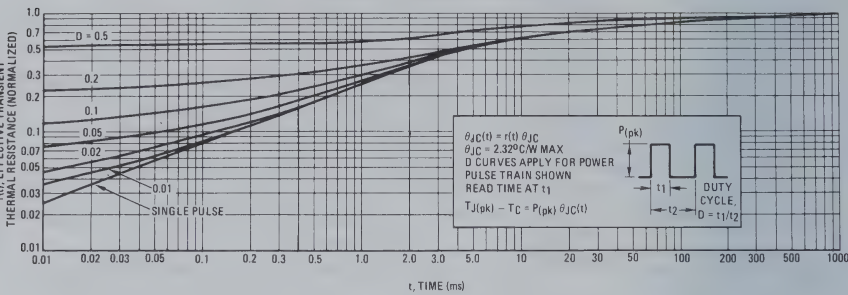
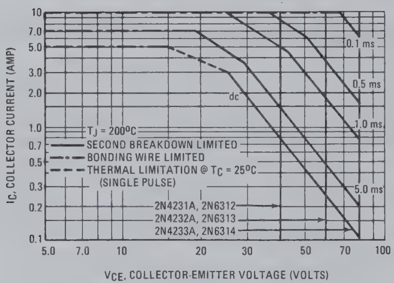


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — TURN "OFF" TIME

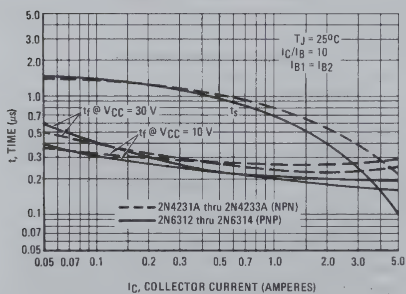
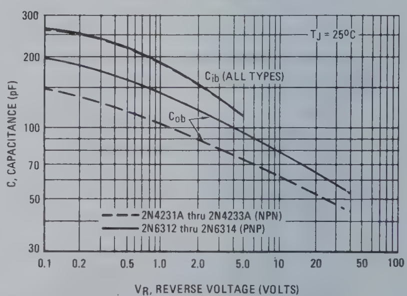


FIGURE 7 — CAPACITANCE



NPN
2N4231A thru 2N4233A

PNP
2N6312 thru 2N6314

FIGURE 8 – DC CURRENT GAIN

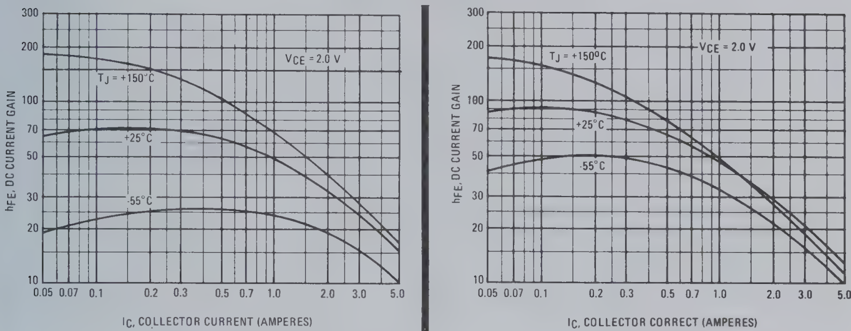


FIGURE 9 – COLLECTOR SATURATION REGION

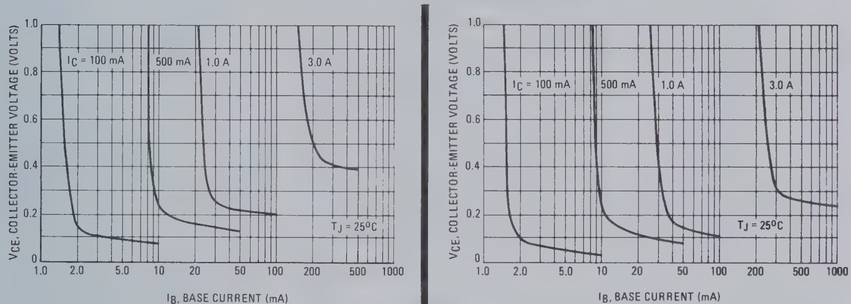
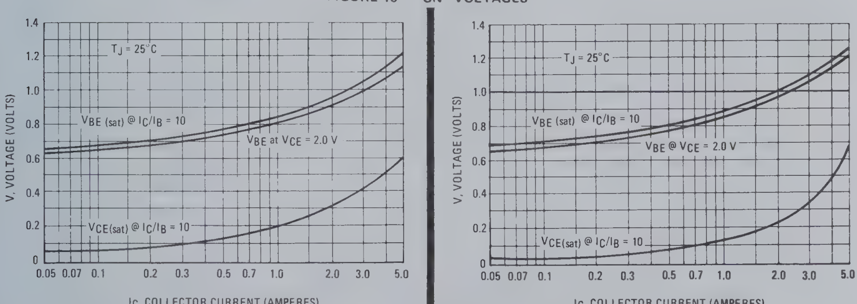


FIGURE 10 – "ON" VOLTAGES



2N4398
2N4399
2N5745

MOTOROLA

1.3

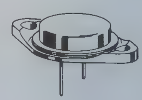
PNP SILICON HIGH-POWER TRANSISTORS

. . . designed for use in power amplifier and switching circuits.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 15 Adc (2N4398, 2N4399)
- DC Current Gain Specified — 1.0 to 30 Adc
- Complements to NPN 2N5301, 2N5302, 2N5303

20, 30 AMPERE POWER TRANSISTORS
PNP SILICON

40–60–180 VOLTS
200 WATTS



*MAXIMUM RATINGS

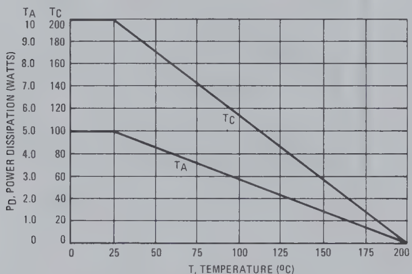
Rating	Symbol	2N4398	2N4399	2N5745	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	30 50	30 50	20 50	Adc
Base Current — Continuous Peak	I_B	← 7.5 → ← 15 →			Adc
Total Device Dissipation @ T_A = 25°C** Derate above 25°C	P_D	← 5.0 → ← 28.6 →			Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 200 → ← 1.15 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

THERMAL CHARACTERISTICS

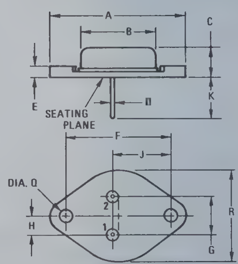
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	35	°C/W

*Indicates JEDEC Registered Data
**Motorola guarantees this data in addition to JEDEC Registered Data.

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 13. All limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11–01
(TO-3)

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage(1) (I_C = 200 mAdc, I_B = 0)	2N4398	$V_{CEO(sus)}$	40	–	Vdc
	2N4399		60	–	
	2N5745		80	–	
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	2N4398	I_{CEO}		5.0	mAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N4399		–	5.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5745			5.0	
Collector Cutoff Current (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4398	I_{CEX}		5.0	mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4399		–	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5745			5.0	
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N4398, 2N4399		–	10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5745		–	10	
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	2N4398	I_{CBO}	–	1.0	mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N4399			1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5745		–	1.0	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	All Types	h_{FE}	40	–	–
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5745		15	60	
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4398, 2N4399		15	60	
(I_C = 20 Adc, V_{CE} = 2.0 Vdc)	2N5745		5.0	–	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N4398, 2N4399		5.0		
Collector-Emitter Saturation Voltage(1) (I_C = 10 Adc, I_B = 1.0 Adc)	2N4398, 2N4399	$V_{CE(sat)}$	–	0.75	Vdc
	2N5745		–	1.0	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N4398, 2N4399		–	1.0	
	2N5745		–	1.5	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N4398, 2N4399		–	2.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5745		–	2.0	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N4398, 2N4399		–	4.0	
Base-Emitter Saturation Voltage(1) (I_C = 10 Adc, I_B = 1.0 Adc)**	2N4398, 2N4399	$V_{BE(sat)}$	–	1.6	Vdc
	2N5745			1.7	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N4398, 2N4399		–	1.85	
	2N5745		–	2.0	
(I_C = 20 Adc, I_B = 2.0 Adc)**	2N4398, 2N4399		–	2.5	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5745		–	2.5	
Base-Emitter On Voltage(1) (I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5745	$V_{BE(on)}$	–	1.5	Vdc
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4398, 2N4399			1.7	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5745		–	2.5	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N4398, 2N4399		–	3.0	
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product(2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	2N4398, 2N4399	f_T	4.0	–	MHz
	2N5745		2.0	–	
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	40	–	–
SWITCHING CHARACTERISTICS (See Figures 2 and 3)					
Rise Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	2N4398, 2N4399	t_r	–	0.4	µs
	2N5745		–	1.0	
Storage Time	2N4398, 2N4399	t_s	–	1.5	µs
	2N5745			2.0	
Fall Time	2N4398, 2N4399	t_f	–	0.6	µs
	2N5745		–	1.0	

*Indicates JEDEC Registered Data.
**Motorola Guarantees this Data in Addition to JEDEC Registered Data.
(1)Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.
(2)f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

FIGURE 2 — TURN-ON TIME

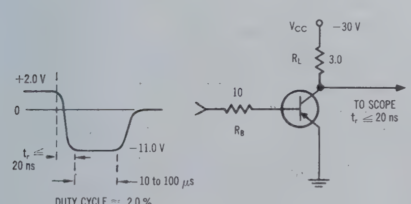
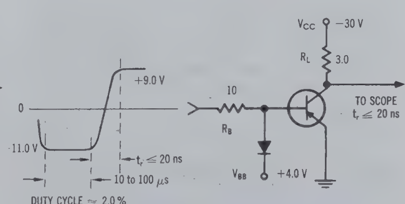


FIGURE 3 — TURN-OFF TIME



1.3

TYPICAL "ON" REGION CHARACTERISTICS

FIGURE 4 – DC CURRENT GAIN

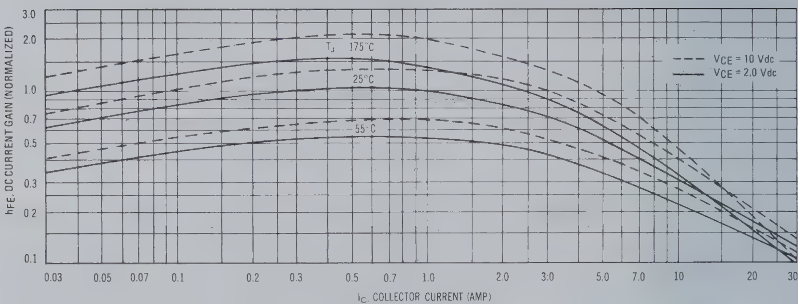


FIGURE 5 – COLLECTOR SATURATION REGION

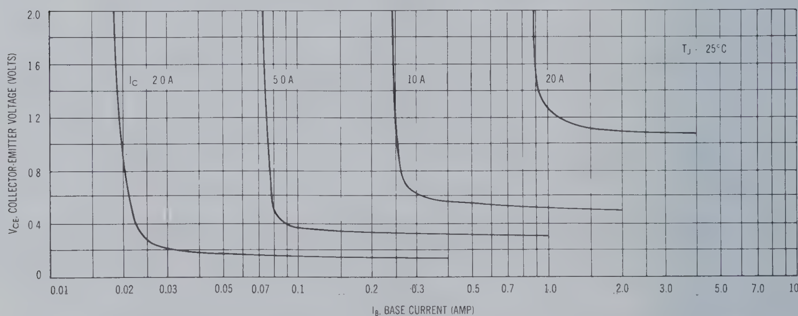


FIGURE 6 – "ON" VOLTAGES

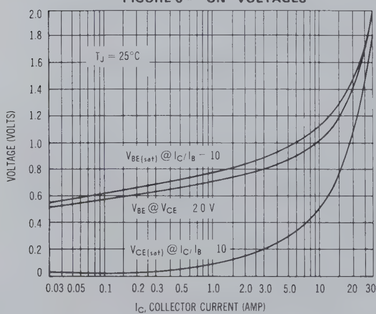
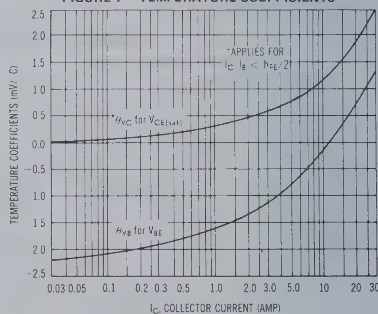
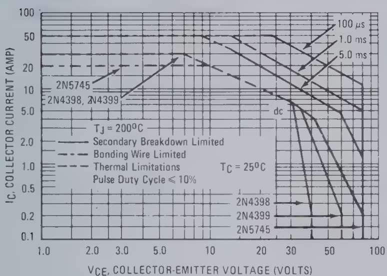


FIGURE 7 – TEMPERATURE COEFFICIENTS



RATINGS AND THERMAL DATA

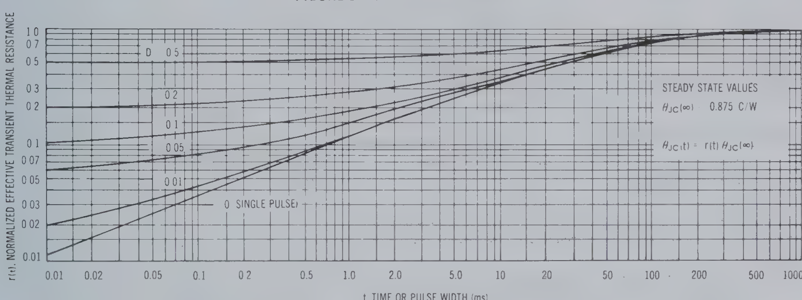
FIGURE 8 — ACTIVE REGION SAFE OPERATING AREA



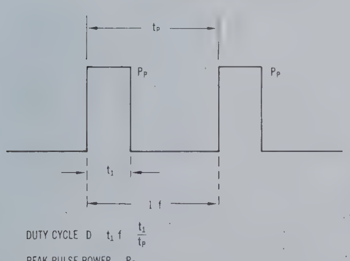
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 8 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 9 — THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



A train of periodical power pulses can be represented by the model as shown in Figure A. Using the model and the device thermal reponse, the normalized effective transient thermal resistance of Figure 9 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 9 by the steady state value $\theta_{JC}(\infty)$.

Example:
The 2N4398 is dissipating 100 watts under the following conditions: t_1 = 1.0 ms, t_P = 5.0 ms. (D = 0.2)

Using Figure 9, at a pulse width of 1.0 ms and D = 0.2, the reading of r (t) is 0.28.

The peak rise in junction temperature is therefore

$T = r(t) \times P_P \times \theta_{JC}(\infty) = 0.28 \times 100 \times 0.875 = 24.5°C$

2N4898 thru 2N4900

MOTOROLA

1.3

MEDIUM-POWER PNP SILICON TRANSISTORS

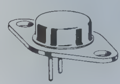
. . . designed for driver circuits, switching, and amplifier applications. These high-performance devices feature:

- Low Saturation Voltage — $V_{CE(sat)} = 0.6$ V max @ $I_C = 1.0$ Amp
- Excellent Safe Operating Area
- Gain Specified to $I_C = 1.0$ Ampere
- 2N4900 Complementary to NPN 2N4912

4 AMPERE

GENERAL PURPOSE POWER TRANSISTORS

40-80 VOLTS
25 WATTS



MAXIMUM RATINGS

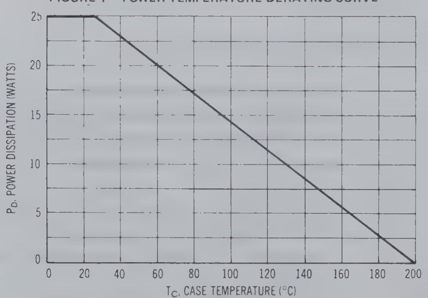
Rating	Symbol	2N4898	2N4899	2N4900	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous*	I_C*	← 1.0 → ← 4.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Device Dissipation $T_C = 25°C$ Derate above 25°C	P_D	← 25 → ← 0.143 →			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +200 →			°C

THERMAL CHARACTERISTICS

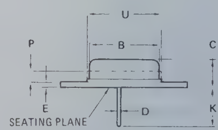
Characteristic	Symbol	Max	Unit
Thermal Reistance, Junction to Case	θ_{JC}	7.0	°C/W

*The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements.
The 4.0 Amp maximum value is based upon actual current-handling capability of the device (see Figure 5).

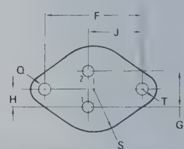
FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	2N4898	$BV_{CEO(sus)}$*	40	-	Vdc
	2N4899		60	-	
	2N4900		80	-	
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	2N4898	I_{CEO}	-	0.5	mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N4899		-	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	2N4900		-	0.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEX}	-	0.1	mAdc
(V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			-	1.0	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	-	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	-	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)		h_{FE}*	40	-	-
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			20	100	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			10	-	
Collector-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$*	-	0.6	Vdc
Base-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$*	-	1.3	Vdc
Base-Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$*	-	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C - 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	-	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	-	-

* Pulse Test: PW ≈300 μs, Duty Cycle ≈ 2.0%

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

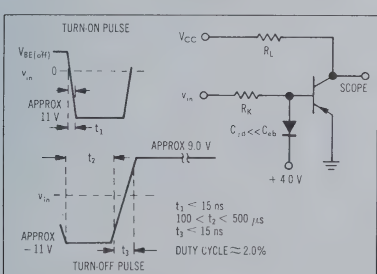
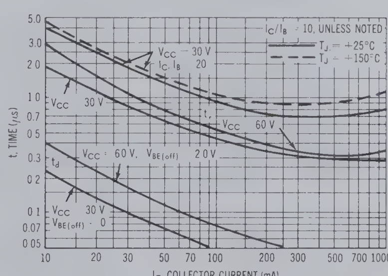


FIGURE 3 – TURN-ON TIME



1.3

FIGURE 4 — THERMAL RESPONSE

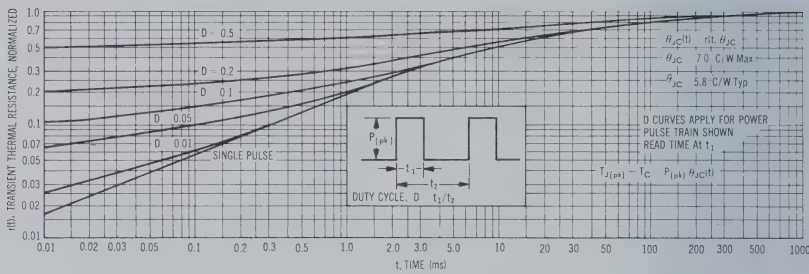
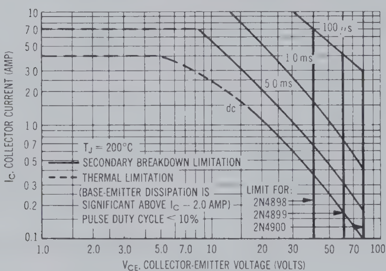


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



The safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor which must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 5 is based upon $T_{J(pk)} = 200°C$; T_C is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \le 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power which can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 — STORAGE TIME

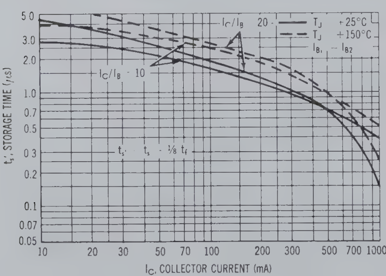
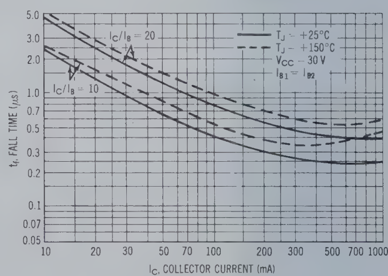


FIGURE 7 — FALL TIME



MOTOROLA

NPN SILICON TRANSISTOR

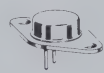
. . . designed for driver circuits, switching, and amplifier applications. This high-performance device features:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 V max @ I_C = 1.0 Amp
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to PNP 2N4900

1 AMPERE

NPN SILICON POWER TRANSISTOR

80 VOLTS
25 WATTS



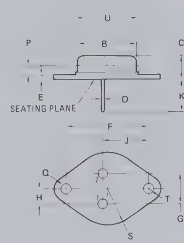
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous*	I_C*	1.0	Adc
Base Current — Continuous	I_B	1.0	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	25 0.143	Watts mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.0	°C/W

*The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements.



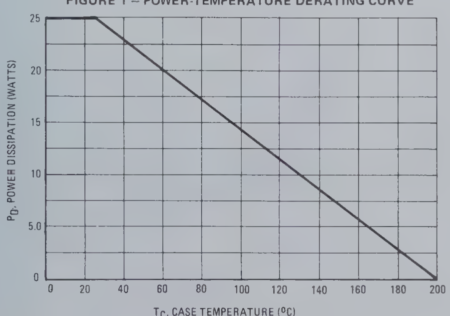
STYLE 1
PIN 1 BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2 41	2.67	0.095	0.105
J	14.48	14 99	0.570	0.590
K	9.14		0.360	–
P		1.27	–	0.050
Q	3.61	3 86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15 75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	$BV_{CEO(sus)}$	80	–	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	–	0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	0.1 1.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	–	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40 20 10	– 100 –	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	–	0.6	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	–	1.3	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} - 1.0 Vdc)	$V_{BE(on)}$	–	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	25	–	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

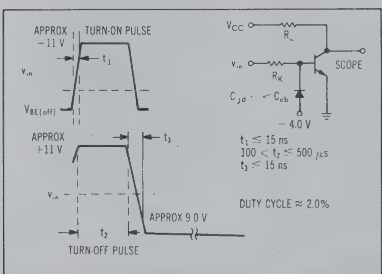


FIGURE 3 – TURN-ON TIME

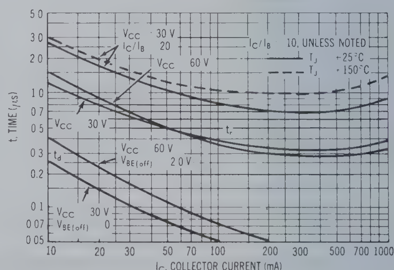


FIGURE 4 — THERMAL RESPONSE

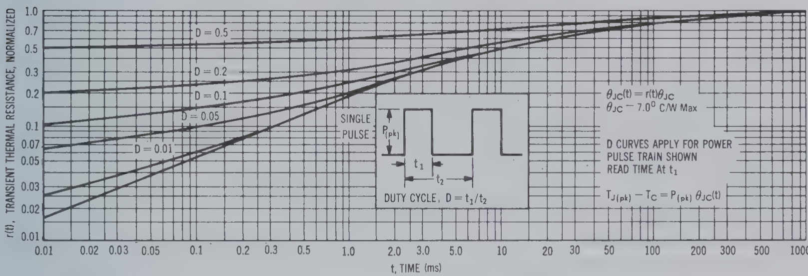
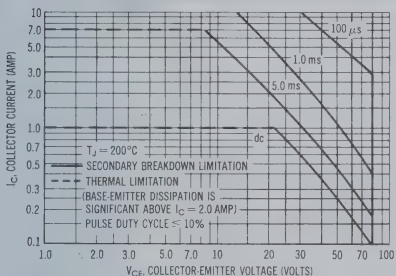


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 — STORAGE TIME

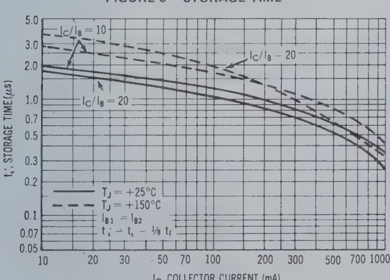
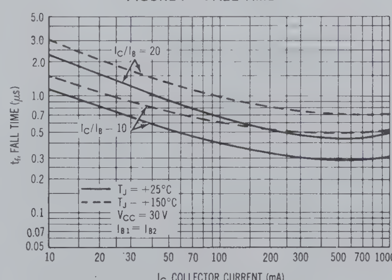


FIGURE 7 — FALL TIME



2N4918 thru 2N4920

MOTOROLA

1.3

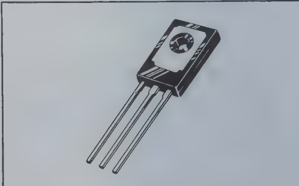
MEDIUM-POWER PLASTIC PNP SILICON TRANSISTORS

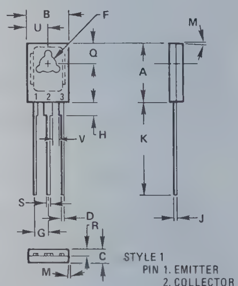
. . . designed for driver circuits, switching, and amplifier applications. These high-performance plastic devices feature:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction — P_D = 30 @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to NPN 2N4921, 2N4922, 2N4923

3 AMPERE GENERAL-PURPOSE POWER TRANSISTORS

40-80 VOLTS
30 WATTS





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	[illegible]	0.040	–

CASE 77-04
TO-126

*MAXIMUM RATINGS

Ratings	Symbol	2N4918	2N4919	2N4920	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current - Continuous (1)	I_C*	1.0 3.0			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C

THERMAL CHARACTERISTICS (2)

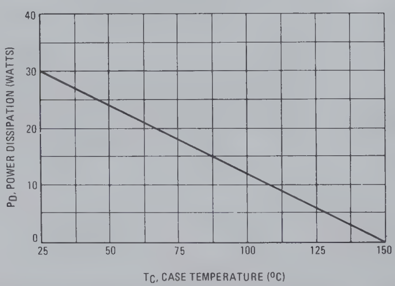
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

*Indicates JEDEC Registered Data for 2N4918 Series

(1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current-handling capability of the device (See Figure 5).

(2) Recommend use of thermal compound for lowest thermal resistance.

FIGURE 1 — POWER DERATING



1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	2N4918 2N4919 2N4920	$V_{CEO(sus)}$	40 60 80	– – –	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	2N4918 2N4919 2N4920	I_{CEO}	– – –	0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEX}	– –	0.1 0.5	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	40 30 10	– 150 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	–	0.6	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	–	1.3	Vdc
Base-Emitter On Voltage (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.3	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

*Indicates JEDEC Registered Data
(1) Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

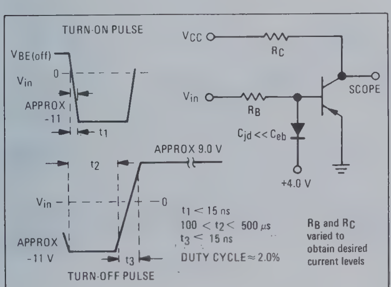
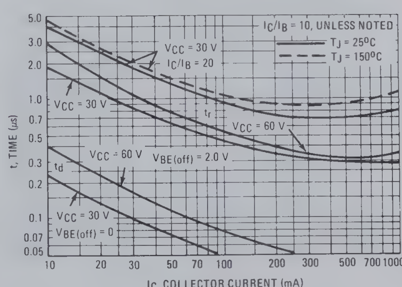


FIGURE 3 – TURN-ON TIME



1.3

FIGURE 4 — THERMAL RESPONSE

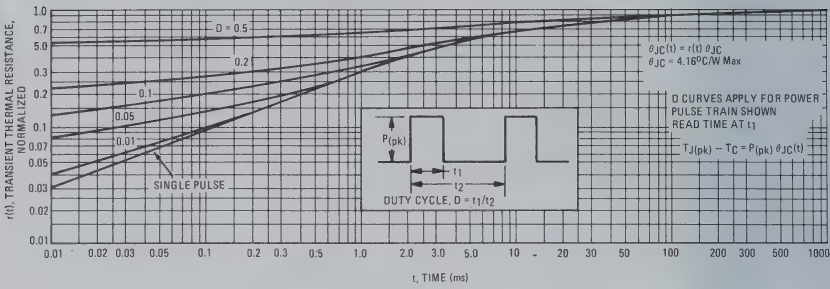
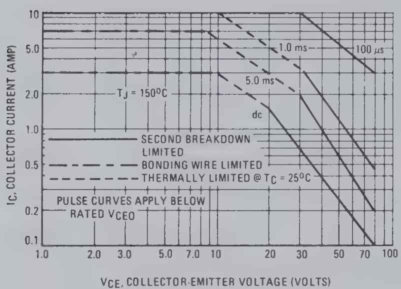


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — STORAGE TIME

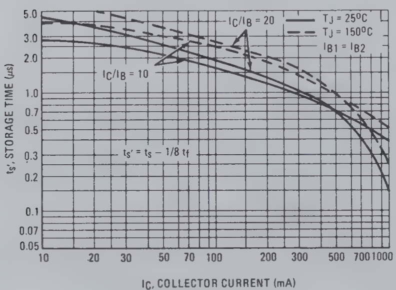
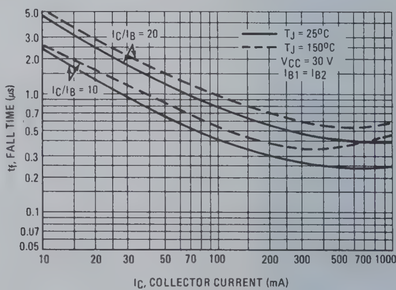


FIGURE 7 — FALL TIME



TYPICAL DC CHARACTERISTICS

FIGURE 8 – CURRENT GAIN

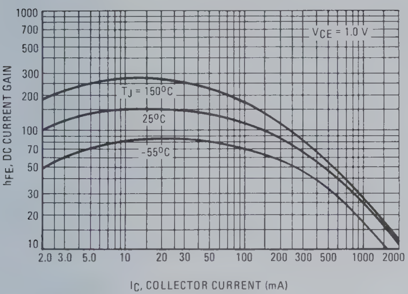


FIGURE 9 – COLLECTOR SATURATION REGION

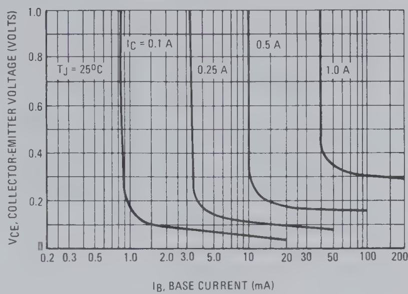


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

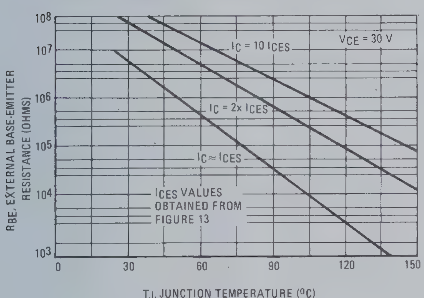


FIGURE 11 – "ON" VOLTAGE

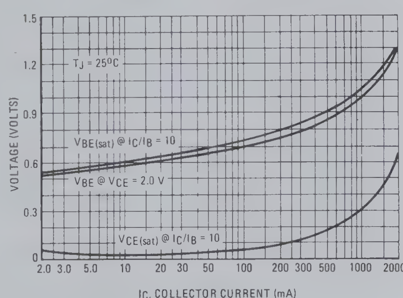


FIGURE 12 – COLLECTOR CUTOFF REGION

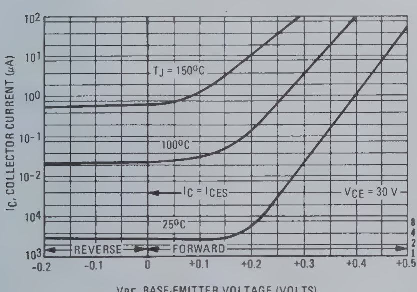
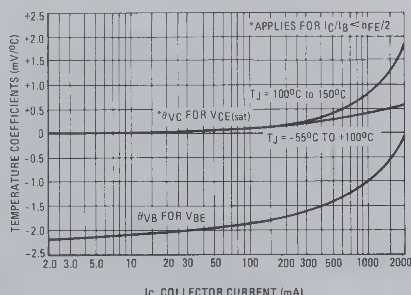


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N4921 thru 2N4923

MOTOROLA

1.3

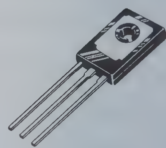
MEDIUM-POWER PLASTIC NPN SILICON TRANSISTORS

. . . designed for driver circuits, switching, and amplifier applications. These high-performance plastic devices feature:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction — P_D = 30 W @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to PNP 2N4918, 2N4919, 2N4920

3 AMPERE GENERAL-PURPOSE POWER TRANSISTORS

40-80 VOLTS
30 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N4921	2N4922	2N4923	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous (1)	I_C	← 1.0 → ← 3.0 →			Adc
Base Current Continuous	I_B	← 1.0 →			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

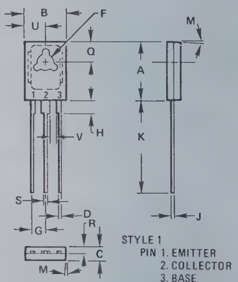
THERMAL CHARACTERISTICS (2)

Characteristic	Symbol		Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

(1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current-handling capability of the device (see Figures 5 and 6)

(2) Recommend use of thermal compound for lowest thermal resistance.

*Indicates JEDEC Registered Data.

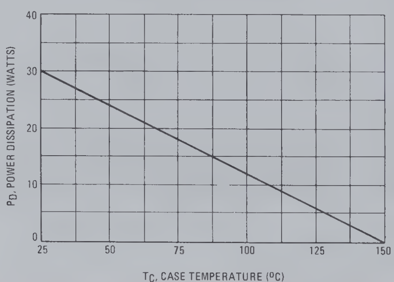


STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

FIGURE 1 — POWER DERATING



Safe Area Curves are indicated by Figure 5   All limits are applicable and must be observed

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	2N4921 2N4922 2N4923	$V_{CEO(sus)}$	40 60 80	– – 	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	2N4921 2N4922 2N4923	I_{CEO}	– –	0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEX}	– –	0.1 0.5	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	40 30 10	– 150 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	–	0.6	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$		1.3	Vdc
Base-Emitter On Voltage (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	-	1.3	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25		–

(1) Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%.
*Indicates JEDEC Registered Data

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

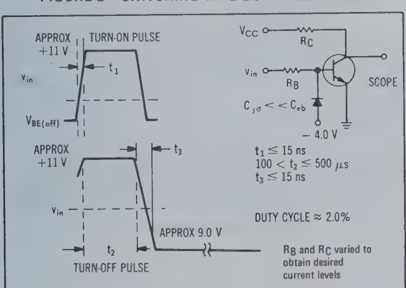


FIGURE 3 – TURN-ON TIME

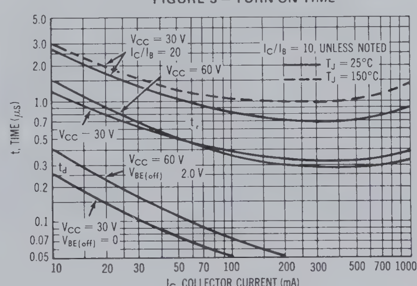


FIGURE 4 – THERMAL RESPONSE

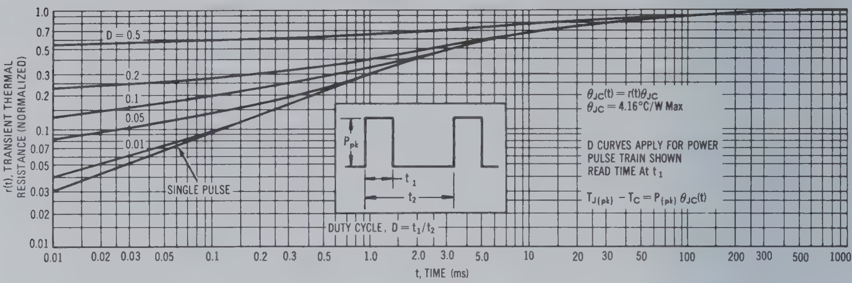
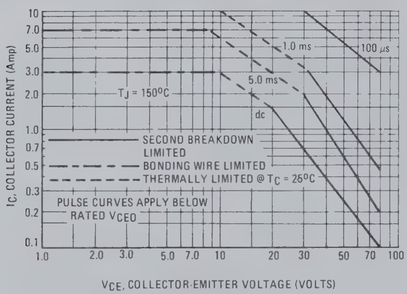


FIGURE 5 – ACTIVE – REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – STORAGE TIME

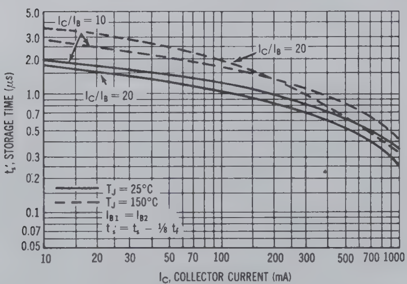


FIGURE 7 – FALL TIME

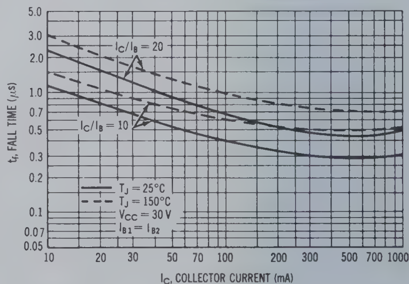


FIGURE 8 – CURRENT GAIN

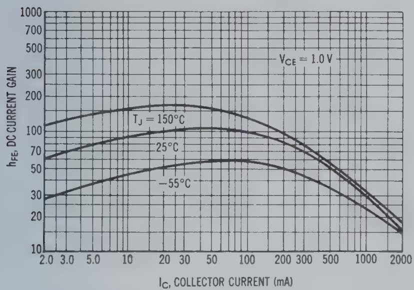


FIGURE 9 – COLLECTOR SATURATION REGION

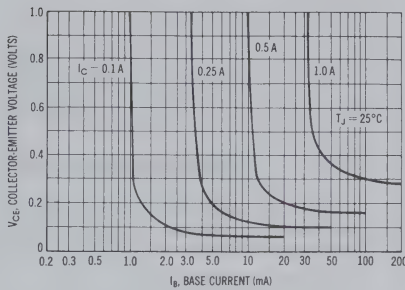


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

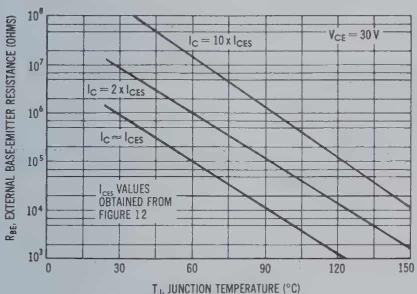


FIGURE 11 – "ON" VOLTAGE

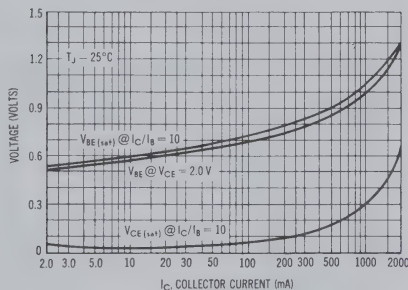


FIGURE 12 – COLLECTOR CUTOFF REGION

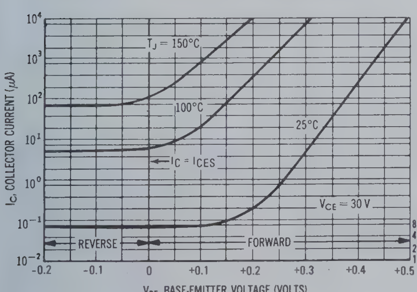
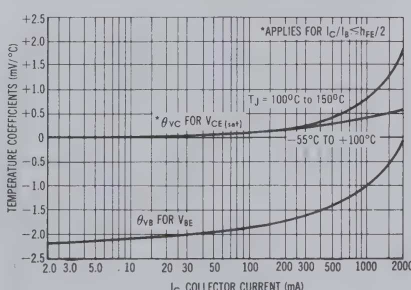


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N5038
2N5039

MOTOROLA

1.3

NPN SILICON TRANSISTORS

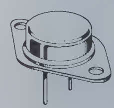
. . . fast switching speeds and high current capacity ideally suit these parts for use in switching regulators, inverters, wide-band amplifiers and power oscillators in industrial and commercial applications.

- High Speed — t_f = 0.5 µs (Max)
- High Current — $I_{C(max)}$ = 30 Amps
- Low Saturation — $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 20 Amps

20 AMPERE

NPN SILICON POWER TRANSISTORS

75 and 90 VOLTS
140 WATTS



*MAXIMUM RATINGS

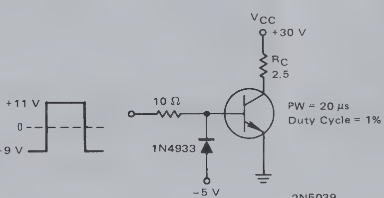
Rating	Symbol	2N5038	2N5039	Unit
Collector-Base Voltage	V_{CBO}	150	120	Vdc
Collector-Emitter Voltage	V_{CEV}	150	120	Vdc
Emitter-Base Voltage	V_{EBO}	7		Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	140 0.8		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^oC/W$

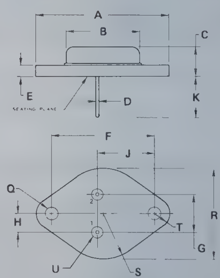
*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 10 ms, Duty Cycle ≤ 50%.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT



2N5038
I_C = 12 Amps
$I_{B1} = I_{B2}$ = 1.2 Amps

2N5039
I_C = 10 Amps
$I_{B1} = I_{B2}$ = 1.0 Amps



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1–04

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5038		90	–	
	2N5039		75	–	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 V)	2N5038		–	50	
(V_{CE} = 110 Vdc, $V_{BE(off)}$ = 1.5 V)	2N5039		–	50	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5038		–	10	
(V_{CE} = 85 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5039		–	10	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{EB} = 5 Vdc, I_C = 0)	2N5038		–	5	
	2N5039		–	15	
(V_{EB} = 7 Vdc, I_C = 0)	Both		–	50	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 12 Adc, V_{CE} = 5 Vdc)	2N5038		20	100	
(I_C = 10 Adc, V_{CE} = 5 Vdc)	2N5039		20	100	
Collector-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 5 Adc)		$V_{CE(sat)}$	–	2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 5 Adc)		$V_{BE(sat)}$	–	3.3	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common-Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 2 Adc, V_{CE} = 10 Vdc, f = 5 MHz)		$\|h_{fe}\|$	12	–	–

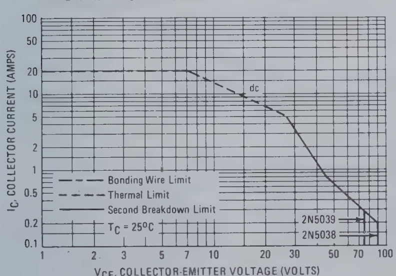
SWITCHING CHARACTERISTICS

RESISTIVE LOAD			Symbol	Min	Max	Unit
Rise Time	(V_{CC} = 30 Vdc)		t_r	–	0.5	μs
Storage Time	(I_C = 12 Adc, I_{B1} = I_{B2} = 1.2 Adc)	2N5038	t_s	–	1.5	μs
Fall Time	(I_C = 10 Adc, I_{B1} = I_{B2} = 1 Adc)	2N5039	t_f	–	0.5	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Second breakdown pulse limits are valid for duty cycles to 10%. At high case temperatures, thermal limitations may reduce the power that can be handled to values less than the limitations imposed by second breakdown.

2N5050
2N5051
2N5052

MOTOROLA

1.3

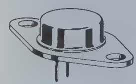
MEDIUM-POWER NPN SILICON TRANSISTORS

. . . designed for untuned amplifier and switching applications.

- High Voltage Ratings —
  V_{CEO} = 125, 150 and 200 Vdc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 0.75 Adc
- Packaged in the Compact, High Efficiency TO-66 Case

2 AMPERE POWER TRANSISTORS NPN SILICON

125-200 VOLTS 40 WATTS



*MAXIMUM RATINGS

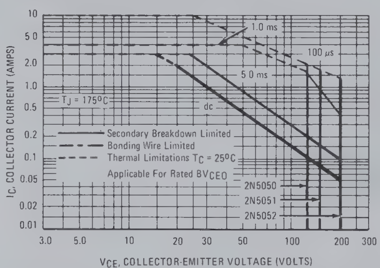
Rating	Symbol	2N5050	2N5051	2N5052	Unit
Collector-Emitter Voltage	V_{CEO}	125	150	200	Vdc
Collector-Base Voltage	V_{CB}	125	150	200	Vdc
Emitter-Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous	I_C	2.0			Adc
Base Current	I_B	1.0			Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	40 0.266			Watts $W/^oC$
Operating Junction Temperature Range	T_J	-65 to +175			^oC
Storage Temperature Range	T_{stg}	-65 to +200			^oC

*THERMAL CHARACTERISTICS

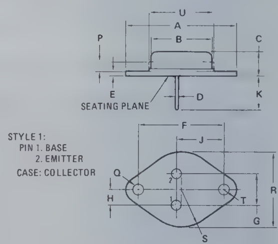
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.76	$^oC/W$

*Indicates JEDEC Registered Data.

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C—V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

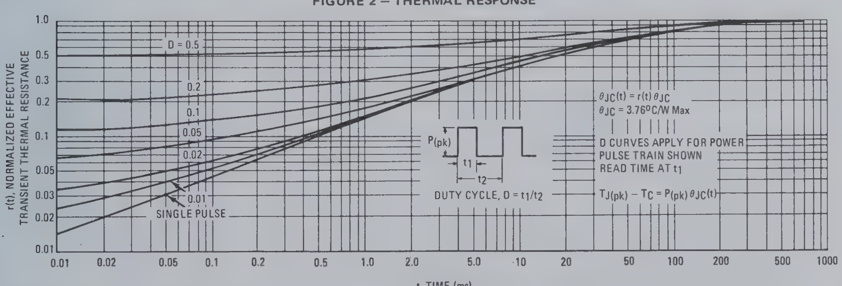
CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc, I_B = 0) 2N5050	$V_{CEO(sus)}$	125	–	Vdc
2N5051		150	–	
2N5052		200	–	
Collector-Emitter Cutoff Current (V_{CE} = 62.5 Vdc, I_B = 0) 2N5050	I_{CEO}	–	0.1	mAdc
(V_{CE} = 75 Vdc, I_B = 0) 2N5051		–	0.1	
(V_{CE} = 100 Vdc, I_B = 0) 2N5052		–	0.1	
Collector-Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	–	0.5	mAdc
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, $T_C = 150^oC$)		–	5.0	
Emitter-Base Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	0.1	mAdc
***ON CHARACTERISTICS**				
DC Current Gain (Note 1) (I_C = 0.75 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	25	100	–
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		25	–	
(I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)		5.0	–	
Collector-Emitter Saturation Voltage (Note 1) (I_C = 0.75 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	–	1.0	Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)		–	5.0	
Base-Emitter On Voltage (Note 1) (I_C = 0.75 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	1.2	Vdc
***DYNAMIC CHARACTERISTICS**				
Current-Gain—Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 5.0 MHz)	f_T	10	–	MHz
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	25	–	–
Common Base Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	250	pF
***SWITCHING CHARACTERISTICS**				
Rise Time (V_{CC} = 120 Vdc, I_C = 750 mAdc, R_L = 150 Ohms, $I_{B1} = I_{B2}$ = 100 mAdc)	t_r	–	300	ns
Storage Time	t_s	–	3.5	μs
Fall Time	t_f	–	1.2	μs

*Indicates JEDEC Registered Data. Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – THERMAL RESPONSE



2N5190 thru 2N5192

MOTOROLA

1.3

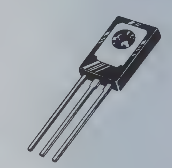
SILICON NPN POWER TRANSISTORS

. . . for use in power amplifier and switching circuits, — excellent safe area limits. Complement to PNP 2N5193, 2N5194, 2N5195

4 AMPERE POWER TRANSISTORS SILICON NPN

40-80 VOLTS

40 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N5190	2N5191	2N5192	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current	I_C		4.0		Adc
Base Current	I_B		1.0		Adc
Total Power Dissipation @ $T_C = 25^{\circ}C$ Derate above $25^{\circ}C$	P_D		40 320		Watts $mW/^{\circ}C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +150		$^{\circ}C$

THERMAL CHARACTERISTICS

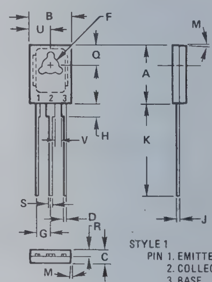
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	$^{\circ}C/W$

*ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 0.1$ Adc; $I_B = 0$)	2N5190 2N5191 2N5192	$V_{CEO(sus)}$	40 60 80	– – –	Vdc
Collector Cutoff Current ($V_{CE} = 40$ Vdc, $I_B = 0$) ($V_{CE} = 60$ Vdc, $I_B = 0$) ($V_{CE} = 80$ Vdc, $I_B = 0$)	2N5190 2N5191 2N5192	I_{CEO}	– – –	1.0 1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 40$ Vdc, $V_{EB(off)} = 1.5$ Vdc) ($V_{CE} = 60$ Vdc, $V_{EB(off)} = 1.5$ Vdc) ($V_{CE} = 80$ Vdc, $V_{EB(off)} = 1.5$ Vdc) ($V_{CE} = 40$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 125^{\circ}C$) ($V_{CE} = 60$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 125^{\circ}C$) ($V_{CE} = 80$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 125^{\circ}C$)	2N5190 2N5191 2N5192 2N5190 2N5191 2N5192	I_{CEX}	– – – – –	0.1 0.1 0.1 2.0 2.0 2.0	mAdc
Collector Cutoff Current ($V_{CB} = 40$ Vdc, $I_E = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	2N5190 2N5191 2N5192	I_{CBO}	– – –	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1) ($I_C = 1.5$ Adc, $V_{CE} = 2.0$ Vdc) ($I_C = 4.0$ Adc, $V_{CE} = 2.0$ Vdc)	2N5190 2N5191 2N5192 2N5190 2N5191 2N5192	h_{FE}	25 25 20 10 10 7.0	100 100 80 – –	–
Collector-Emitter Saturation Voltage(1) ($I_C = 1.5$ Adc, $I_B = 0.15$ Adc) ($I_C = 4.0$ Adc, $I_B = 1.0$ Adc)		$V_{CE(sat)}$	– –	0.6 1.4	Vdc
Base-Emitter On Voltage (1) ($I_C = 1.5$ Adc, $V_{CE} = 2.0$ Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc, f = 1.0 MHz)		f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width $\leqslant 300\ \mu s$, Duty Cycle $\leqslant 2.0\%$.

*Indicates JEDEC Registered Data



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

FIGURE 1 – DC CURRENT GAIN

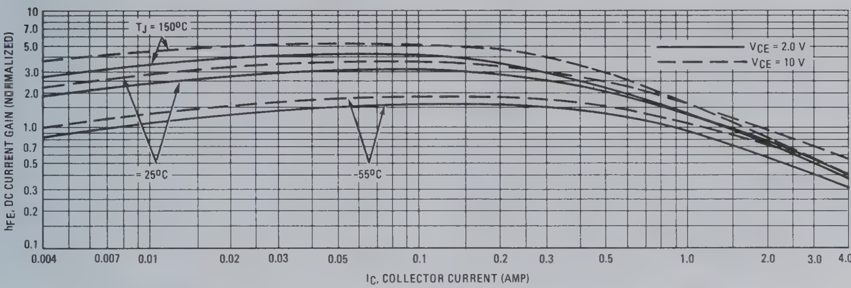


FIGURE 2 – COLLECTOR SATURATION REGION

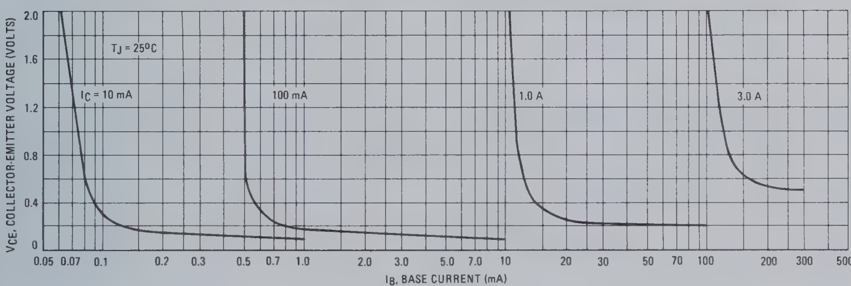


FIGURE 3 – "ON" VOLTAGES

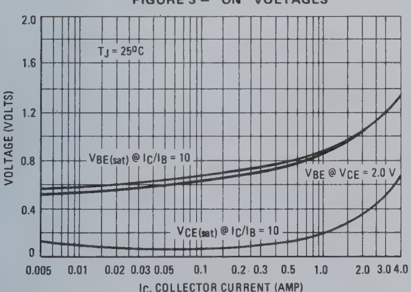
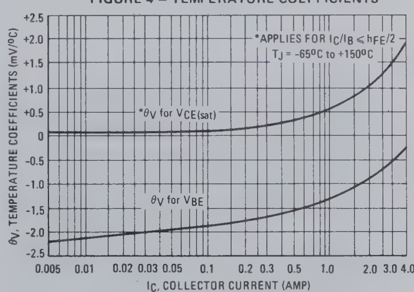


FIGURE 4 – TEMPERATURE COEFFICIENTS



1.3

FIGURE 5 – COLLECTOR CUT-OFF REGION

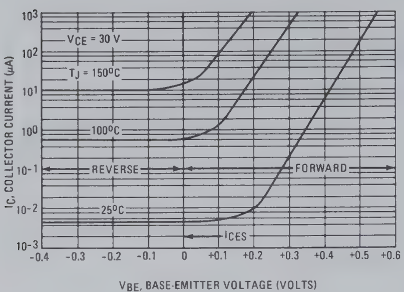


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

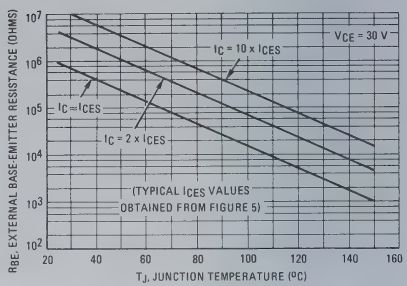


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT

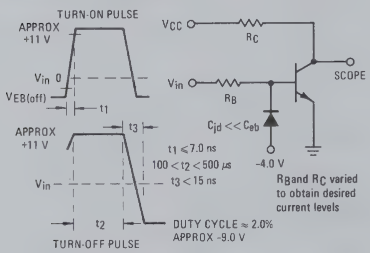


FIGURE 8 – CAPACITANCE

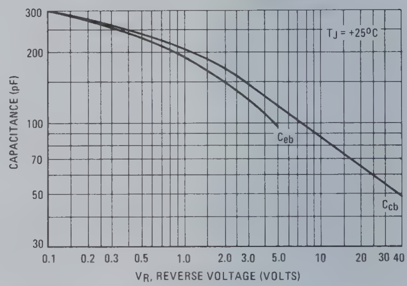


FIGURE 9 – TURN-ON TIME

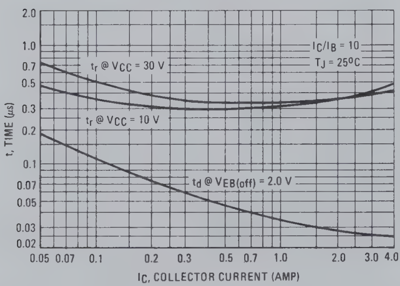


FIGURE 10 – TURN-OFF TIME

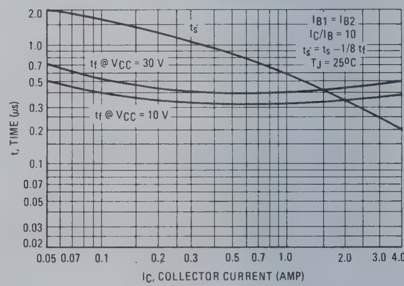
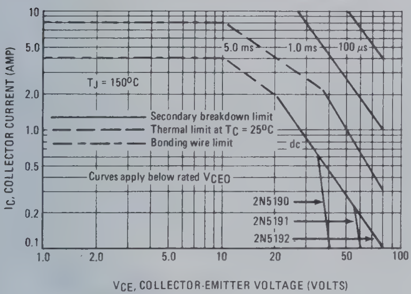


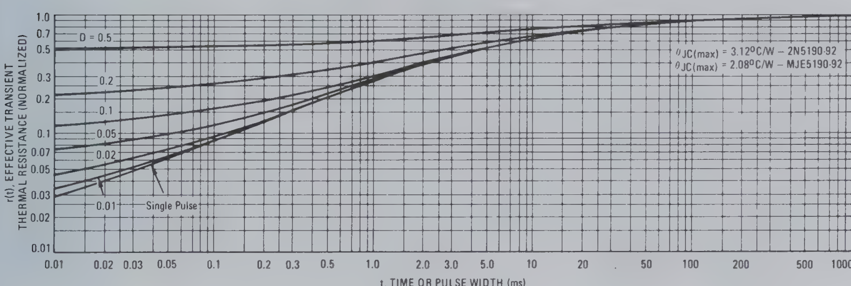
FIGURE 11 RATING AND THERMAL DATA
ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

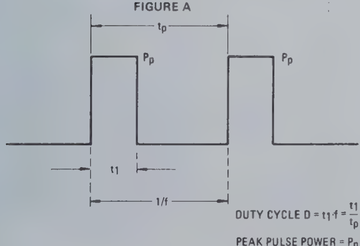
The data of Figure 11 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 12 — THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N5190 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, tp = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2°C$$

2N5193 thru 2N5195

MOTOROLA

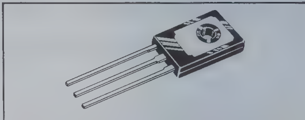
1.3

SILICON PNP POWER TRANSISTORS

. . . for use in power amplifier and switching circuits, – excellent safe area limits. Complement to NPN 2N5190, 2N5191, 2N5192

4 AMPERE POWER TRANSISTORS SILICON PNP

40-80 VOLTS
40 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N5193	2N5194	2N5195	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current	I_C	← 4.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	← 40 → ← 320 →			Watts $mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			$^oC/W$

THERMAL CHARACTERISTICS

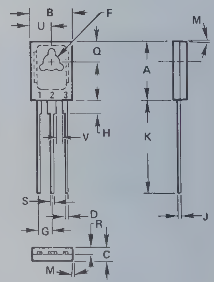
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	$^oC/W$

*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0) 2N5193 2N5194 2N5195	$V_{CEO(sus)}$	 40 60 80		Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) 2N5193 (V_{CE} = 60 Vdc, I_B = 0) 2N5194 (V_{CE} = 80 Vdc, I_B = 0) 2N5195	I_{CEO}	 – – 	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5193 (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5194 (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5195 (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 125^oC$) 2N5193 (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 125^oC$) 2N5194 (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 125^oC$) 2N5195	I_{CEX}	 – – – 	 0.1 0.1 0.1 2.0 2.0 2.0	mAdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) 2N5193 (V_{CB} = 60 Vdc, I_E = 0) 2N5194 (V_{CB} = 80 Vdc, I_E = 0) 2N5195	I_{CBO}	 – –	 0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		 1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc) 2N5193 2N5194 2N5195 (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc) 2N5193 2N5194 2N5195	h_{FE}	 25 25 20 10 10 7.0	 100 100 80 – – –	–
Collector-Emitter Saturation Voltage (1) (I_C = 1.5 Adc, I_B = 0.15 Adc) (I_C = 4.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	 – –	 0.6 1.4	Vdc
Base-Emitter On Voltage (1) (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	 –	 1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	 2.0	 –	MHz

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3^0 TYP		3^0 TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

FIGURE 1 – DC CURRENT GAIN

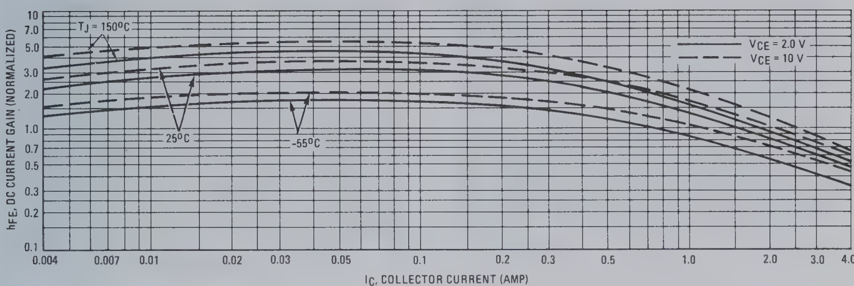


FIGURE 2 – COLLECTOR SATURATION REGION

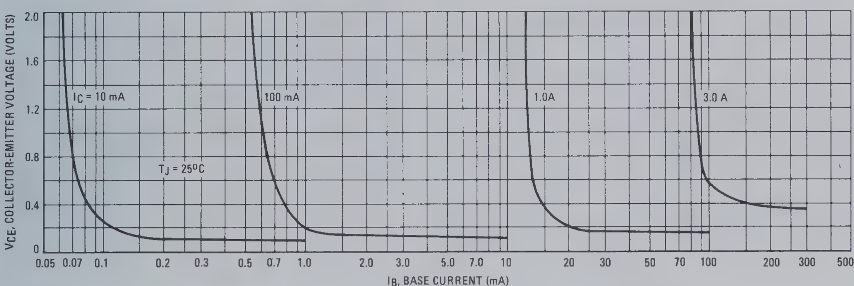


FIGURE 3 – "ON" VOLTAGE

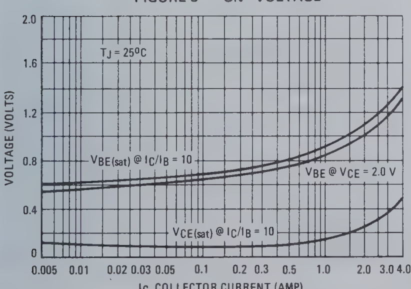


FIGURE 4 – TEMPERATURE COEFFICIENTS

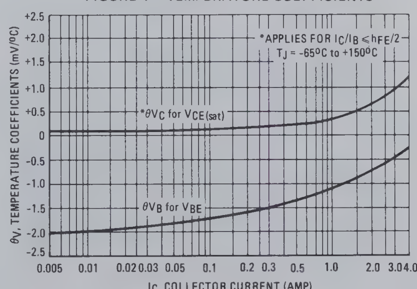


FIGURE 5 – COLLECTOR CUT-OFF REGION

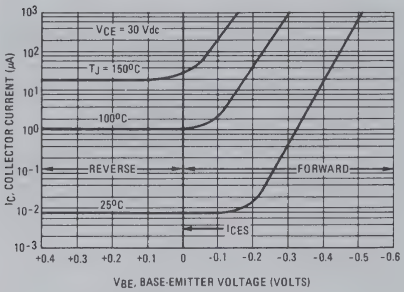


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

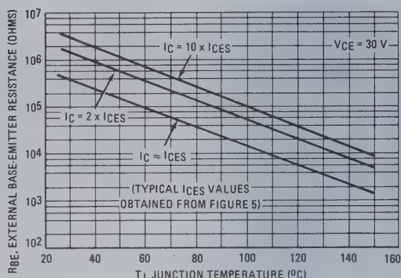


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT

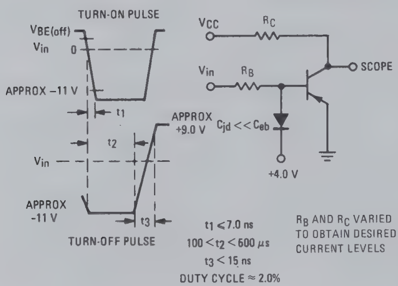


FIGURE 8 – CAPACITANCE

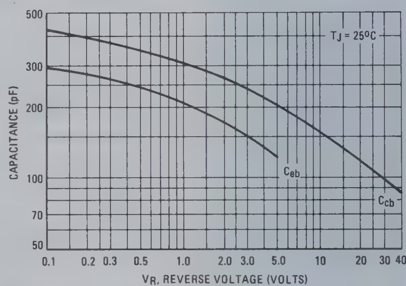


FIGURE 9 – TURN-ON TIME

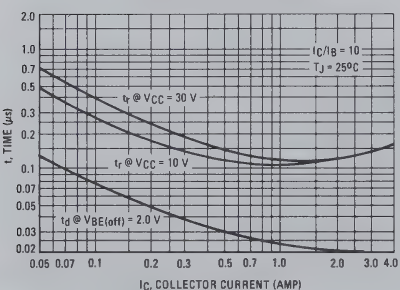


FIGURE 10 – TURN-OFF TIME

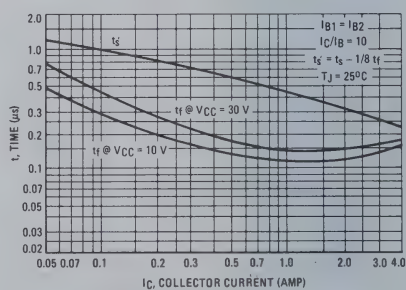
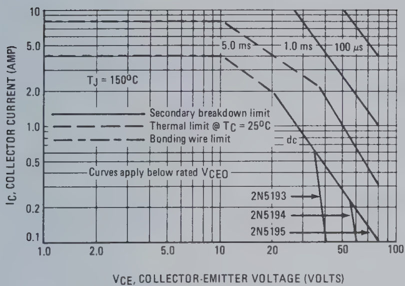


FIGURE 11

RATING AND THERMAL DATA
ACTIVE-REGION SAFE OPERATING AREA

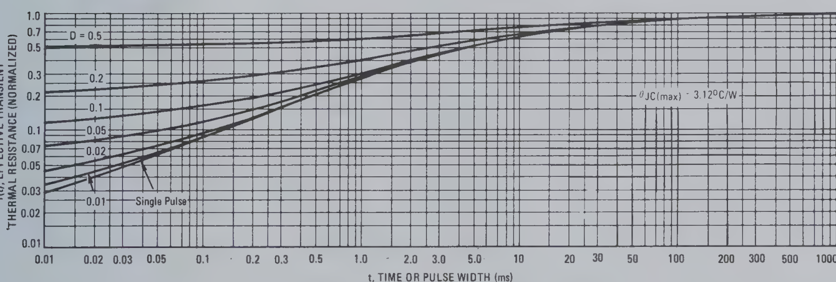


Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

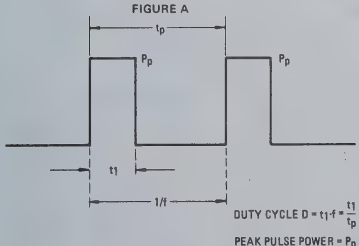
The data of Figure 11 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant$ 150°C. At high-case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 12 — THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N5193 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, tp = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of r(t_1, D) is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^{\circ}C$$

2N5301
2N5302
2N5303

MOTOROLA

1.3

HIGH-POWER NPN SILICON TRANSISTORS

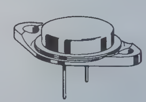
. . . for use in power amplifier and switching circuits applications.

- High Collector-Emitter Sustaining Voltage —
  $BV_{CEO(sus)}$ = 80 Vdc (Min) @ I_C = 200 mAdc (2N5303)
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.75 Vdc (Max) @ I_C = 10 Adc (2N5301, 2N5302)
  1.0 Vdc (Max) @ I_C = 10 Adc (2N5303)
- Excellent Safe Operating Area —
  200 Watt dc Power Rating to 30 Vdc (2N5303)
- Complements to PNP 2N4398, 2N4399 and 2N5745

20 AND 30 AMPERE POWER TRANSISTORS

NPN SILICON

40-60-80 VOLTS
200 WATTS



*MAXIMUM RATINGS

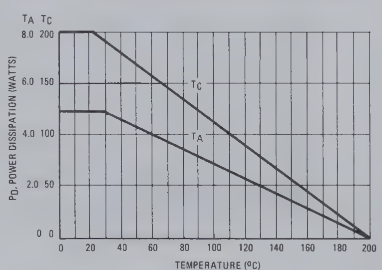
Rating	Symbol	2N5301	2N5302	2N5303	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Collector Current — Continuous	I_C	30	30	20	Adc
Base Current	I_B	← 7.5 →			Adc
Total Device Dissipation @ T_C=25°C Derate above 25°C	P_D	← 200 → ← 1.14 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

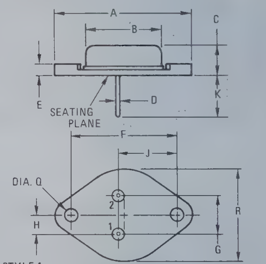
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Case to Ambient	θ_{CA}	34	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37	–	1.550
B	–	21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	2N5301	$V_{CEO(sus)}$	40	–	Vdc
	2N5302		60	–	
	2N5303		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N5301		–	5.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5302		–	5.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5303		–	5.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5301		–	1.0	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5302		–	1.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5303		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5301		–	10	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5302		–	10	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5303		–	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N5301		–	1.0	
(V_{CB} = 60 Vdc, I_E = 0)	2N5302		–	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5303		–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1)		h_{FE}			–
*(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	ALL TYPES		40	–	
*(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5303		15	60	
*(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N5301,2N5302		15	60	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5303		5.0	–	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N5301,2N5302		5.0	–	
*Collector-Emitter Saturation Voltage (Note 1)		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	2N5301,2N5302		–	0.75	
(I_C = 10 Adc, I_B = 1.0 Adc)	2N5303		–	1.0	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5303			1.5	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N5301,2N5302		–	2.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5303		–	2.0	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N5301,2N5302		–	3.0	
*Base-Emitter Saturation Voltage (Note 1)		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	ALL TYPES		–	1.7	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5301,2N5302		–	1.8	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5303		–	2.0	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N5301,2N5302		–	2.5	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5303		–	2.5	
*Base-Emitter On Voltage (Note 1)		$V_{BE(on)}$			Vdc
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5303		–	1.5	
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N5301,2N5302		–	1.7	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5303		–	2.5	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N5301,2N5302		–	3.0	
***DYNAMIC CHARACTERISTICS**					
Current-Gain—Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.0	–	MHz
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	40	–	–
***SWITCHING CHARACTERISTICS**					
Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	–	1.0	μs
Storage Time		t_s	–	2.0	μs
Fall Time		t_f	–	1.0	μs

*Indicates JEDEC Registered Data.
Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

FIGURE 2 – TURN-ON TIME

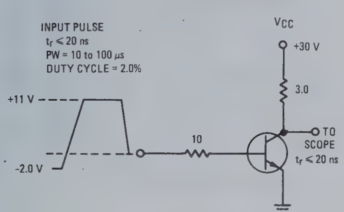
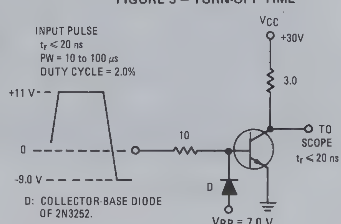


FIGURE 3 – TURN-OFF TIME



1.3

FIGURE 4 — THERMAL RESPONSE

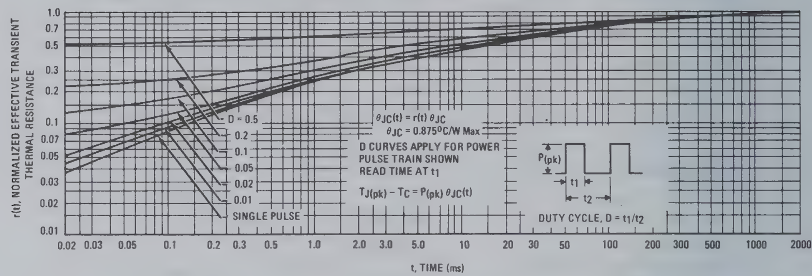


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA

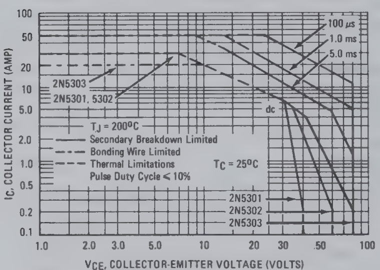


FIGURE 6 — CAPACITANCE versus VOLTAGE

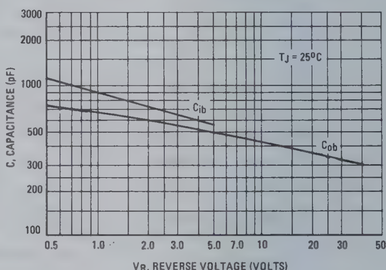


FIGURE 7 — TURN-ON TIME

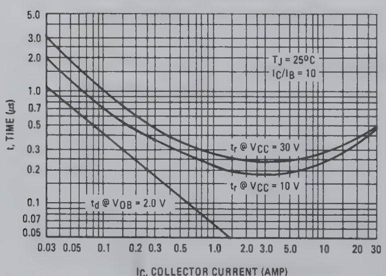


FIGURE 8 — TURN-OFF TIME

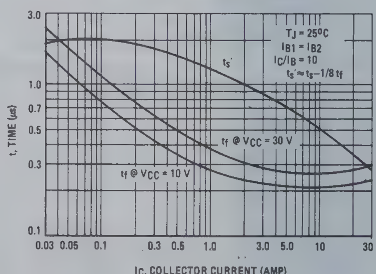


FIGURE 9 – DC CURRENT GAIN

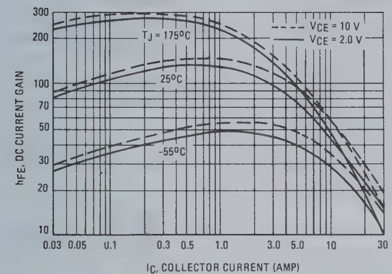


FIGURE 10 – COLLECTOR SATURATION REGION

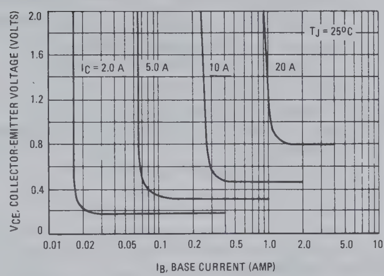


FIGURE 11 – EFFECTS OF BASE-EMITTER RESISTANCE

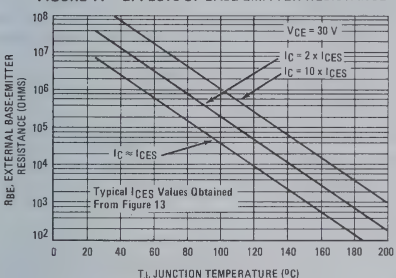


FIGURE 12 – "ON" VOLTAGES

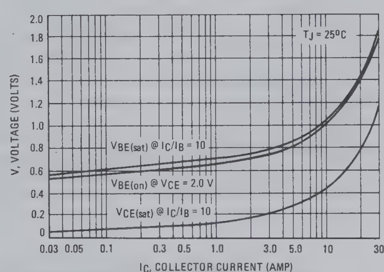


FIGURE 13 – COLLECTOR CUT-OFF REGION

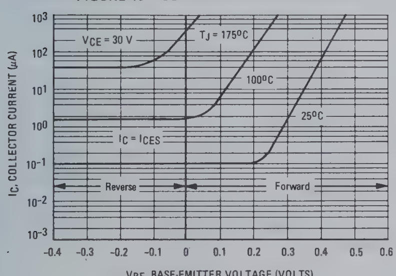
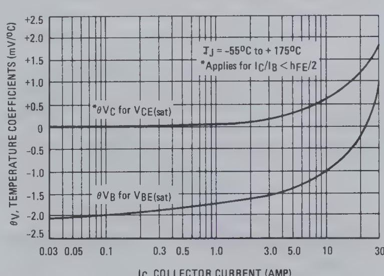


FIGURE 14 – TEMPERATURE COEFFICIENTS



2N5336
thru
2N5339

MOTOROLA

1.3

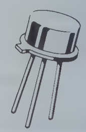
MEDIUM-POWER NPN SILICON TRANSISTORS

. . . designed for switching and wide band amplifier applications.

- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 5.0 Amp
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-39 Case for Critical Space-Limited Applications
- Complement to 2N6190 thru 2N6193

5 AMPERE
POWER TRANSISTORS
NPN SILICON

80–100 VOLTS
6 WATTS

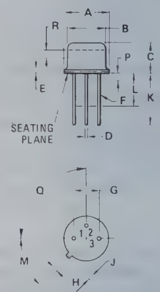


MAXIMUM RATINGS

Rating	Symbol	2N5336 2N5337	2N5338 2N5339	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	6.0 34.3		Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	29.2	$^oC/W$

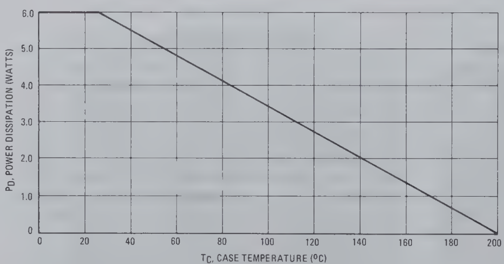


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45^o NOM		45^o NOM	
P	–	1.27	–	0.050
Q	90^o NOM		90^o NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79–02
(TO-39)

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$, unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage*		–	$BV_{CEO(sus)}$*			Vdc
(I_C = 50 mAdc, I_B = 0)	2N5336, 2N5337			80	–	
	2N5338, 2N5339			100	–	
Collector Cutoff Current		–	I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N5336, 2N5337			–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N5338, 2N5339			–	100	
Collector Cutoff Current		12	I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5336, 2N5337			–	10	
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5338, 2N5339			–	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, $T_C = 150^oC$)	2N5336, 2N5337			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc, $T_C = 150^oC$)	2N5338, 2N5339			–	1.0	
Collector Cutoff Current		–	I_{CBO}			μAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N5336, 2N5337			–	10	
(V_{CB} = 100 Vdc, I_E = 0)	2N5338, 2N5339			–	10	
Emitter Cutoff Current		–	I_{EBO}			μAdc
(V_{BE} = 6.0 Vdc, I_C = 0)				–	100	
ON CHARACTERISTICS						
DC Current Gain*		8	h_{FE}*			–
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N5336, 2N5338			30	–	
	2N5337, 2N5339			60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N5336, 2N5338			30	120	
	2N5337, 2N5339			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N5336, 2N5338			20	–	
	2N5337, 2N5339			40	–	
Collector-Emitter Saturation Voltage*		9, 11, 13	$V_{CE(sat)}$*			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	0.7	
(I_C = 5.0 Adc, I_B = 0.5 Adc)				–	1.2	
Base-Emitter Saturation Voltage*		11, 13	$V_{BE(sat)}$*			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	1.2	
(I_C = 5.0 Adc, I_B = 0.5 Adc)				–	1.8	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product		–	f_T			MHz
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 10 MHz)				30	–	
Output Capacitance		7	C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)				–	250	
Input Capacitance		7	C_{ib}			pF
(V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)				–	1,000	
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc,	2, 3	t_d	–	100	ns
Rise Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc)		t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	2, 6	t_s	–	2.0	μs
Fall Time	$I_{B1} = I_{B2}$ = 0.2 Adc)		t_f	–	200	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

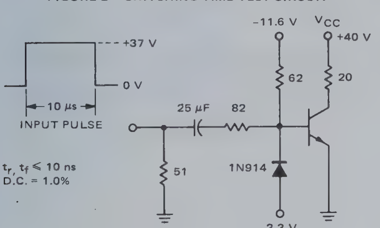


FIGURE 3 — TURN-ON TIME

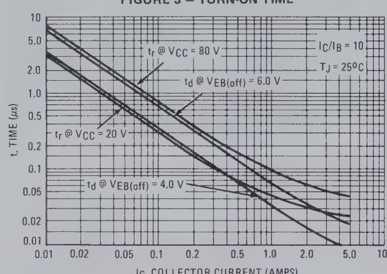


FIGURE 4 — THERMAL RESPONSE

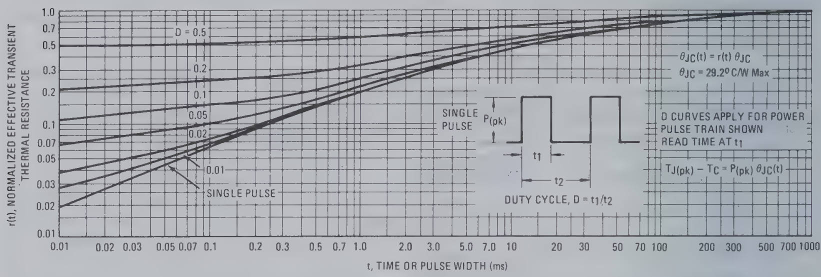
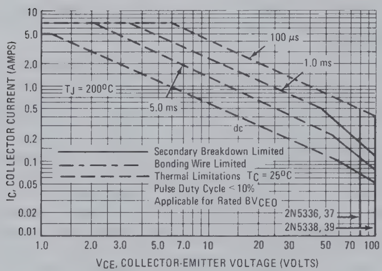


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 — TURN-OFF TIME

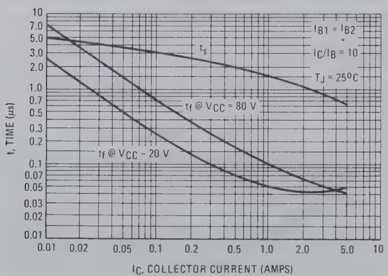


FIGURE 7 — CAPACITANCE versus VOLTAGE

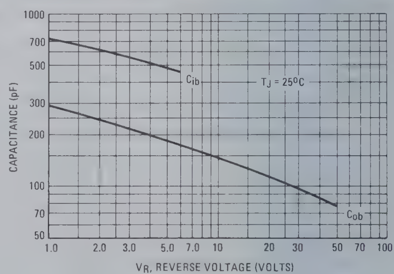


FIGURE 8 — DC CURRENT GAIN

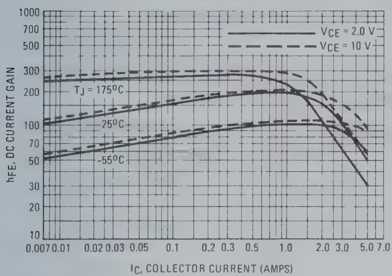


FIGURE 9 — COLLECTOR SATURATION REGION

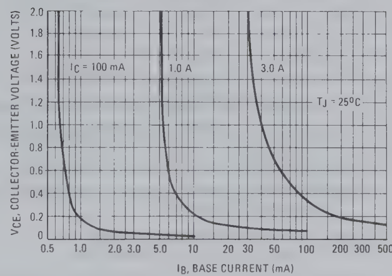


FIGURE 10 — EFFECTS OF BASE-EMITTER RESISTANCE

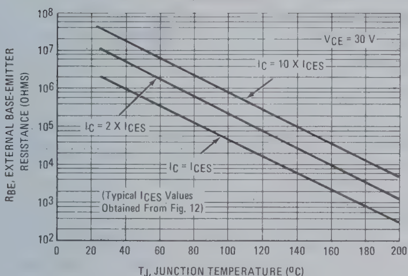


FIGURE 11 — ON VOLTAGES

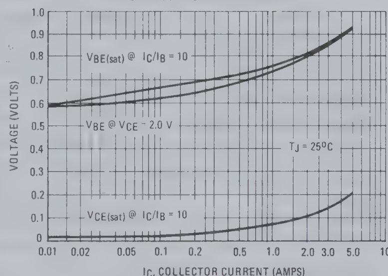


FIGURE 12 — COLLECTOR CUT-OFF REGION

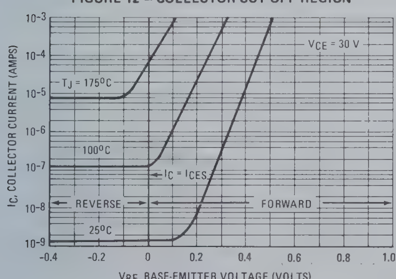
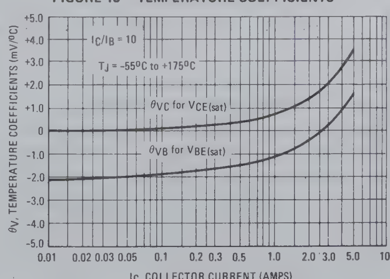


FIGURE 13 — TEMPERATURE COEFFICIENTS



2N5344
2N5345

MOTOROLA

1.3

HIGH VOLTAGE POWER PNP SILICON TRANSISTORS

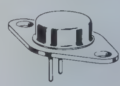
. . . designed for high-voltage switching and amplifier applications.

- High Voltage Ratings – V_{CEO} = 250 and 300 Vdc
- Fast Switching Times – Typically Less Than 550 ns Total @ V_{CC} = 100 Vdc
- High Current-Gain-Bandwidth Product – f_T = 60 MHz (Min) @ I_C = 100 mAdc
- Packaged in the Compact, High-Efficiency TO-66 Case

1 AMPERE

POWER TRANSISTORS
PNP SILICON

250-300 VOLTS
40 WATTS



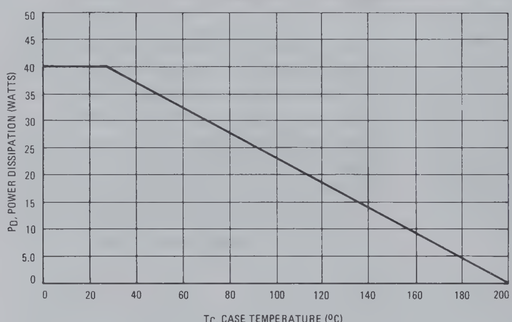
MAXIMUM RATINGS

Rating	Symbol	2N5344	2N5345	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	Vdc
Collector-Base Voltage	V_{CB}	250	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	1.0		Adc
Base Current – Continuous	I_B	0.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 228		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

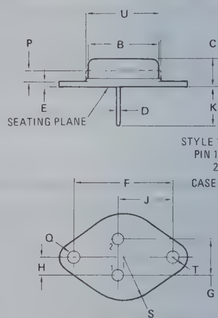
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.38	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves Are Indicated By Figure 5.
All Limits Are Applicable And Must Be Observed



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	-	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	2N5344	5	$V_{CEO(sus)}$	250	—	Vdc
	2N5345			300	—	
Collector Cutoff Current (V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5344	10, 12	I_{CEX}	—	100	μAdc
(V_{CE} = 270 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5345			—	100	
(V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5344			—	1.0	mAdc
(V_{CE} = 270 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5345			—	1.0	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		—	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		—	I_{EBO}	—	0.1	mAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)		8	h_{FE}	25	150	—
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)				7.0	—	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		9, 11, 13	$V_{CE(sat)}$	—	3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		11, 13	$V_{BE(sat)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 100 mAdc, V_{CE} = 20 Vdc, f = 10 MHz)		—	f_T	60	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0)		7	C_{ob}	—	200	pF
SWITCHING CHARACTERISTICS						
Turn-On	(V_{CC} = 100 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc)	2, 3	t_{on}	—	200	ns
Turn-Off	(V_{CC} = 100 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc)	2, 6	t_{off}	—	700	ns

(1) Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

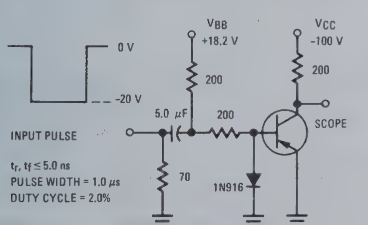
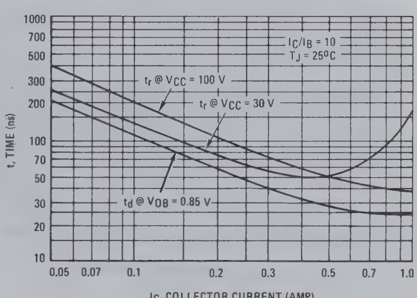


FIGURE 3 – TURN-ON TIME



1.3

FIGURE 4 – THERMAL RESPONSE

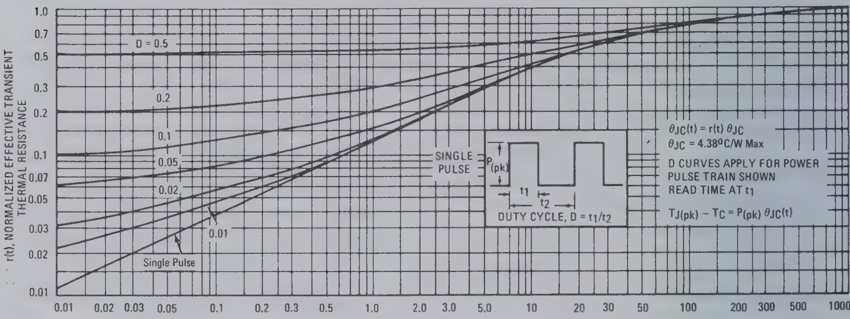
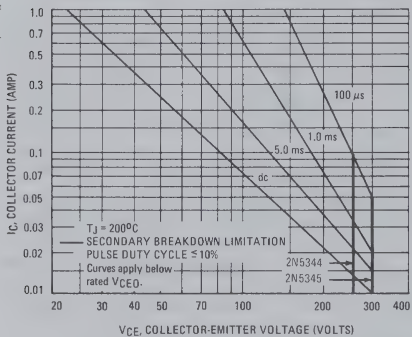


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

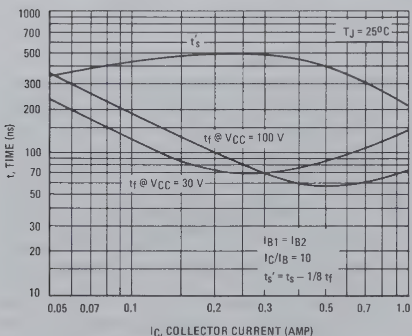
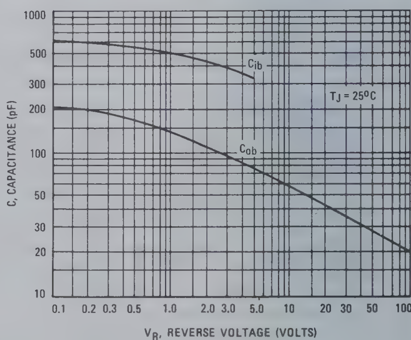


FIGURE 7 – CAPACITANCES



1.3

TYPICAL DC CHARACTERISTICS

FIGURE 8 – DC CURRENT GAIN

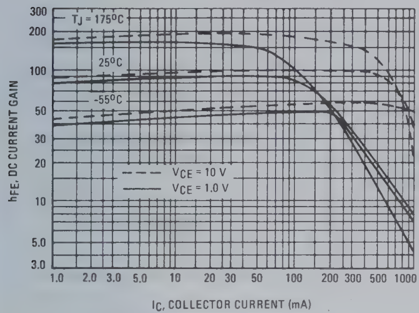


FIGURE 9 – COLLECTOR SATURATION REGION

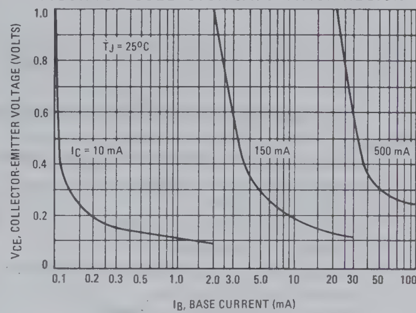


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

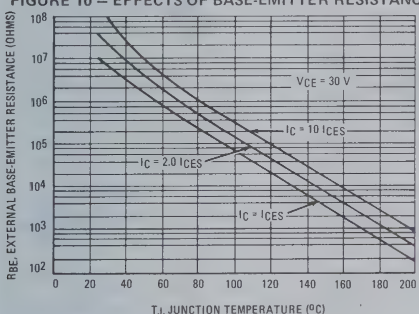


FIGURE 11 – "ON" VOLTAGES

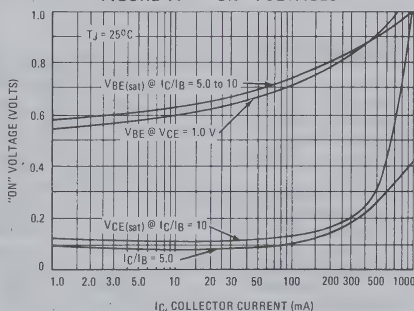


FIGURE 12 – COLLECTOR CUT-OFF REGION

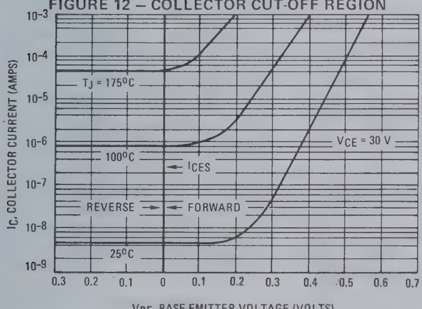
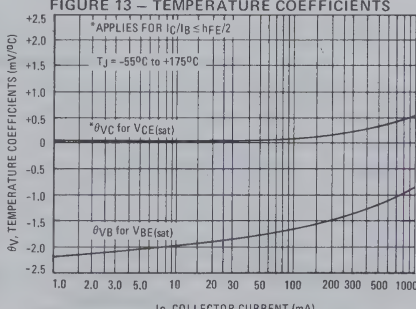


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N5346 thru 2N5349

MOTOROLA

1.3

MEDIUM-POWER NPN SILICON TRANSISTORS

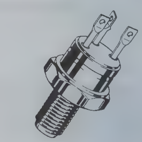
. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 7.0 Adc
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact, High Dissipation TO-59 Case
- Isolated Collector Configuration
- Complementary to 2N6186 thru 2N6189

7 AMPERE

POWER TRANSISTORS NPN SILICON

80–100 VOLTS
60 WATTS



*MAXIMUM RATINGS

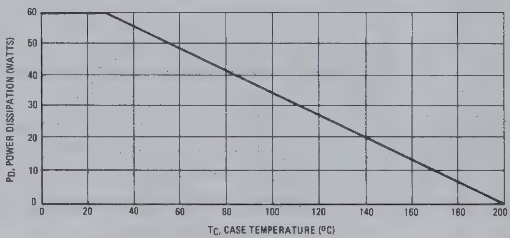
Rating	Symbol	2N5346 2N5347	2N5348 2N5349	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	7.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 343		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

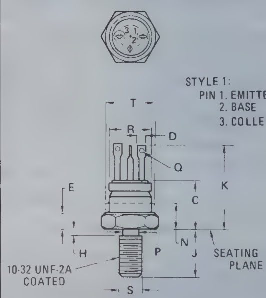
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.91	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	10.77	11.10	0.424	0.437
C	8.13	11.89	0.320	0.468
E	2.29	3.81	0.090	0.150
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	10.16	11.56	0.400	0.455
K	14.48	19.38	0.570	0.763
L	2.29	2.79	0.090	0.110
N	–	6.35	–	0.250
P	4.14	4.80	0.163	0.189
Q	1.02	1.65	0.040	0.065
R	8.08	9.65	0.318	0.380
S	4.212	4.310	0.1658	0.1697
T	9.65	11.10	0.380	0.437

All JEDEC dimensions and notes apply
Collector isolated from case.

CASE 160-03
TO-59

*ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		–	$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N5346, 2N5347			80	–	
	2N5348, 2N5349			100	–	
Collector Cutoff Current		–	I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N5346, 2N5347			–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N5348, 2N5349			–	100	
Collector Cutoff Current		12	I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5346, 2N5347			–	10	
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5348, 2N5349			–	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5346, 2N5347			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5348, 2N5349			–	1.0	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		–	I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		–	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)						
DC Current Gain		8	h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N5346, 2N5348			30	–	
	2N5347, 2N5349			60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N5346, 2N5348			30	120	
	2N5347, 2N5349			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N5346, 2N5348			20	–	
	2N5347, 2N5349			40	–	
Collector-Emitter Saturation Voltage		9, 11, 13	$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	0.7	
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	1.2	
Base-Emitter Saturation Voltage		11, 13	$V_{BE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	1.2	
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	2.0	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		–	f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		7	C_{ob}	–	250	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		7	C_{ib}	–	1,000	pF
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc,	2, 3	t_d	–	100	ns
Rise Time	I_C = 2.0 Adc, I_{B1} = 200 mAdc)		t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	2, 6	t_s	–	2.0	μs
Fall Time	I_{B1} = I_{B2} = 200 mAdc)		t_f	–	200	ns

*Indicates JEDEC Registered Data. (1) Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

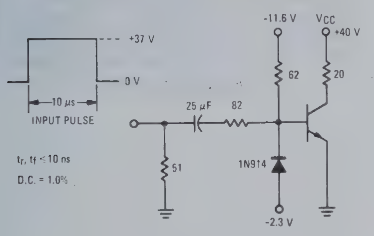
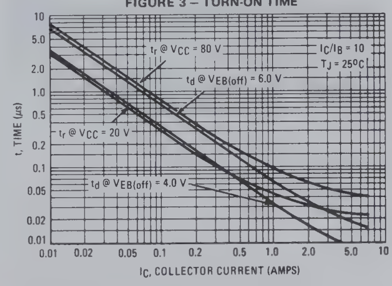


FIGURE 3 – TURN-ON TIME



1.3

FIGURE 4 – THERMAL RESPONSE

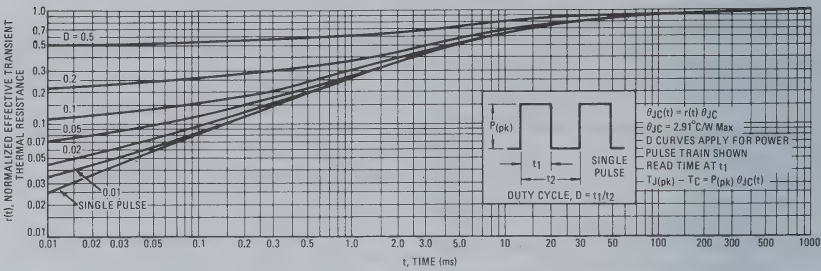
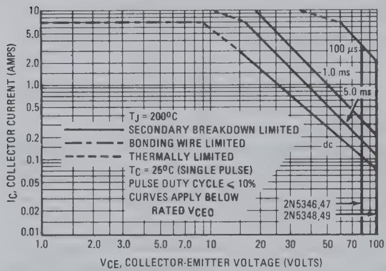


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leqslant 200^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

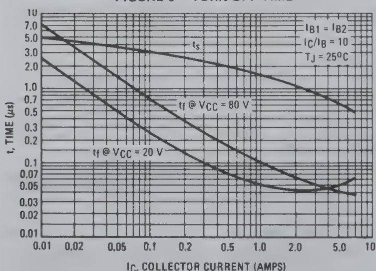


FIGURE 7 – CAPACITANCE versus VOLTAGE

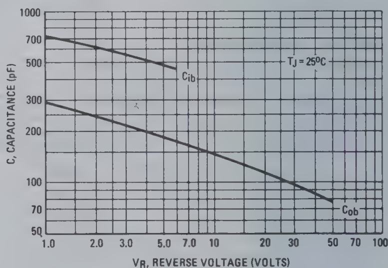


FIGURE 8 – DC CURRENT GAIN

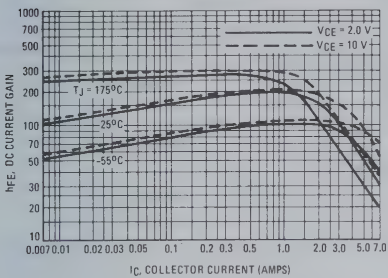


FIGURE 9 – COLLECTOR SATURATION REGION

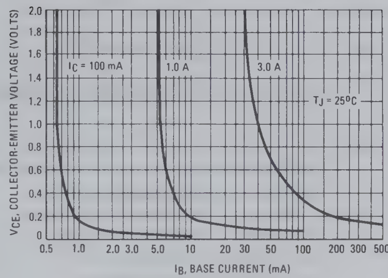


FIGURE 10 – EFFECTS OF BASE EMITTER RESISTANCE

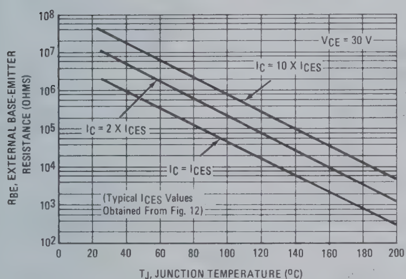


FIGURE 11 – "ON" VOLTAGES

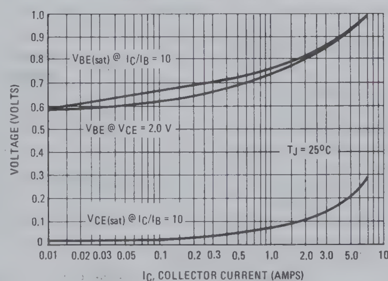


FIGURE 12 – COLLECTOR CUT-OFF REGION

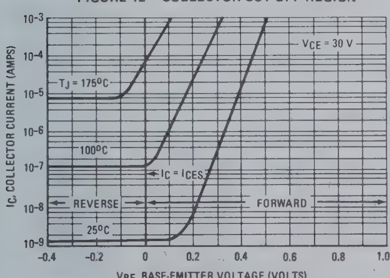
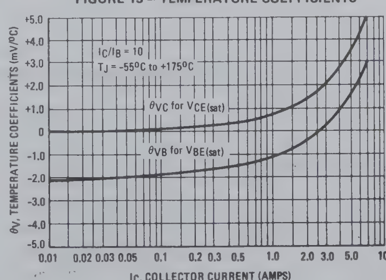


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N5427 thru 2N5430

MOTOROLA

1.3

MEDIUM-POWER NPN SILICON TRANSISTORS

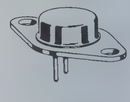
. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 7.0 Adc
- DC Current Gain Specified to 7 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-66 Case

7 AMPERE

POWER TRANSISTORS NPN SILICON

80–100 VOLTS 40 WATTS



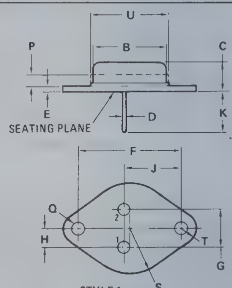
*MAXIMUM RATINGS

Rating	Symbol	2N5427 2N5428	2N5429 2N5430	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	7.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 228		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.37	°C/W

* Indicates JEDEC Registered Data



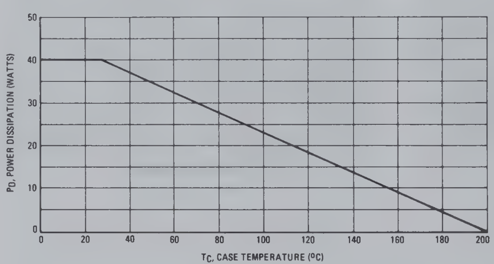
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



***ELECTRICAL CHARACTERISTICS** (T_C = 25°C, unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		–	$BV_{CEO(sus)}$*			Vdc
(I_C = 50 mAdc, I_B = 0)	2N5427, 2N5428			80	–	
	2N5429, 2N5430			100	–	
Collector Cutoff Current		–	I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N5427, 2N5428			–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N5429, 2N5430			–	100	
Collector Cutoff Current		12	I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5427, 2N5428			–	10	
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5429, 2N5430			–	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5427, 2N5428			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5429, 2N5430			–	1.0	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		–	I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		–	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)						
DC Current Gain		8	h_{FE}*			–
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N5427, 2N5429			30	–	
	2N5428, 2N5430			60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N5427, 2N5429			30	120	
	2N5428, 2N5430			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N5427, 2N5429			20	–	
	2N5428, 2N5430			40	–	
Collector-Emitter Saturation Voltage		9, 11, 13	$V_{CE(sat)}$*			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	0.7	
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	1.2	
Base-Emitter Saturation Voltage		11, 13	$V_{BE(sat)}$*			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	1.2	
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	2.0	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		–	f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		7	C_{ob}	–	250	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		7	C_{ib}	–	1,000	pF
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc,	2, 3	t_d	–	100	ns
Rise Time	I_C = 2.0 Adc, I_{B1} = 200 mAdc)		t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	2, 6	t_s	–	2.0	μs
Fall Time	I_{B1} = I_{B2} = 200 mAdc)		t_f	–	200	ns

*Indicates JEDEC Registered Data. (1)Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

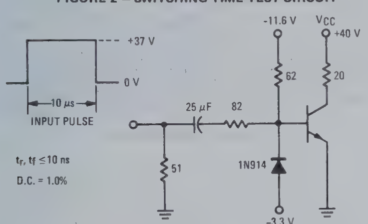


FIGURE 3 – TURN-ON TIME

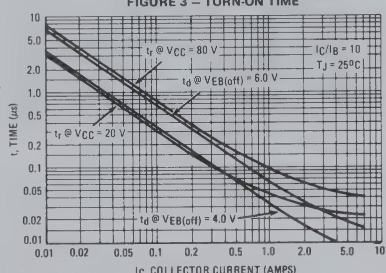


FIGURE 4 — THERMAL RESPONSE

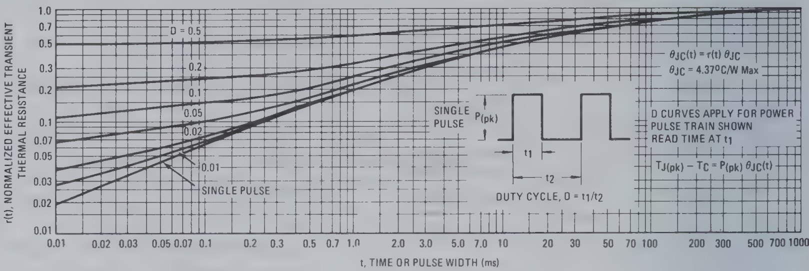
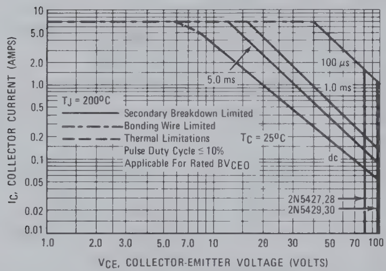


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 — TURN-OFF TIME

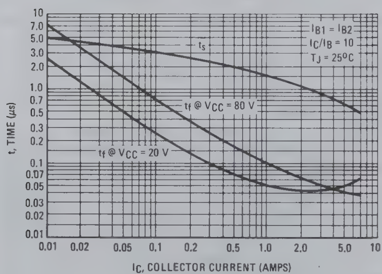
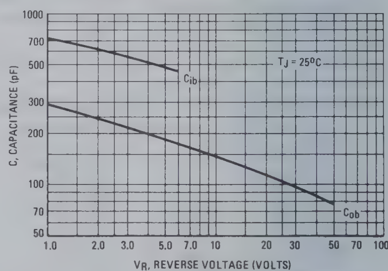


FIGURE 7 — CAPACITANCE versus VOLTAGE



1.3

FIGURE 8 – DC CURRENT GAIN

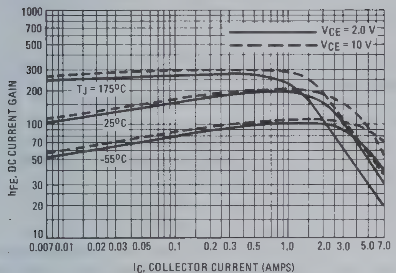


FIGURE 9 – COLLECTOR SATURATION REGION

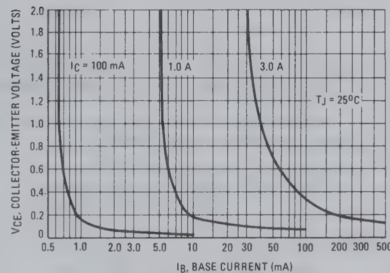


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

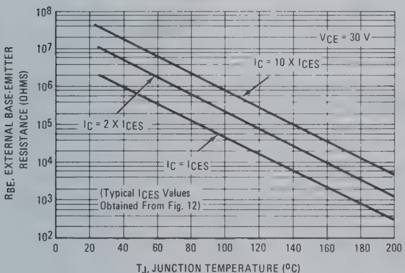


FIGURE 11 – "ON" VOLTAGES

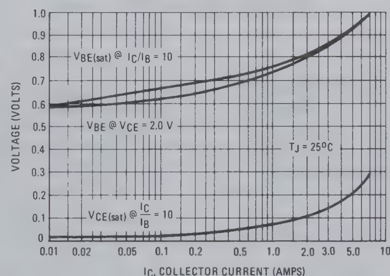


FIGURE 12 – COLLECTOR CUT-OFF REGION

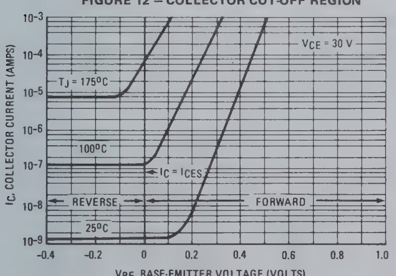
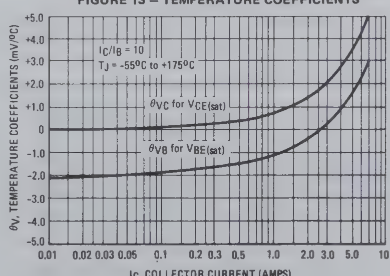


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N5629, 2N5630, 2N5631 NPN
2N6029, 2N6030, 2N6031 PNP

MOTOROLA

1.3

HIGH-VOLTAGE – HIGH POWER TRANSISTORS

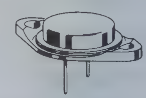
. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc – 2N5629, 2N6029
  = 120 Vdc – 2N5630, 2N6030
  = 140 Vdc – 2N5631, 2N6031
- High DC Current Gain – @ I_C = 8.0 Adc
  h_{FE} = 25 (Min) – 2N5629, 2N6029
  = 20 (Min) – 2N5630, 2N6030
  = 15 (Min) – 2N5631, 2N6031
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc

16 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

100-120-140 VOLTS
200 WATTS



*MAXIMUM RATINGS

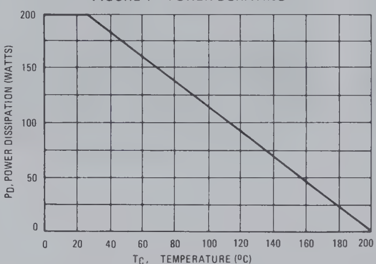
Rating	Symbol	2N5629 2N6029	2N5630 2N6030	2N5631 2N6031	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	7.0			Vdc
Collector Current – Continuous Peak	I_C	16 20			Adc
Base Current Continuous	I_B	5.0			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

*THERMAL CHARACTERISTICS

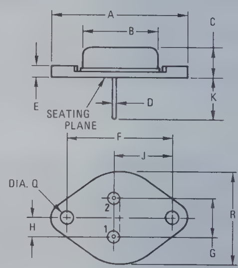
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



Safe Area Curves are indicated by Figure 5 All Limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

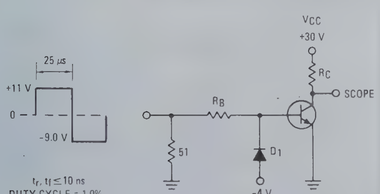
Collector connected to case.
CASE 11-01
(TO-3)

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5629, 2N6029	$V_{CEO(sus)}$	100	—	Vdc
	2N5630, 2N6030		120		
	2N5631, 2N6031		140	—	
Collector-Emitter Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	2N5629, 2N6029	I_{CEO}	—	1.0	mAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N5630, 2N6030		—	1.0	
(V_{CE} = 70 Vdc, I_B = 0)	2N5631, 2N6031		—	1.0	
Collector-Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)		I_{CEX}	—	1.0	mAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			—	5.0	
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)	2N5629, 2N6029	h_{FE}	25	100	—
	2N5630, 2N6030		20	80	
	2N5631, 2N6031		15	60	
(I_C = 16 Adc, V_{CE} = 2.0 Vdc)	All Types		4.0	—	
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)	All Types	$V_{CE(sat)}$	—	1.0	Vdc
(I_C = 16 Adc, I_B = 4.0 Adc)			—	2.0	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	—	1.8	Vdc
Base-Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5629, 30, 31	C_{ob}	—	500	pF
	2N6029, 30, 31			1000	
Small-Signal Current Gain (I_C = 4.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15	—	—

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤300 µs, Duty Cycle ≥2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ~100 mA
MSD6100 USED BELOW I_B ~100 mA

For PNP test circuit, reverse all polarities and D1.

FIGURE 3 — TURN-ON TIME

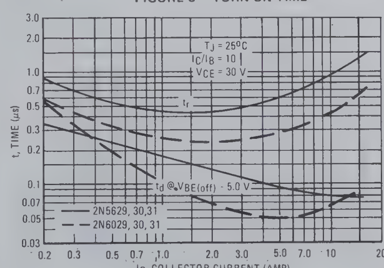


FIGURE 4 – THERMAL RESPONSE

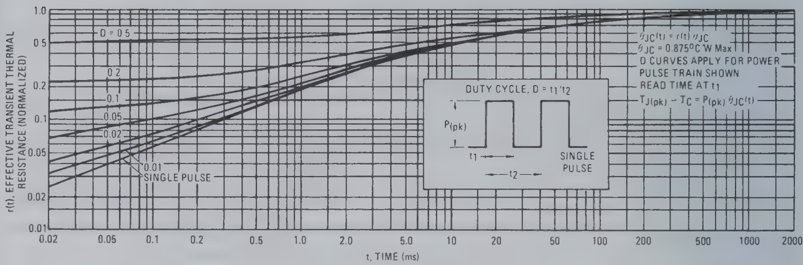
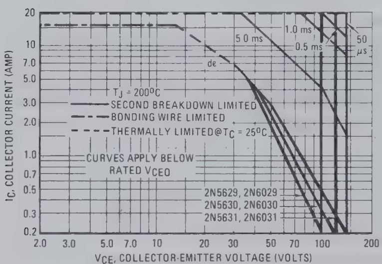


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



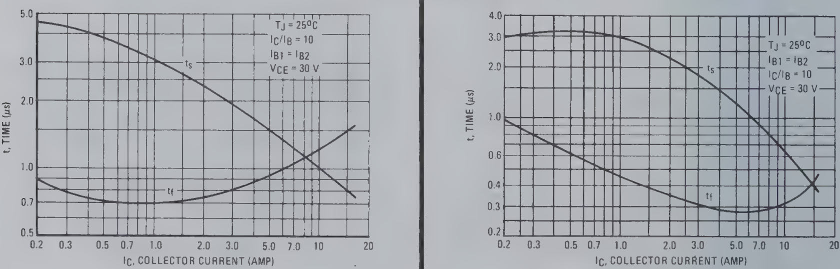
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN
2N5629, 2N5630, 2N5631

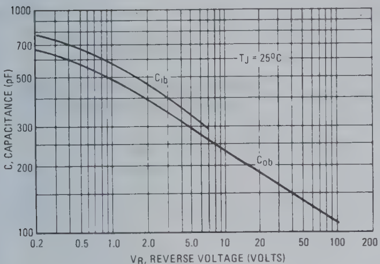
PNP
2N6029, 2N6030, 2N6031

FIGURE 6 – TURN-OFF TIME



NPN 2N5629, 2N5630, 2N5631	PNP 2N6029, 2N6030, 2N6031

FIGURE 7 – CAPACITANCE



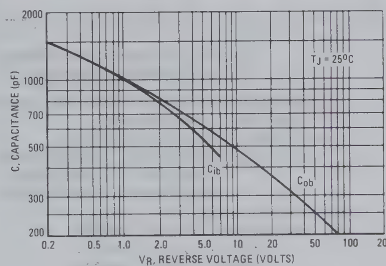
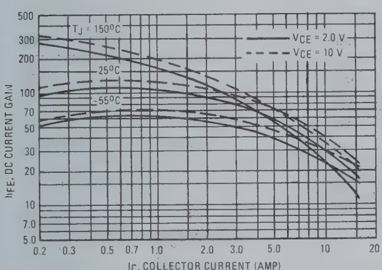


FIGURE 8 – DC CURRENT GAIN



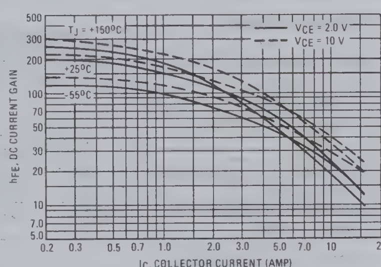
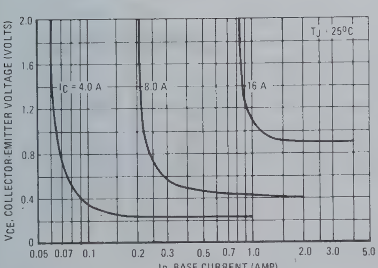
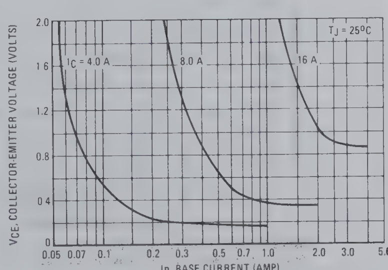


FIGURE 9 – COLLECTOR SATURATION REGION





2N5632, 2N5633, 2N5634 NPN
2N6229, 2N6230, 2N6231 PNP

MOTOROLA

HIGH VOLTAGE-HIGH-POWER SILICON TRANSISTORS

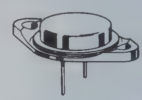
. . . designed for use in high power audio amplifier applications and high-voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min) — 2N5632, 2N6229
  = 120 Vdc (Min) — 2N5633, 2N6230
  = 140 Vdc (Min) — 2N5634, 2N6231
- High DC Current Gain @ I_C = 5.0 Adc —
  h_{FE} = 25 (Min) — 2N5632, 2N6229
  = 20 (Min) — 2N5633, 2N6230
  = 15 (Min) — 2N5634, 2N6231
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 7.5 Adc

10 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

100-120-140 VOLTS
150 WATTS



*MAXIMUM RATINGS

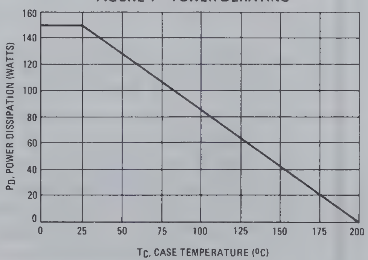
Rating	Symbol	2N5632 2N6229	2N5633 2N6230	2N5634 2N6231	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}		7.0		Vdc
Collector Current — Continuous — Peak	I_C		10 15		Adc
Base Current — Continuous	I_B		5.0		Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D		150 0.857		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +200		°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data.

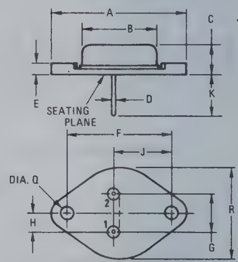
FIGURE 1 — POWER DERATING



Safe area limits are indicated by Figure 5.
Both limits are applicable and must be observed.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

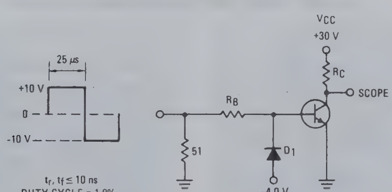
1.3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage[1] (I_C = 200 mAdc, I_B = 0)	2N5632, 2N6229 2N5633, 2N6230 2N5634, 2N6231	$V_{CEO(sus)}$	100 120 140	– – –	Vdc
Collector-Emitter Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 70 Vdc, I_B = 0)	2N5632, 2N6229 2N5633, 2N6230 2N5634, 2N6231	I_{CEO}	– – –	1.0 1.0 1.0	mAdc
Collector-Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	– –	1.0 5.0	mAdc
Collector Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain[1] (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5632, 2N6229 2N5633, 2N6230 2N5634, 2N6231 All Types	h_{FE}	25 20 15 5.0	100 80 60 –	–
Collector-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)		$V_{CE(sat)}$	– –	1.0 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)		$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5632, 2N5633, 2N5634 2N6229, 2N6230, 2N6231	C_{ob}	– –	300 600	pF
Small Signal Current Gain (V_{CE} = 10 Vdc, I_C = 2.0 Adc, f = 1.0 kHz)		h_{fe}	15	–	–

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

For PNP test, reverse all polarities and D1.

1.3

NPN	PNP
2N5632, 2N5633, 2N5634	2N6229, 2N6230, 2N6231

FIGURE 3 – TURN-ON TIME

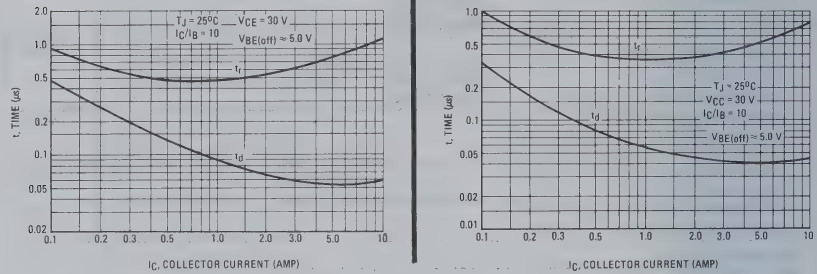


FIGURE 4 – THERMAL RESPONSE

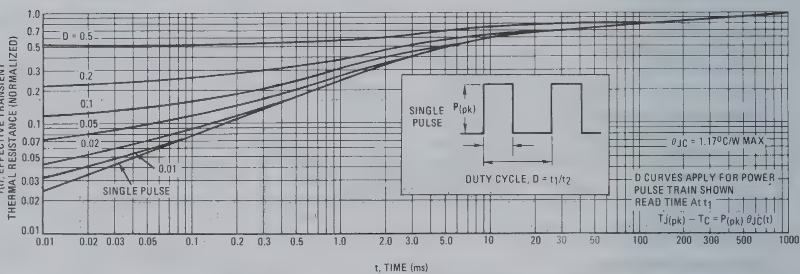
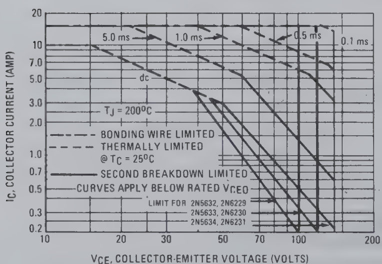


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN 2N5632, 2N5633, 2N5634	PNP 2N6229, 2N6230, 2N6231

FIGURE 6 — TURN-OFF TIME

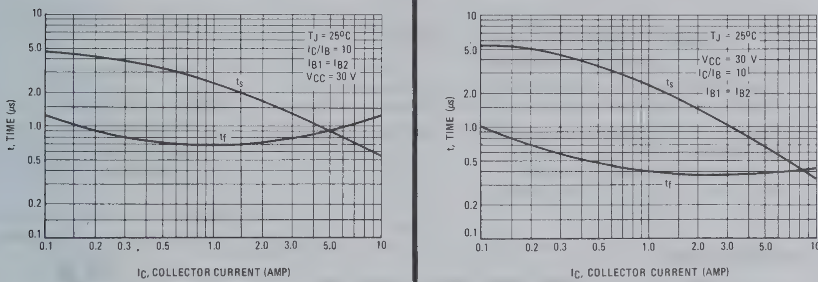


FIGURE 7 — CAPACITANCE

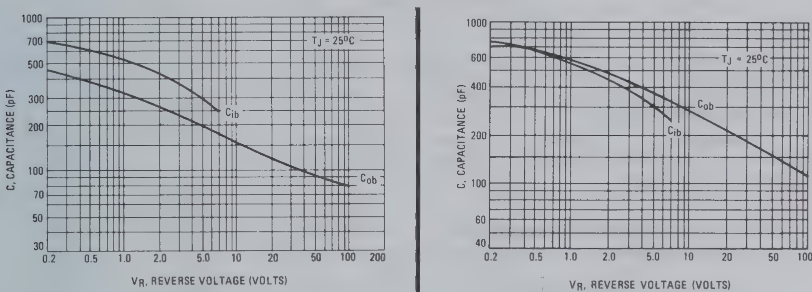
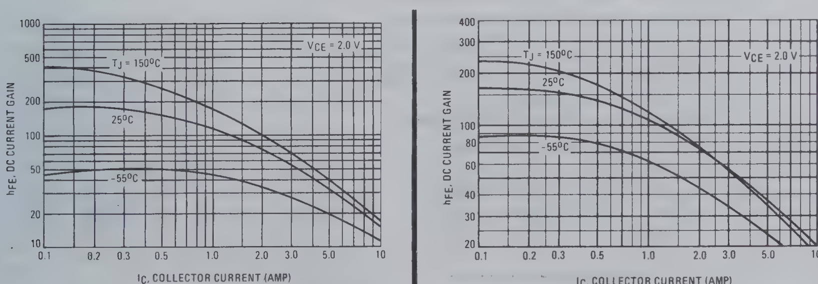


FIGURE 8 — DC CURRENT GAIN



2N5655, 2N5656, 2N5657

MOTOROLA

1.3

PLASTIC NPN SILICON HIGH-VOLTAGE POWER TRANSISTOR

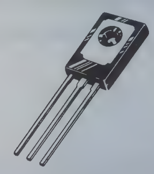
. . . designed for use in line-operated equipment such as audio output amplifiers; low-current, high-voltage converters; and AC line relays

- Excellent DC Current Gain — h_{FE} = 30-250 @ I_C = 100 mAdc
- Current-Gain — Bandwidth Product — f_T = 10 MHz (Min) @ I_C = 50 mAdc
- Packaged in Thermopad Case for Low Cost

0.5 AMPERE

POWER TRANSISTORS NPN SILICON

250-300-350 VOLTS 20 WATTS



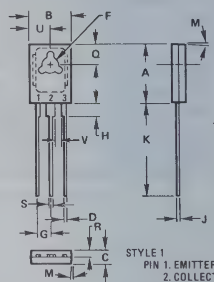
*MAXIMUM RATINGS

Rating	Symbol	2N5655	2N5656	2N5657	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector-Base Voltage	V_{CB}	275	325	375	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current — Continuous	I_C	← 0.5 →			Adc
Peak		← 1.0 →			
Base Current	I_B	← 0.25 →			Adc
Total Power Dissipation @ $T_C = 25^oC$	P_D	20			Watts
Derate above 25^oC		0.16			$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^oC/W$

*Indicates JEDEC Registered Data



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3^0 TYP		3^0 TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

FIGURE 1 – POWER DERATING

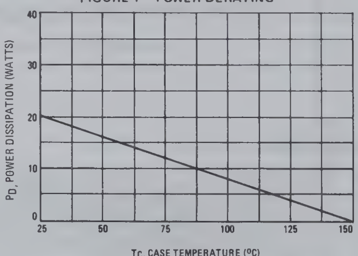
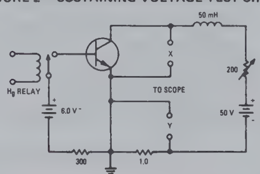


FIGURE 2 – SUSTAINING VOLTAGE TEST CIRCUIT



Safe Area Limits are indicated by Figures 3 and 4. Both limits are applicable and must be observed.

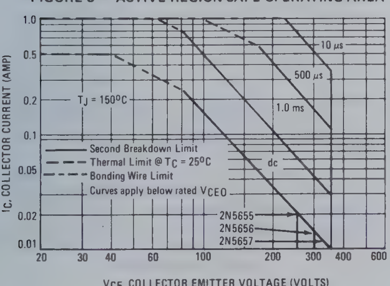
1.3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc (inductive), L = 50 mH)	2N5655 2N5656 2N5657	$V_{CEO(sus)}$	250 300 350		Vdc
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	2N5655 2N5656 2N5657	BV_{CEO}	250 300 350	- – –	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0) (V_{CE} = 250 Vdc, I_B = 0)	2N5655 2N5656 2N5657	I_{CEO}	– –	0.1 0.1 0.1	mAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 350 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 150 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C) (V_{CE} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C) (V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5655 2N5656 2N5657 2N5655 2N5656 2N5657	I_{CEX}	- - – – 	0.1 0.1 0.1 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CB} = 275 Vdc, I_E = 0) (V_{CB} = 325 Vdc, I_E = 0) (V_{CB} = 375 Vdc, I_E = 0)	2N5655 2N5656 2N5657	I_{CBO}	–	10 10 10	μAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}		10	μAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 10 Vdc) (I_C = 100 mAdc, V_{CE} = 10 Vdc) (I_C = 250 mAdc, V_{CE} = 10 Vdc) (I_C = 500 mAdc, V_{CE} = 10 Vdc)		h_{FE}	25 30 15 5.0	 250 – 	-
Collector-Emitter Saturation Voltage (1) (I_C = 100 mAdc, I_B = 10 mAdc) (I_C = 250 mAdc, I_B = 25 mAdc) (I_C = 500 mAdc, I_B = 100 mAdc)		$V_{CE(sat)}$	 –	1.0 2.5 10	Vdc
Base-Emitter Voltage (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc)		V_{BE}	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	10		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	25	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	–	-

*Indicates JEDEC Registered Data for 2N5655 Series
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity

FIGURE 3 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 – CURRENT GAIN

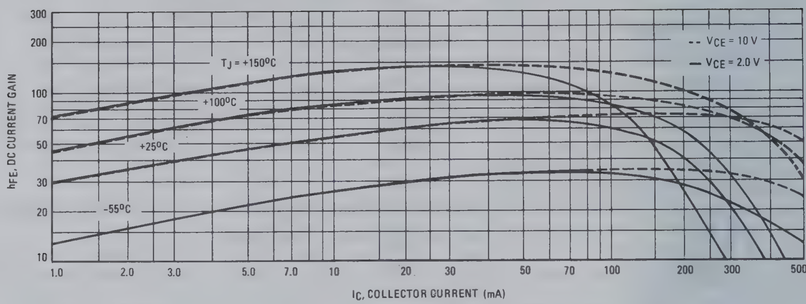


FIGURE 5 – "ON" VOLTAGES

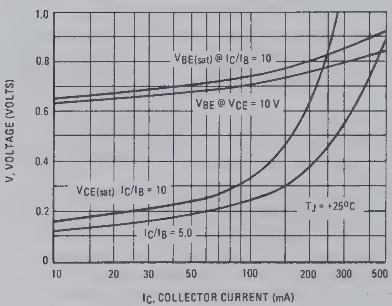


FIGURE 6 – CAPACITANCE

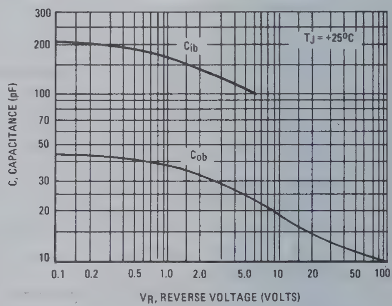


FIGURE 7 – TURN-ON TIME

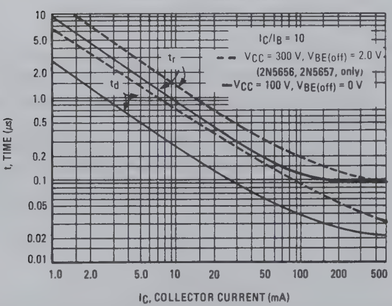
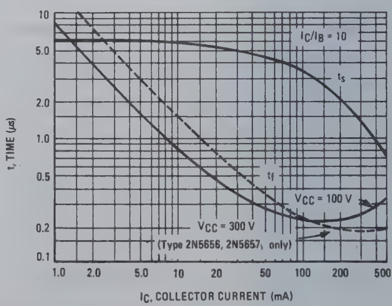


FIGURE 8 – TURN-OFF TIME



MOTOROLA

2N5683, 2N5684 PNP
2N5685, 2N5686 NPN

HIGH-CURRENT COMPLEMENTARY SILICON POWER TRANSISTORS

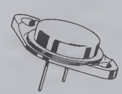
. . . designed for use in high-power amplifier and switching circuit applications.

- High Current Capability — I_C Continuous = 50 Amperes.
- DC Current Gain — h_{FE} = 15 - 60 @ I_C = 25 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 25 Adc

50 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60–80 VOLTS
300 WATTS

1.3



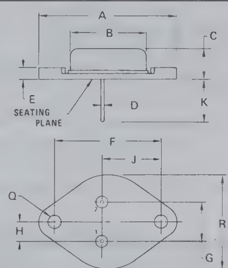
*MAXIMUM RATINGS

Rating	Symbol	2N5683 2N5685	2N5684 2N5686	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	50		Adc
Base Current	I_B	15		Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	300 1.715		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.584	$^oC/W$

*Indicates JEDEC Registered Data.

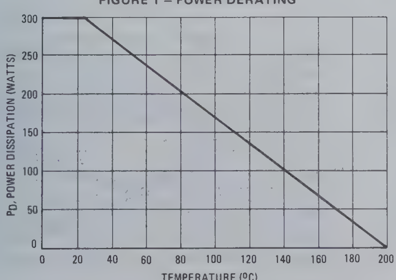


STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-3 Except Pin Diameter

FIGURE 1 — POWER DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

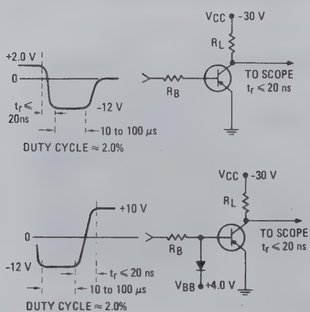
1.3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Note 1) (I_C = 0.2 Adc, I_B = 0)	2N5683, 2N5685 2N5684, 2N5686	$V_{CEO(sus)}$	60 80	– –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	2N5683, 2N5685 2N5684, 2N5686	I_{CEO}	– –	1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5683, 2N5685 2N5684, 2N5686 2N5683, 2N5685 2N5684, 2N5686	I_{CEX}	– – –	2.0 2.0 10 10	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	2N5683, 2N5685 2N5684, 2N5686	I_{CBO}	– –	2.0 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1) (I_C = 25 Adc, V_{CE} = 2.0 Vdc) (I_C = 50 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	15 5.0	60 –	–
Collector-Emitter Saturation Voltage (Note 1) (I_C = 25 Adc, I_B = 2.5 Adc) (I_C = 50 Adc, I_B = 10 Adc)		$V_{CE(sat)}$	– –	1.0 5.0	Vdc
Base-Emitter Saturation Voltage (Note 1) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter On Voltage (Note 1) (I_C = 25 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 5.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5683, 2N5684 2N5685, 2N5686	C_{ob}	– –	2000 1200	pF
Small-Signal Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	15	–	

*Indicates JEDEC Registered Data
Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

FIGURE 3 – TURN-ON TIME

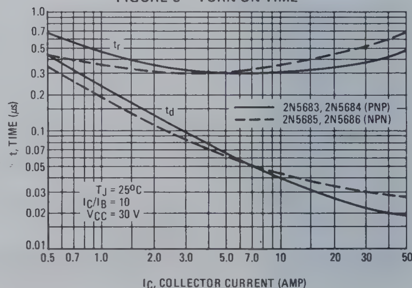


FIGURE 4 – THERMAL RESPONSE

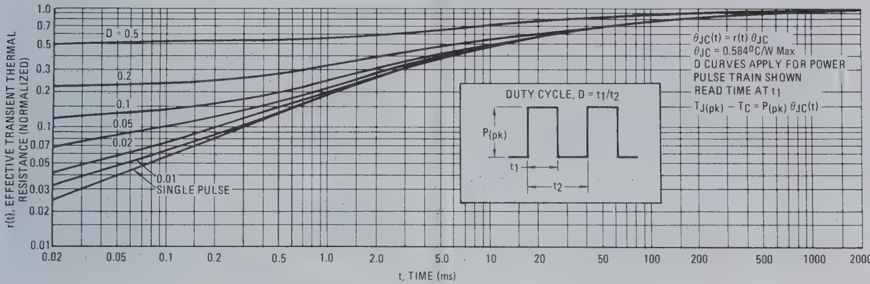
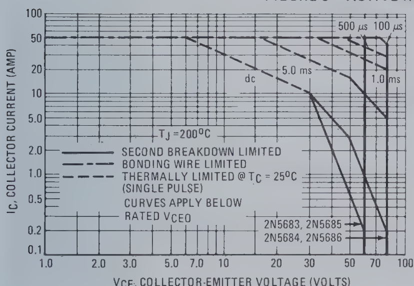


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

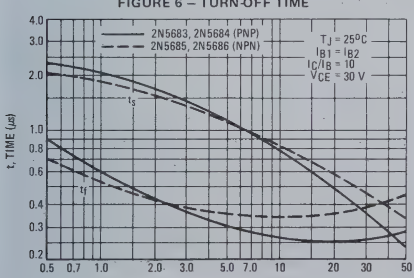
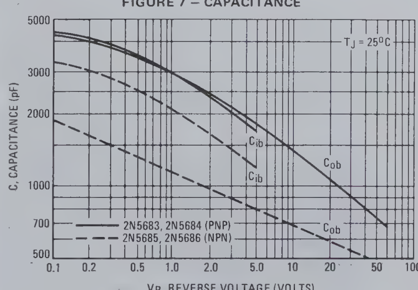


FIGURE 7 – CAPACITANCE



1.3

PNP
2N5683, 2N5684

NPN
2N5685, 2N5686

FIGURE 8 – DC CURRENT GAIN

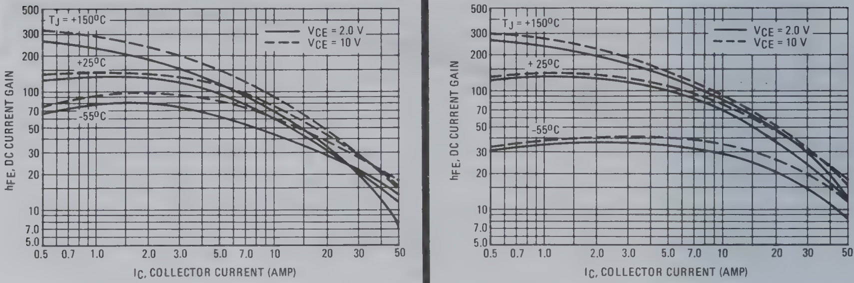


FIGURE 9 – COLLECTOR SATURATION REGION

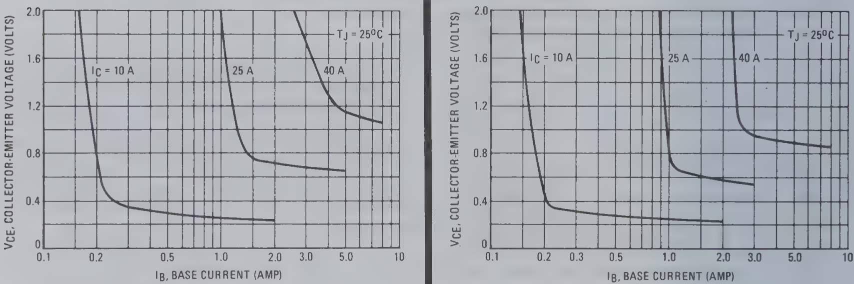
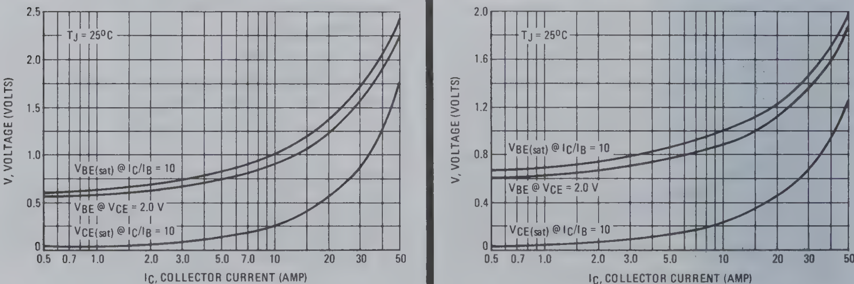


FIGURE 10 – "ON" VOLTAGES



MOTOROLA

2N5758, 2N5759, 2N5760 NPN
2N6226, 2N6227, 2N6228 PNP

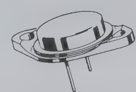
1.3

HIGH-VOLTAGE HIGH-POWER SILICON TRANSISTORS

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N5758, 2N6226
  = 120 Vdc (Min) – 2N5759, 2N6227
  = 140 Vdc (Min) – 2N5760, 2N6228
- DC Current Gain @ I_C = 3.0 Adc –
  h_{FE} = 25 (Min) – 2N5758, 2N6226
  = 20 (Min) – 2N5759, 2N6227
  = 15 (Min) – 2N5760, 2N6228
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 3.0 Adc

6 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
100-120-140 VOLTS
150 WATTS



*MAXIMUM RATINGS

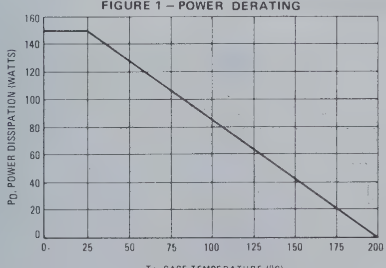
Rating	Symbol	2N5758 2N6226	2N5759 2N6227	2N5760 2N6228	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	7.0			Vdc
Collector Current - Continuous Peak	I_C	6.0 10			Adc
Base Current	I_B	4.0			Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	150 0.857			Watts $W/^oC$
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200			^oC

THERMAL CHARACTERISTICS

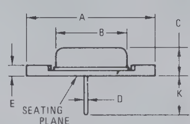
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^oC/W$

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING

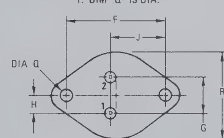


Safe area limits are indicated by Figure 5.
Both limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

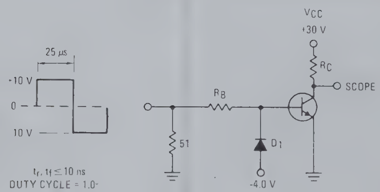
1.3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5758, 2N6226 2N5759, 2N6227 2N5760, 2N6228	$V_{CEO(sus)}$	100 120 140	– – –	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 70 Vdc, I_B = 0)	2N5758, 2N6226 2N5759, 2N6227 2N5760, 2N6228	I_{CEO}	– – –	1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	– –	1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)	2N5758, 2N6226 2N5759, 2N6227 2N5760, 2N6228 All Types	h_{FE}	25 20 15 5.0	100 80 60 –	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc) (I_C = 6.0 Adc, I_B = 1.2 Adc)		$V_{CE(sat)}$	– –	1.0 2.0	Vdc
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain - Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	300	pF
Small-Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15		

*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
(2) f_T $|h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ~100 mA
MSD6100 USED BELOW I_B ~100 mA

*For PNP test circuit, reverse all polarities and D1.

FIGURE 3 – TURN-ON TIME

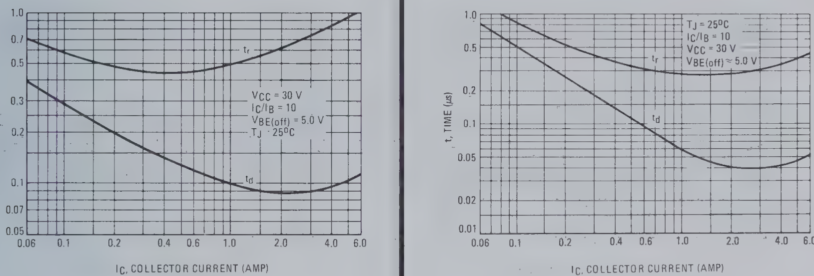


FIGURE 4 – THERMAL RESPONSE

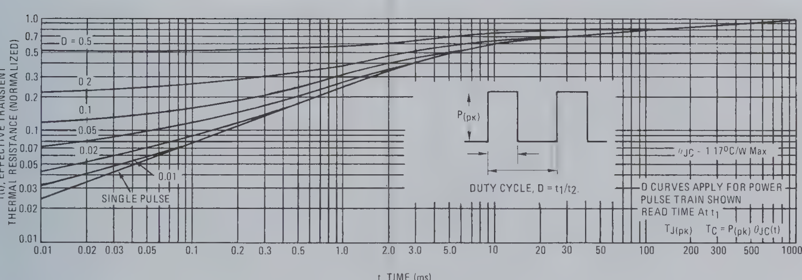
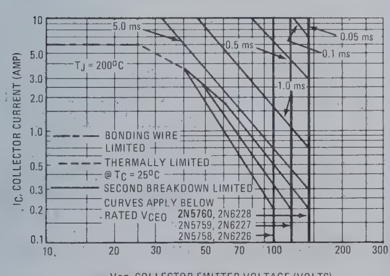


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



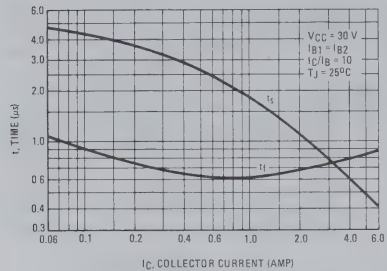
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

1.3

NPN 2N5758, 2N5759, 2N5760	PNP 2N6226, 2N6227, 2N6228

FIGURE 6 – TURN-OFF TIME



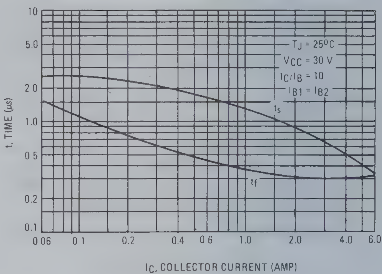
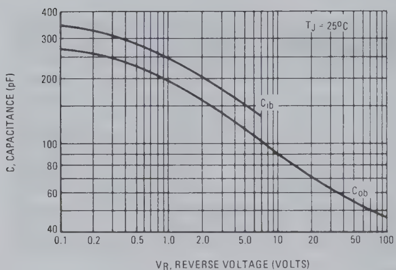


FIGURE 7 – CAPACITANCE



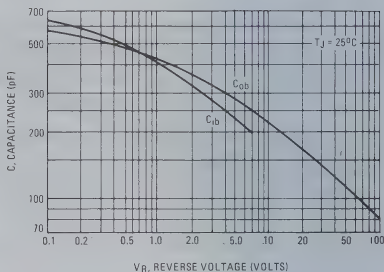
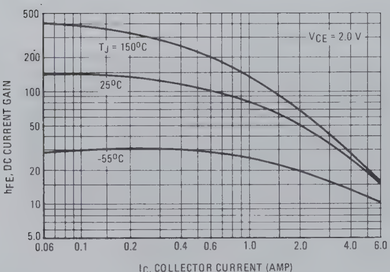
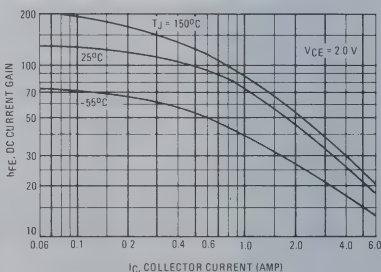


FIGURE 8 – DC CURRENT GAIN





![MOTOROLA]

2N5838
2N5839
2N5840

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

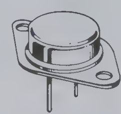
. . . designed for high voltage inverters, switching regulators, and line-operated amplifier applications. Especially well suited for switching power supply applications.

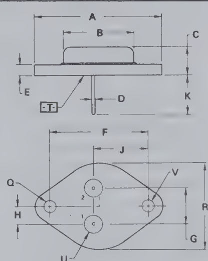
- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 250 Vdc (Min) —
  = 275 Vdc (Min) —
  = 350 Vdc (Min) —
- Excellent DC Current Gain —
  h_{FE} = 10–50 @ I_C = 2.0 Adc — 2N5839, 2N5840
  = 8–40 @ I_C = 3.0 Adc — 2N5838

3 AMPERE

NPN SILICON POWER TRANSISTORS

250–350 VOLTS
100 WATTS





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⊕	Ø .13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⊕	Ø .13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

*MAXIMUM RATINGS

Rating	Symbol	2N5838	2N5839	2N5840	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	275	350	Vdc
Collector-Emitter Voltage (R_{BE} = 50 Ω)	V_{CER}	275	300	375	Vdc
Collector-Emitter Voltage	V_{CEV}	275	300	375	Vdc
Collector-Base Voltage	V_{CB}	275	300	375	Vdc
Emitter-Base Voltage	V_{EB}	6			Vdc
Collector Current — Continuous Peak	I_C	3 5			Adc
Base Current	I_B	1.5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.56			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	°C/W

*Indicates JEDEC Registered Data.

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$)	2N5838 2N5839 2N5840	$V_{CEO(sus)}$	250 275 350	– – –	Vdc
Collector-Emitter Sustaining Voltage ($I_C = 100$ mA, $V_{BE(off)} = 1.5$ V, L = 10 mH)	2N5838 2N5839 2N5840	$V_{CEX(sus)}$	275 300 375	– – –	Vdc
Collector-Emitter Sustaining Voltage ($I_C = 200$ mAdc, $R_{BE} = 50$ Ohms)	2N5838 2N5839 2N5840	$V_{CER(sus)}$	275 300 375	– – –	Vdc
Emitter-Base Breakdown Voltage ($I_E = 20$ mAdc, $I_C = 0$)		V_{EBO}	6	–	Vdc
Emitter Cutoff Current ($V_{CE} = 6$ Vdc, $I_C = 0$)		I_{EBO}	–	1	mAdc
Collector Cutoff Current ($V_{CE} = 200$ Vdc, $I_B = 0$) ($V_{CE} = 250$ Vdc, $I_B = 0$) ($V_{CE} = 250$ Vdc, $I_B = 0$)	 2N5838 2N5839 2N5840	I_{CEO}	 – – –	 2 2 2	mAdc
Collector Cutoff Current ($V_{CEV} = 265$ Vdc, $V_{BE(off)} = 1.5$ Vdc) ($V_{CEV} = 290$ Vdc, $V_{BE(off)} = 1.5$ Vdc) ($V_{CEV} = 360$ Vdc, $V_{BE(off)} = 1.5$ Vdc)	 2N5838 2N5839 2N5840	I_{CEV}	 – – –	 5 2 2	mAdc
Collector Cutoff Current ($V_{CEV} = 265$ Vdc, $V_{BE(off)} = 1.5$ Vdc, $T_C = 100^oC$) ($V_{CEV} = 290$ Vdc, $V_{BE(off)} = 1.5$ Vdc, $T_C = 100^oC$) ($V_{CEV} = 360$ Vdc, $V_{BE(off)} = 1.5$ Vdc, $T_C = 100^oC$)	 2N5838 2N5839 2N5840	I_{CEV}	 – – –	 8 5 5	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 0.5$ Adc, $V_{CE} = 5$ Vdc) ($I_C = 2$ Adc, $V_{CE} = 3$ Vdc) ($I_C = 3$ Adc, $V_{CE} = 2$ Vdc)	 ALL TYPES 2N5839, 40 2N5838	h_{FE}	 20 10 8	 – 50 40	–
Collector-Emitter Saturation Voltage ($I_C = 3$ Adc, $I_B = 0.375$ Adc) ($I_C = 2$ Adc, $I_B = 0.2$ Adc) ($I_C = 2$ Adc, $I_B = 0.2$ Adc)	 2N5838 2N5839 2N5840	$V_{CE(sat)}$	 – – –	 1.0 1.5 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 3$ Adc, $I_B = 0.375$ Adc) ($I_C = 2$ Adc, $I_B = 0.2$ Adc) ($I_C = 2$ Adc, $I_B = 0.2$ Adc)	 2N5838 2N5839 2N5840	$V_{BE(sat)}$	 – – –	 2 2 2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product ($I_C = 200$ mAdc, $V_{CE} = 10$ Vdc, $f_{test} = 1$ Mhz)		$\|h_{fe}\|$	5	–	MHz
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f_{test} = 1$ MHz)		C_{ob}	–	150	pF
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased t = 1.0 s (non-repetitive) ($V_{CE} = 40$ Vdc)		$I_{S/b}$	2.5	–	Adc
Second Breakdown Energy with Base Reverse Biased ($I_C = 3.0$, $V_{BE(off)} = 4.0$ Vdc, L = 100 μH)		$E_{S/b}$	0.45	–	mJ

SWITCHING CHARACTERISTICS, MAXIMUM LIMITS

Resistive Load		Symbol	2N5838(2)	2N5839	2N5840	Unit
Rise Time	($V_{CC} = 200$ Vdc, $I_C = 2$ Adc, $I_{B1} = I_{B2} = 0.2$ Adc, $t_p = 100$ μs, Duty Cycle ≤ 2%)	t_r	1.5	1.5	1.75	μs
Storage Time		t_s	3.0	3.75	3.0	μs
Fall Time		t_f	1.5	1.5	1.5	μs

(1) Pulse Test: Pulse Width = 100 μs, Duty Cycle = 2%.
(2) For 2N5838, $I_C = 3$ Adc, $I_{B1} = I_{B2} = 0.375$ Adc

FIGURE 1 – THERMAL RESPONSE

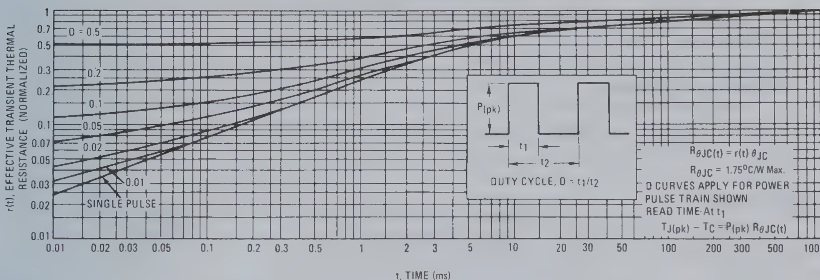
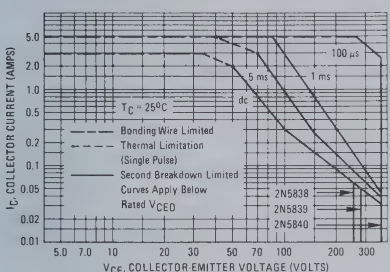


FIGURE 2 – SAFE OPERATING AREA

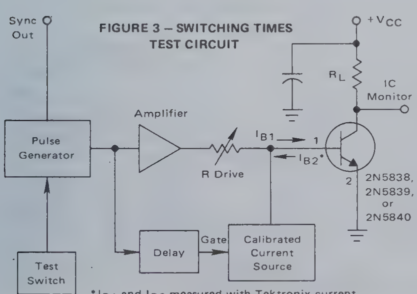


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 2 may be found at any case temperature by using the appropriate curve on Figure 4.

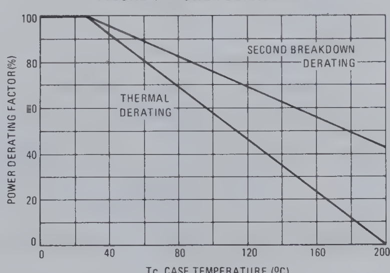
$T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 3 – SWITCHING TIMES TEST CIRCUIT



*I_{B1} and I_{B2} measured with Tektronix current probe P6019 or equivalent.

FIGURE 4 – POWER DERATING



2N5875, 2N5876 PNP
2N5877, 2N5878 NPN

MOTOROLA

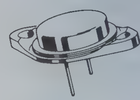
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . .designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 5.0 Adc
- Low Leakage Current — I_{CEX} = 0.5 mAdc (Max) @ Rated Voltage
- Excellent DC Current Gain — h_{FE} = 20 (Min) @ I_C = 4.0 Adc
- High Current Gain — Bandwidth Product — f_T = 4.0 MHz (Min) @ I_C = 0.5 A

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
150 WATTS



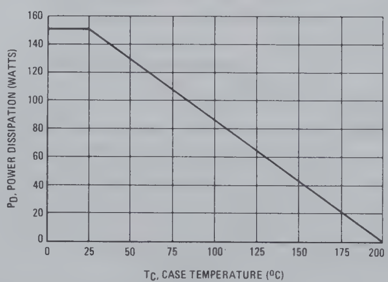
*MAXIMUM RATINGS

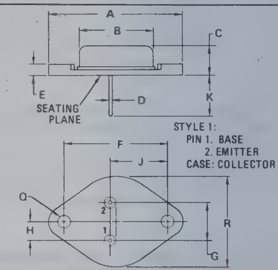
Rating	Symbol	2N5875 2N5877	2N5876 2N5878	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	10 20		Adc
Base Current	I_B	4.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 — POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-3

NOTE:
1. DIM "Q" IS DIA.

Collector connected to case.

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5875, 2N5877	$V_{CEO(sus)}$	60	–	Vdc
	2N5876, 2N5878		80	–	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	2N5875, 2N5877	I_{CEO}	–	1.0	mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N5876, 2N5878		–	1.0	
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5875, 2N5877	I_{CEX}	–	0.5	mAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5876, 2N5878		–	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150^oC$)	2N5875, 2N5877		–	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150^oC$)	2N5876, 2N5878		–	5.0	
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)	2N5875, 2N5877	I_{CBO}	–	0.5	mAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N5876, 2N5878		–	0.5	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_E = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	35	–	–
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
Collector-Emitter Saturation Voltage (1) (I_C = 5.0 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	–	1.0	Vdc
(I_C = 10 Adc, I_B = 2.5 Adc)			–	3.0	
Base-Emitter Saturation Voltage (1) (I_C = 10 Adc, I_B = 2.5 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2) (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5875, 2N5876	C_{ob}	–	500	pF
	2N5877, 2N5878		–	300	
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 4.0 Adc, $I_{B1} = I_{B2}$ = 0.4 Adc, See Figure 2)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

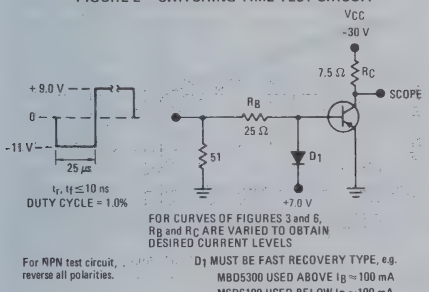


FIGURE 3 – TURN-ON TIME

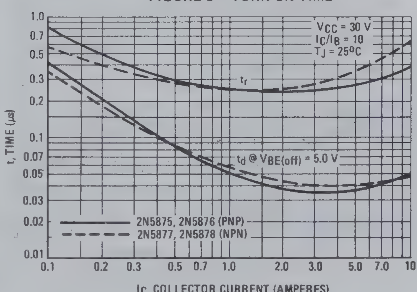


FIGURE 4 – THERMAL RESPONSE

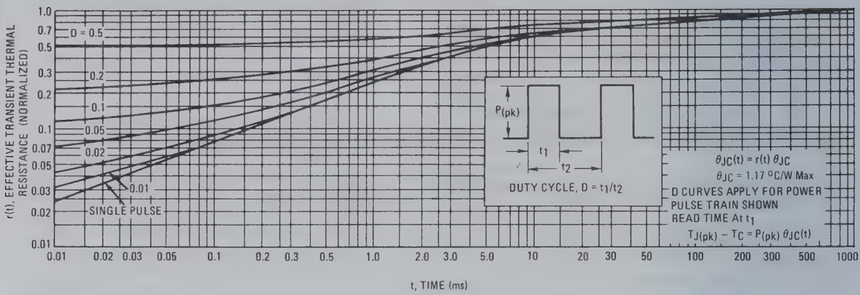
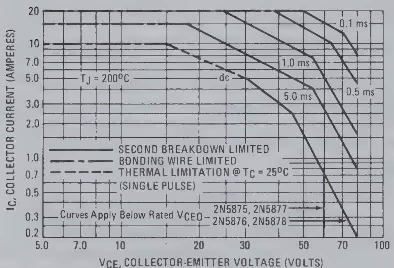


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

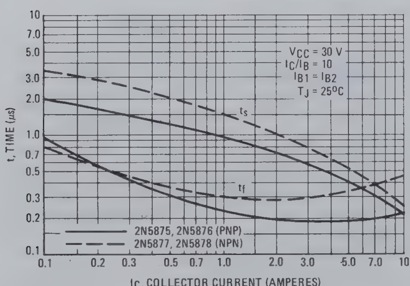
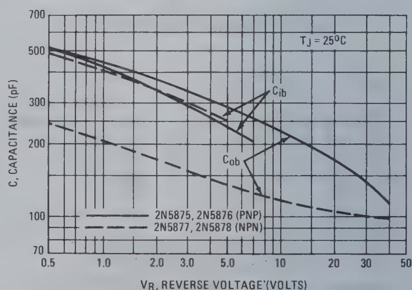


FIGURE 7 – CAPACITANCE



2N5879, 2N5880, PNP
2N5881, 2N5882 NPN

MOTOROLA

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for general-purpose power amplifier and switching applications.

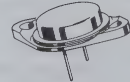
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N5879, 2N5881
  = 80 Vdc (Min) — 2N5880, 2N5882
- DC Current Gain —
  h_{FE} = 20 (Min) @ I_C = 6.0 Adc
- Low Collector — Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 7.0 Adc
- High Current — Gain-Bandwidth Product —
  f_T = 4.0 MHz (Min) @ I_C = 1.0 Adc
- Recommended for New Circuit Designs

15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60–80 VOLTS
160 WATTS

1.3



*MAXIMUM RATINGS

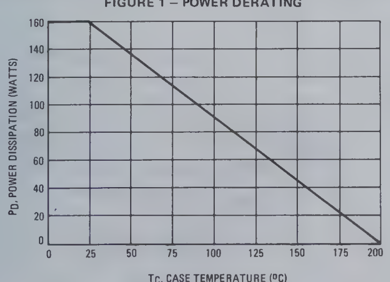
Rating	Symbol	2N5879 2N5881	2N5880 2N5882	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	15 30		Adc
Base Current	I_B	5.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	160 0.915		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

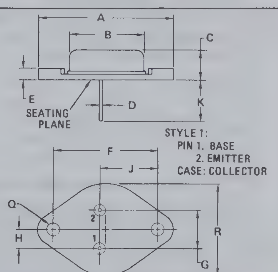
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.1	°C/W

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	-	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	–	1.050

CASE 11-01
TO-3

NOTE:
1. DIM "Q" IS DIA.

Collector connected to case.

1.3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5879, 2N5881 2N5880, 2N5882	$V_{CEO(sus)}$	60 80	– –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	2N5879, 2N5881 2N5880, 2N5882	I_{CEO}	– –	1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5879, 2N5881 2N5880, 2N5882 2N5879, 2N5881 2N5880, 2N5882	I_{CEX}	– – – –	0.5 0.5 5.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	2N5879, 2N5881 2N5880, 2N5882	I_{CBO}	– –	0.5 0.5	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	35 20 4.0	– 100 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 7.0 Adc, I_B = 0.7 Adc) (I_C = 15 Adc, I_B = 3.75 Adc)		$V_{CE(sat)}$	–	1.0 4.0	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 15 Adc, I_B = 3.75 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	2N5879, 2N5880 2N5881, 2N5882	C_{ob}	– –	600 400	pF
Small-Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 6.0 Adc, I_{B1} = I_{B2} = 0.6 Adc See Figure 2)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

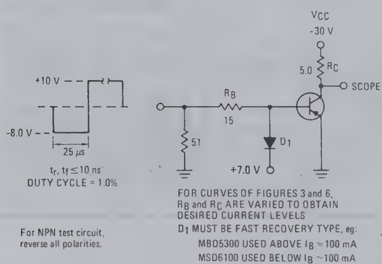


FIGURE 3 – TURN-ON TIME

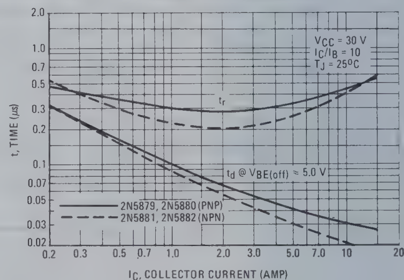


FIGURE 4 – THERMAL RESPONSE

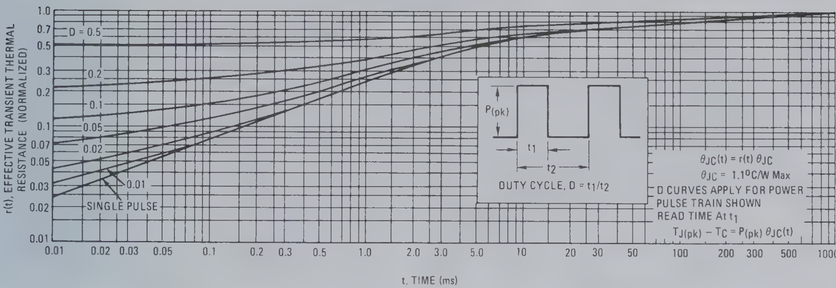
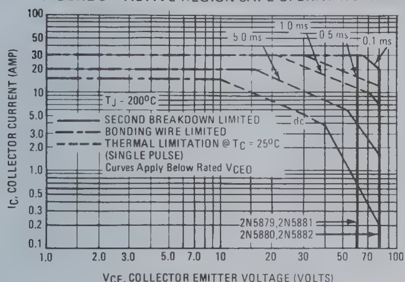


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

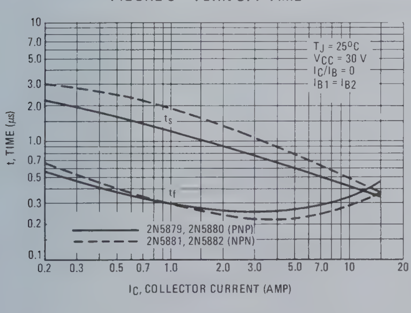
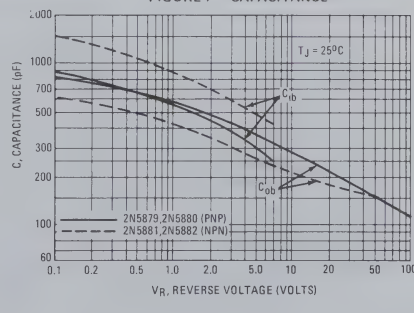


FIGURE 7 – CAPACITANCE



1.3

PNP 2N5879, 2N5880	NPN 2N5881, 2N5882

FIGURE 8 – DC CURRENT GAIN

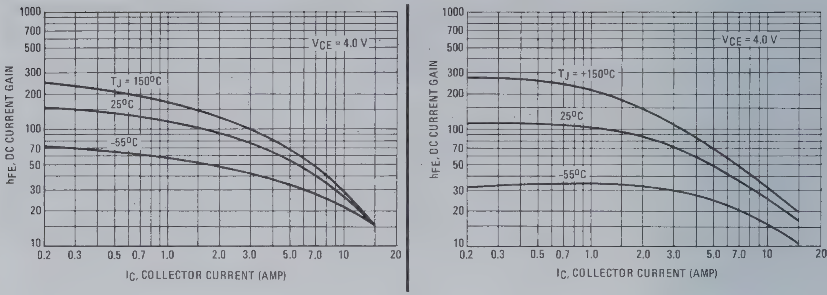


FIGURE 9 – COLLECTOR SATURATION REGION

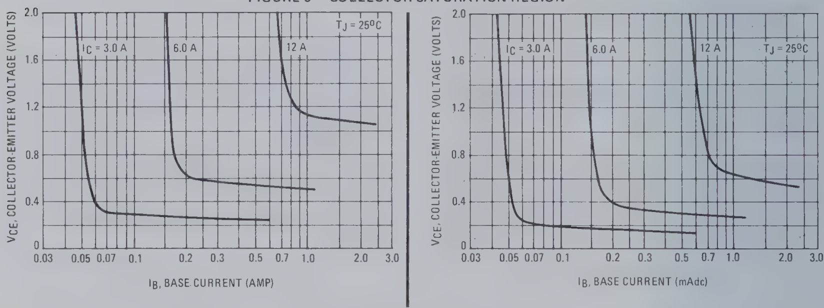
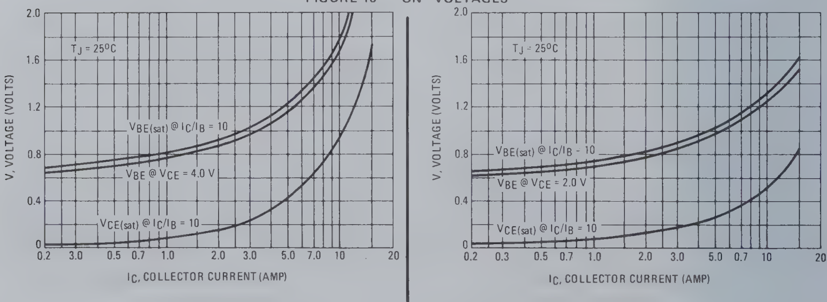


FIGURE 10 – "ON" VOLTAGES



2N5883, 2N5884 PNP
2N5885, 2N5886 NPN

MOTOROLA

1.3

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for general-purpose power amplifier and switching applications.

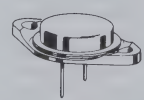
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc, (max) at I_C = 15 Adc
- Low Leakage Current
  I_{CEX} = 1.0 mAdc (max) at Rated Voltage
- Excellent DC Current Gain —
  h_{FE} = 20 (min) at I_C = 10 Adc
- High Current Gain Bandwidth Product —
  f_T = 4.0 MHz (min) at I_C = 1.0 Adc

25 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60–80 VOLTS

200 WATTS



*MAXIMUM RATINGS

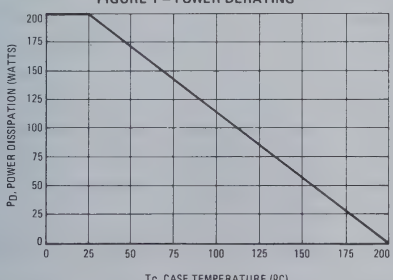
Rating	Symbol	2N5883 2N5885	2N5884 2N5886	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	25 50		Adc
Base Current	I_B	7.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.15		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

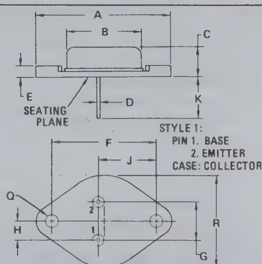
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

Collector connected to case.

CASE 11-01
TO-3

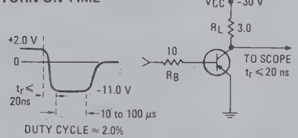
*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5883, 2N5885		60	–	
	2N5884, 2N5886		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5883, 2N5885		–	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5884, 2N5886			2.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5883, 2N5885		–	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5884, 2N5886		–	1.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5883, 2N5885		–	10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5884, 2N5886		–	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5883, 2N5885			1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5884, 2N5886		–	1.0	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0		I_{EBO}		1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			35		
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 25 Adc, V_{CE} = 4.0 Vdc)			4.0	-	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 1.5 Adc)			–	1.0	
(I_C = 25 Adc, I_B = 6.25 Adc)				4.0	
Base-Emitter Saturation Voltage (1) (I_C = 25 Adc, I_B = 6.25 Adc)		$V_{BE(sat)}$		2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5883, 2N5884			1000	
	2N5885, 2N5886			500	
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 kHz)		h_{fe}	20	-	-
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc,	t_r	-	0.7	μs
Storage Time	$I_{B1} = I_{B2}$ = 1.0 Adc)	t_s		1.0	μs
Fall Time		t_f		0.8	μs

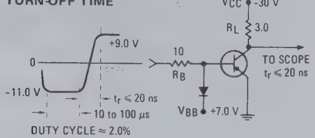
*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUITS

TURN-ON TIME



TURN-OFF TIME



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

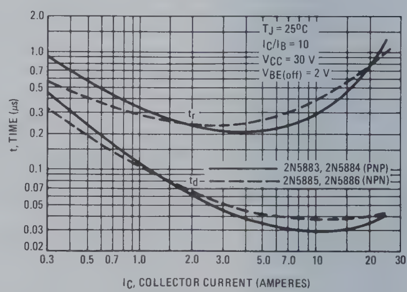


FIGURE 4 – THERMAL RESPONSE

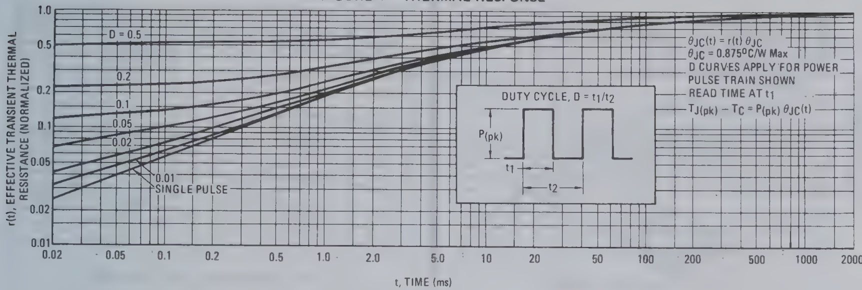
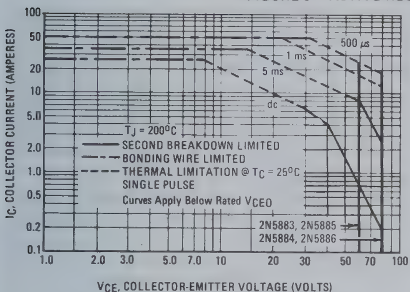


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

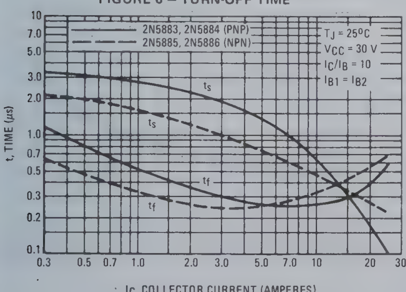
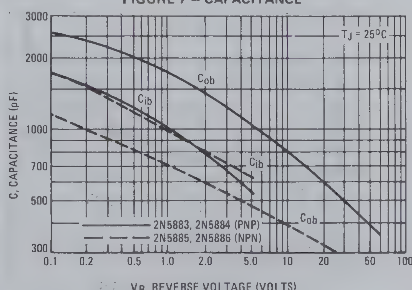


FIGURE 7 – CAPACITANCE



1.3

PNP DEVICES
2N5883 and 2N5884

NPN DEVICES
2N5885 and 2N5886

FIGURE 8 – DC CURRENT GAIN

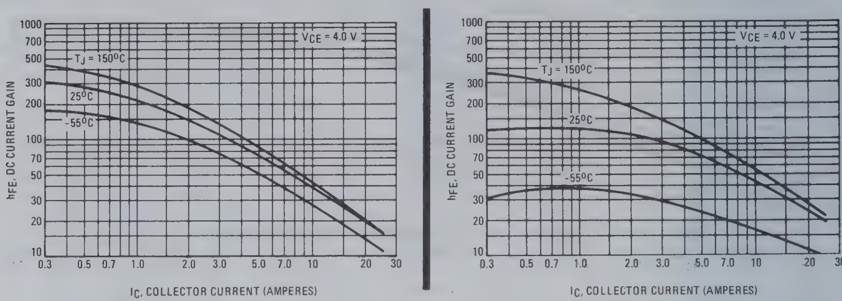


FIGURE 9 – COLLECTOR SATURATION REGION

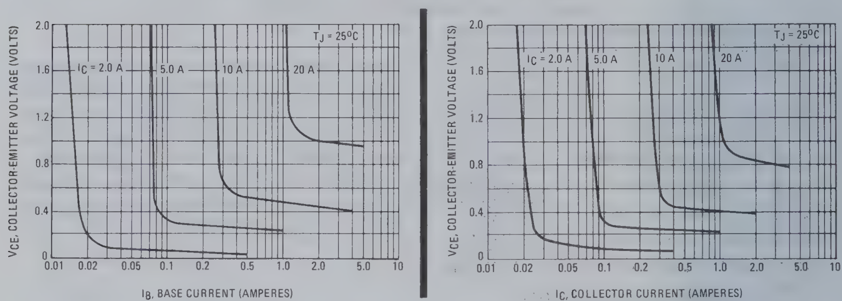
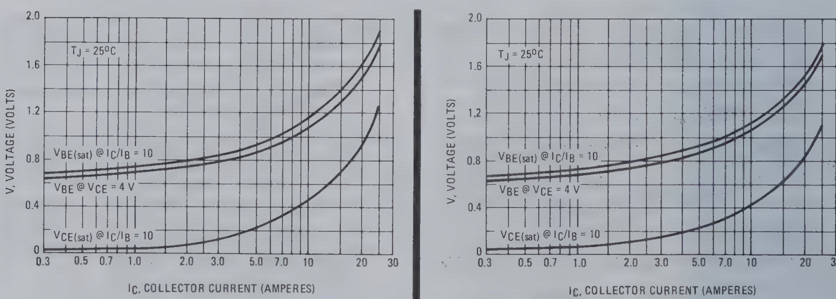


FIGURE 10 – "ON" VOLTAGES



2N5974, 2N5975, 2N5976

MOTOROLA

1.3

PNP SILICON PLASTIC POWER TRANSISTORS

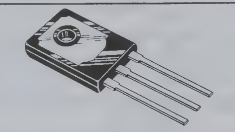
. . . designed for use in general purpose amplifier and switching applications.

- DC Current Gain Specified to 5 Amperes
  h_{FE} = 20-120 @ I_C = 2.5 Adc
  = 7.0 (Min) @ I_C = 5.0 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc (Min) — 2N5974
  = 60 Vdc (Min) — 2N5975
  = 80 Vdc (Min) — 2N5976
- High Current Gain — Bandwidth Product —
  f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Complements to NPN Transistors 2N5977, 2N5978, 2N5979

5 AMPERE POWER TRANSISTORS

PNP SILICON

40-60-80 VOLTS
75 WATTS



*MAXIMUM RATINGS

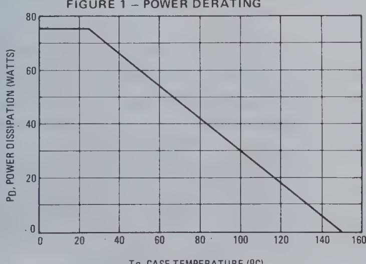
Rating	Symbol	2N5974	2N5975	2N5976	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current - Continuous Peak	I_C	← 5.0 → ← 10 →			Adc
Base Current	I_B	← 2.0 →			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 75 → ← 0.60 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +150 →			°C

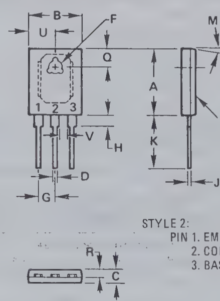
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W

*Indicates JEDEC Registered Data for 2N5974 Series.

FIGURE 1 – POWER DERATING





STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

1.3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	2N5974	$V_{CEO(sus)}$	40	–	Vdc
	2N5975		60	–	
	2N5976		80		
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	2N5974	I_{CEO}	–	1.0	mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5975		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5976		–	1.0	
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5974	I_{CEX}	–	100	μAdc
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5975		–	100	
(V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5976		–	100	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5974		–	1.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5975		–	1.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5976		–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	40	–	–
(I_C = 2.5 Adc, V_{CE} = 2.0 Vdc)			20	120	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)			7.0	–	
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 250 mAdc)		$V_{CE(sat)}$	–	0.6	Vdc
(I_C = 5.0 Adc, I_B = 750 mAdc)			–	1.7	
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 750 mAdc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (I_C = 2.5 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.4	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	2.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	300	pF
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

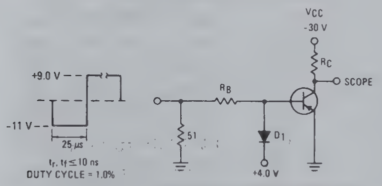


FIGURE 3 – TURN-ON TIME

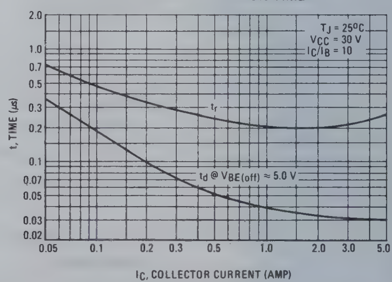


FIGURE 4 – THERMAL RESPONSE

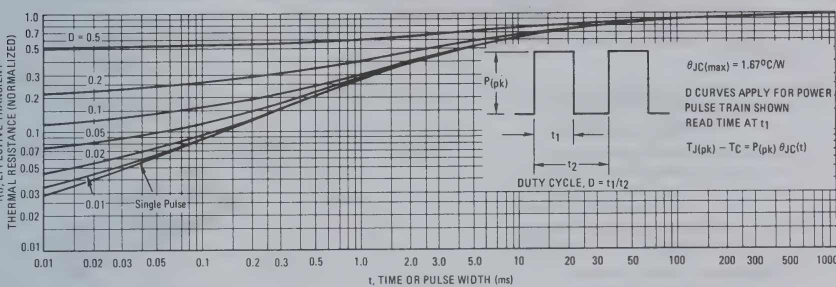
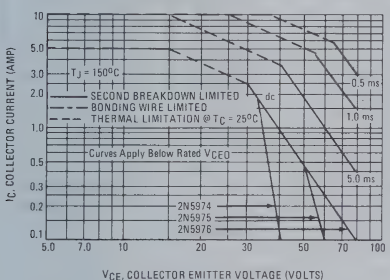


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

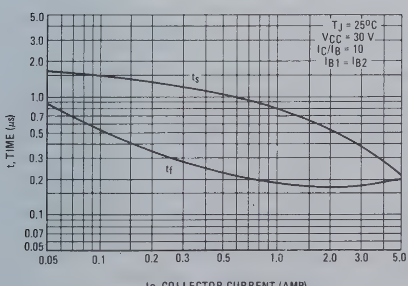
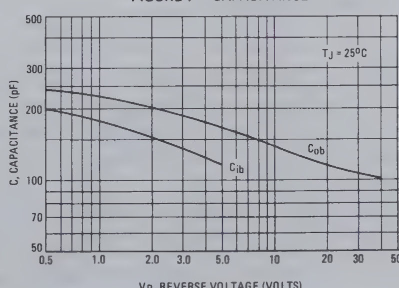


FIGURE 7 – CAPACITANCE



2N5977, 2N5978, 2N5979

MOTOROLA

1.3

NPN SILICON PLASTIC POWER TRANSISTORS

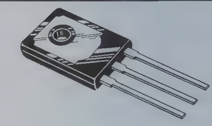
. . . designed for use in general purpose amplifier and switching applications.

- DC Current Gain Specified to 5 Amperes
  h_{FE} = 20-120 @ I_C = 2.5 Adc
  = 7.0 (Min) @ I_C = 5.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 40 Vdc (Min) – 2N5977
  = 60 Vdc (Min) – 2N5978
  = 80 Vdc (Min) – 2N5979
- High Current Gain – Bandwidth Product
  f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Complement to PNP Transistors –
  2N5974, 2N5975, 2N5976

5 AMPERE POWER TRANSISTORS

NPN SILICON

40-60-80 VOLTS
75 WATTS



*MAXIMUM RATINGS

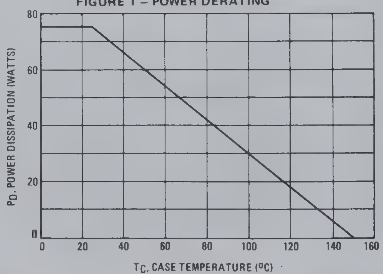
Rating	Symbol	2N5977	2N5978	2N5979	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	←	5.0	→	Vdc
Collector Current - Continuous Peak	I_C	← ←	5.0 10	→ →	Adc
Base Current	I_B	←	2.0	→	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		75 0.60		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	←	-65 to +150	→	°C

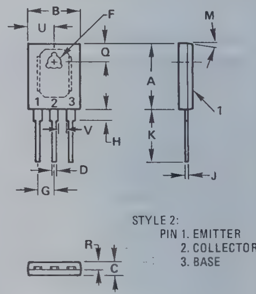
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING





STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1)	$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0) 2N5977		40	–	
2N5978		60	–	
2N5979		80		
Collector Cutoff Current	I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0) 2N5977		–	1.0	
(V_{CE} = 30 Vdc, I_B = 0) 2N5978		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0) 2N5979		–	1.0	
Collector Cutoff Current	I_{CEX}			
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) 2N5977		–	100	μAdc
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) 2N5978		–	100	
(V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc) 2N5979		–	100	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) 2N5977		–	1.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) 2N5978		–	1.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) 2N5979		–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)		40	–	
(I_C = 2.5 Adc, V_{CE} = 2.0 Vdc)		20	120	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)		7.0	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 2.5 Adc, I_B = 250 mAdc)		–	0.6	
(I_C = 5.0 Adc, I_B = 750 mAdc)		–	1.7	
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 750 mAdc)	$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (I_C = 2.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.4	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	2.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	200	pF
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	20	–	–

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

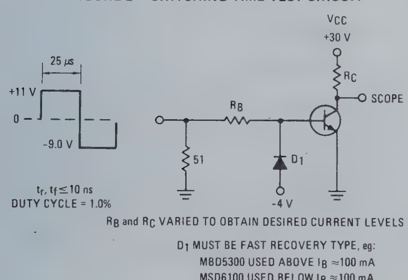


FIGURE 3 — TURN-ON TIME

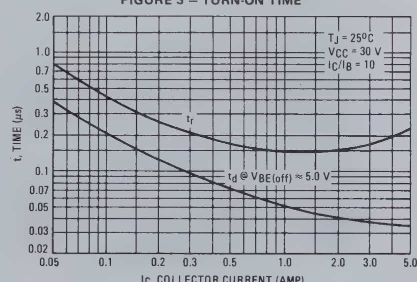


FIGURE 4 – THERMAL RESPONSE

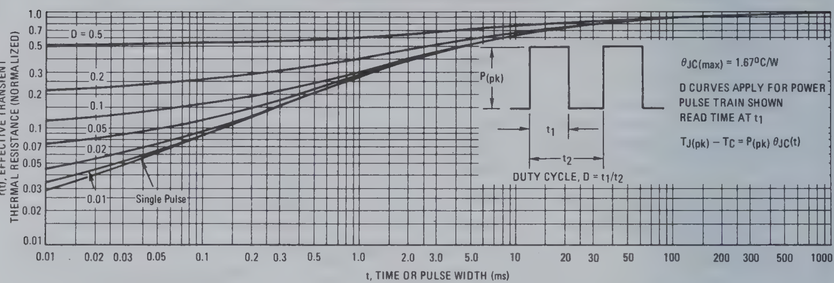
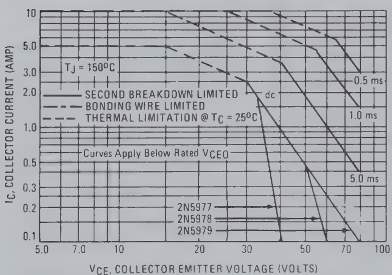


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

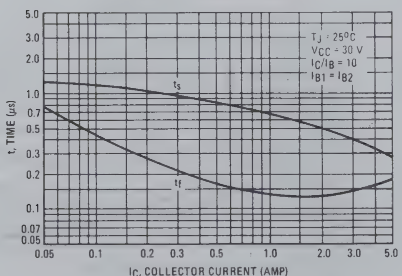
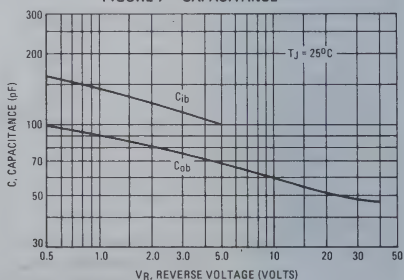


FIGURE 7 – CAPACITANCE



MOTOROLA

2N5986, 2N5987, 2N5988 PNP
2N5989, 2N5990, 2N5991 NPN

HIGH POWER PLASTIC COMPLEMENTARY SILICON POWER TRANSISTORS

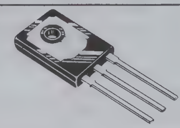
. . . designed for use in general-purpose amplifier and switching circuits.

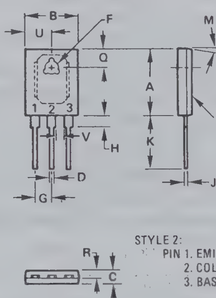
- Collector-Base Voltage — V_{CBO} = 60 Vdc — 2N5986, 2N5989
  = 80 Vdc — 2N5987, 2N5990
  = 100 Vdc — 2N5988, 2N5991
- Collector-Emitter Voltage — V_{CEO} = 40 Vdc — 2N5986, 2N5989
  = 60 Vdc — 2N5987, 2N5990
  = 80 Vdc — 2N5988, 2N5991
- DC Current Gain —
  h_{FE} = 20-120 @ I_C = 6.0 Adc
  = 7.0 (Min) @ I_C = 12 Adc
- Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 6.0 Adc

12 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

40, 60, 80 VOLTS
100 WATTS





STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

*MAXIMUM RATINGS

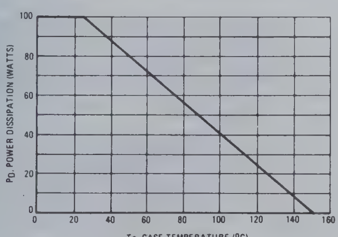
Rating	Symbol	2N5986 2N5989	2N5987 2N5990	2N5988 2N5991	Unit
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	12 20			Adc
Base Current	I_B	4.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.25	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING



1.3

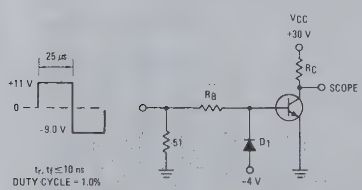
***ELECTRICAL CHARACTERISTICS** ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 0.2 Adc, I_B = 0)	2N5986, 2N5989	$BV_{CEO(sus)}$	40	–	Vdc
	2N5987, 2N5990		60	–	
	2N5988, 2N5991		80	–	
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	2N5986, 2N5989	I_{CEO}	–	2.0	mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5987, 2N5990		–	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5988, 2N5991		–	2.0	
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5986, 2N5989	I_{CEX}	–	200	µAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5987, 2N5990		–	200	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5988, 2N5991		–	200	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 125^oC$)	2N5986, 2N5989		–	2.0	mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 125^oC$)	2N5987, 2N5990		–	2.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 125^oC$)	2N5988, 2N5991		–	2.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	40	–	–
(I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)			20	120	
(I_C = 12 Adc, V_{CE} = 2.0 Vdc)			7.0	–	
Collector-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 0.6 Adc)		$V_{CE(sat)}$	–	0.6	Vdc
(I_C = 12 Adc, I_B = 1.8 Adc)			–	1.7	
Base-Emitter Saturation Voltage (I_C = 12 Adc, I_B = 1.8 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.4	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	2.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5986 thru 2N5988	C_{ob}	–	500	pF
	2N5989 thru 2N5991		–	300	
Small-Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–

*Indicates JEDEC Registered Data.

(1) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE IB ≈100 mA
MSD6100 USED BELOW IB ≈100 mA

For PNP test circuit reverse diode and voltage polarities.

FIGURE 3 – TURN-ON TIME

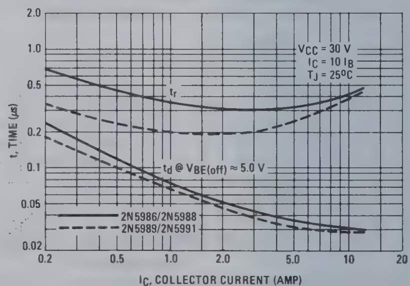


FIGURE 4 — THERMAL RESPONSE

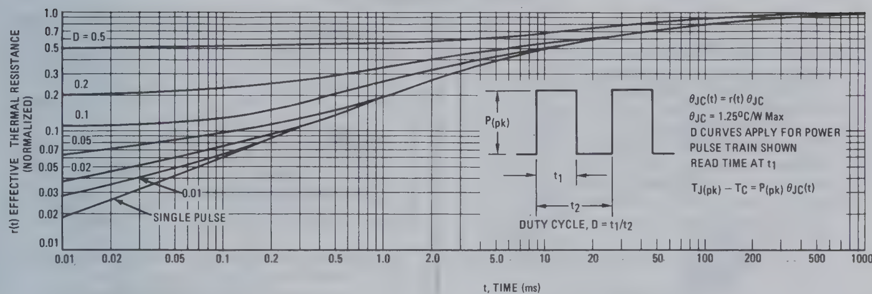
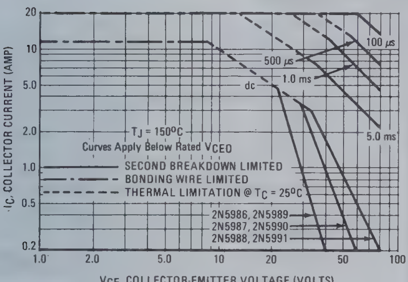


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$ $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — TURN-OFF TIME

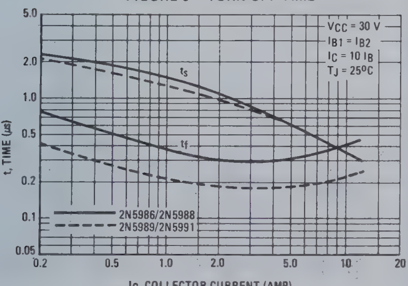
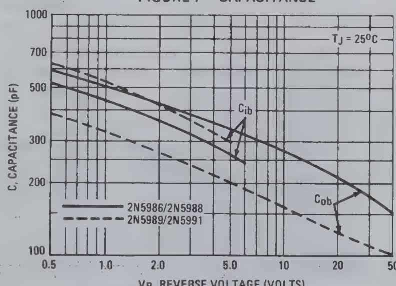


FIGURE 7 — CAPACITANCE



PNP 2N5986 thru 2N5988	NPN 2N5989 thru 2N5991

FIGURE 8 — DC CURRENT GAIN

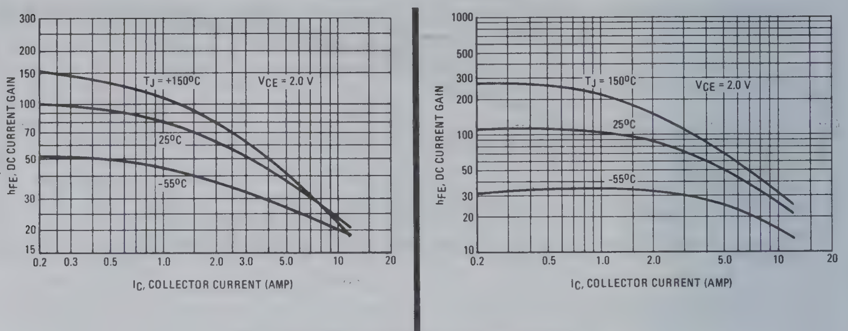


FIGURE 9 — COLLECTOR SATURATION REGION

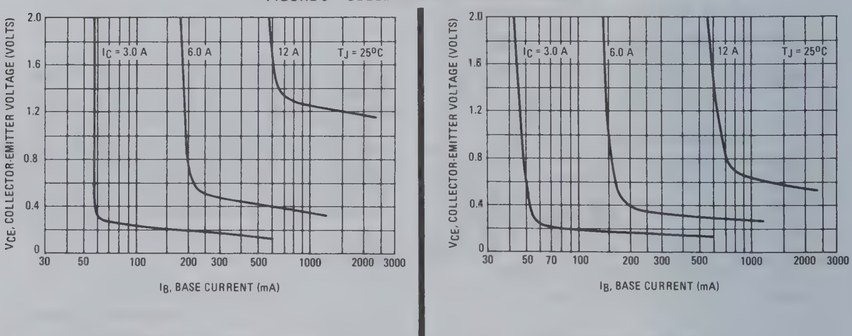
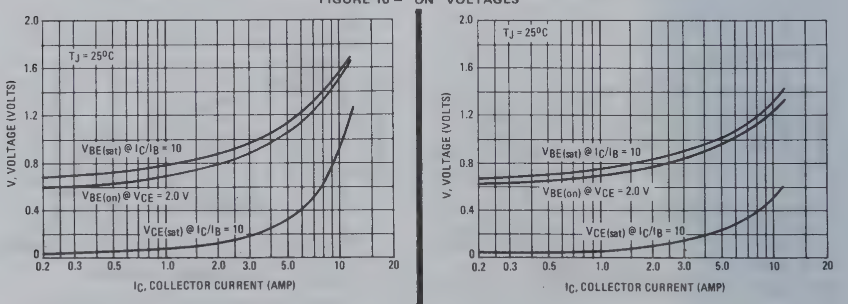


FIGURE 10 — "ON" VOLTAGES



2N6034, 2N6035, 2N6036 PNP
2N6037, 2N6038, 2N6039 NPN

PLASTIC DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

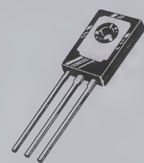
. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain — h_{FE} = 2000 (Typ) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 40 Vdc (Min) — 2N6034, 2N6037
  = 60 Vdc (Min) — 2N6035, 2N6038
  = 80 Vdc (Min) — 2N6036, 2N6039
- Forward Biased Second Breakdown Current Capability
  $I_{S/b}$ = 1.5 Adc @ 25 Vdc
- Monolithic Construction with Built-In Base-Emitter Resistors to Limit Leakage Multiplication
- Space-Saving High Performance-to-Cost Ratio TO-126 Plastic Package

DARLINGTON
4-AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40, 60, 80 VOLTS
40 WATTS



*MAXIMUM RATINGS

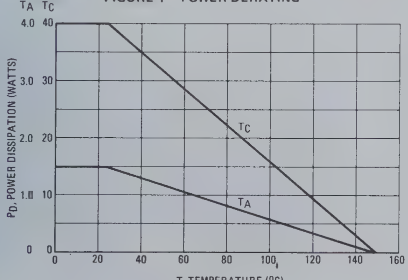
Rating	Symbol	2N6034 2N6037	2N6035 2N6038	2N6036 2N6039	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous	I_C		4.0		Adc
Peak			8.0		
Base Current	I_B		100		mAdc
Total Power Dissipation @ $T_C = 25^oC$	P_D		40		Watts
Derate above 25^oC			0.32		$W/^oC$
Total Power Dissipation @ $T_A = 25^oC$	P_D		1.5		Watts
Derate above 25^oC			0.012		$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150		^oC

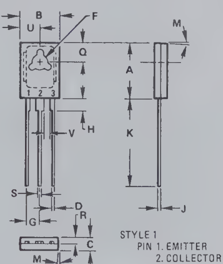
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	$^oC/W$
Thermal Resistance, Junction to Ambient	θ_{JA}	83.3	$^oC/W$

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. TO DIM. "A" & "B" AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3^o TYP		3^o TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

1.3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6034, 2N6037		40	–	
	2N6035, 2N6038		60	–	
	2N6036, 2N6039		80	–	
Collector-Cutoff Current		I_{CEO}			μA
(V_{CE} = 40 Vdc, I_B = 0)	2N6034, 2N6037		–	100	
(V_{CE} = 60 Vdc, I_B = 0)	2N6035, 2N6038		–	100	
(V_{CE} = 80 Vdc, I_B = 0)	2N6036, 2N6039		–	100	
Collector Cutoff Current		I_{CEX}			μA
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6034, 2N6037		–	100	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6035, 2N6038		–	100	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6036, 2N6039		–	100	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C)	2N6034, 2N6037		-	500	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C)	2N6035, 2N6038		–	500	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C)	2N6036, 2N6039		–	500	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N6034, 2N6037		–	0.5	
(V_{CB} = 60 Vdc, I_E = 0)	2N6035, 2N6038		–	0.5	
(V_{CB} = 80 Vdc, I_E = 0)	2N6036, 2N6039		–	0.5	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 3.0 Vdc)			500	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			750	15,000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 8.0 mAdc)			–	2.0	
(I_C = 4.0 Adc, I_B = 40 mAdc)			–	3.0	
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current-Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		$\lvert h_{fe} \rvert$	25	–	–
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E =0, f = 0.1 MHz)	2N6034, 2N6035, 2N6036		–	200	
	2N6037, 2N6038, 2N6039		–	100	

*Indicates JEDEC Registered Data.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

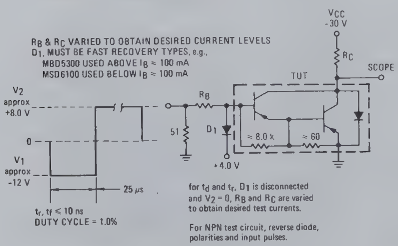


FIGURE 3 – SWITCHING TIMES

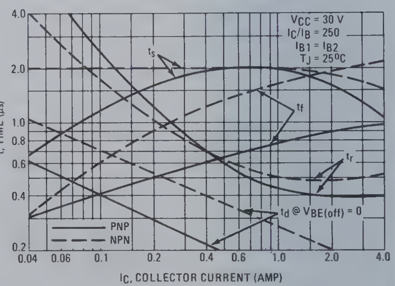
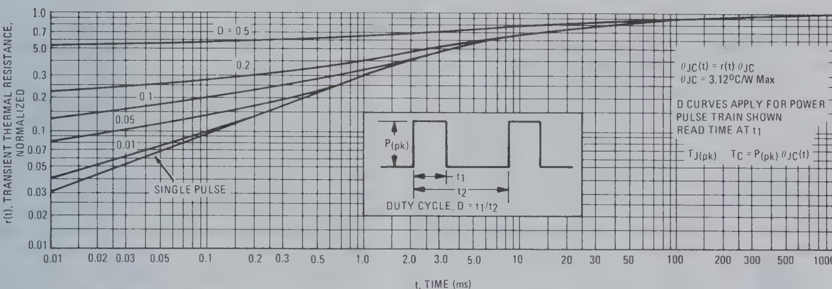


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 5 – 2N6034, 2N6035, 2N6036

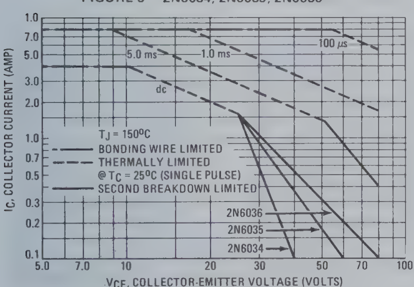
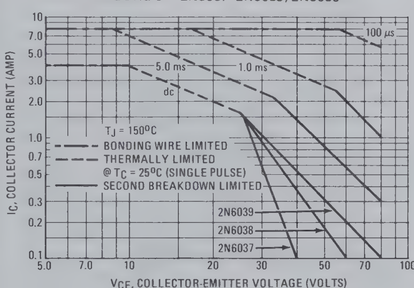


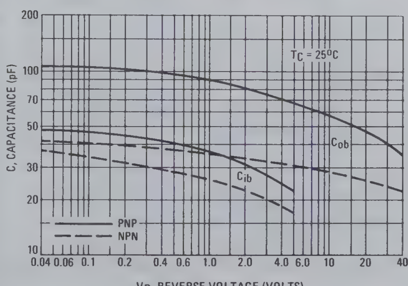
FIGURE 6 – 2N6037 2N6038, 2N6039



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 – CAPACITANCE



1.3

PNP 2N6034, 2N6035, 2N6036 | **NPN** 2N6037, 2N6038, 2N6039

FIGURE 8 – DC CURRENT GAIN

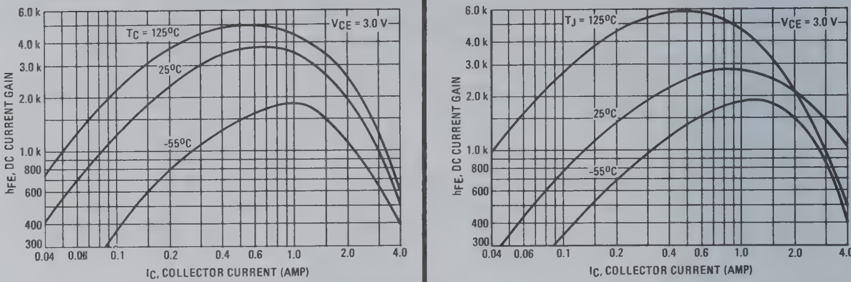


FIGURE 9 – COLLECTOR SATURATION REGION

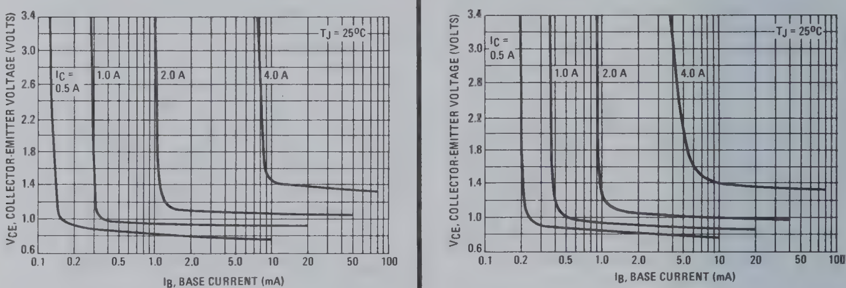
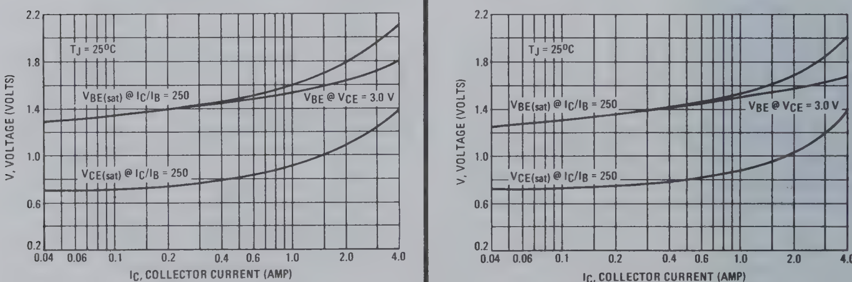


FIGURE 10 – "ON" VOLTAGES



2N6040 thru 2N6042 PNP
2N6043 thru 2N6045 NPN
MJE6040 thru MJE6042 PNP
MJE6043 thru MJE6045 NPN

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mAdc (1)
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6040, 2N6043
  = 80 Vdc (Min) — 2N6041, 2N6044
  = 100 Vdc (Min) — 2N6042, 2N6045
- Low Collector-Emitter Saturation Voltage — (1)
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc — 2N6040,41,2N6043,44
  = 2.0 Vdc (Max) @ I_C = 3.0 Adc — 2N6042, 2N6045
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

(1) Applies to corresponding in-house part numbers also.

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
75 WATTS

*MAXIMUM RATINGS

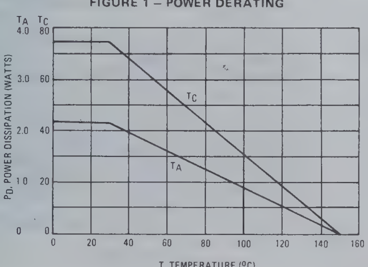
Rating	Symbol	2N6040 2N6043 MJE6040 MJE6043	2N6041 2N6044 MJE6041 MJE6044	2N6042 2N6045 MJE6042 MJE6045	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 8.0 → ← 16 →			Adc
Base Current	I_B	← 120 →			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 75 → ← 0.60 →			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.2 → ← 0.0175 →			Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

THERMAL CHARACTERISTICS

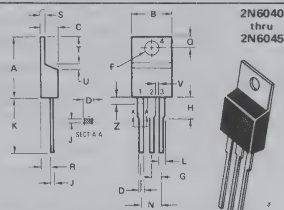
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	57	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING



2N6040 thru 2N6045



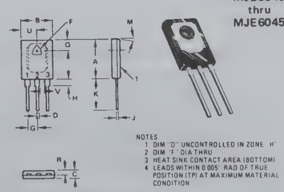
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3
3 DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M 1982
5 CONTROLLING DIMENSION INCH

CASE 221A-02
TO-220AB

MJE6040 thru MJE6045



NOTES
1 DIM "D" UNCONTROLLED IN ZONE "H"
2 DIM "F" DIA THRU
3 HEAT SINK CONTACT AREA (BOTTOM)
4 LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION

STYLE 2
PIN 1. EMITTER
2 COLLECTOR
3 BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	-	0.080	-

CASE 90-05
TO 127

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	2N6040, 2N6043, MJE6040, MJE6043	$V_{CEO(sus)}$	60	–	Vdc
	2N6041, 2N6044, MJE6041, MJE6044		80	–	
	2N6042, 2N6045, MJE6042, MJE6045		100	–	
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	2N6040, 2N6043, MJE6040, MJE6043	I_{CEO}	–	20	μA
(V_{CE} = 80 Vdc, I_B = 0)	2N6041, 2N6044, MJE6041, MJE6044		–	20	
(V_{CE} = 100 Vdc, I_B = 0)	2N6042, 2N6045, MJE6042, MJE6045		–	20	
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6040, 2N6043, MJE6040, MJE6043	I_{CEX}	–	20	μA
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6041, 2N6044, MJE6041, MJE6044		–	20	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6042, 2N6045, MJE6042, MJE6045		–	20	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6040, 2N6043, MJE6040, MJE6043		–	200	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6041, 2N6044, MJE6041, MJE6044		–	200	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6042, 2N6045, MJE6042, MJE6045		–	200	
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)	2N6040, 2N6043, MJE6040, MJE6043	I_{CBO}	–	20	μA
(V_{CB} = 80 Vdc, I_E = 0)	2N6041, 2N6044, MJE6041, MJE6044		–	20	
(V_{CB} = 100 Vdc, I_E = 0)	2N6042, 2N6045, MJE6042, MJE6045		–	20	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	2N6040,41, 2N6043,44, MJE6040,41, MJE6043,44	h_{FE}	1000	20,000	–
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N6042, 2N6045, MJE6042, MJE6045		1000	20,000	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	All Types		100		
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 16 mAdc)	2N6040,41,2N6043,44,MJE6040,41,MJE6043,44	$V_{CE(sat)}$	–	2.0	Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)	2N6042,2N6045,MJE6042,MJE6045		–	2.0	
(I_C = 8.0 Adc, I_B = 80 mAdc)	All Types		–	4.0	
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 80 mAdc)		$V_{BE(sat)}$	–	4.5	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6040/2N6042, MJE6040/MJE6042	C_{ob}	–	300	pF
	2N6043/2N6045, MJE6043/MJE6045		–	200	
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

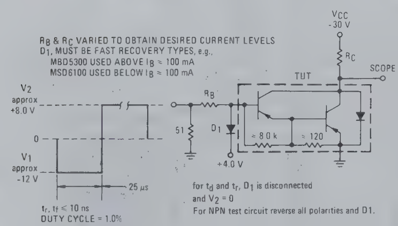


FIGURE 3 – SWITCHING TIMES

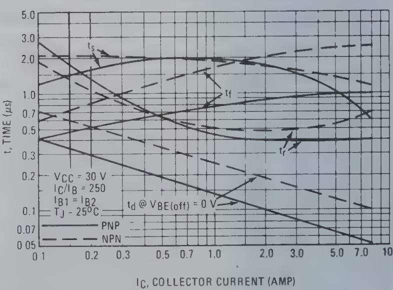


FIGURE 4 — THERMAL RESPONSE

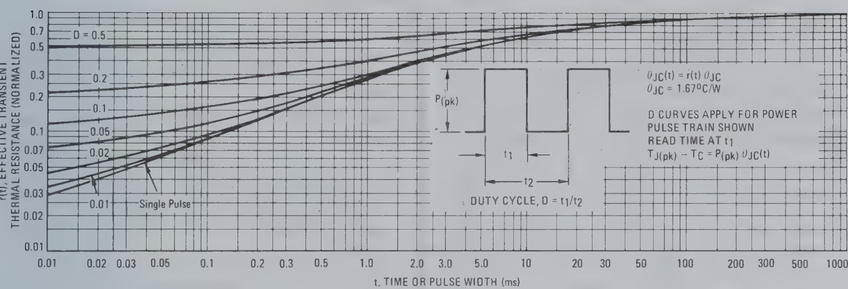
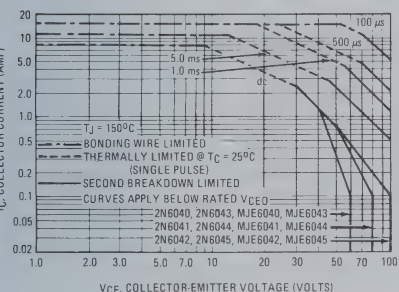


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — SMALL-SIGNAL CURRENT GAIN

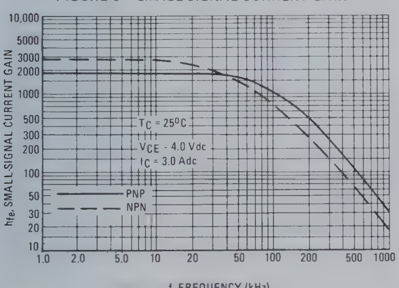
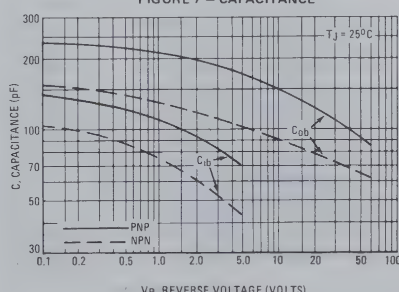


FIGURE 7 — CAPACITANCE



PNP
2N6040, 2N6041, 2N6042
MJE6040, MJE6041, MJE6042

NPN
2N6043, 2N6044, 2N6045
MJE6043, MJE6044, MJE6045

FIGURE 8 – DC CURRENT GAIN

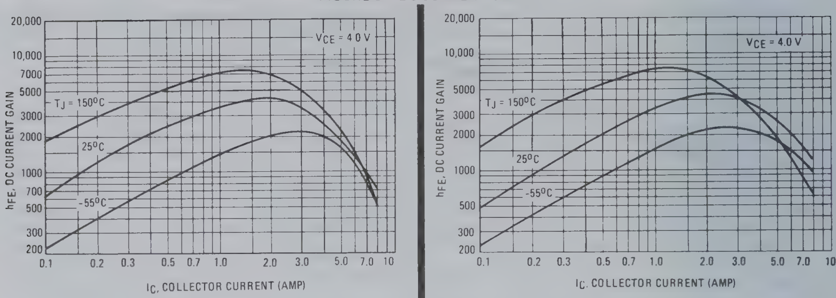


FIGURE 9 – COLLECTOR SATURATION REGION

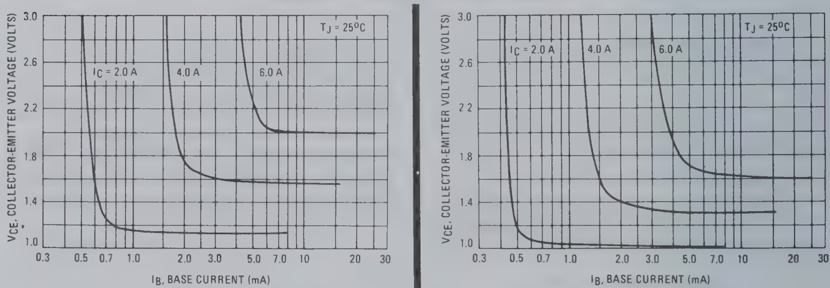
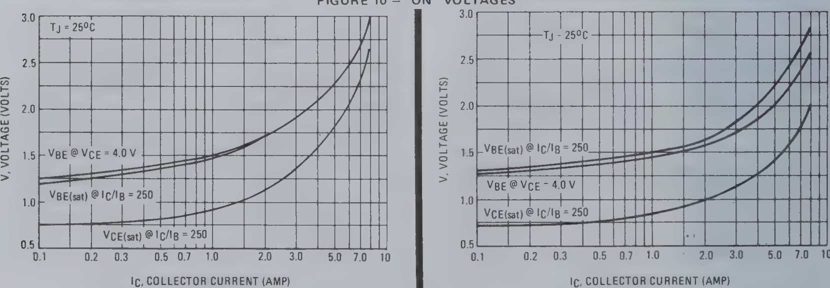


FIGURE 10 – "ON" VOLTAGES



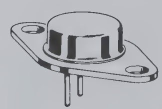
MOTOROLA

MEDIUM-POWER PNP SILICON TRANSISTOR

. . . designed for general-purpose switching and amplifier applications

- Excellent Safe Operating Area
- DC Current Gain Specified to 4.0 Amperes
- Complement to NPN Type 2N3054A

4 AMPERE
POWER TRANSISTOR
PNP SILICON
55 VOLTS
75 WATTS



*MAXIMUM RATINGS

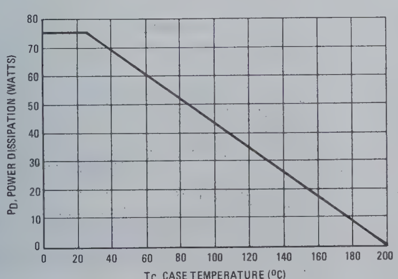
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	55	Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	60	Vdc
Collector-Base Voltage	V_{CB}	90	Vdc
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak	I_C	4.0 10	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°	P_D	75 0.43	Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200	°C

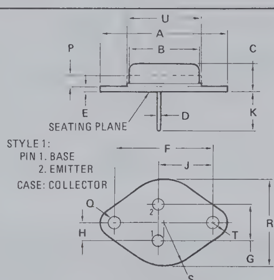
*Indicates JEDEC Registered Data

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.33	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.
CASE 80-02
TO-66

1.3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	55	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, R_{BE} = 100 Ω)	$V_{CER(sus)}$	60	–	Vdc
Collector Cuttoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	500	µAdc
Collector Cutoff Current (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 6.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 500 mAdc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	25 6.0	100	– –
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 4.0 Adc, I_B = 800 mAdc)	$V_{CE(sat)}$	– –	0.5 2.0	Vdc
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc)	f_T	3.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	200	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	25	180	

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUIT

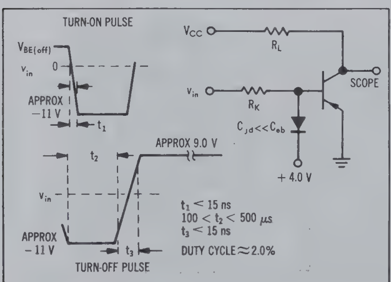


FIGURE 3 – TURN-ON TIME

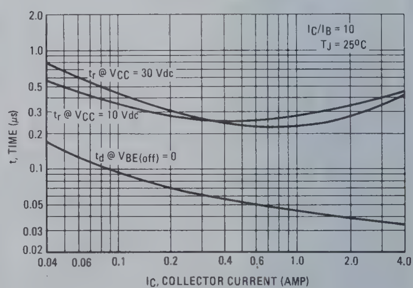


FIGURE 4 – THERMAL RESPONSE

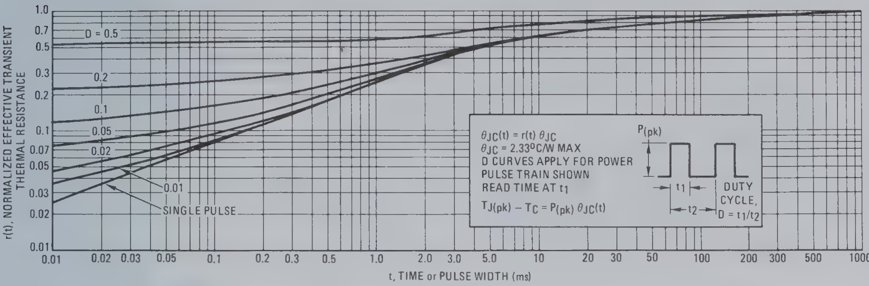
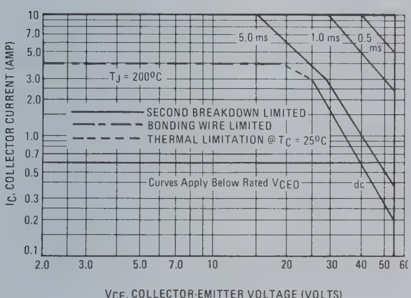


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

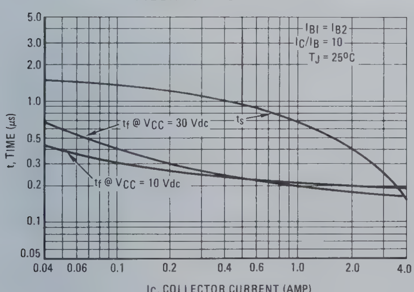
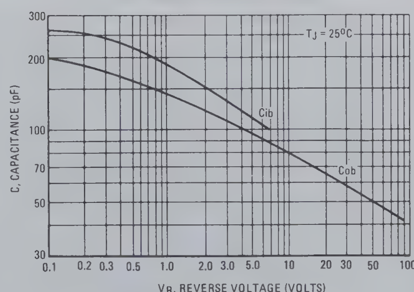


FIGURE 7 – CAPACITANCE



2N6050 thru 2N6052 PNP
2N6057 thru 2N6059 NPN

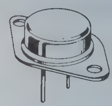
MOTOROLA

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain —
  h_{FE} = 3500 (Typ) @ I_C = 5.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6050, 2N6057
  80 Vdc (Min) — 2N6051, 2N6058
  100 Vdc (Min) — 2N6052, 2N6059
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON
12 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
150 WATTS



*MAXIMUM RATINGS

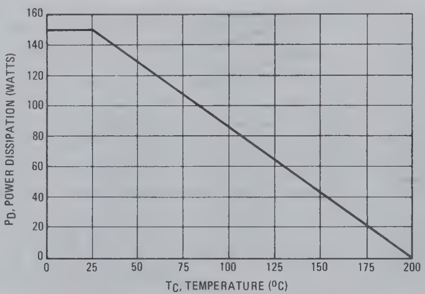
Rating	Symbol	2N6050 2N6057	2N6051 2N6058	2N6052 2N6059	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 12 → ← 20 →			Adc
Base Current	I_B	← 0.2 →			Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C	P_D	← 150 → ← 0.857 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200°C →			°C

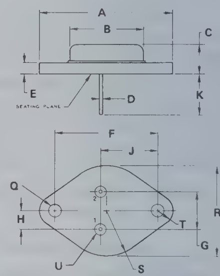
THERMAL CHARACTERISTICS

Characteristic	Symbol	Rating	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1–04

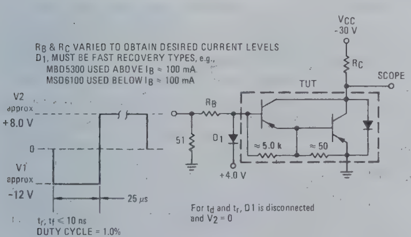
NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	2N6050, 2N6057 2N6051, 2N6058 2N6052, 2N6059	$V_{CEO(sus)}$	60 80 100	– – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	2N6050, 2N6057 2N6051, 2N6058 2N6052, 2N6059	I_{CEO}	– – –	1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	–	0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 12 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	750 100	18,000 –	–
Collector-Emitter Saturation Volatage (I_C = 6.0 Adc, I_B = 24 mAdc) (I_C = 12 Adc, I_B = 120 mAdc)		$V_{CE(sat)}$	– –	2.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 12 Adc, I_B = 120 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\lvert h_{fe}\rvert$	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6050/2N6052 2N6057/2N6059	C_{ob}	– –	500 300	pF
Small-Signal Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data
(1)Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 – SWITCHING TIMES

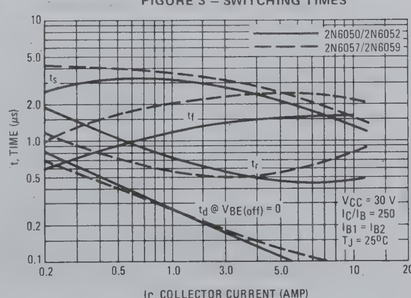
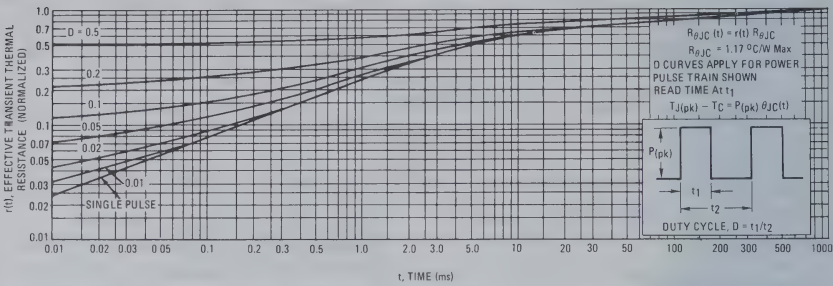


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6050, 2N6057

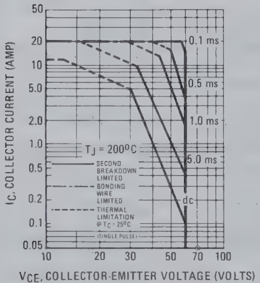


FIGURE 6 – 2N6051, 2N6058

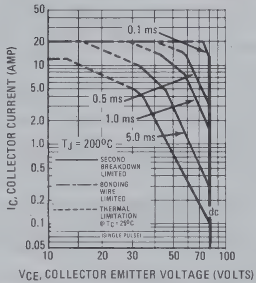
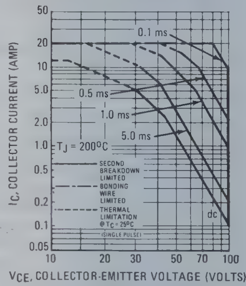


FIGURE 7 – 2N6052, 2N6059



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6 and 7 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200°C$ $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 – SMALL-SIGNAL CURRENT GAIN

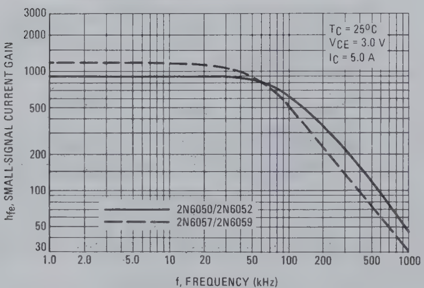
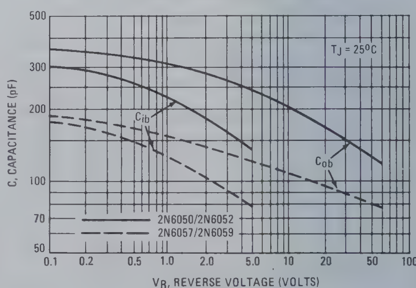


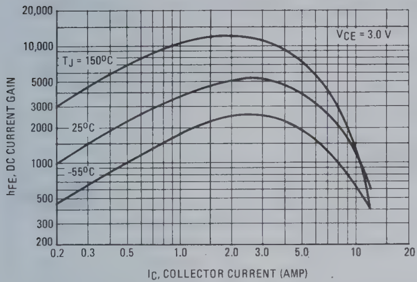
FIGURE 9 – CAPACITANCE



PNP
2N6050, 2N6051, 2N6052

NPN
2N6057, 2N6058, 2N6059

FIGURE 10 – DC CURRENT GAIN



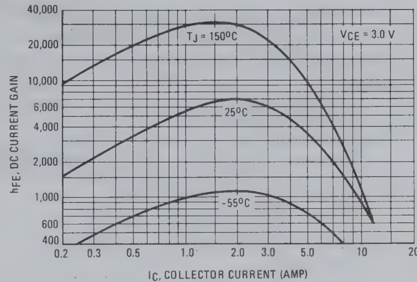
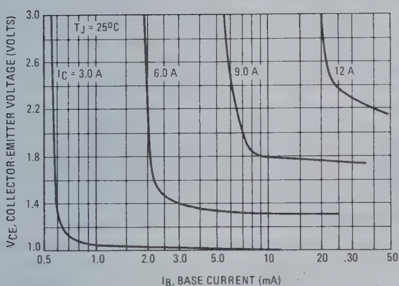


FIGURE 11 – COLLECTOR SATURATION REGION



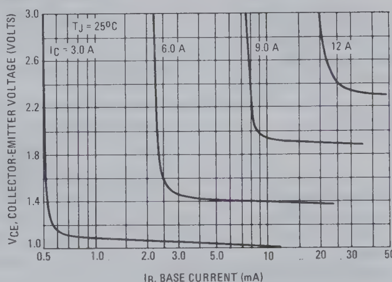
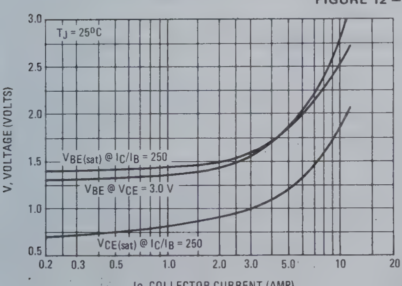
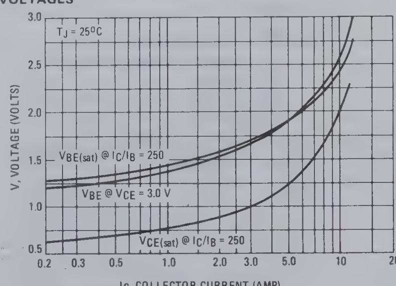


FIGURE 12 – "ON" VOLTAGES





2N6053, 2N6054, 2N6298, 2N6299 PNP
2N6055, 2N6056, 2N6300, 2N6301 NPN

MOTOROLA

1.3

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain —
  h_{FE} = 3000 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6053, 2N6055, 2N6298, 2N6300
  = 80 Vdc (Min) — 2N6054, 2N6056, 2N6299, 2N6301
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc
  = 3.0 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

*MAXIMUM RATINGS

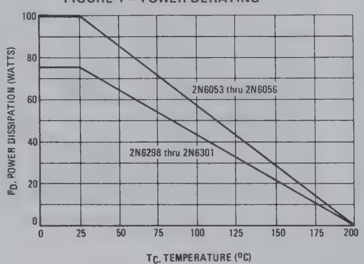
Rating	Symbol	2N6053 2N6055 2N6298 2N6300	2N6054 2N6056 2N6299 2N6301	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	8.0 16		Adc
Base Current	I_B	120		mAdc
		2N6053 2N6054 2N6055 2N6056	2N6298 2N6299 2N6300 2N6301	
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	100 0.571	75 0.428	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N6053 2N6054 2N6055 2N6056	2N6298 2N6299 2N6300 2N6301	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	2.33	$^oC/W$

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING

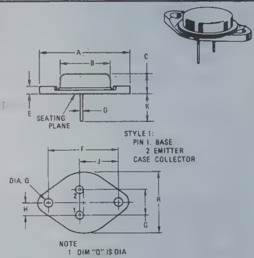


DARLINGTON 8 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
75,100 WATTS

2N6053
2N6054
2N6055
2N6056

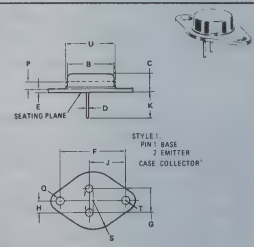


NOTE
1. DIM "Q" IS DIA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37	-	1.550
B		21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E		3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	–	1.050

Collector connected to case
CASE 11-01
(TO-3)

2N6298
2N6299
2N6300
2N6301



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S		8.89	–	0.350
T		3.68	–	0.145
U		15.75	-	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

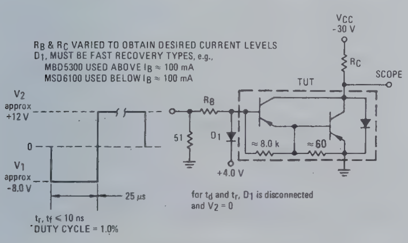
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6053, 2N6055, 2N6298, 2N6300		60	–	
	2N6054, 2N6056, 2N6299, 2N6301		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N6053, 2N6055, 2N6298, 2N6300		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	2N6054, 2N6056, 2N6299, 2N6301		–	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)			–	0.5	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	5.0	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)			–	2.0	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			750	18000	
(I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 16 mAdc)			–	2.0	
(I_C = 8.0 Adc, I_B = 80 mAdc)			–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 8.0 Adc, I_B = 80 mAdc)			–	4.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			–	2.8	
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short Circuit Current Transfer Ratio		$\|h_{fe}\|$			–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)			4.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6053, 2N6054, 2N6298, 2N6299		–	300	
	2N6055, 2N6056, 2N6300, 2N6301		–	200	
Small-Signal Current Gain		h_{fe}			–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)			300	–	

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0 %.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode, polarities and input pulses.

FIGURE 3 – SWITCHING TIMES

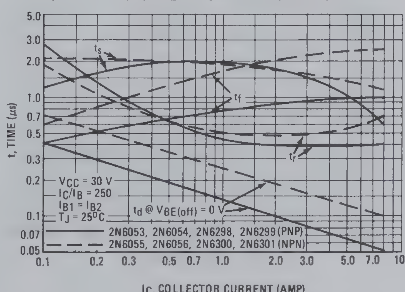
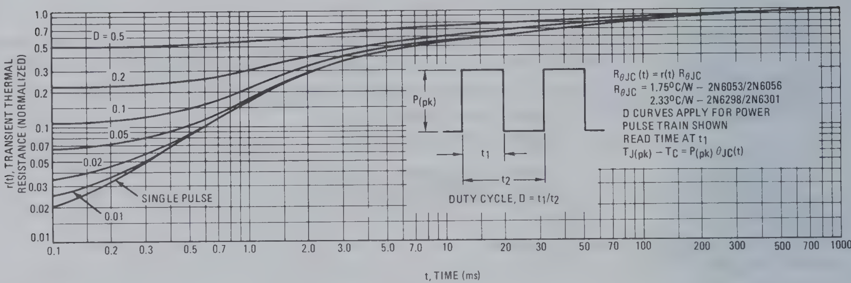


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6053 thru 2N6056

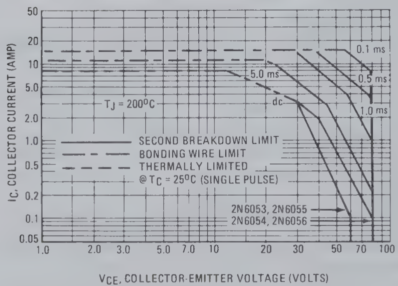
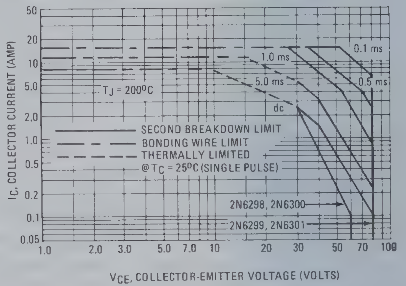


FIGURE 6 – 2N6298 thru 2N6301



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 – SMALL-SIGNAL CURRENT GAIN

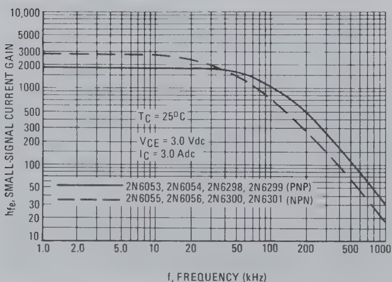
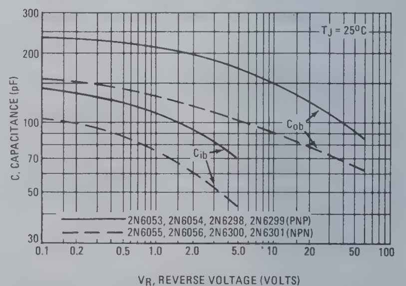


FIGURE 8 – CAPACITANCE



PNP — 2N6053, 2N6054, 2N6298, 2N6299

NPN — 2N6055, 2N6056, 2N6300, 2N6301

FIGURE 9 – DC CURRENT GAIN

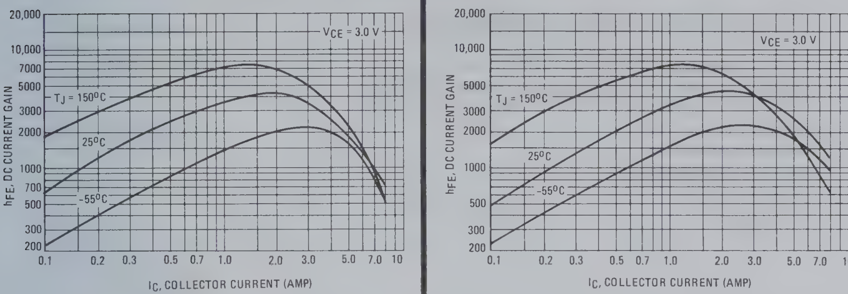


FIGURE 10 – COLLECTOR SATURATION REGION

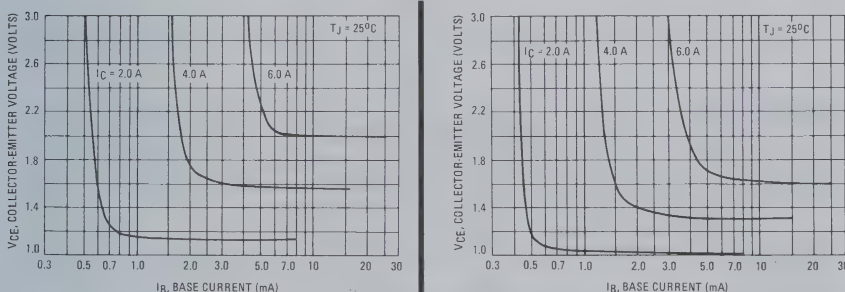
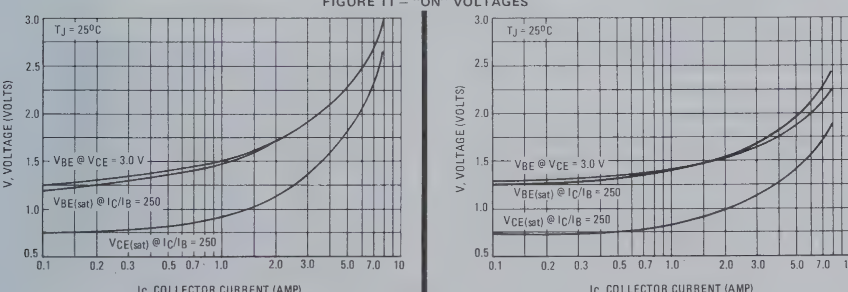


FIGURE 11 – "ON" VOLTAGES



2N6077
2N6078

MOTOROLA

1.3

HIGH VOLTAGE NPN SILICON TRANSISTORS

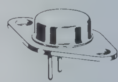
. . . the 2N6077 and 2N6078 transistors are designed for high-voltage, high-speed switching applications. They are characterized for operating directly off the rectified 110 Volt power lines in circuits such as:

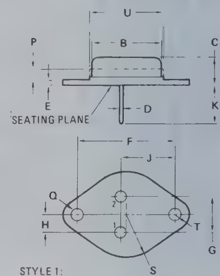
- Switching Regulators
- Solenoid and Relay Drivers
- Motor Controls
- Inverters

7 AMPERES

NPN SILICON POWER TRANSISTORS

275–300 VOLTS
45 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89		0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and Notes Apply.

CASE 80-02
TO-66

*MAXIMUM RATINGS

Rating	Symbol	2N6077	2N6078	Unit
Collector-Emitter Voltage	V_{CEX}	300	275	Vdc
Collector-Base Voltage	V_{CBO}	300	275	Vdc
Emitter-Base Voltage	V_{EBO}	6		Vdc
Collector Current — Continuous — Peak	I_C I_{CM}	7 10		Adc
Base Current — Continuous	I_B	4		Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	45 0.257		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.9	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

*Indicates JEDEC Registered Data

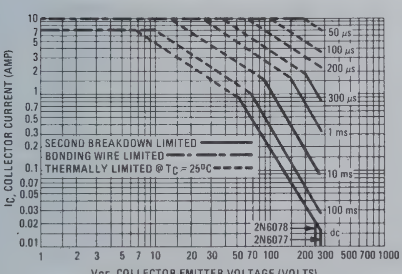
1.3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 200 mA, I_B = 0)	2N6077	$V_{CEO(sus)}$	275	–	Vdc
	2N6078		250	–	
Emitter Cutoff Current (V_{BE} = 6 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
Collector Cutoff Current (V_{CEV} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6077	I_{CEV}	–	5.0	mAdc
	2N6078		–	0.05	
(V_{CEV} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6077		–	8.0	
	2N6078		–	0.2	
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6077	I_{CEO}	–	2.0	mA
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.2 Adc, V_{CE} = 1 Vdc)		h_{FE}	12	70	–
Collector-Emitter Saturation Voltage (I_C = 1.2 Adc, I_B = 0.2 Adc)	2N6077 2N6078	$V_{CE(sat)}$	–	0.5	Vdc
(I_C = 3 Adc, I_B = 0.6 Adc)	2N6077		–	1.0	
(I_C = 5 Adc, I_B = 1 Adc)	2N6078		–	3.0	
Base-Emitter Saturation Voltage (I_C = 1.2 Adc, I_B = 0.2 Adc)	2N6077 2N6078	$V_{BE(sat)}$	–	1.6	Vdc
(I_C = 3 Adc, I_B = 0.6 Adc)	2N6077		–	1.9	
(I_C = 5 Adc, I_B = 1 Adc)	2N6078		–	2.0	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		$\|h_{fe}\|$	1.0	–	MHz
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Rise Time	(V_{CC} = 250 Vdc, I_C = 1.2 Adc,	t_r	–	0.75	µs
Storage Time	I_{B1} = I_{B2} = 200 mAdc = 100 µs,	t_s	–	5.0	µs
Fall Time	Duty Cycle ≤ 2.0%)	t_f	–	0.75	µs

* Indicates JEDEC Registered Data

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe Operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 12 and 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

PNP NPN

2N6107 2N6288
2N6109 2N6290
2N6111 2N6292

MOTOROLA

1.3

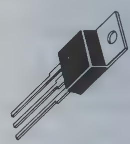
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 7.0 Amperes
  h_{FE} = 30–150 @ I_C = 3.0 Adc – 2N6111, 2N6288
  = 2.3 (Min) @ I_C = 7.0 Adc – All Devices
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 30 Vdc (Min) – 2N6111, 2N6288
  = 50 Vdc (Min) – 2N6109, 2N6290
  = 70 Vdc (Min) – 2N6107, 2N6292
- High Current Gain – Bandwidth Product
  f_T = 4.0 MHz (Min) @ I_C = 500 mAdc – 2N6288, 90, 92
  = 10 MHz (Min) @ I_C = 500 mAdc – 2N6107, 09, 11
- TO-220AB Compact Package
- TO-66 Leadform Also Available

7 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

30–50–70 VOLTS
40 WATTS



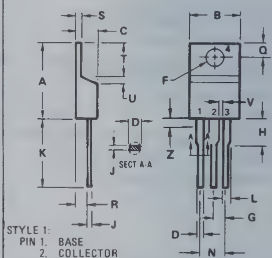
*MAXIMUM RATINGS

Rating	Symbol	2N6111 2N6288	2N6109 2N6290	2N6107 2N6292	Unit
Collector-Emitter Voltage	V_{CEO}	30	50	70	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current – Continuous Peak	I_C		7.0 10		Adc
Base Current	I_B		3.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		40 0.32		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

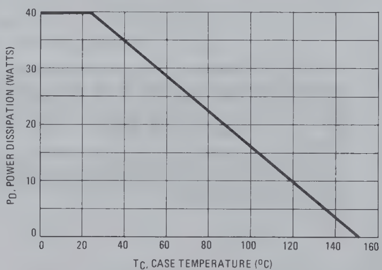
*Indicates JEDEC Registered Data



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

FIGURE 1 – POWER DERATING

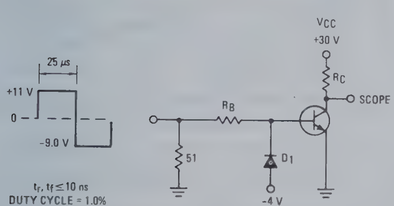


***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6111, 2N6288		30	–	
	2N6109, 2N6290		50	–	
	2N6107, 2N6292		70	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N6111, 2N6288		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6109, 2N6290		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6107, 2N6292		–	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6111, 2N6288		–	100	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6109, 2N6290		–	100	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6107, 2N6292		–	100	
(V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6111, 2N6288		–	2.0	mAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6109, 2N6290		–	2.0	
(V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6107, 2N6292		–	2.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)	2N6107, 2N6292		30	150	
(I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)	2N6109, 2N6290		30	150	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N6111, 2N6288		30	150	
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)	All Devices		2.3	–	
Collector-Emitter Saturation Voltage (I_C = 7.0 Adc, I_B = 3.0 Adc)		$V_{CE(sat)}$	–	3.5	Vdc
Base-Emitter On Voltage (I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	3.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)		f_T			MHz
	2N6288, 90, 92		4.0	–	
	2N6107, 09, 11		10	–	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	250	pF
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 50 kHz)		h_{fe}	20	–	–

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE IB ≈100 mA
MSD6100 USED BELOW IB ≈100 mA

FIGURE 3 — TURN-ON TIME

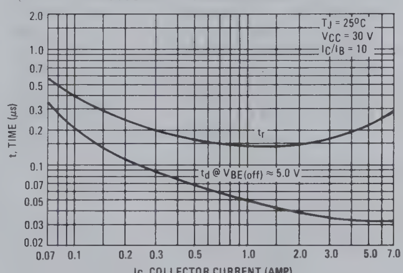


FIGURE 4 — THERMAL RESPONSE

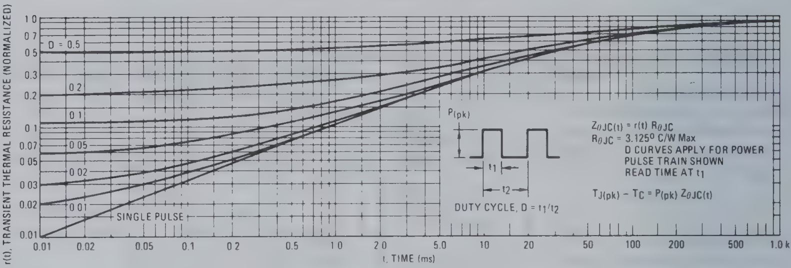
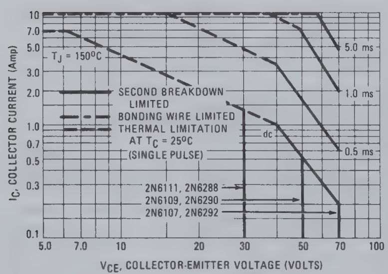


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high-case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 — TURN-OFF TIME

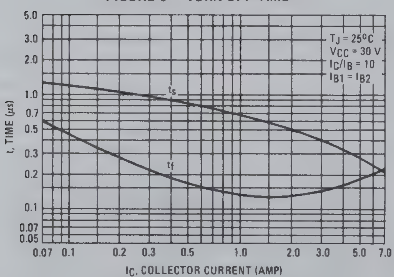
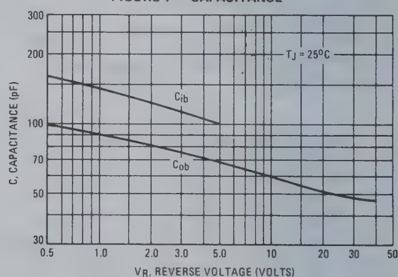


FIGURE 7 — CAPACITANCE



MOTOROLA

NPN **PNP**
2N6121 2N6124
2N6122 2N6125
2N6123 2N6126

1.3

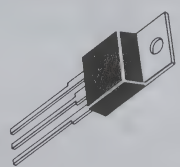
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in power amplifier and switching circuits, — packaged in the compact TO-220AB outline. TO-66 leadform also available.

4 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

45-80 VOLTS
40 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N6121 2N6124	2N6122 2N6125	2N6123 2N6126	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current	I_C		4.0		Adc
Base Current	I_B		1.0		Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D		40 320		Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–65 to +150		^oC

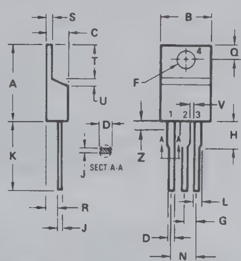
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	$^oC/W$

*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 0.1$ Adc, $I_B = 0$)	2N6121, 2N6124 2N6122, 2N6125 2N6123, 2N6126	$V_{CEO(sus)}$	45 60 80	– – –	Vdc
Collector Cutoff Current ($V_{CE} = 45$ Vdc, $I_B = 0$) ($V_{CE} = 60$ Vdc, $I_B = 0$) ($V_{CE} = 80$ Vdc, $I_B = 0$)	 2N6121, 2N6124 2N6122, 2N6125 2N6123, 2N6126	I_{CEO}	 – - –	 1.0 1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 45$ Vdc, $V_{EB(off)} = 1.5$ Vdc) ($V_{CE} = 60$ Vdc, $V_{EB(off)} = 1.5$ Vdc) ($V_{CE} = 80$ Vdc, $V_{EB(off)} = 1.5$ Vdc) ($V_{CE} = 45$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 125^oC$) ($V_{CE} = 60$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 125^oC$) ($V_{CE} = 80$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 125^oC$)	 2N6121, 2N6124 2N6122, 2N6125 2N6123, 2N6126 2N6121, 2N6124 2N6122, 2N6125 2N6123, 2N6126	I_{CEX}	 - – 	 0.1 0.1 0.1 2.0 2.0 2.0	mAdc
Collector Cutoff Current ($V_{CB} = 45$ Vdc, $I_E = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	 2N6121, 2N6124 2N6122, 2N6125 2N6123, 2N6126	I_{CBO}	 – – –	 0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) ($I_C = 1.5$ Adc, $V_{CE} = 2.0$ Vdc) ($I_C = 4.0$ Adc, $V_{CE} = 2.0$ Vdc)	 2N6126, 2N6124 2N6122, 2N6125 2N6123, 2N6126 2N6121, 2N6124 2N6122, 2N6125 2N6123, 2N6126	h_{FE}	 25 25 20 10 10 7.0	 100 100 80 – –	–
Collector-Emitter Saturation Voltage (1) ($I_C = 1.5$ Adc, $I_B = 0.15$ Adc) ($I_C = 4.0$ Adc, $I_B = 1.0$ Adc)		$V_{CE(sat)}$	 – –	 0.6 1.4	Vdc
Base-Emitter On Voltage (1) ($I_C = 1.5$ Adc, $V_{CE} = 2.0$ Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 0.1$ Adc, $V_{CE} = 2.0$ Vdc, f = 1.0 kHz)		h_{fe}	25	–	–
Current-Gain-Bandwidth Product ($I_C = 1.0$ Adc, $V_{CE} = 4.0$ Vdc, f = 1.0 MHz)		f_T	2.5	–	MHz

(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.
*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

1.3

FIGURE 1 — DC CURRENT GAIN

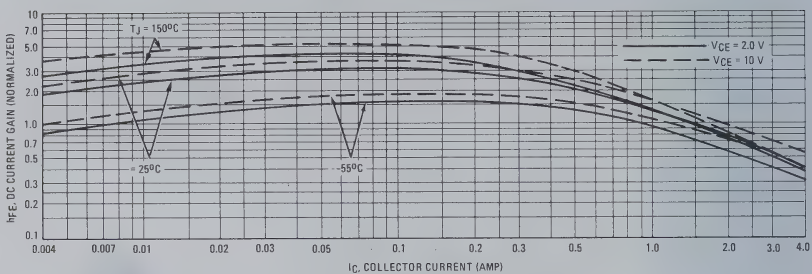


FIGURE 2 — COLLECTOR SATURATION REGION

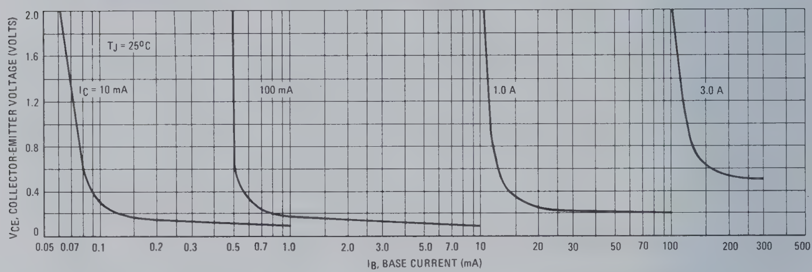


FIGURE 3 — "ON" VOLTAGES

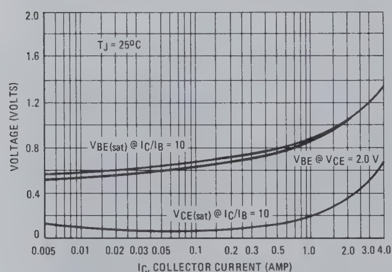


FIGURE 4 — TEMPERATURE COEFFICIENTS

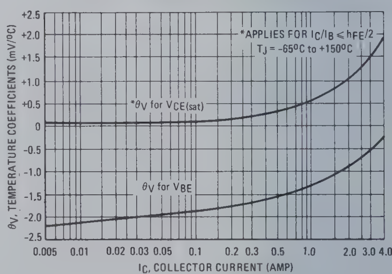


FIGURE 5 – COLLECTOR CUT-OFF REGION

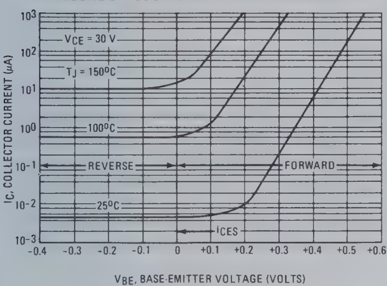


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

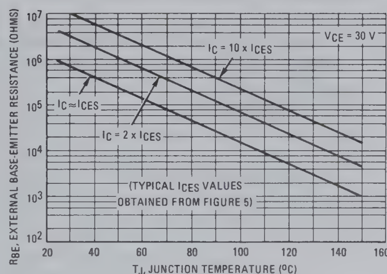
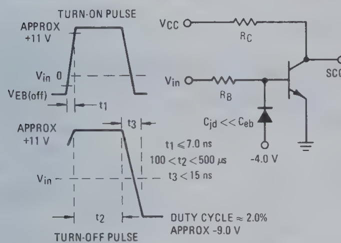


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT



RB AND RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

Reverse all polarities and diode for PNP transistors.

FIGURE 8 – CAPACITANCE

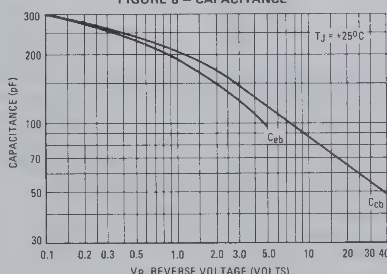


FIGURE 9 – TURN-ON TIME

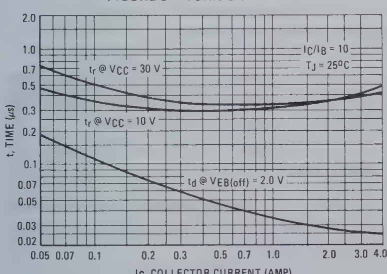
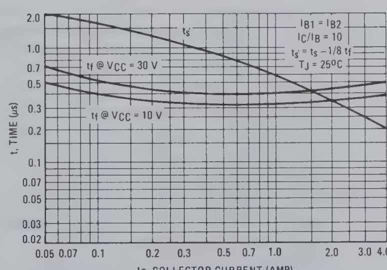


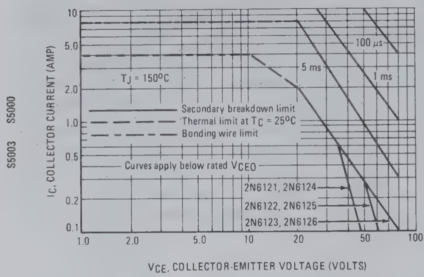
FIGURE 10 – TURN-OFF TIME



RATING AND THERMAL DATA

1.3

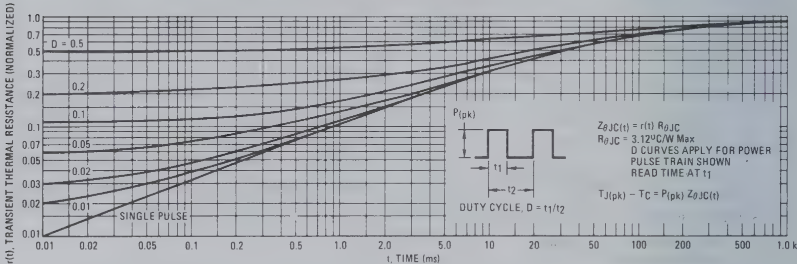
FIGURE 11 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: peak junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

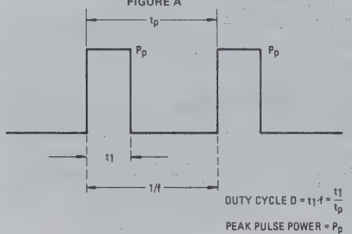
The data of Figure 11 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 12 – THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:
The 2N6121 is dissipating 50 watts under the following conditions: $t_1 = 0.1$ ms, $t_p = 0.5$ ms. (D = 0.2).
Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.
The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2°C$$

MOTOROLA

2N6186 thru 2N6189

MEDIUM-POWER PNP SILICON TRANSISTORS

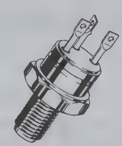
. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 10 Adc
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact, High Dissipation TO-59 Case
- Isolated Collector Configuration
- Complement to NPN 2N5346 thru 2N5349

10 AMPERE

POWER TRANSISTORS
PNP SILICON

80–100 VOLTS
60 WATTS



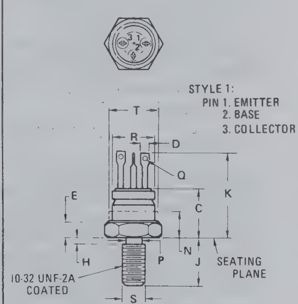
*MAXIMUM RATINGS

Rating	Symbol	2N6186 2N6187	2N6188 2N6189	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 343		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.91	°C/W

*Indicates JEDEC Registered Data.

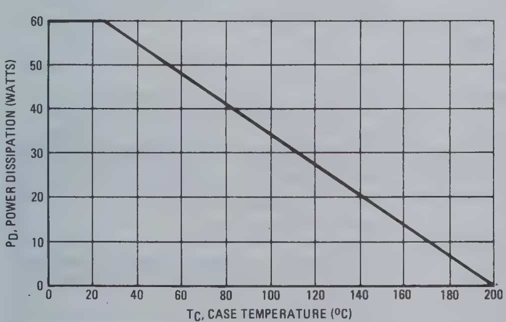


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	10.77	11.10	0.424	0.437
C	8.13	11.89	0.320	0.468
E	2.29	3.81	0.090	0.150
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	10.16	11.56	0.400	0.455
K	14.48	19.38	0.570	0.763
L	2.29	2.79	0.090	0.110
N	–	6.35	–	0.250
P	4.14	4.80	0.163	0.189
Q	1.02	1.65	0.040	0.065
R	8.08	9.65	0.318	0.380
S	4.212	4.310	0.1658	0.1697
T	9.65	11.10	0.380	0.437

All JEDEC dimensions and notes apply
Collector isolated from case.

CASE 160-03
TO-59

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



1.3

*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$, unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6186, 87		80	–	
	2N6188, 89		100	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N6186, 87		–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N6188, 89		–	100	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6186, 87		–	10	
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6188, 89		–	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, $T_C = 150^oC$)	2N6186, 87		–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150^oC$)	2N6188, 89		–	1.0	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	2N6186, 88		30	–	
	2N6187, 89		60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N6186, 88		30	120	
	2N6187, 89		60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N6186, 88		20	–	
	2N6187, 89		40	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)			–	0.7	
(I_C = 7.0 Adc, I_B = 0.7 Adc)			–	1.2	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)			–	1.2	
(I_C = 10 Adc, I_B = 1.0 Adc)			–	2.0	
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{Test} = 10 MHz)		f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	300	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		C_{ib}	–	1250	pF
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc,	t_d	–	100	ns
Rise Time	I_C = 2.0 Adc, I_{B1} = 200 mAdc)	t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	t_s	–	2.0	μs
Fall Time	$I_{B1} = I_{B2}$ = 200 mAdc)	t_f	–	200	ns

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{Test}$

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

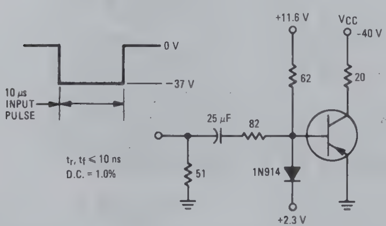


FIGURE 3 — TURN-ON TIME

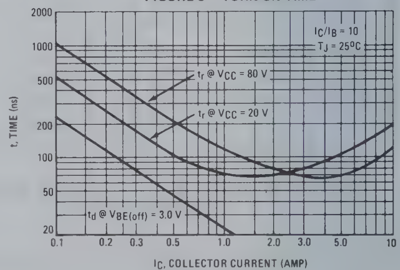


FIGURE 4 — THERMAL RESPONSE

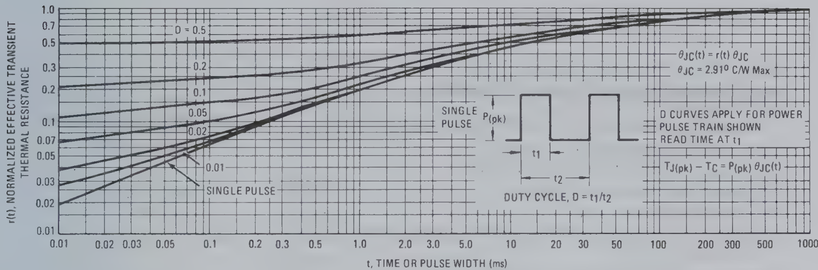
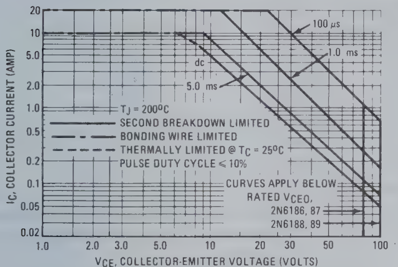


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — TURN-OFF TIME

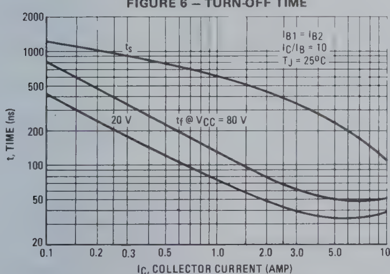
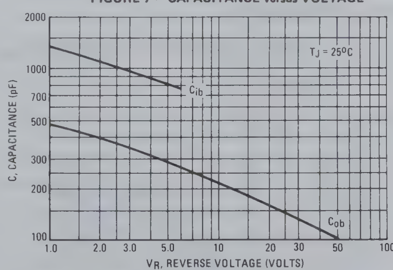


FIGURE 7 — CAPACITANCE versus VOLTAGE



2N6190 thru 2N6193

MOTOROLA

MEDIUM-POWER PNP SILICON TRANSISTORS

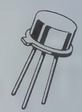
. . . designed for switching and wide band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 5.0 Amp
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-39 Case for Critical Space Limited Applications
- Complement to NPN 2N5336 thru 2N5339

5 AMPERE

POWER TRANSISTORS PNP SILICON

80-100 VOLTS 10 WATTS



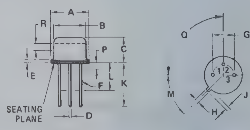
*MAXIMUM RATINGS

Rating	Symbol	2N6190 2N6191	2N6192 2N6193	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25^oC$	P_D	10		Watts
Derate above 25^oC		57.1		$mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	17.5	$^oC/W$

*Indicates JEDEC Registered Data.



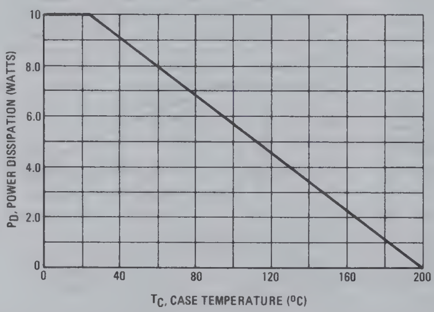
STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45^o NOM		45^o NOM	
P	–	1.27	–	0.050
Q	90^o NOM		90^o NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

FIGURE 1 — POWER-TEMPERATURE DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

*** ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	2N6190, 2N6191 2N6192, 2N6193	$V_{CEO(sus)}$	80 100	– –	Vdc
Collector Cutoff Current (V_{CE} = 75 Vdc, I_B = 0) (V_{CE} = 90 Vdc, I_B = 0)	2N6190, 2N6191 2N6192, 2N6193	I_{CEO}	– –	100 100	μAdc
Collector Cutoff Current (V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6190, 2N6191 2N6192, 2N6193 2N6190, 2N6191 2N6192, 2N6193	I_{CEX}	– – – –	10 10 1.0 1.0	μAdc mAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	2N6190, 2N6191 2N6192, 2N6193	I_{CBO}	– –	10 10	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 2.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N6190, 2N6192 2N6191, 2N6193 2N6190, 2N6192 2N6191, 2N6193 2N6190, 2N6192 2N6191, 2N6193	h_{FE}	30 60 30 60 20 40	– – 120 240 – –	–
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc) (I_C = 5.0 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	– –	0.7 1.2	Vdc
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc) (I_C = 5.0 Adc, I_B = 0.5 Adc)		$V_{BE(sat)}$	– –	1.2 1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (2) (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{Test} = 10 MHz)		f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	300	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		C_{ib}	–	1250	pF
SWITCHING CHARACTERISTICS					
Delay Time (V_{CC} = 40 Vdc, $V_{BE(off)}$ = 3.0 Vdc, I_C = 2.0 Adc, I_{B1} = 0.2 Adc)		t_d	–	100	ns
Rise Time		t_r	–	100	ns
Storage Time (V_{CC} = 40 Vdc, I_C = 2.0 Adc, I_{B1} = I_{B2} = 0.2 Adc)		t_s	–	2.0	μs
Fall Time		t_f	–	200	ns

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
(2) $f_T = |h_{fe}| \cdot f_{Test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

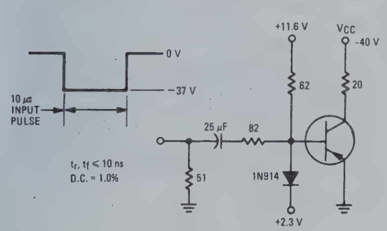


FIGURE 3 – TURN ON TIME

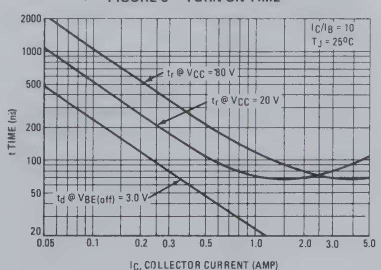


FIGURE 4 – THERMAL RESPONSE

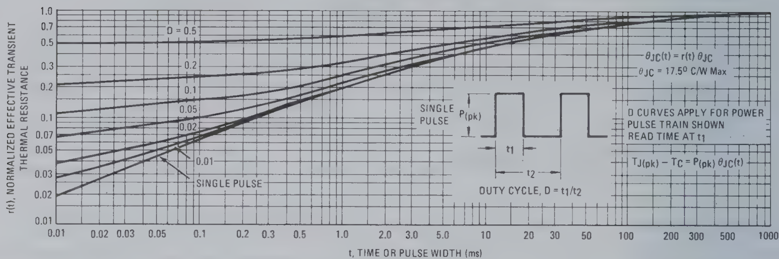
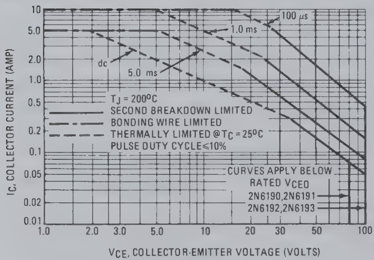


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitaitons imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

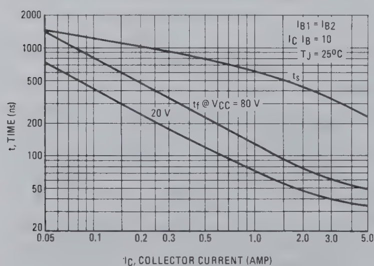
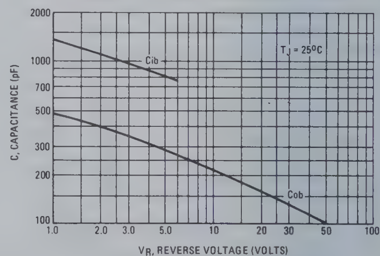


FIGURE 7 – CAPACITANCE versus VOLTAGE



MOTOROLA

2N6211
2N6212
2N6213

1.3

MEDIUM-POWER HIGH-VOLTAGE PNP POWER TRANSISTORS

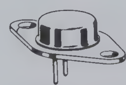
. . . designed for high-speed switching and linear amplifier applications for high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

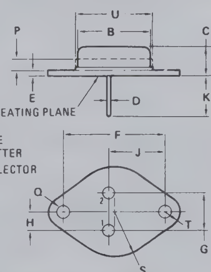
- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 225 to 350 Vdc @ I_C = 200 mAdc
- Second Breakdown Collector Current — $I_{s/b}$ = 875 mAdc @ V_{CE} = 40 Vdc
- t_f = 0.6 μs Resistive Fall Time
- Usable DC Current Gain to 2.0 Adc

2 AMPERE

POWER TRANSISTORS PNP SILICON

225–350 VOLTS
35 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

*MAXIMUM RATINGS

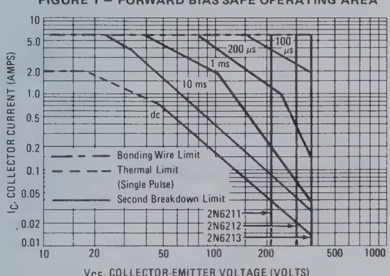
Rating	Symbol	2N6211	2N6212	2N6213	Unit
Collector-Emitter Voltage	V_{CEO}	225	300	350	Vdc
Collector-Base Voltage	V_{CB}	275	350	400	Vdc
Emitter-Base Voltage	V_{EB}		6		Vdc
Collector Current — Continuous	I_C		2		Adc
Peak			5		
Base Current	I_B		1		Adc
Total Power Dissipation @ T_C = 25°C	P_D		35		Watts
Derate above 25°C			0.2		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See Figure 8).

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6211		225	–	
	2N6212		300	–	
	2N6213		350	–	
*Collector-Emitter Sustaining Voltage		$V_{CEX(sus)}$			Vdc
(I_C = 200 mA, V_{BE} = −1.5 V, L = 10 mH)	2N6211		275	–	
	2N6212		350	–	
	2N6213		400	–	
*Collector-Emitter Sustaining Voltage (1)		$V_{CER(sus)}$			Vdc
(I_C = 200 mA, I_B = 0, R_{BE} = 50 Ω)	2N6211		250	–	
	2N6212		325	–	
	2N6213		375	–	
*Emitter-Base Breakdown Voltage (1)		V_{EBO}			Vdc
(I_E = 0.5 mAdc, I_C = 0)	2N6212/13		6.0	–	
(I_E = 1.0 mAdc, I_C = 0)	2N6211		6.0	–	
*Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 25°C)			–	0.5	
(T_C = 100°C)			–	5.0	
(V_{CE} = 315 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 25°C)			–	0.5	
(T_C = 100°C)			–	5.0	
(V_{CE} = 360 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 25°C)			–	0.5	
(T_C = 100°C)			–	5.0	
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	All Types	I_{CEO}	–	5.0	mAdc
*Emitter Cutoff Current		I_{EBO}			mAdc
(V_{EB} = 6.0 Vdc, I_C = 0)	2N6211		–	1.0	
	2N6212		–	0.5	
	2N6213		–	0.5	
***ON CHARACTERISTICS (1)**					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 2.8 Vdc)	2N6211		10	100	
(I_C = 1.0 Adc, V_{CE} = 3.2 Vdc)	2N6212		10	100	
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)	2N6213		10	100	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 125 mAdc)	2N6211		–	1.4	
	2N6212		–	1.6	
	2N6213		–	2.0	
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 125 mAdc)	All Types	$V_{BE(sat)}$	–	1.4	Vdc
DYNAMIC CHARACTERISTICS					
*Current Gain—Bandwidth Product (2) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 5.0 MHz)		f_T	20	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	220	pF
***SECOND BREAKDOWN**					
*Second Breakdown Collector Current with Base Forward Biased t = 1.0 s (non-repetitive) (V_{CE} = 40 Vdc)		$I_{S/b}$	0.875	–	Adc
***SWITCHING CHARACTERISTICS**					
Rise Time	(V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.125 Adc)	t_r	–	0.6	μs
Storage Time		t_s	–	2.5	μs
Fall Time		t_f	–	0.6	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

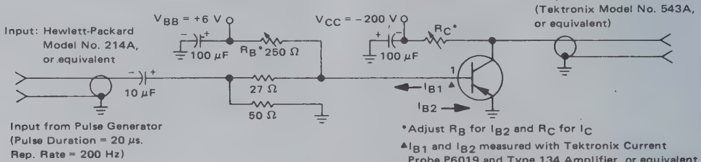


FIGURE 3 – DC CURRENT GAIN

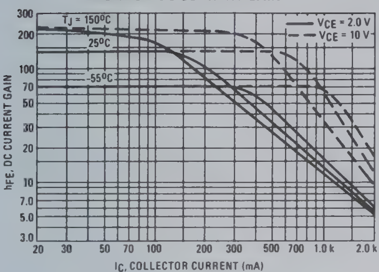


FIGURE 4 – COLLECTOR SATURATION REGION

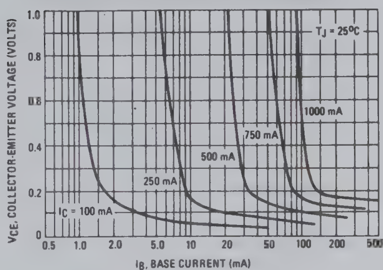


FIGURE 5 – COLLECTOR CUTOFF REGION

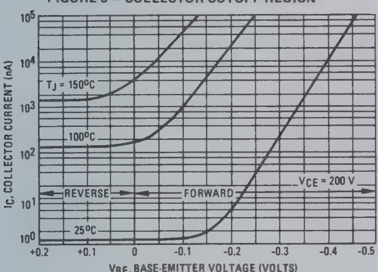


FIGURE 6 – TEMPERATURE COEFFICIENTS

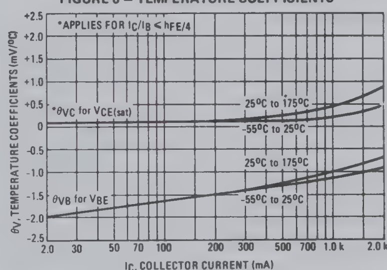


FIGURE 7 – BASE CUTOFF REGION

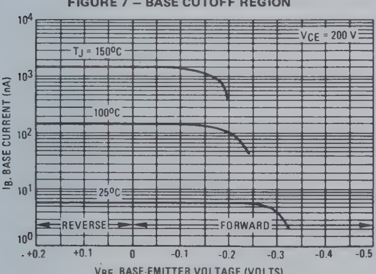
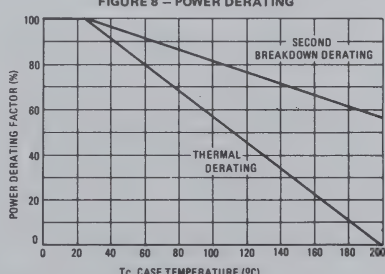


FIGURE 8 – POWER DERATING



2N6233
2N6234
2N6235

MOTOROLA

1.3

HIGH VOLTAGE NPN SILICON TRANSISTORS

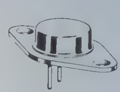
. . . useful for high-voltage medium power applications such as switching regulators.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 225 Vdc — 2N6233
  275 Vdc — 2N6234
  325 Vdc — 2N6235
- DC Current Gain — h_{FE} = 25 to 125 — I_C = 1.0 Adc
- Low Collector-Emitter Saturation Voltage
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 1.0 Adc
- High Frequency Response — f_T = 20 MHz (Min)
- Fast Switching Times @ 1.0 Adc —
  t_r = 0.5 μs (Max)
  t_s = 3.5 μs (Max)
  t_f = 0.5 μs (Max)

5 AMPERE

POWER TRANSISTORS
NPN SILICON

225,275,325 VOLTS
50 WATTS



*MAXIMUM RATINGS

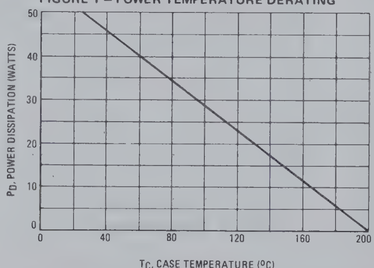
Rating	Symbol	2N6233	2N6234	2N6235	Unit
Collector-Emitter Voltage	V_{CEO}	225	275	325	Vdc
Collector-Base Voltage	V_{CB}	250	300	350	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 5.0 → ← 10 →			Adc
Base Current	I_B	← 2.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 50 → ← 0.286 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

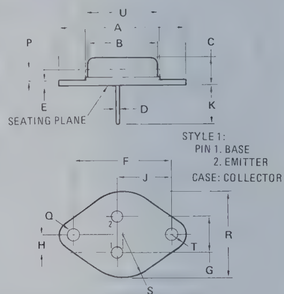
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.5	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER TEMPERATURE DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27		0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

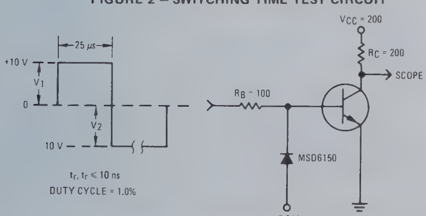
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 20 mAdc, I_B = 0)	2N6233		225	–	
	2N6234		275	–	
	2N6235		325	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 225, I_B = 0)	2N6233		–	1.0	
(V_{CE} = 275, I_B = 0)	2N6234		–	1.0	
(V_{CE} = 325, I_B = 0)	2N6235		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6233			1.0	
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6234		–	1.0	
(V_{CE} = 350 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6235			1.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 250 Vdc, I_E = 0)	2N6233			0.1	
(V_{CB} = 300 Vdc, I_E = 0)	2N6234		–	0.1	
(V_{CB} = 350 Vdc, I_E = 0)	2N6235		–	0.1	
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.1 Adc, V_{CE} = 5.0 Vdc)			25	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)			25	125	
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)				0.5	
(I_C = 5.0 Adc, I_B = 1.0 Adc)			–	2.5	
Base Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)				1.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc)			–	2.0	
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (2) (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	20	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	250	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_B = 0.1 Adc)		t_r	–	0.5	µs
Storage Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)		t_s	–	3.5	µs
Fall Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)		t_f		0.5	µs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ⩽ 300 µs, Duty Cycle ⩽ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



FOR INFORMATION ON FIGURES 3 and 6 R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS; D_1 DISCONNECTED AND V_2 REDUCED TO 5 VOLTS FOR t_d MEASUREMENT.

FIGURE 3 – TURN-ON TIME

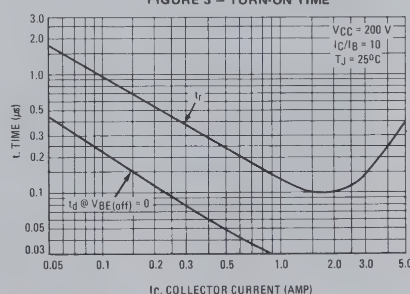


FIGURE 4 – THERMAL RESPONSE

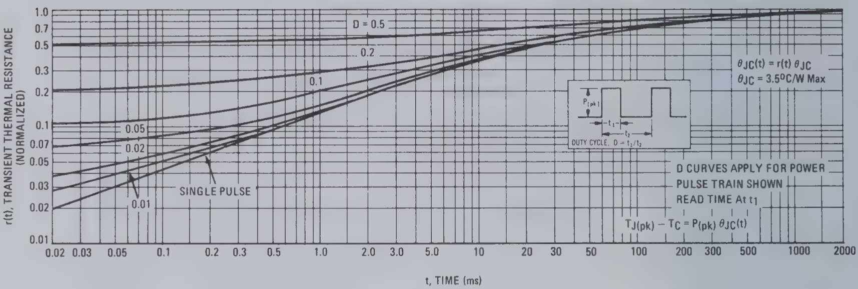
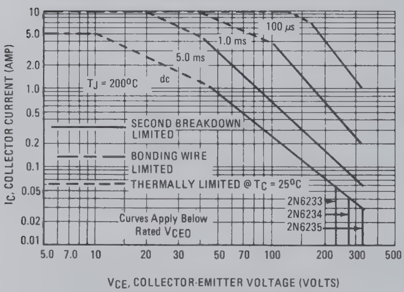


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

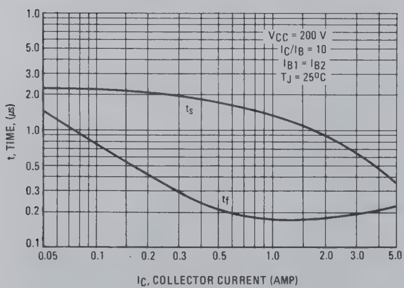
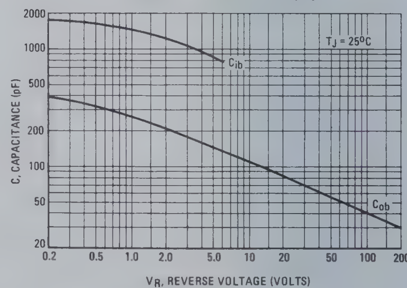


FIGURE 7 – CAPACITANCES



MOTOROLA

2N6249
2N6250
2N6251

1.3

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

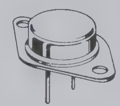
. . . designed for high voltage inverters, switching regulators and line operated amplifier applications. Especially well suited for switching power supply applications.

- High Voltage Breakdown Rating
- Low Saturation Voltages
- Fast Switching Capability
- High $E_{S/b}$ Energy Handling Capability

15 AMPERE

POWER TRANSISTORS
NPN SILICON

200, 275, 350 VOLTS
175 WATTS



MAXIMUM RATINGS

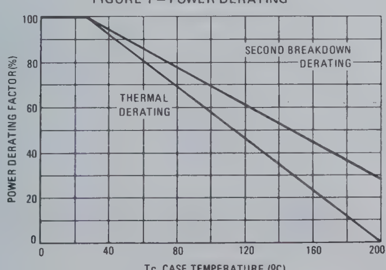
Rating	Symbol	2N6249	2N6250	2N6251	Unit
*Collector-Emitter Voltage	$V_{CEO(sus)}$	200	275	350	Vdc
*Collector-Emitter Voltage	$V_{CER(sus)}$	225	300	375	Vdc
*Collector-Base Voltage	V_{CB}	300	375	450	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current — Continuous**	I_C	← 15 →			Adc
— Peak	I_{CM}	← 30 →			
Base Current — Continuous*	I_B	← 10 →			Adc
— Peak	I_{BM}	← 20 →			
Emitter Current — Continuous	I_E	← 25 →			Adc
— Peak	I_{EM}	← 50 →			
Total Power Dissipation @ $T_C = 25^oC$	P_D	← 175 →			Watts
@ $T_C = 100^oC$		← 100 →			
Derate above 25^oC*		← 1.0 →			$W/^oC$
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +200 →			^oC

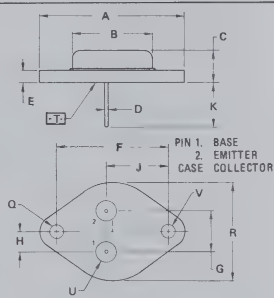
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data.
**JEDEC Registered Value is 10 A, Motorola Guaranteed Value is 15 A.

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	∅0.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	∅0.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

1.3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 200 mA, I_B = 0)	2N6249 2N6250 2N6251	$V_{CEO(sus)}$	200 275 350	– – –	Vdc
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 200 mA)	2N6249 2N6250 2N6251	$V_{CER(sus)}$	225 300 375	– – –	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CER}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CER}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEV}	– –	5.0 10	mAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 225 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	2N6249 2N6250 2N6251	I_{CEO}	– – –	5.0 5.0 5.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive)	(V_{CE} = 30 V) (V_{CE} = 100 V)	$I_{S/b}$	5.8 0.3	– –	Vdc
Second Breakdown Energy with base reverse biased (Table 1) (I_C = 10 A, $V_{BE(off)}$ = 4.0 Vdc, L = 50 µH)		$E_{S/b}$	2.5	–	mJ
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6249 2N6250 2N6251	h_{FE}	10 8.0 6.0	50 50 50	–
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.25 Adc) (I_C = 10 Adc, I_B = 1.67 Adc)	2N6249 2N6250 2N6251	$V_{CE(sat)}$	– – –	1.5 1.5 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.25 Adc) (I_C = 10 Adc, I_B = 1.67 Adc)	2N6249 2N6250 2N6251	$V_{BE(sat)}$	– – –	2.5 2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	2.5	–	MHz
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Rise Time	(V_{CC} = 200 Vdc, I_C = 10 A, Duty Cycle ≤ 2.0%, t_p = 100 µs)	t_r	–	2.0	µs
Storage Time	(I_{B1} = I_{B2} = 1.0 Adc) 2N6249 (I_{B1} = I_{B2} = 1.25 Adc) 2N6250 (I_{B1} = I_{B2} = 1.67 Adc) 2N6251	t_s		3.5	µs
Fall Time		t_f	–	1.0	µs

* Indicates JEDEC Registered Data.
(1) Measured on a curve tracer (60 Hz full-wave rectified sine wave).

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

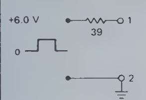
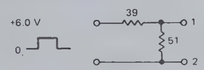
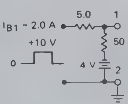
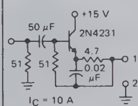
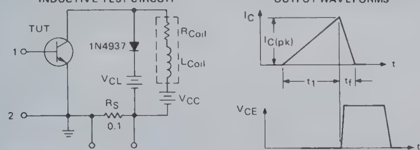
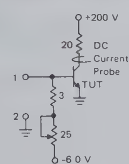
	$V_{CEO(sus)}$	$V_{CER(sus)}$	$E_{S/b}$	RESISTIVE SWITCHING
INPUT CONDITIONS				 I_C = 10 A PW ≈ 100 µs $t_r \leq$ 5 ns $t_f \leq$ 50 ns Duty Cycle ≤ 2%
CIRCUIT VALUES	L_{coil} = 42 mH R_{coil} = 0.7 Ω, f_o = 60 Hz V_{CC} = 0 to 50 V	L_{coil} = 14 mH R_{coil} = 0.05 Ω V_{CC} = 0 to 50 V f_o = 60 Hz	L_{coil} = 50 µH V_{CC} = 11.5 V R_{coil} = 0.2 Ω	V_{CC} = 200 V R_L = 20 Ω
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT / OUTPUT WAVEFORMS t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$ NOTE: Set $I_{C(pk)}$ to Obtain I_C = 200 mA at $V_{CEO(sus)}$ Equal to Rated Value. Adjust V_{Clamp} Voltage for $V_{CEO(sus)}$ Rated Value.			RESISTIVE TEST CIRCUIT 

FIGURE 2 – THERMAL RESPONSE

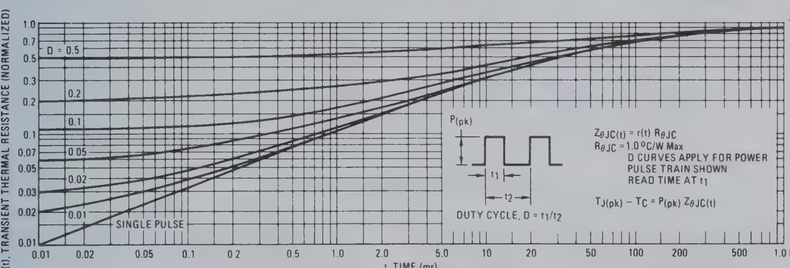
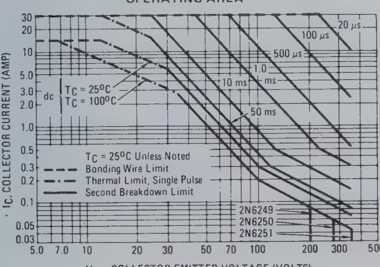


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on T_C = 25°C, $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 3 may be found at any case temperature by using the appropriate curve on Figure 1.

$T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

1.3

DC CHARACTERISTICS

FIGURE 4 — DC CURRENT GAIN

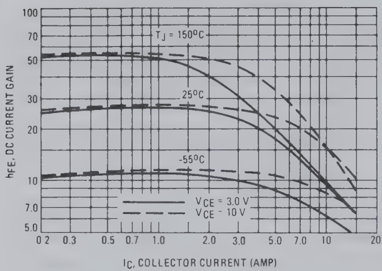


FIGURE 5 — COLLECTOR SATURATION REGION

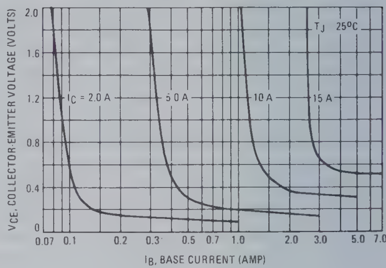


FIGURE 6 — "ON" VOLTAGE

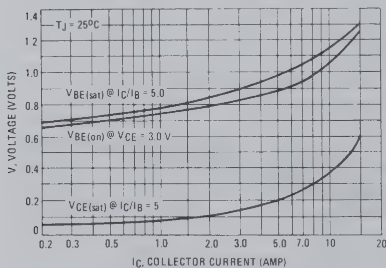
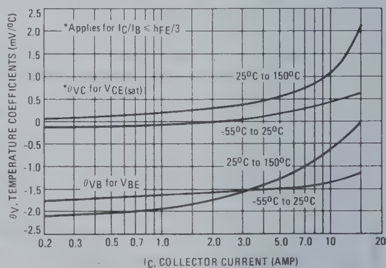


FIGURE 7 — TEMPERATURE COEFFICIENTS



RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

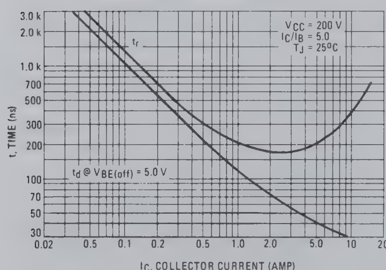
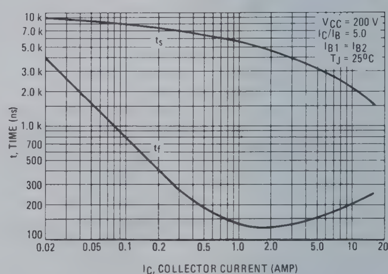


FIGURE 9 — TURN-OFF TIME



2N6274 thru 2N6277

1.3

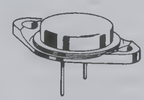
HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifer and switching circuit applications.

- High Collector Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N6274
  = 120 Vdc (Min) – 2N6275
  = 140 Vdc (Min) – 2N6276
  = 150 Vdc (Min) – 2N6277
- High DC Current Gain –
  h_{FE} = 30-120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35 μs (Max)
  t_s = 0.8 μs (Max
  t_f = 0.25 μs (Max)
- Complement to 2N6377-79

50 AMPERE
POWER TRANSISTORS
NPN SILICON

100, 120, 140, 150 VOLTS
250 WATTS



*MAXIMUM RATINGS

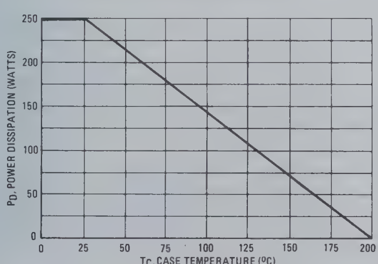
Rating	Symbol	2N6274	2N6275	2N6276	2N6277	Unit
Collector-Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →				Vdc
Collector Current – Continuous Peak	I_C	← 50 → ← 100 →				Adc
Base Current	I_B	← 20 →				Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	← 250 → ← 1.43 →				Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← –65 to +200 →				^oC

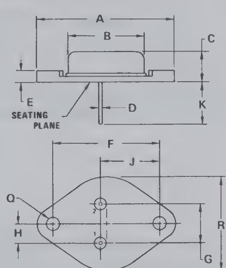
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^oC/W$

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

1.3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

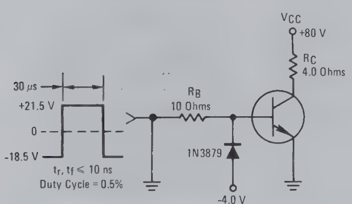
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6274		100	–	
	2N6275		120	–	
	2N6276		140	–	
	2N6277		150	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6274		–	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6275		–	50	
(V_{CE} = 70 Vdc, I_B = 0)	2N6276		–	50	
(V_{CE} = 75 Vdc, I_B = 0)	2N6277		–	50	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)			–	10	μAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			50	–	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)			30	120	
(I_C = 50 Adc, V_{CE} = 4.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)			–	1.0	
(I_C = 50 Adc, I_B = 10 Adc)			–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)			–	1.8	
(I_C = 50 Adc, I_B = 10 Adc)			–	3.5	
Base-Emitter On Voltage (I_C = 20 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	600	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = 2.0 Adc, $V_{BE(off)}$ = 5.0 Vdc)		t_r	–	0.35	μs
Storage Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)		t_s	–	0.80	μs
Fall Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)		t_f	–	0.25	μs

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN-ON TIME

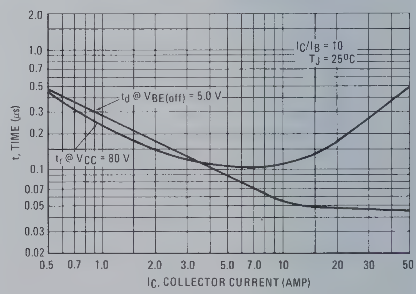


FIGURE 4 — THERMAL RESPONSE

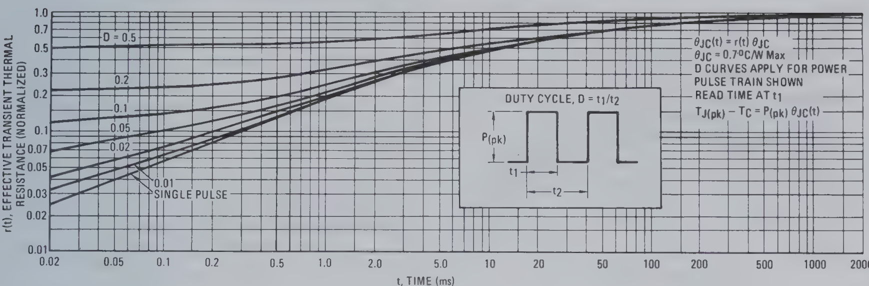
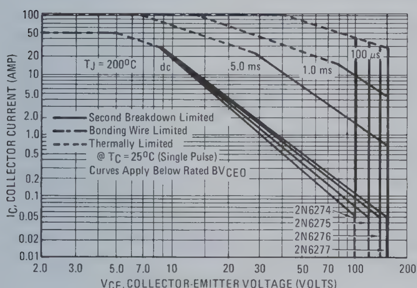


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — TURN-OFF TIME

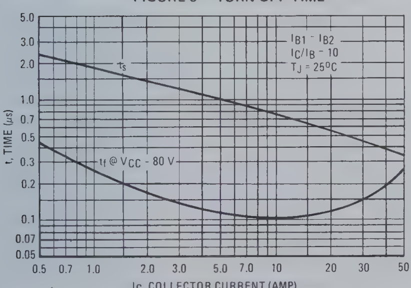


FIGURE 7 — CAPACITANCE

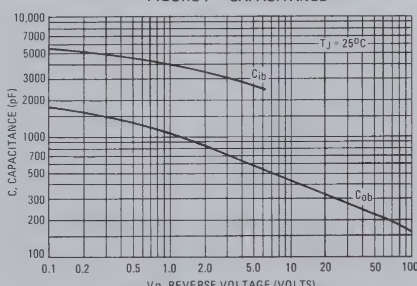


FIGURE 8 – DC CURRENT GAIN

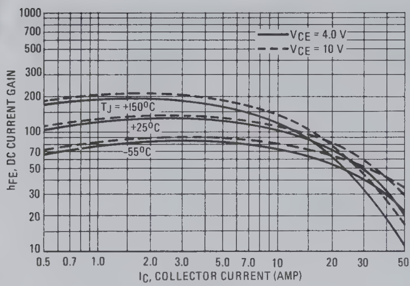


FIGURE 9 – COLLECTOR SATURATION REGION

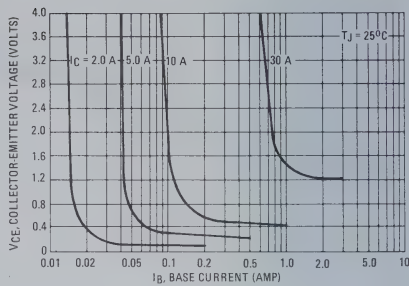


FIGURE 10 – "ON" VOLTAGES

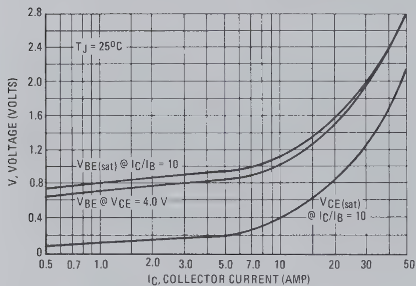


FIGURE 11 – TEMPERATURE COEFFICIENTS

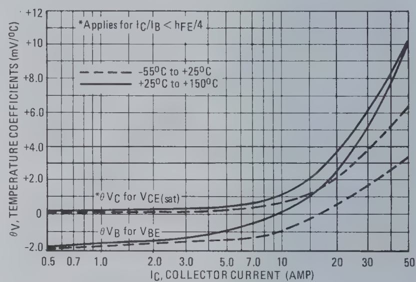


FIGURE 12 – COLLECTOR CUT-OFF REGION

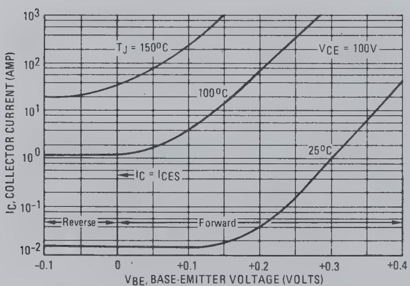
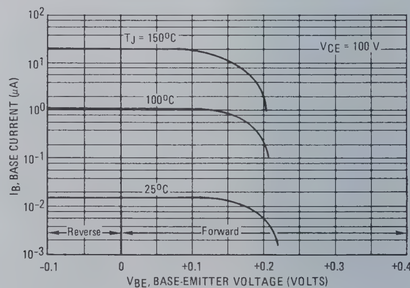


FIGURE 13 – BASE CUT-OFF REGION



2N6282 thru 2N6284 NPN
2N6285 thru 2N6287 PNP

MOTOROLA

1.3

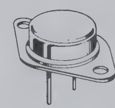
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low-frequency switching applications.

- High DC Current Gain @ I_C = 10 Adc —
  h_{FE} = 2400 (Typ) — 2N6282, 2N6283, 2N6284
  = 4000 (Typ) — 2N6285, 2N6286, 2N6287
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6282, 2N6285
  = 80 Vdc (Min) — 2N6283, 2N6286
  = 100 Vdc (Min) — 2N6284, 2N6287
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON
20 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS

60, 80, 100 VOLTS
160 WATTS



*MAXIMUM RATINGS

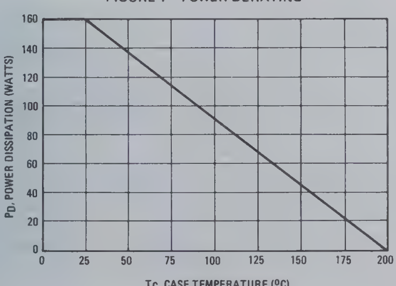
Rating	Symbol	2N6282 2N6285	2N6283 2N6286	2N6284 2N6287	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous Peak	I_C		20 40		Adc
Base Current	I_B		0.5		Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D		160 0.915		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +200		°C

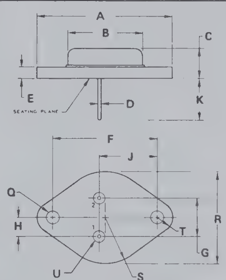
*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.09	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1–04

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

1.3

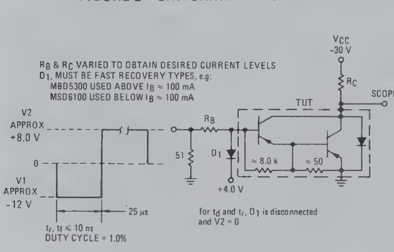
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0)	2N6282, 2N6285		60	–	
	2N6283, 2N6286		80	–	
	2N6284, 2N6287		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N6282, 2N6285		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6283, 2N6286		–	1.0	
(V_{CE} = 50 Vdc, I_B = 0)	2N6284, 2N6287		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)			–	0.5	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)			750	18,000	
(I_C = 20 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 40 mAdc)			–	2.0	
(I_C = 20 Adc, I_B = 200 mAdc)			–	3.0	
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\lvert h_{fe}\rvert$	4.0	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6282, 83, 84		–	400	
	2N6285, 86, 87		–	600	
Small-Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data.

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2%

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 – SWITCHING TIMES

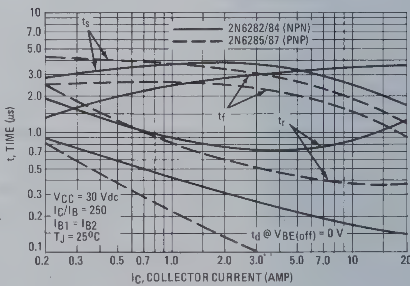
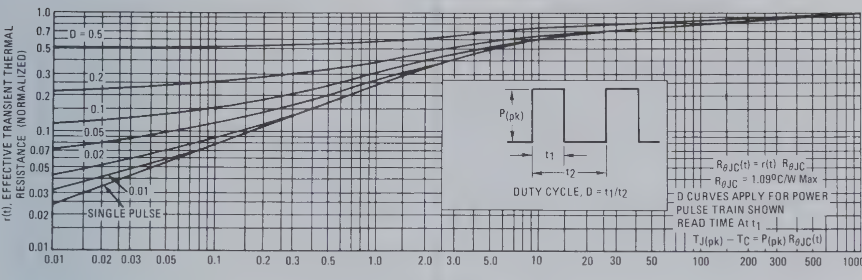


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6282, 2N6285

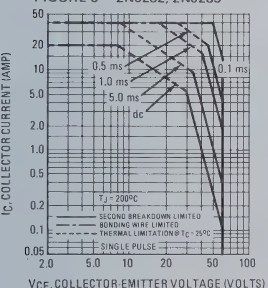


FIGURE 6 – 2N6283, 2N6286

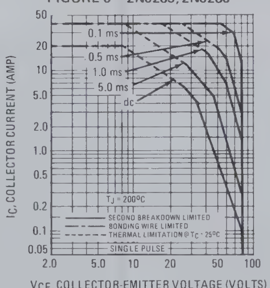
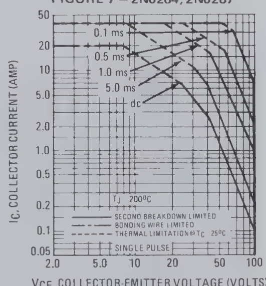


FIGURE 7 – 2N6284, 2N6287



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6 and 7 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 – SMALL-SIGNAL CURRENT GAIN

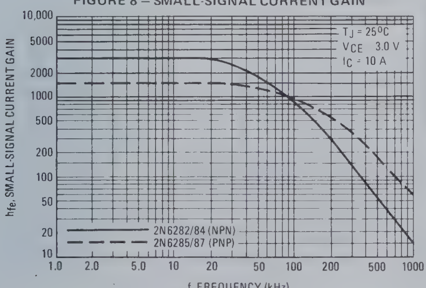
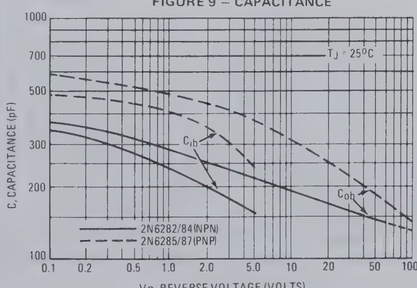


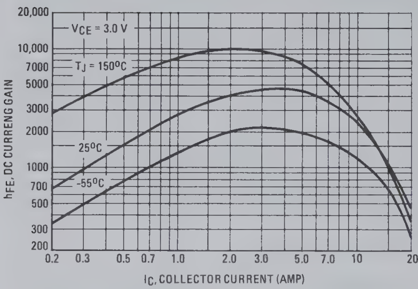
FIGURE 9 – CAPACITANCE



1.3

NPN	PNP
2N6282, 2N6283, 2N6284	2N6285, 2N6286, 2N6287

FIGURE 10 — DC CURRENT GAIN



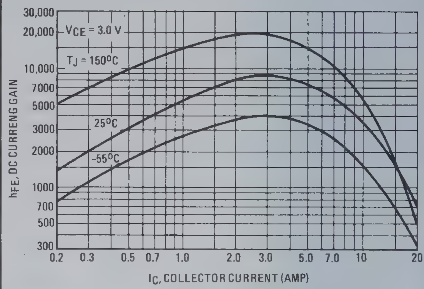
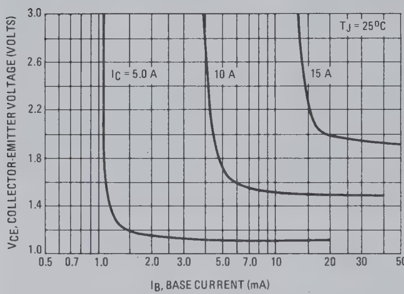


FIGURE 11 — COLLECTOR SATURATION REGION



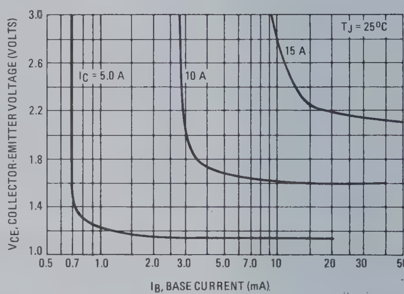
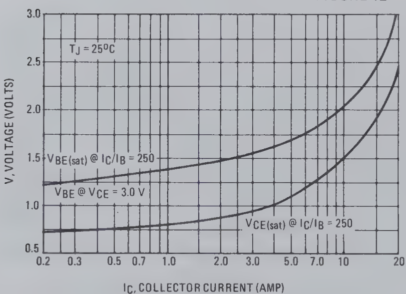
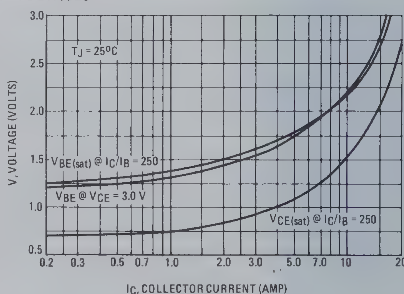


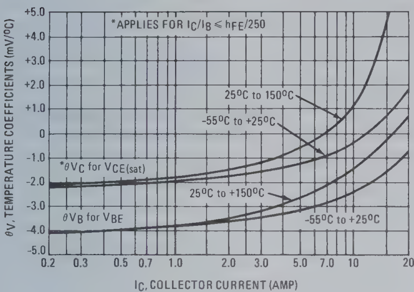
FIGURE 12 — "ON" VOLTAGES





NPN 2N6282, 2N6283, 2N6284	PNP 2N6285, 2N6286, 2N6287

FIGURE 13 – TEMPERATURE COEFFICIENTS



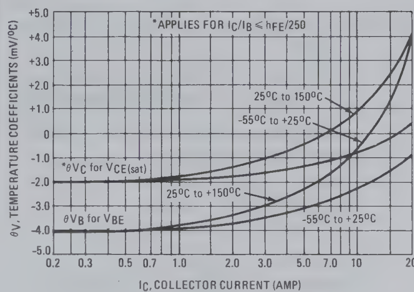
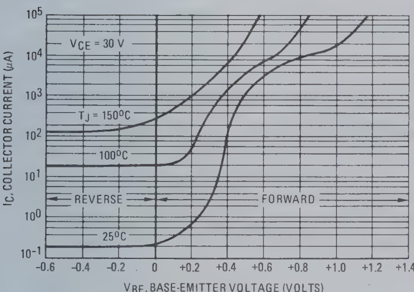


FIGURE 14 – COLLECTOR CUTOFF REGION



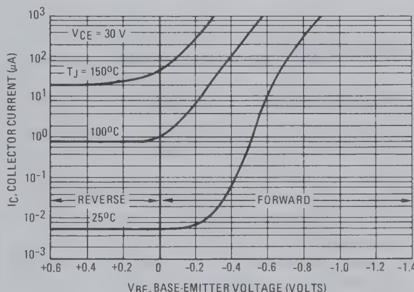
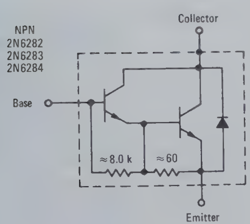
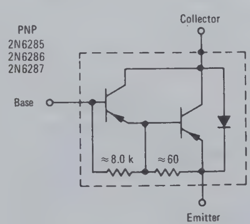


FIGURE 15 – DARLINGTON SCHEMATIC





2N6294, 2N6295 NPN
2N6296, 2N6297 PNP

MOTOROLA

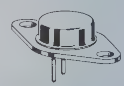
1.3

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier, low-frequency switching and hammer driver applications.

- High DC Current Gain — h_{FE} = 3000 (Typ) @ I_C = 2.0 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6294, 2N6296
  = 80 Vdc (Min) — 2N6295, 2N6297
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

4 AMPERES
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS
60, 80 VOLTS
50 WATTS



*MAXIMUM RATINGS

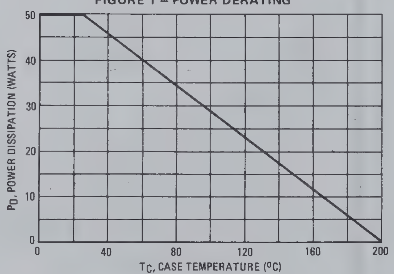
Rating	Symbol	2N6294 2N6296	2N6295 2N6297	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	4.0 8.0		Adc
Base Current	I_B	80		mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.286		Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200		°C

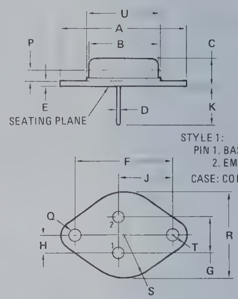
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

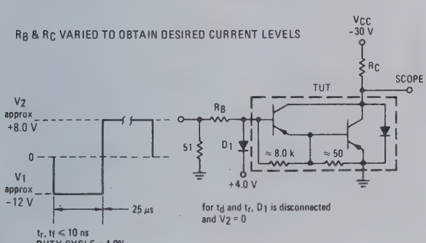
CASE 80-02
TO-66

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	2N6294, 2N6296	$V_{CEO(sus)}$	60	–	Vdc
	2N6295, 2N6297		80	–	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	2N6294, 2N6296	I_{CEO}	–	0.5	mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6295, 2N6297		–	0.5	
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)	2N6294, 2N6295	I_{CEX}	–	0.5	mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)	2N6296, 2N6297		–	0.5	
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6294, 2N6295		–	5.0	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6296, 2N6297		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	750	18000	–
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 8.0 mAdc)		$V_{CE(sat)}$	–	2.0	Vdc
(I_C = 4.0 Adc, I_B = 40 mAdc)			–	3.0	
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6294, 2N6295	C_{ob}	–	120	pF
	2N6296, 2N6297		–	200	
Small-Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit, reverse all polarities.

FIGURE 3 – SWITCHING TIMES

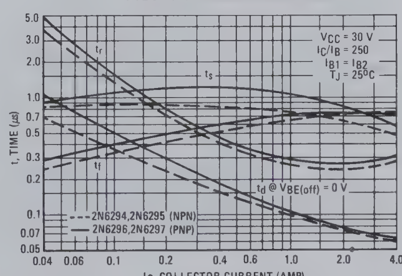


FIGURE 4 – THERMAL RESPONSE

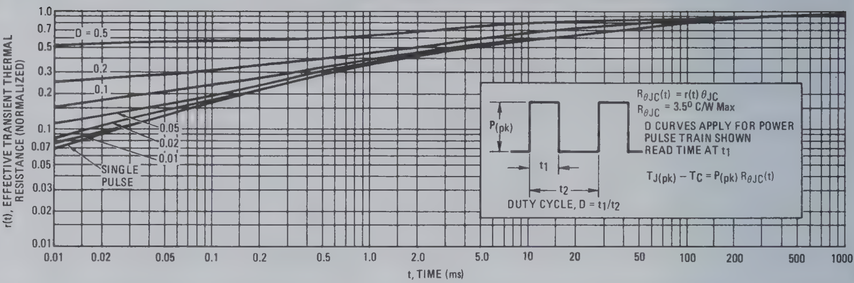
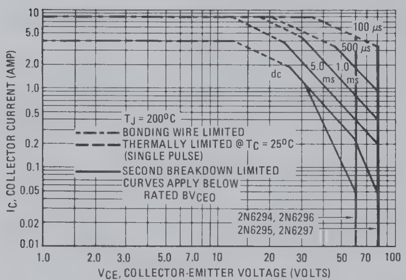


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

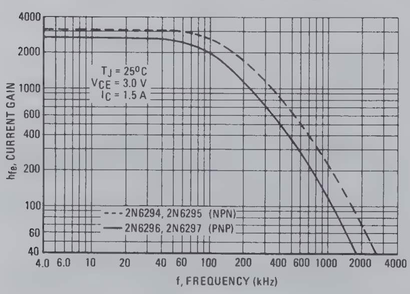
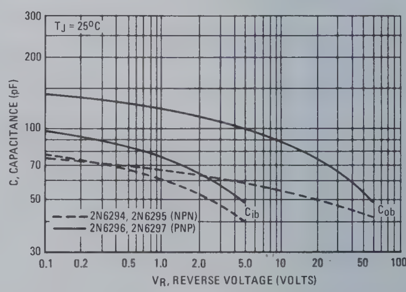


FIGURE 7 – CAPACITANCE



NPN 2N6294, 2N6295	PNP 2N6296, 2N6297

FIGURE 8 – DC CURRENT GAIN

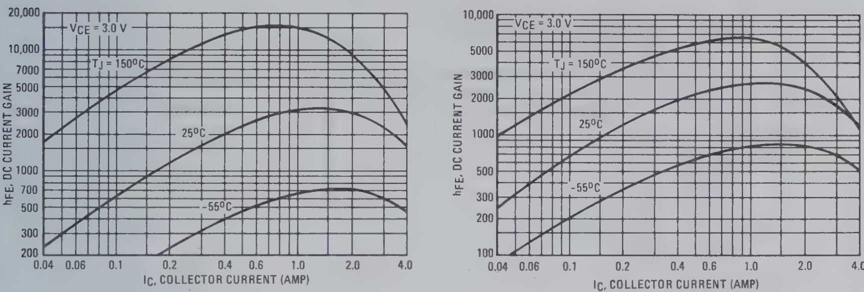


FIGURE 9 – COLLECTOR SATURATION REGION

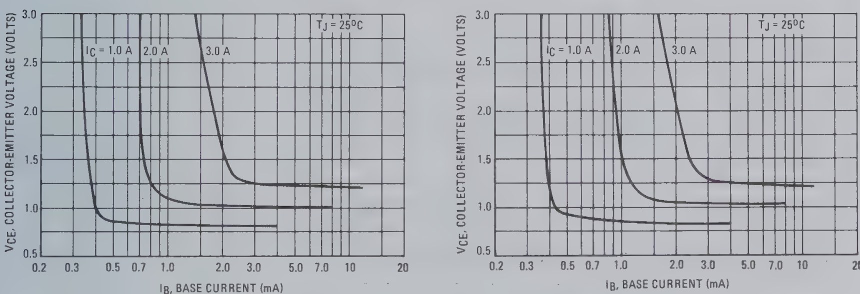
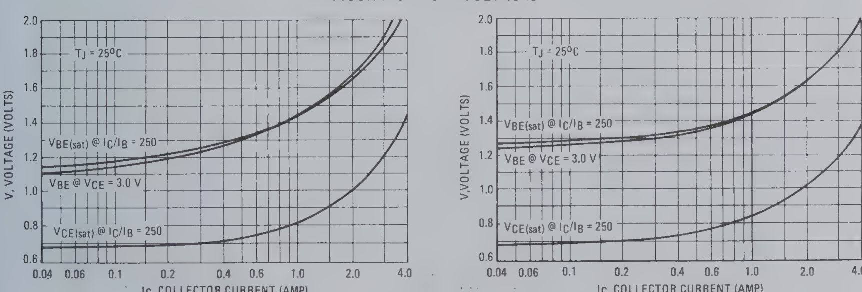


FIGURE 10 – "ON" VOLTAGES



2N6306, 2N6307, 2N6308

MOTOROLA

1.3

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

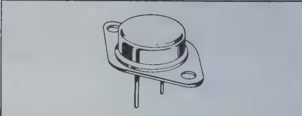
. . . designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications in associated consumer products.

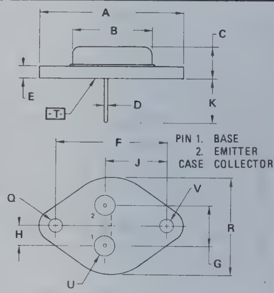
- High Collector-Base Voltage —
  V_{CB} = 500 Vdc — 2N6306
  = 600 Vdc — 2N6307
  = 700 Vdc — 2N6308
- Excellent DC Current Gain @ I_C = 3.0 Adc
  h_{FE} = 15 - 75 — 2N6306, 2N6307
  = 12 - 60 — 2N6308
- Low Collector-Emitter Saturation Voltage @ I_C = 3.0 Adc
  $V_{CE(sat)}$ = 0.8 Vdc (Max) — 2N6306
  = 1.0 Vdc (Max) — 2N6307
  = 1.5 Vdc (Max) — 2N6308
- Current Gain Bandwidth Product —
  f_T = 5.0 MHz (Min) @ I_C = 0.3 Adc

8 AMPERE POWER TRANSISTORS

NPN SILICON

250-300-350 VOLTS
125 WATTS





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [-T-] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	⌀0.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	⌀0.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

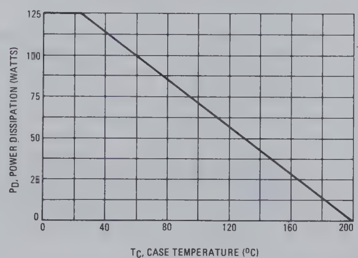
*MAXIMUM RATINGS

Rating	Symbol	2N6306	2N6307	2N6308	Unit
Collector-Base Voltage	V_{CB}	500	600	700	Vdc
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Emitter-Base Voltage	V_{EB}	← 8.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 8.0 → 16			Adc
Base Current	I_B	← 4.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 125 → 0.714			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +200 →			°C

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.4	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING



1.3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6306		250	–	
	2N6307		300	–	
	2N6308		350	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = Rated V_{CEO}, I_B = 0)			–	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 500 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6306		–	0.5	
(V_{CE} = 600 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6307		–	0.5	
(V_{CE} = 700 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6308		–	0.5	
(V_{CE} = 450 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6306		–	2.5	
(V_{CE} = 550 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6307		–	2.5	
(V_{CE} = 650 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6308		–	2.5	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 8.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	2N6306, 2N6307		15	75	
	2N6308		12	60	
(I_C = 8.0 Adc, V_{CE} = 5.0 Vdc)	2N6306, 2N6307		4.0	–	
	2N6308		3.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc)	2N6306			0.8	
	2N6307			1.0	
	2N6308			1.5	
(I_C = 8.0 Adc, I_B = 2.0 Adc)	2N6306, 2N6307		–	5.0	
(I_C = 8.0 Adc, I_B = 2.67 Adc)	2N6308		–	5.0	
Base-Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 8.0 Adc, I_B = 2.0 Adc)	2N6306, 2N6307		–	2.3	
(I_C = 8.0 Adc, I_B = 2.67 Adc)	2N6308			2.5	
Base-Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	2N6306, 2N6307		–	1.3	
	2N6308			1.5	
Second Breakdown Energy (Figure 2)		$E_{s/b}$			mJ
($I_{C(PK)}$ = 3.0 Adc, L = 40 mH, R_{BE} = 3 kΩ, V_{BB2} = 1.5 Vdc)				180	
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2)		f_T			MHz
(I_C = 0.3 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)			5.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)				250	
SWITCHING CHARACTERISTICS					
Rise Time		t_r			μs
(V_{CC} = 125 Vdc, I_C = 3.0 Adc, I_B = 0.6 Adc)				0.6	
Storage Time (3)		t_s			μs
(V_{CC} = 125 Vdc, I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc)	Pulse Width = 25 μs		–	1.6	
	Pulse Width = 5.0 μs			0.8	
Fall Time		t_f			μs
(V_{CC} = 125 Vdc, I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc)				0.4	

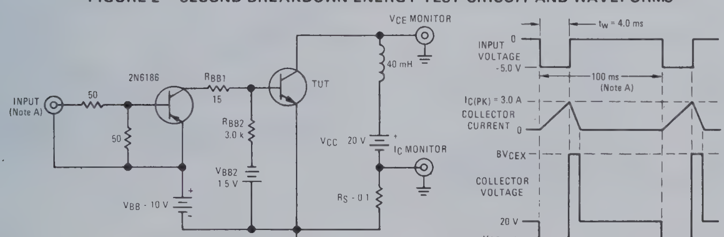
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%

(2) $f_T = |h_{fe}| \bullet f_{test}$

(3) "On" time is 25 μs. t_s decreases with shorter pulse widths, being approximately 50% of the values shown at a 5.0 μs pulse width

*Indicates JEDEC Registered Data

FIGURE 2 – SECOND BREAKDOWN ENERGY TEST CIRCUIT AND WAVEFORMS



Note A: Input pulse width is increased until $I_{C(PK)}$ = 3.0 A

FIGURE 3 – THERMAL RESPONSE

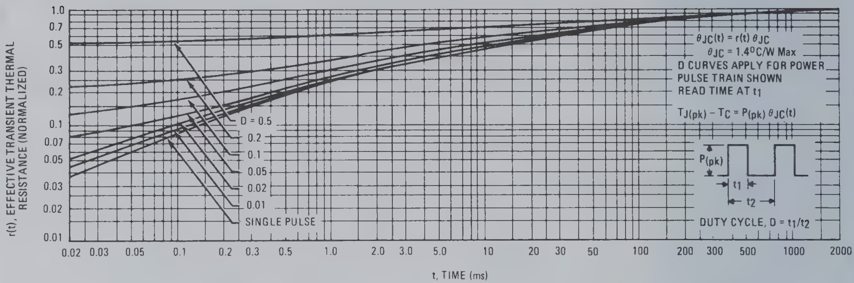
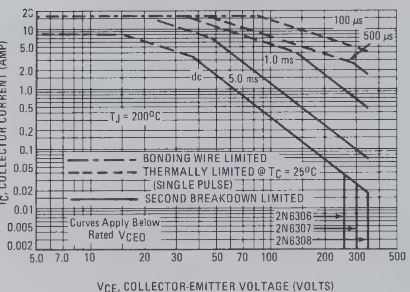


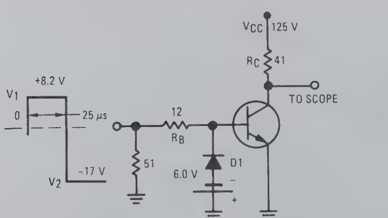
FIGURE 4 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 5 – SWITCHING TIMES TEST CIRCUIT



DUTY CYCLE 1%
t_r, $t_f \leq 10$ ns
D_1 – 1N3879
COLLECTOR-BASE JUNCTION

FOR DATA IN FIGURE 6, R_B & R_C ARE VARIED TO OBTAIN DESIRED TEST CONDITIONS. D_1 OMITTED AND V_2 REDUCED TO 5.0 V FOR t_d and t_r MEASUREMENTS

FIGURE 6 – TURN-ON AND TURN-OFF TIMES

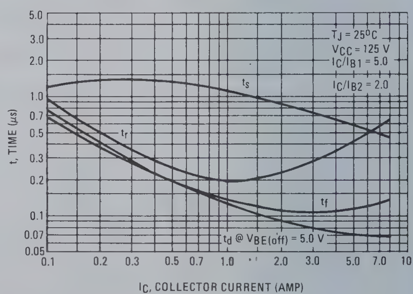


FIGURE 7 – DC CURRENT GAIN

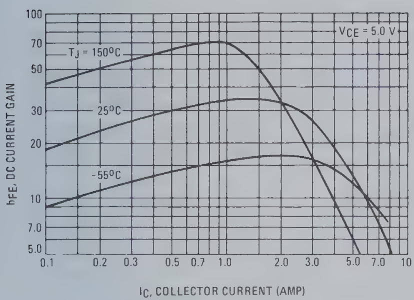


FIGURE 8 – COLLECTOR SATURATION REGION

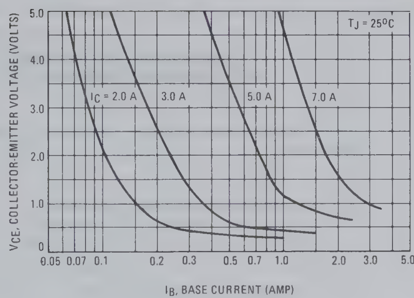


FIGURE 9 – "ON" VOLTAGES

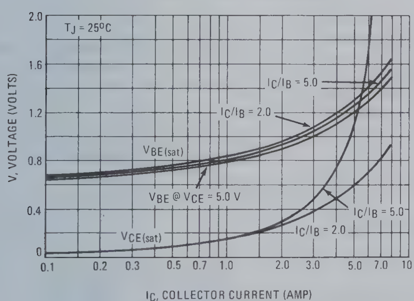


FIGURE 10 – TEMPERATURE COEFFICIENTS

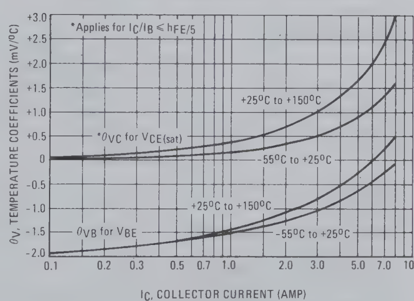


FIGURE 11 – COLLECTOR-CUTOFF REGION

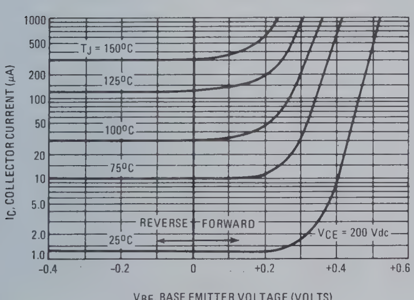
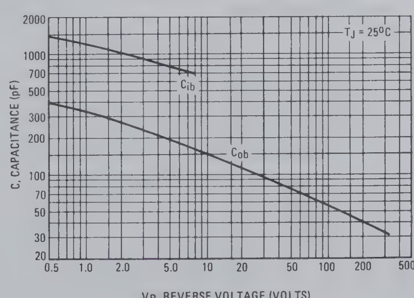


FIGURE 12 – CAPACITANCE



NPN
2N6315 2N6316
PNP
2N6317 2N6318

MOTOROLA

1.3

COMPLEMENTARY SILICON MEDIUM-POWER TRANSISTORS

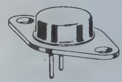
. . . designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 4.0 Adc
- Low Leakage Current — I_{CEX} = 0.25 mAdc (Max)
- Excellent DC Current Gain — h_{FE} = 20 (Min) @ I_C = 2.5 Adc
- High Current Gain — Bandwidth Product — f_T = 4.0 MHz @ I_C = 0.25 Adc

7.0 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
90 WATTS



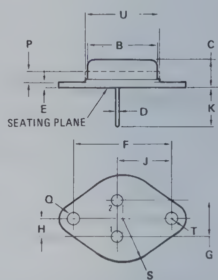
*MAXIMUM RATINGS

Rating	Symbol	2N6315 2N6317	2N6316 2N6318	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	7.0 15		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation — T_C = 25°C Derate above 25°C	P_D	90 0.515		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.94	°C/W

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.



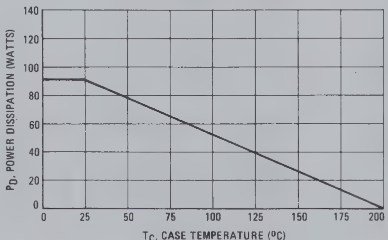
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89		0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

FIGURE 1 — POWER DERATING



Safe Area Limits are indicated by Figure 13.

1.3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	2N6315,2N6317	$V_{CEO(sus)}$	60	–	Vdc
	2N6316,2N6318		80	–	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	2N6315,2N6317	I_{CEO}	–	0.5	mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6316,2N6318		–	0.5	
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6315,2N6317	I_{CEX}	–	0.25	mAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6316,2N6318			0.25	
(V_{CE} = 60 Vdc,$V_{BE(off)}$ =1.5 Vdc,T_C =150°C)	2N6315,2N6317		–	2.0	
(V_{CE} = 80 Vdc,$V_{BE(off)}$ =1.5 Vdc,T_C =150°C)	2N6316,2N6318		–	2.0	
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)	2N6315,2N6317	I_{CBO}	–	0.25	mAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N6316,2N6318		–	0.25	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	35	–	–
(I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
Collector-Emitter Saturation Voltage (1) (I_C = 4.0 Adc, I_B = 0.4 Adc)		$V_{CE(sat)}$	–	1.0	Vdc
(I_C = 7.0 Adc, I_B = 1.75 Adc)			–	2.0	
Base-Emitter Saturation Voltage (1) (I_C = 7.0 Adc, I_B = 1.75 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2) (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N6317,2N6318	C_{ob}	–	300	pF
	2N6315,2N6316		–	200	
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.25 Adc)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

1.3

NPN	PNP
2N6315 and 2N6316	2N6317 and 2N6318

FIGURE 2 — DC CURRENT GAIN

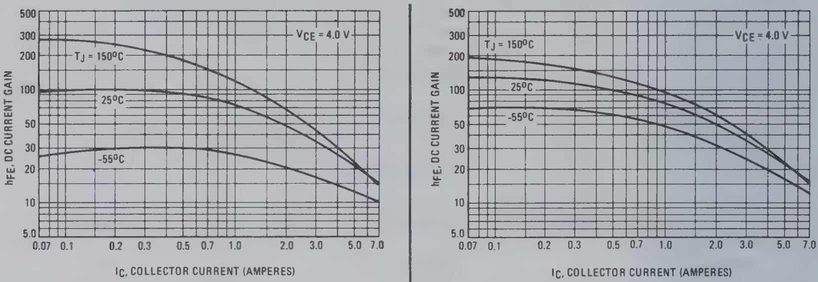


FIGURE 3 — COLLECTOR SATURATION REGION

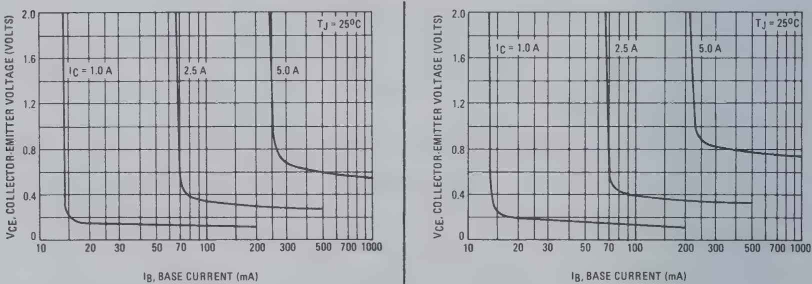


FIGURE 4 — "ON" VOLTAGES

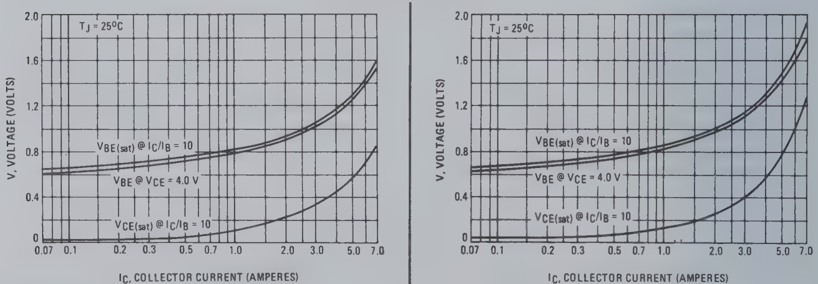
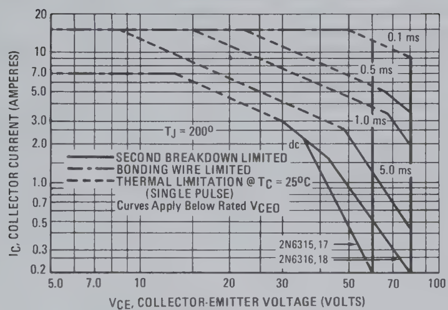


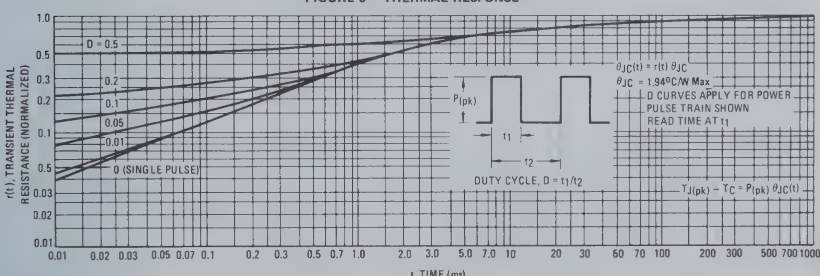
FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – THERMAL RESPONSE



2N6338
thru
2N6341

MOTOROLA

1.3

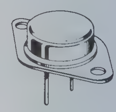
HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min) — 2N6338
  = 120 Vdc (Min) — 2N6339
  = 140 Vdc (Min) — 2N6340
  = 150 Vdc (Min) — 2N6341
- High DC Current Gain —
  h_{FE} = 30-120 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 μs (Max)
  t_s = 1.0 μs (Max)
  t_f = 0.25 μs (Max)
- Complement to 2N6436–38

25 AMPERE
POWER TRANSISTORS
NPN SILICON

100, 120, 140, 150 VOLTS
200 WATTS



*MAXIMUM RATINGS

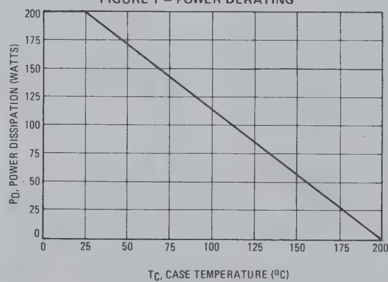
Rating	Symbol	2N6338	2N6339	2N6340	2N6341	Unit
Collector-Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter-Base Voltage	V_{EB}	6.0				Vdc
Collector Current — Continuous Peak	I_C	25 50				Adc
Base Current	I_B	10				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200				°C

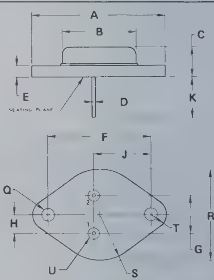
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1–04

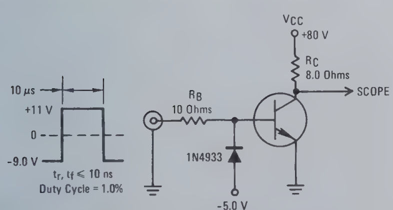
NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6338		100	–	
	2N6339		120	–	
	2N6340		140	–	
	2N6341		150	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6338			50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6339		–	50	
(V_{CE} = 70 Vdc, I_B = 0)	2N6340			50	
(V_{CE} = 75 Vdc, I_B = 0)	2N6341		–	50	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc)				10	μAdc
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)				1.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			50		
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)			30	120	
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)			12	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)				1.0	
(I_C = 25 Adc, I_B = 2.5 Adc)			–	1.8	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			–	1.8	
(I_C = 25 Adc, I_B = 2.5 Adc)				2.5	
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$		1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}		300	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 6.0 Vdc)		t_r		0.3	μs
Storage Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_s		1.0	μs
Fall Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_f	–	0.25	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 — TURN-ON TIME

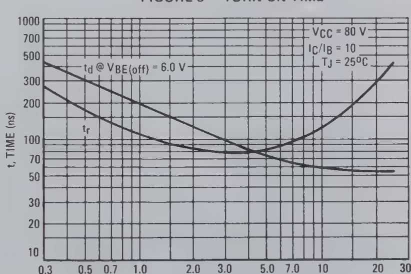


FIGURE 4 – THERMAL RESPONSE

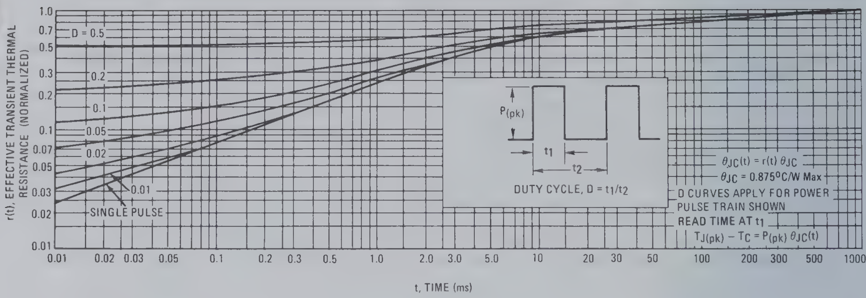
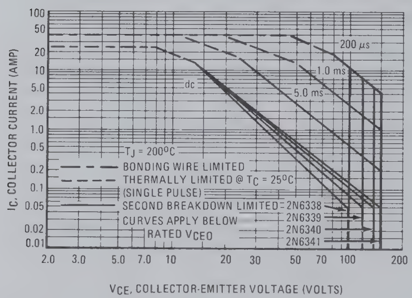


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

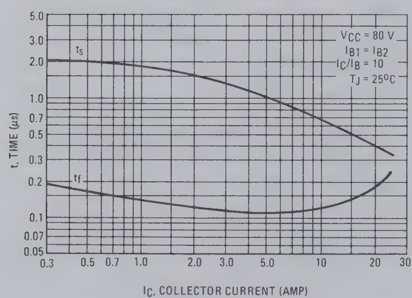
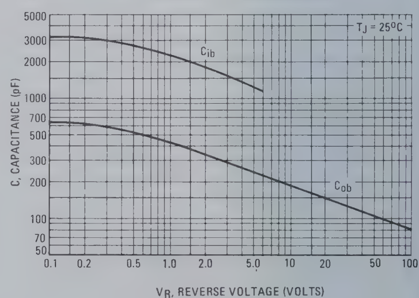


FIGURE 7 – CAPACITANCE



![MOTOROLA]

MOTOROLA

2N6377 thru 2N6379

1.3

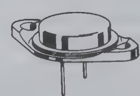
HIGH-POWER PNP SILICON TRANSISTORS

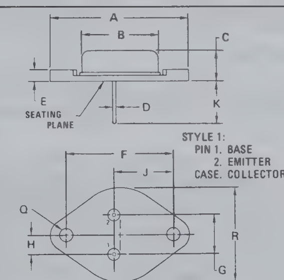
. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector Emitter Sustaining Voltage —
  $V_{CEO\,(sus)}$ = 80 Vdc (Min) — 2N6377
  = 100 Vdc (Min) — 2N6378
  = 120 Vdc (Min) — 2N6379
- High DC Current Gain —
  h_{FE} = 30-120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35 μs (Max)
  t_s = 0.8 μs (Max)
  t_f = 0.25 μs (Max)
- Complement to 2N6274–77

50 AMPERE POWER TRANSISTORS PNP SILICON

80, 100, 120 VOLTS 250 WATTS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

* MAXIMUM RATINGS

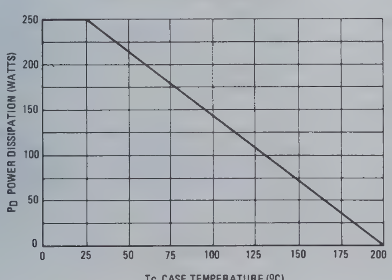
Rating	Symbol	2N6377	2N6378	2N6379	Unit
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Collector-Emitter Voltage	V_{CEO}	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 50 → ← 100 →			Adc
Base Current	I_B	← 20 →			Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	← 250 → ← 1.43 →			Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^oC/W$

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING



1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

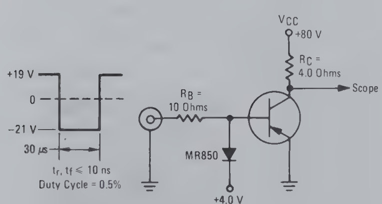
Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$			Vdc
2N6377		80	–	
2N6378		100	–	
2N6379		120	–	
Collector Cutoff Current	I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0) 2N6377		–	50	
(V_{CE} = 60 Vdc, I_B = 0) 2N6378		–	50	
(V_{CE} = 70 Vdc, I_B = 0) 2N6379		–	50	
Collector Cutoff Current	I_{CEX}			
(V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)		–	10	μAdc
(V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150^oC$)		–	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
***ON CHARACTERISTICS** (1)				
DC Current Gain	h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		50	–	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)		30	120	
(I_C = 50 Adc, V_{CE} = 4.0 Vdc)		10	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	–		Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)		–	1.2	
(I_C = 50 Adc, I_B = 10 Adc)		–	3.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)		–	1.8	
(I_C = 50 Adc, I_B = 10 Adc)		–	3.5	
DYNAMIC CHARACTERISTICS				
*Current-Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	30	–	MHz
*Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	1500	pF
***SWITCHING CHARACTERISTICS** (Figure 2)				
Rise Time	t_r	–	0.35	μs
Storage Time (V_{CC} = 80 Vdc, I_C = 20 Adc, $I_{B1} = I_{B2}$ = 2.0 Adc)	t_s	–	0.80	μs
Fall Time	t_f	–	0.25	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



Note: For information on Figures 3 & 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN ON TIME

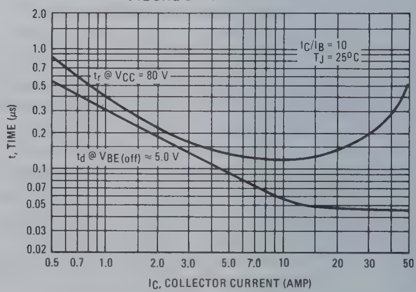


FIGURE 4 – THERMAL RESPONSE

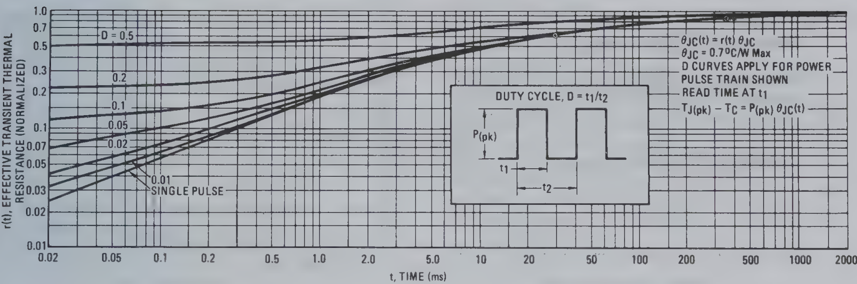
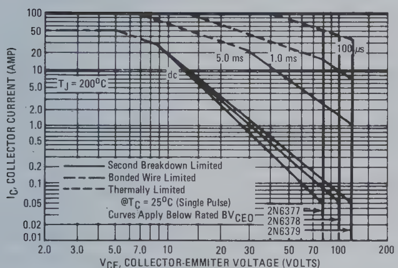


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

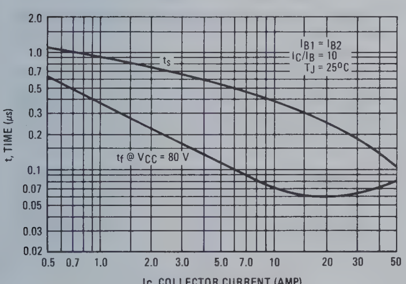
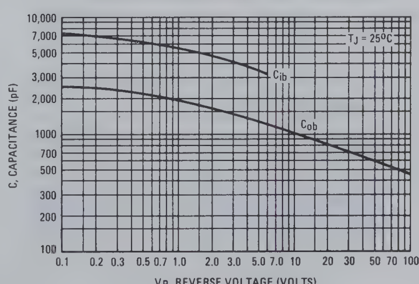


FIGURE 7 – CAPACITANCE



1.3

FIGURE 8 – DC CURRENT GAIN

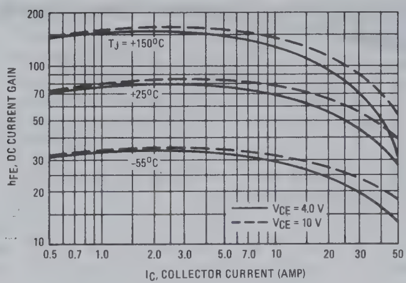


FIGURE 9 – COLLECTOR SATURATION REGION

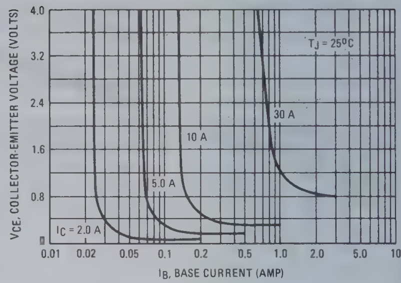


FIGURE 10 – "ON" VOLTAGES

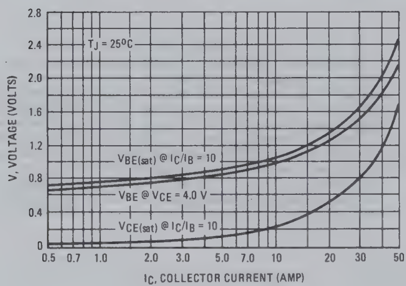


FIGURE 11 – TEMPERATURE COEFFICIENTS

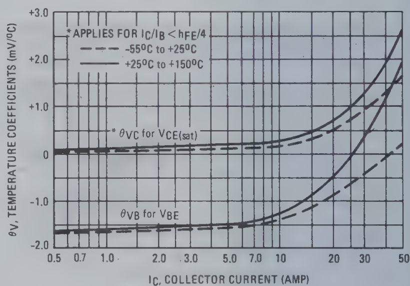


FIGURE 12 – COLLECTOR CUT-OFF REGION

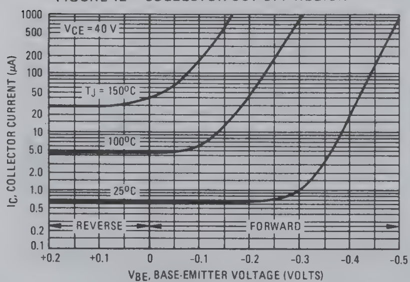
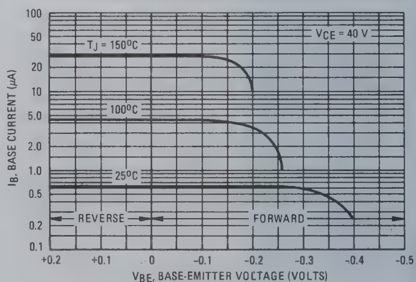


FIGURE 13 – BASE CUTOFF REGION



MOTOROLA

NPN 2N6383 2N6384 2N6385
PNP 2N6648 2N6649 2N6650

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

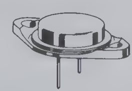
. . . monolithic complementary silicon Darlington transistors designed for low and medium frequency power applications such as power switching, audio amplifiers, hammer drivers, and shunt and series regulators.

- High Gain Darlington Performance
- True Complementary Specifications

15 AMPERE PEAK

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

40–60–80 VOLTS
100 WATTS



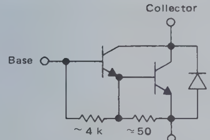
*MAXIMUM RATINGS

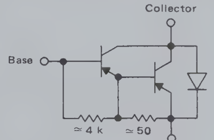
Rating	Symbol	2N6383 2N6648	2N6384 2N6649	2N6385 2N6650	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	40	60	80	Vdc
Collector-Emitter Voltage	V_{CEX}	40	60	80	Vdc
Collector-Emitter Voltage	V_{CBO}	40	60	80	Vdc
Emitter Base Voltage	V_{EBO}	← 5.0 →			Vdc
Collector Current — Continuous	I_C	← 10 →			Adc
Peak (1)**	I_{CM}	← 15 →			
Base Current — Continuous	I_B	← 0.25 →			Adc
Total Power Dissipation @ $T_C = 25°C$ (2)	P_D	← 100 →			Watts
Derate above 25°C		← 0.571 →			W/°C
Operating and Storage Junction Temperature Range (2)	T_J, T_{stg}	← −65 to +200 →			°C

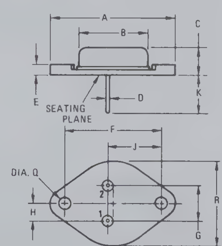
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1 75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/32″ from Case for 5 Seconds	T_L	235	°C

*Indicates JEDEC Registered Data.
**Not JEDEC Registered.
(1) Pulse Width = 50 ms, Duty Cycle ≤ 10%.
(2) Exceeds JEDEC Registration for 2N6648, 2N6649, 2N6650. JEDEC Registration gives P_D = 70 W, T_J = 150°C.







STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	-	39.37	-	1.550
B	-	21.08		0.830
C	6.35	7 62	0.250	0.300
D	0 99	1.09	0.039	0.043
E		3.43	–	0.135
F	29.90	30 40	1.177	1.197
G	10.67	11.18	0.420	0 440
H	5.33	5.59	0 210	0 220
J	16.64	17 15	0 655	0 675
K	11.18	12 19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67		1 050

Collector connected to case
CASE 11-01
(TO-3)

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N6383, 2N6648	$V_{CEO(sus)}$	40	–	Vdc
	2N6384, 2N6649		60	–	
	2N6385, 2N6650		80	–	
Collector Cutoff Current (V_{CE} = Rated Value)		I_{CEO}	–	1.0	mAdc
*Collector Cutoff Current (V_{CE} = Rated $V_{CEO(sus)}$ Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	0.3	mAdc
(V_{CE} = Rated $V_{CEO(sus)}$ Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)				3.0	
*Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}		10	mAdc
Collector-Emitter Sustaining Voltage (1) (R_{BE} = 100 Ω, I_C = 200 mA)	2N6383, 2N6648	$V_{CER(sus)}$	40	–	Vdc
	2N6384, 2N6649		60	–	
	2N6385, 2N6650		80		
Collector-Emitter Sustaining Voltage (1) ($V_{BE(off)}$ = 1.5 V, I_C = 200 mA)	2N6383, 2N6648	$V_{CEV(sus)}$	40	–	Vdc
	2N6384, 2N6649		60	–	
	2N6385, 2N6650		80	–	
ON CHARACTERISTICS (1)					
*DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	20,000	–
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)			100	–	
*Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.01 Adc)		$V_{CE(sat)}$	–	2.0	Vdc
(I_C = 10 Adc, I_B = 0.1 Adc)			–	3.0	
*Base-Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)			–	4.5	
Diode Forward Voltage (I_F = 10 Adc)		V_F	–	4.0	Vdc
***DYNAMIC CHARACTERISTICS**					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)		C_{ob}	–	200	pF
*Magnitude of Common-Emitter Small-Signal Short-Circuit Current Transfer Ratio (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	20	–	–
Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	1000	–	–
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base-Forward Biased		$I_{S/B}$	See Figures 8 and 9		
Second Breakdown Energy with Base Reverse-Biased (L = 12 mH, R_{BE} = 100 Ω, $V_{BE(off)}$ = 1.5 Vdc, I_C = 4.5 Adc)		$E_{s/b}$	120	–	mJ

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

* Indicates JEDEC Registered Data.

FIGURE 1 – DC CURRENT GAIN

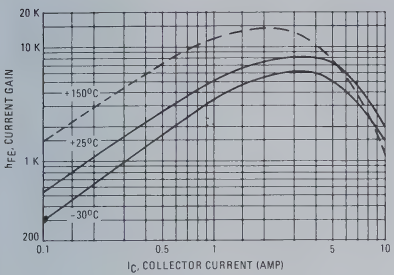


FIGURE 2 – COLLECTOR SATURATION REGION

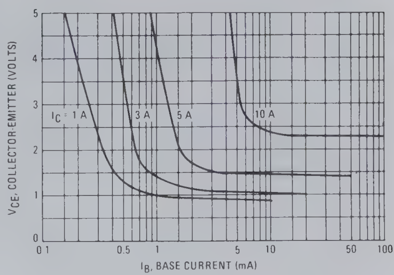


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

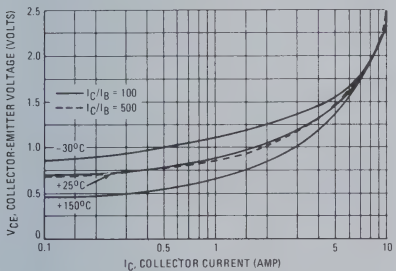


FIGURE 4 – BASE-EMITTER VOLTAGE

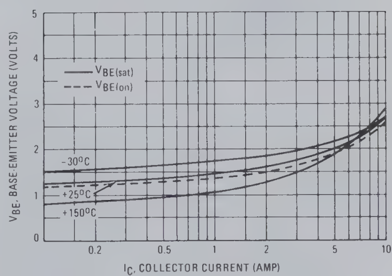


FIGURE 5 – SWITCHING TIME TEST CIRCUIT
(Shown for NPN)

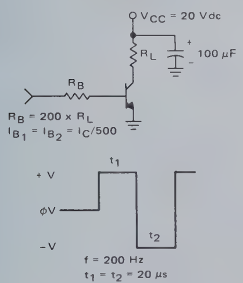
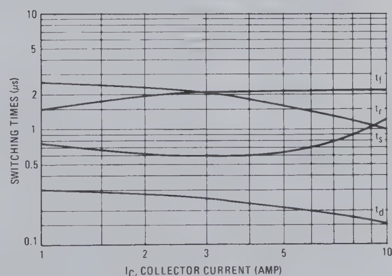
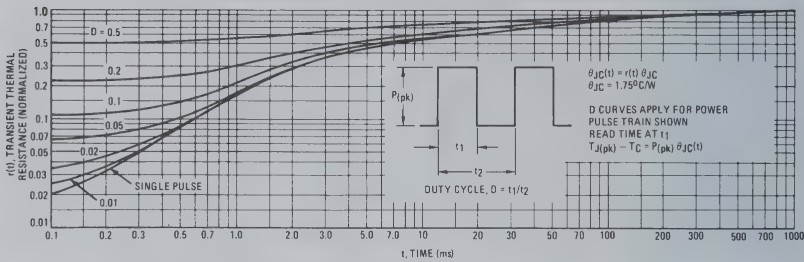


FIGURE 6 – SWITCHING TIMES



1.3

FIGURE 7 – THERMAL RESPONSE



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 8 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature.

$T_{J(pk)}$ may be calculated from the data in Figure 7. At high case temperatures, see Figure 9, thermal limitations will reduce the current that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do derate the same as thermal limitations. Allowable current at the voltages shown on Figure 8 may be found at any case temperature by derating linearly to 200°C.

FORWARD BIASED SAFE OPERATING AREA

FIGURE 8 – $T_C = 25^oC$

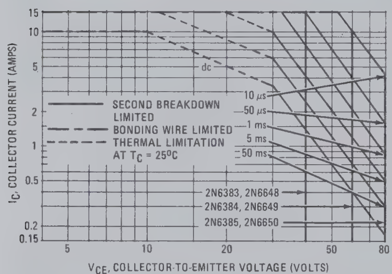


FIGURE 9 – $T_C = 100^oC$

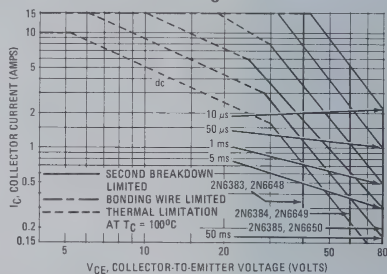
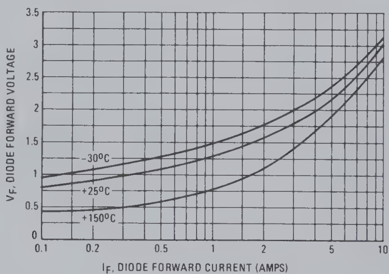


FIGURE 10 – CE DIODE CHARACTERISTICS



2N6386
2N6387
2N6388

PLASTIC MEDIUM-POWER SILICON TRANSISTORS

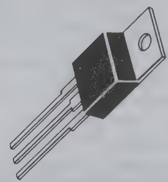
. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 40 Vdc (Min) — 2N6386
  = 60 Vdc (Min) — 2N6387
  = 80 Vdc (Min) — 2N6388
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc — 2N6386
  = 2.0 Vdc (Max) @ I_C = 5.0 Adc — 2N6387, 2N6388
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON
8 AND 10 AMPERE

NPN SILICON POWER TRANSISTORS

40-60-80 VOLTS
65 WATTS



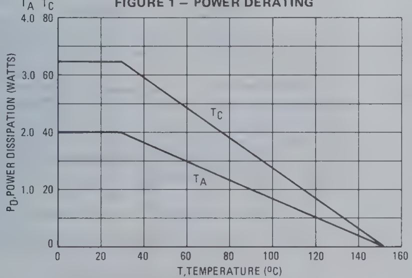
*MAXIMUM RATINGS

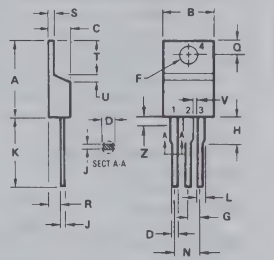
Rating	Symbol	2N6386	2N6387	2N6388	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	8.0 15	10 15	10 15	Adc
Base Current	I_B	← 250 →			mAdc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	← 65 → ← 0.52 →			Watts $W/^oC$
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	← 2.0 → ← 0.016 →			Watts $W/^oC$
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	← -65 to +150 →			^oC

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^oC/W$

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N6386	$V_{CEO(sus)}$	40	–	Vdc
	2N6387		60	–	
	2N6388		80	–	
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	2N6386	I_{CEO}	–	1.0	mAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N6387		–	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N6388		–	1.0	
Collector Cutoff Current (V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6386	I_{CEX}	–	300	µAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6387		–	300	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6388		–	300	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125^{o}C)	2N6386		–	3.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125^{o}C)	2N6387		–	3.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125^{o}C)	2N6388		–	3.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	2N6386	h_{FE}	1000	20000	–
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		1000	20000	
(I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)	2N6386		100	–	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		100	–	
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.006 Adc)	2N6386	$V_{CE(sat)}$	–	2.0	Vdc
(I_C = 5.0 Adc, I_B = 0.01 Adc)	2N6387, 2N6388		–	2.0	
(I_C = 8.0 Adc, I_B = 0.08 Adc)	2N6386		–	3.0	
(I_C = 10 Adc, I_B = 0.1 Adc)	2N6387, 2N6388		–	3.0	
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	2N6386	$V_{BE(on)}$	–	2.8	Vdc
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		–	2.8	
(I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)	2N6386		–	4.5	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		–	4.5	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)		$\|h_{fe}\|$	20	–	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	200	pF
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	1000	–	–

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

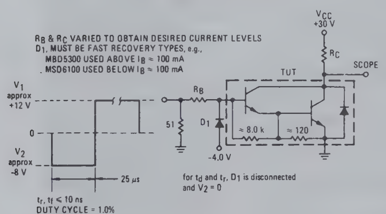


FIGURE 3 – SWITCHING TIMES

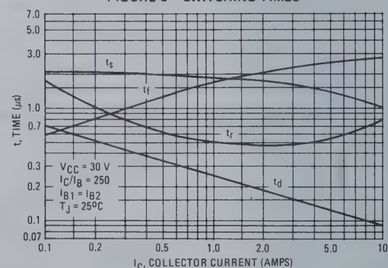


FIGURE 4 — THERMAL RESPONSE

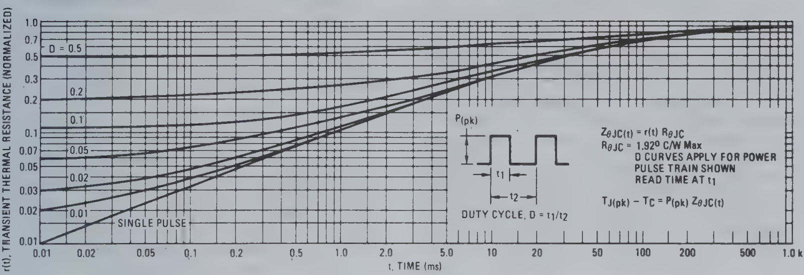
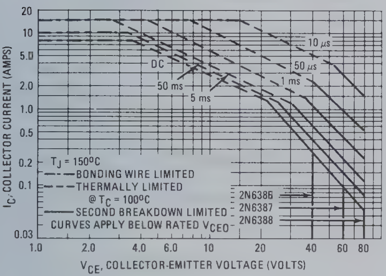


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 — SMALL-SIGNAL CURRENT GAIN

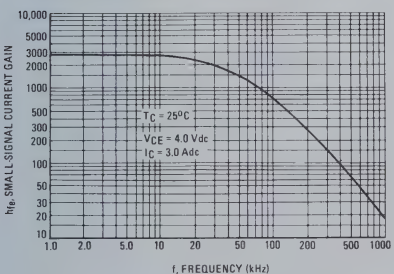
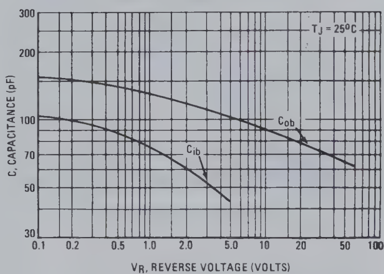


FIGURE 7 — CAPACITANCE



1.3

FIGURE 8 – DC CURRENT GAIN

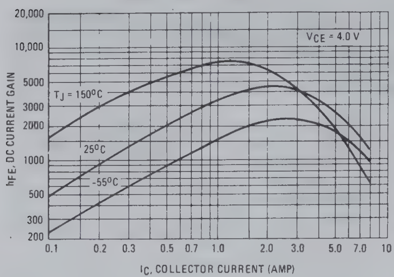


FIGURE 9 – COLLECTOR SATURATION REGION

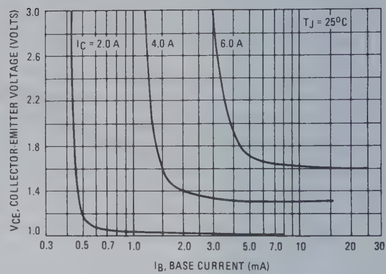


FIGURE 10 – "ON" VOLTAGES

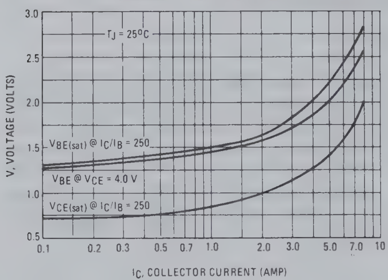


FIGURE 11 – TEMPERATURE COEFFICIENTS

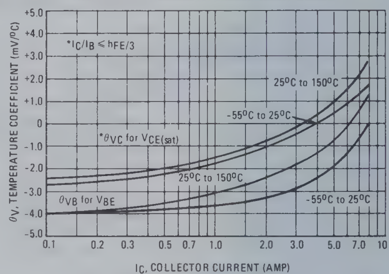


FIGURE 12 – COLLECTOR CUT-OFF REGION

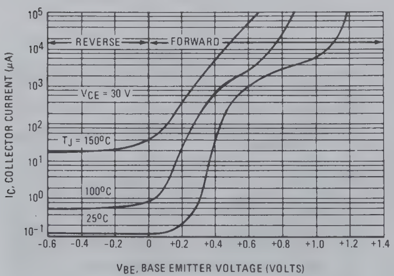
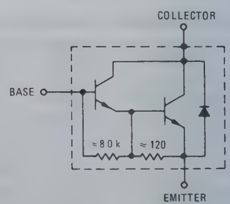


FIGURE 13 – DARLINGTON SCHEMATIC



2N6436
2N6437
2N6438

MOTOROLA

1.3

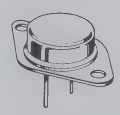
HIGH-POWER PNP SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — 2N6436
  = 100 Vdc (Min) — 2N6437
  = 120 Vdc (Min) — 2N6438
- High DC Current Gain —
  h_{FE} = 20-80 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 μs (Max)
  t_s = 1.0 μs (Max)
  t_f = 0.25 μs (Max)
- Complement to NPN 2N6338 thru 2N6341

25 AMPERE
POWER TRANSISTORS
PNP SILICON

80, 100, 120 VOLTS
200 WATTS



*MAXIMUM RATINGS

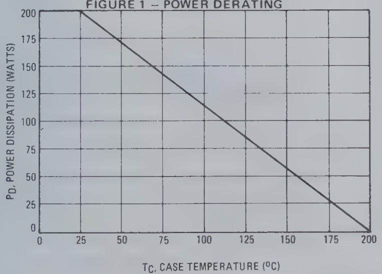
Rating	Symbol	2N6436	2N6437	2N6438	Unit
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Collector-Emitter Voltage	V_{CEO}	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous Peak	I_C	25 50			Adc
Base Current	I_B	10			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

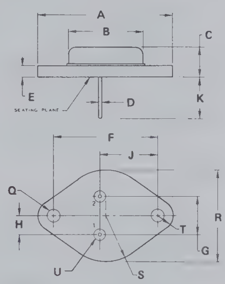
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1–04

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

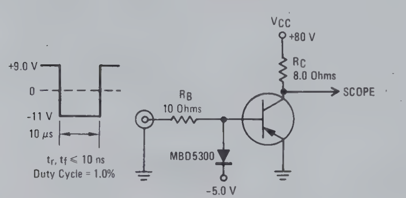
1.3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	2N6436 2N6437 2N6438	$V_{CEO(sus)}$	80 100 120	– – –	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	2N6436 2N6437 2N6438	I_{CEO}	– – –	50 50 50	μAdc
Collector Cutoff Current (V_{CE} = 90 Vdc, $V_{BE(off)}$ = −1.5 Vdc) (V_{CE} = 110 Vdc, $V_{BE(off)}$ = −1.5 Vdc) (V_{CE} = 130 Vdc, $V_{BE(off)}$ = −1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = −1.5 Vdc, T_C = 150°C) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = −1.5 Vdc, T_C = 150°C) (V_{CE} = 120 Vdc, $V_{BE(off)}$ = −1.5 Vdc, T_C = 150°C)	2N6436 2N6437 2N6438 2N6436 2N6437 2N6438	I_{CEX}	– – – – – –	10 10 10 1.0 1.0 1.0	μAdc mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 120 Vdc, I_E = 0) (V_{CB} = 140 Vdc, I_E = 0)	2N6436 2N6437 2N6438	I_{CBO}	– – –	10 10 10	μAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc) (I_C = 10 Adc, V_{CE} = 2.0 Vdc) (I_C = 25 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	30 20 12	– 80 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{CE(sat)}$	– –	1.0 1.8	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{BE(sat)}$	– –	1.8 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	–	MHz
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	700	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = 1.0 Adc)		t_r	–	0.3	μs
Storage (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = I_{B2} = 1.0 Adc)		t_s	–	1.0	μs
Fall Time (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = I_{B2} = 1.0 Adc)		t_f	–	0.25	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN-ON TIME

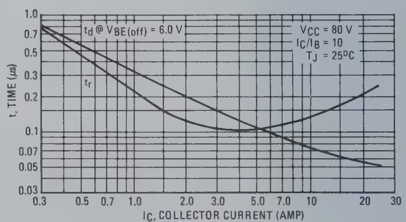


FIGURE 4 — THERMAL RESPONSE

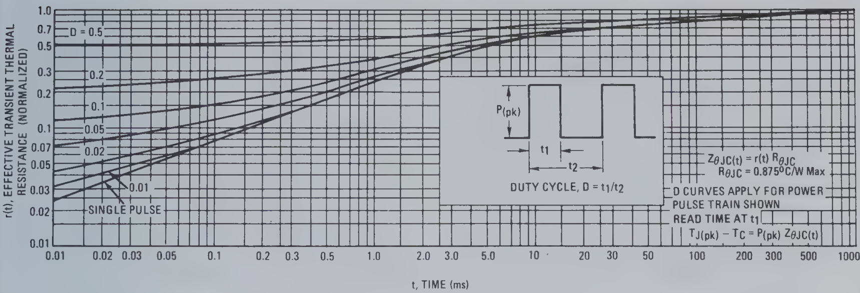
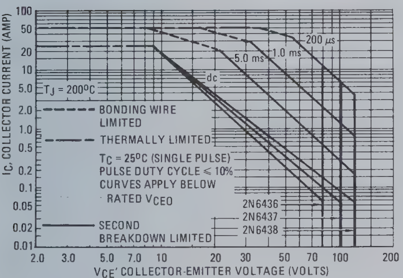


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — TURN-OFF TIME

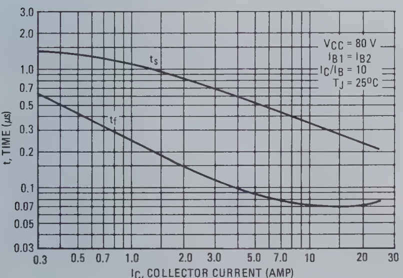
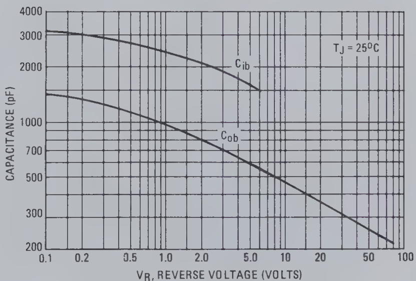


FIGURE 7 — CAPACITANCE



1.3

FIGURE 8 – DC CURRENT GAIN

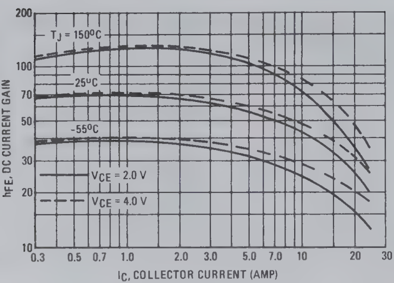


FIGURE 9 – COLLECTOR SATURATION REGION

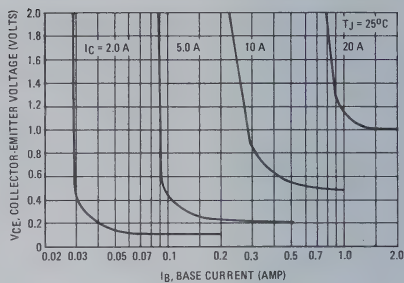


FIGURE 10 – "ON" VOLTAGE

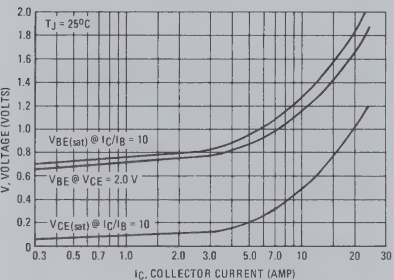


FIGURE 11 – TEMPERATURE COEFFICIENTS

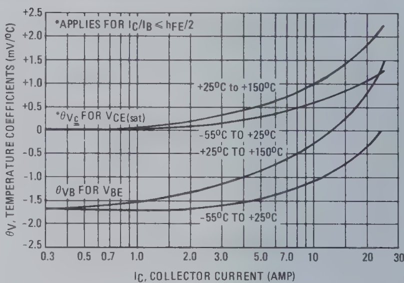


FIGURE 12 – COLLECTOR CUT-OFF REGION

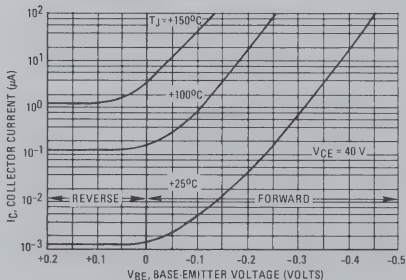
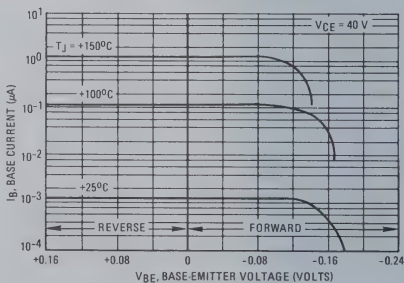


FIGURE 13 – BASE CUT-OFF REGION



2N6486 2N6487 2N6488 NPN
2N6489 2N6490 2N6491 PNP

MOTOROLA

1.3

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

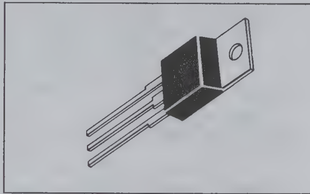
. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 15 Amperes
  h_{FE} = 20–150 @ I_C = 5.0 Adc
  = 5.0 (Min) @ I_C = 15 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO\,(sus)}$ = 40 Vdc (Min) — 2N6486, 2N6489
  = 60 Vdc (Min) — 2N6487, 2N6490
  = 80 Vdc (Min) — 2N6488, 2N6491
- High Current Gain — Bandwidth Product
  f_T = 5.0 MHz (Min) @ I_C = 1.0 Adc
- TO-220AB Compact Package
- TO-66 Leadform Also Available

15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40-60-80 VOLTS
75 WATTS



*MAXIMUM RATINGS

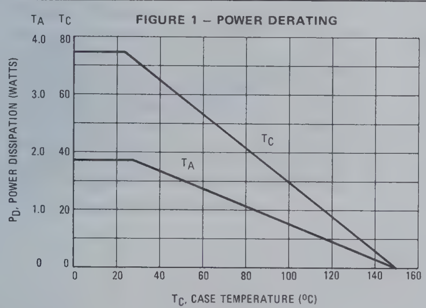
Rating	Symbol	2N6486 2N6489	2N6487 2N6490	2N6488 2N6491	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	50	70	90	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous	I_C	← 15 →			Adc
Base Current	I_B	← 5.0 →			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 75 → ← 0.6 →			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 1.8 → ← 0.014 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

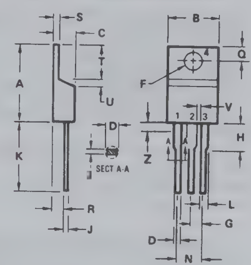
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES
1. DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

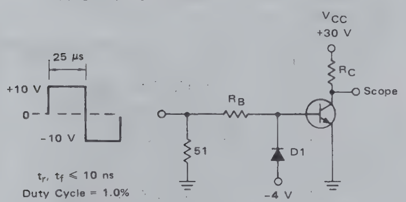
1.3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6486, 2N6489		40	–	
	2N6487, 2N6490		60	–	
	2N6488, 2N6491		80	–	
Collector-Emitter Sustaining Voltage (1)		V_{CEX}			Vdc
(I_C = 200 mAdc, V_{BE} = 1.5 Vdc)	2N6486, 2N6489		50	–	
	2N6487, 2N6490		70	–	
	2N6488, 2N6491		90	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N6486, 2N6489		–	1.0	
(V_{CE} = 30 Vdc, I_B = 0)	2N6487, 2N6490		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6488, 2N6491		–	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6486, 2N6489		–	500	
(V_{CE} = 65 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6487, 2N6490		–	500	
(V_{CE} = 85 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6488, 2N6491		–	500	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6486, 2N6489		–	5.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6487, 2N6490		–	5.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6488, 2N6491		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			20	150	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)			–	1.3	
(I_C = 15 Adc, I_B = 5.0 Adc)			–	3.5	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			–	1.3	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			–	3.5	
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)		f_T	5.0	–	MHz
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

*Indicates JEDEC Registered Data.
(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2)$f_T = |h_{fe}| \bullet f_{test}$.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



R_B and R_C varied to obtain desired current levels.
For PNP reverse all polarities.

D1 must be fast recovery type, e.g.;
MBD5300 used above $I_B \approx$ 100 mA
MSD6100 used below $I_B \approx$ 100 mA

FIGURE 3 — TURN-ON TIME

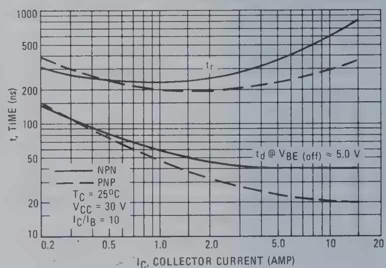


FIGURE 4 – THERMAL RESPONSE

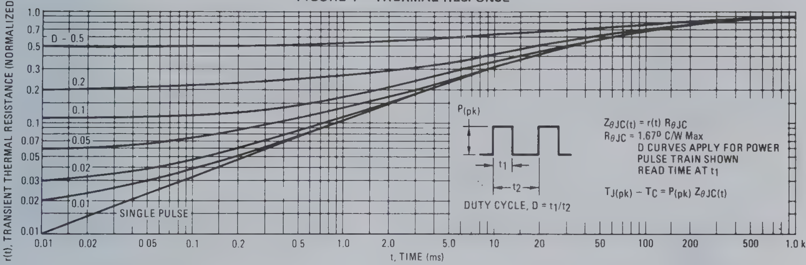
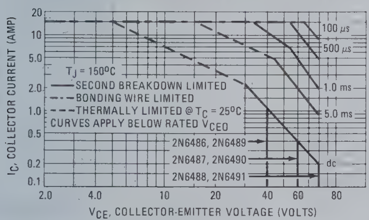


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – TURN-OFF TIME

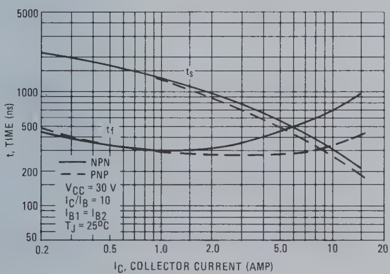
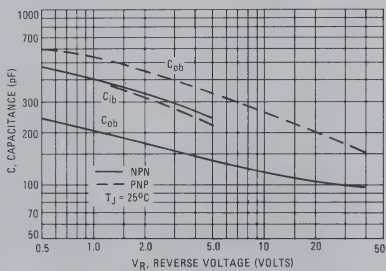


FIGURE 7 – CAPACITANCES



NPN
2N6486, 2N6487, 2N6488

PNP
2N6489, 2N6490, 2N6491

FIGURE 8 – DC CURRENT GAIN

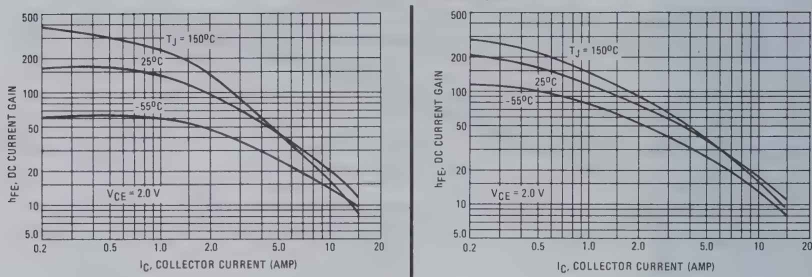


FIGURE 9 – COLLECTOR SATURATION REGION

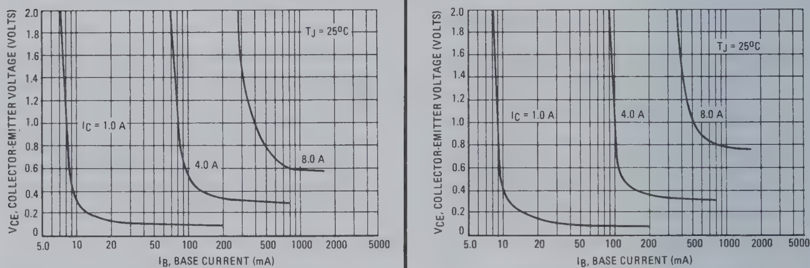
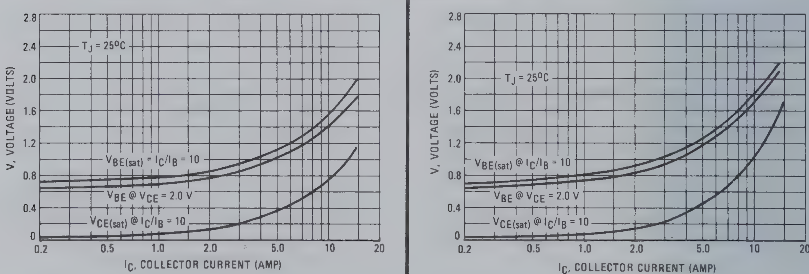


FIGURE 10 – "ON" VOLTAGES



MOTOROLA

2N6497
2N6498
2N6499

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

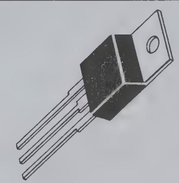
· · · designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications.

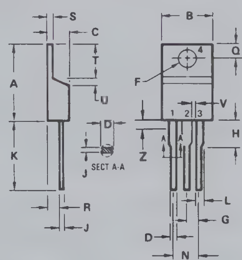
- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 250 Vdc (Min) — 2N6497
  = 300 Vdc (Min) — 2N6498
  = 350 Vdc (Min) — 2N6499
- Excellent DC Current Gain —
  h_{FE} = 10 – 75 @ I_C = 2.5 Adc
- Low Collector-Emitter Saturation Voltage @ I_C = 2.5 Adc —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) — 2N6497
  = 1.25 Vdc (Max) — 2N6498
  = 1.5 Vdc (Max) — 2N6499

5 AMPERE POWER TRANSISTORS

NPN SILICON

250, 300, 350 VOLTS
80 WATTS





STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

*MAXIMUM RATINGS

Rating	Symbol	2N6497	2N6498	2N6499	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector-Base Voltage	V_{CB}	350	400	450	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current — Continuous — Peak	I_C	← 5.0 → ← 10 →			Adc
Base Current	I_B	← 2.0 →			Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	← 80 → ← 0.64 →			Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	$^oC/W$

*Indicates JEDEC Registered Data.

1.3

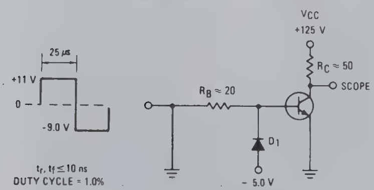
***ELECTRICAL CHARACTERISTICS** ($T_C = 25^oC$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$				Vdc
(I_C = 25 mAdc, I_B = 0)	2N6497		250	–	–	
	2N6498		300	–	–	
	2N6499		350	–	–	
Collector Cutoff Current		I_{CEX}				mAdc
(V_{CE} = 350 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6497		–	–	1.0	
(V_{CE} = 400 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6498		–	–	1.0	
(V_{CE} = 450 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6499		–	–	1.0	
(V_{CE} = 175 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 100^oC$)	2N6497		–	–	10	
(V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 100^oC$)	2N6498		–	–	10	
(V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 100^oC$)	2N6499		–	–	10	
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				–
(I_C = 2.5 Adc, V_{CE} = 10 Vdc)			10	–	75	
(I_C = 5.0 Adc, V_{CE} = 10 Vdc)			3.0	–	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 500 mAdc)	2N6497		–	–	1.0	
	2N6498		–	–	1.25	
	2N6499		–	–	1.5	
(I_C = 5.0 Adc, I_B = 2.0 Adc)	All Devices		–	–	5.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 500 mAdc)			–	–	1.5	
(I_C = 5.0 Adc, I_B = 2.0 Adc)			–	–	2.5	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	5.0	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	–	150	pF
SWITCHING CHARACTERISTICS						
Rise Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = 0.5 Adc)		t_r	–	0.4	1.0	µs
Storage Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, V_{BE} = 5.0 Vdc, $I_{B1} = I_{B2}$ = 0.5 Adc)		t_s	–	1.4	2.5	µs
Fall Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, $I_{B1} = I_{B2}$ = 0.5 Adc)		t_f	–	0.45	1.0	µs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE IB ≈100 mA
MSD6100 USED BELOW IB ≈100 mA

FIGURE 2 — TURN-ON TIME

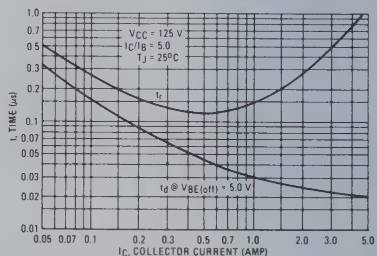


FIGURE 3 – THERMAL RESPONSE

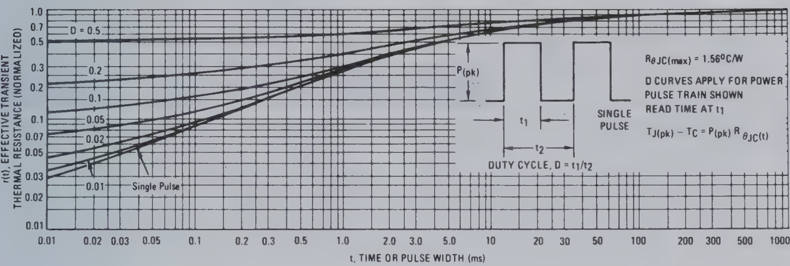
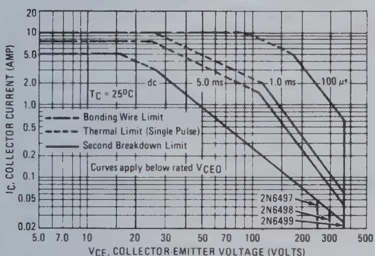


FIGURE 4 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 4 may be found at any case temperature by using the appropriate curve on Figure 6.

FIGURE 5 – TURN-OFF TIME

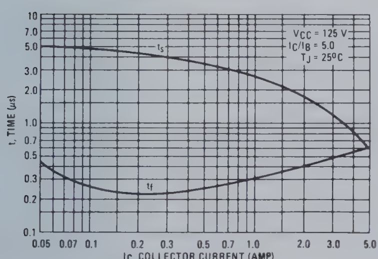
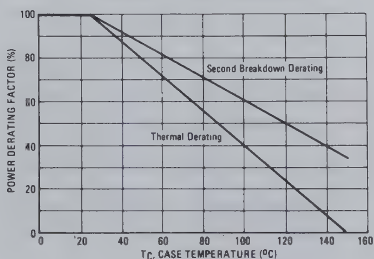


FIGURE 6 – POWER DERATING



1.3

FIGURE 7 – DC CURRENT GAIN

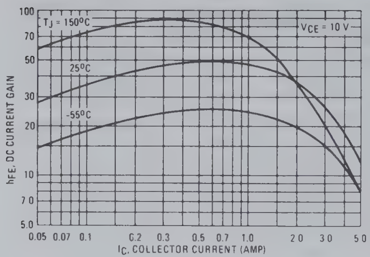


FIGURE 8 – COLLECTOR SATURATION REGION

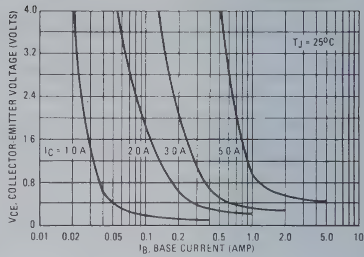


FIGURE 9 – "ON" VOLTAGES

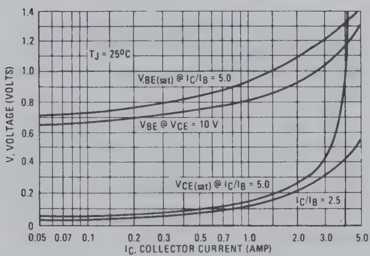


FIGURE 10 – TEMPERATURE COEFFICIENTS

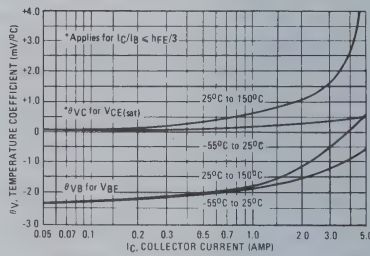


FIGURE 11 – COLLECTOR CUTOFF REGION

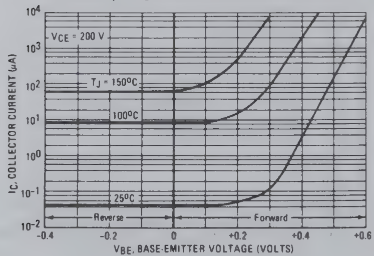
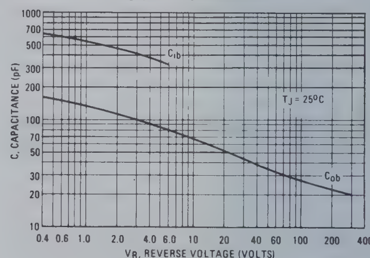


FIGURE 12 – CAPACITANCE



MOTOROLA

2N6542
2N6543

1.3

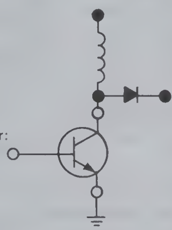
Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

These devices are designed for high-voltage, high-speed, power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated SWITCHMODE applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features —
High Temperature Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

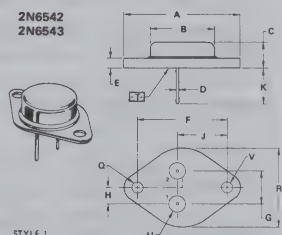


5 AMPERE
NPN SILICON POWER TRANSISTORS
300 and 400 VOLTS
100 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

2N6542
2N6543



STYLE 1
PIN 1. BASE
2 EMITTER
CASE COLLECTOR

NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	∅.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	∅.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0 300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

*MAXIMUM RATINGS

Rating	Symbol	2N6542	2N6543	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	350	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	850	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 10		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	5.0 10		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	10 20		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	100 57.2 0.57		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

1.3

*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	MJ4400 MJ4401	$V_{CEO(sus)}$	300 400	– –	Vdc
Collector-Emitter Sustaining Voltage (Table 2, Figure 12) (I_C = 2.6 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) (I_C = 5.0 Adc, V_{clamp} = Rated V_{CEO} −100 V, T_C = 100°C)	MJ4400 MJ4401 MJ4400 MJ4401	$V_{CEX(sus)}$	350 450 200 300	– – – –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	– –	0.5 3.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 8.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)		$I_{S/b}$	0.2 (See Figure 11)	–	Adc
Clamped Inductive SOA with base reverse biased		RBSOA	(See Figure 12)		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	12 7.0	60 35	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		$V_{CE(sat)}$	– – –	1.0 5.0 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		$V_{BE(sat)}$	– –	1.4 1.4	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	6.0	28	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)		C_{ob}	50	200	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 2)					
Delay Time	(V_{CC} = 250 Vdc, I_C = 3.0 A, I_{B1} = I_{B2} = 0.6 A, t_p = 100 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.05	μs
Rise Time		t_r	–	0.7	μs
Storage Time		t_s	–	4.0	μs
Fall Time		t_f	–	0.8	μs
Inductive Load, Clamped (Table 2)		Symbol	Typ	Max	Unit
Storage Time	(I_C = 3.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 0.6 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_{sv}	–	4.0	μs
Crossover Time		t_c	0.6	–	μs
Fall Time		t_{fi}	–	0.8	μs
Storage Time	(I_C = 3.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 0.6 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_{sv}	0.8	–	μs
Crossover Time		t_c	0.3	–	μs
Fall Time		t_{fi}	0.2	–	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

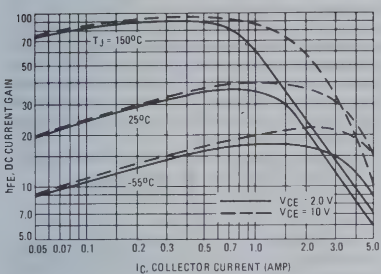


FIGURE 2 – COLLECTOR SATURATION REGION

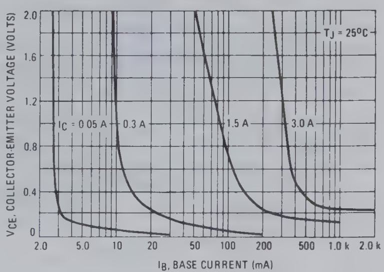


FIGURE 3 – "ON" VOLTAGE

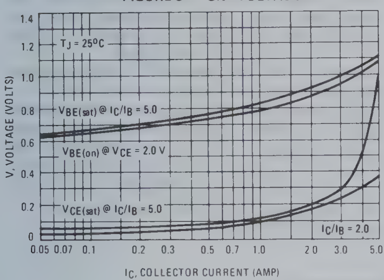


FIGURE 4 – TEMPERATURE COEFFICIENTS

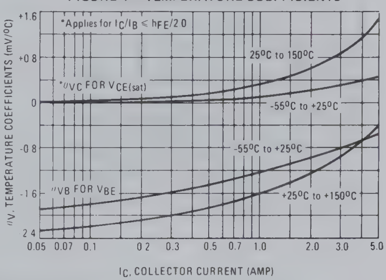


FIGURE 5 – COLLECTOR CUTOFF REGION

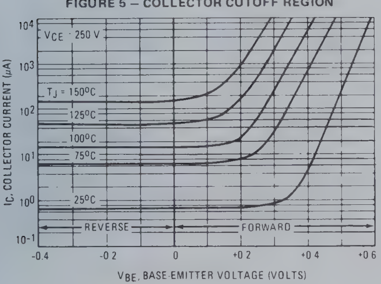


FIGURE 6 – CAPACITANCE

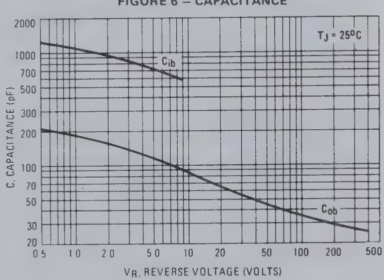


FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

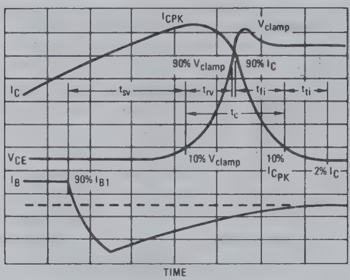


TABLE 1 — INDUCTIVE SWITCHING PERFORMANCE

I_C (A)	T_C ^oC	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
1.0	25	0.70	0.22	0.21	0.23	0.66
	100	1.20	0.37	0.19	0.39	0.95
3.0	25	1.10	0.09	0.12	0.08	0.29
	100	1.60	0.42	0.19	0.40	1.01
5.0	25	1.10	0.16	0.19	0.11	0.46
	100	1.70	0.45	0.37	0.26	1.08

Note: All Data Recorded in the Inductive Switching Circuit Shown in Table 2.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

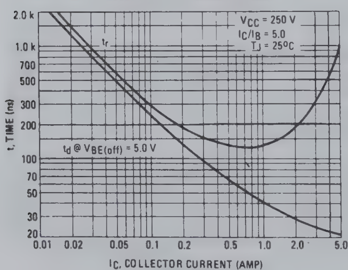


FIGURE 9 — TURN-OFF TIME

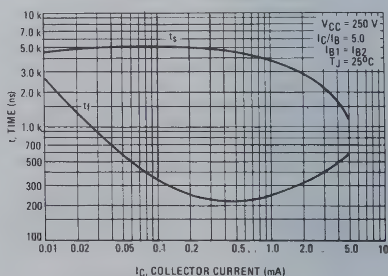


TABLE 2 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

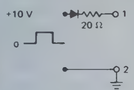
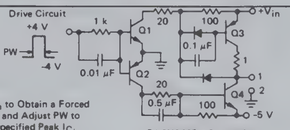
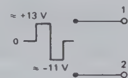
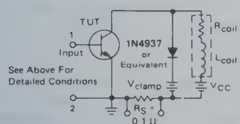
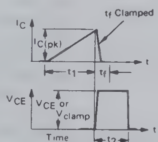
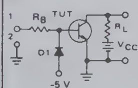
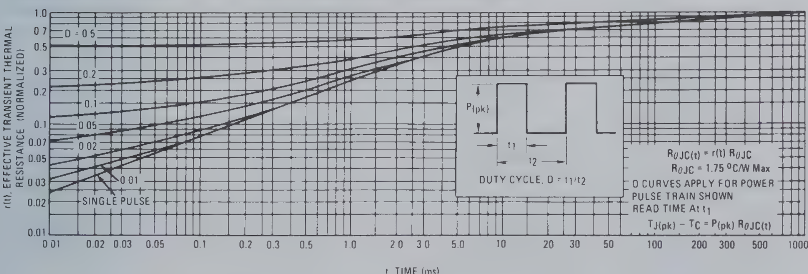
	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Set $+V_{in}$ to Obtain a Forced h_{FE} = 5 and Adjust PW to Attain Specified Peak I_C. Duty Cycle ≤ 3% f = 1 kHz	Q1 2N6408 Q3 2N5875 Q2 2N6406 Q4 2N5877 Diodes 1N4933	 I_C = 3A PW ≈ 100 μs t_r ≤ 5 ns t_f ≤ 50 ns Duty Cycle ≤ 2%
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} (Unclamped)	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V	V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 83 Ω D1 = 1N5820 or Equiv. R_B = 20 Ω
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS 	t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope-Tektronics 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 10 – THERMAL RESPONSE



1.3

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATING AREA

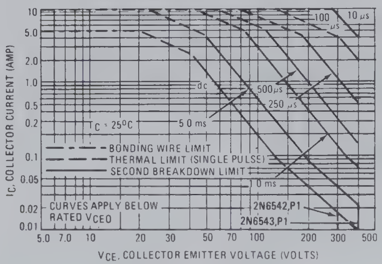


FIGURE 12 — REVERSE BIAS SAFE OPERATING AREA

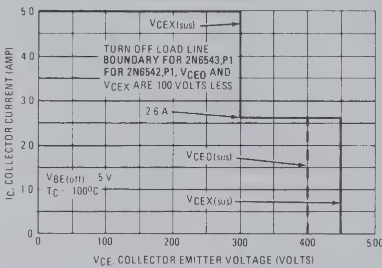
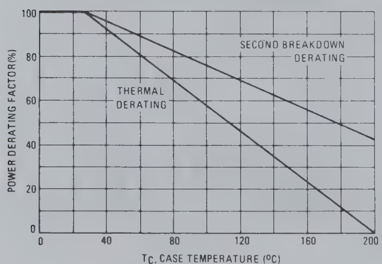


FIGURE 13 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.

MOTOROLA

2N6544
2N6545

1.3

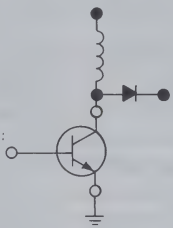
Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The 2N6544 and 2N6545 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features —
- High Temperature Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



8 AMPERE
NPN SILICON
POWER TRANSISTORS

300 and 400 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

*MAXIMUM RATINGS

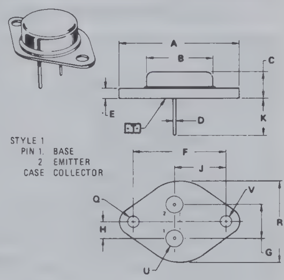
Rating	Symbol	2N6544	2N6545	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	350	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	850	Vdc
Emitter Base Voltage	V_{EB}	9.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8.0 16		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	8.0 16		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	16 32		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	125 71.5 0.714		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

⌖	∅.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS

⌖	∅.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B		21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

1.3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 100 mA, I_B = 0)	2N6544 2N6545	$V_{CEO(sus)}$	300 400	– –	Vdc
Collector-Emitter Sustaining Voltage (I_C = 4.5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) (I_C = 8.0 A, V_{clamp} = Rated V_{CEO} −100 V, T_C = 100°C)	2N6544 2N6545 2N6544 2N6545	$V_{CEX(sus)}$	350 450 200 300	– – – –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	– –	0.5 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)		$I_{S/b}$	0.2	–	Adc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	12 7.0	60 35	–
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 8.0 Adc, I_B = 2.0 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	– – –	1.5 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{BE(sat)}$	– –	1.6 1.6	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 300 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	6.0	28	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)		C_{ob}	75	300	pF
SWITCHING CHARACTERISTICS					
Resistive Load					
Delay Time	(V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = I_{B2} = 1.0 A, t_p = 100 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.05	μs
Rise Time		t_r	–	1.0	μs
Storage Time		t_s	–	4.0	μs
Fall Time		t_f	–	1.0	μs
Inductive Load, Clamped					
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_s	–	4.0	μs
Fall Time		t_f	–	0.9	μs
			Typical		
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_s	1.2		μs
Fall Time		t_f	0.18		μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

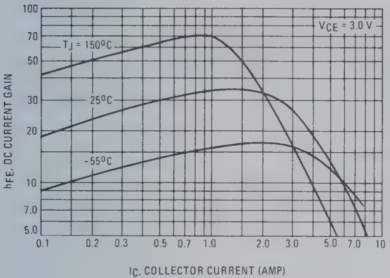


FIGURE 2 – COLLECTOR SATURATION REGION

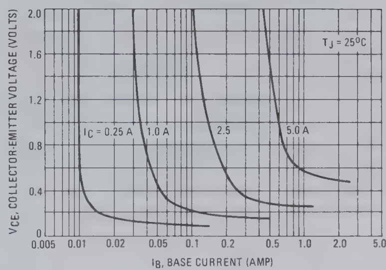


FIGURE 3 – "ON" VOLTAGE

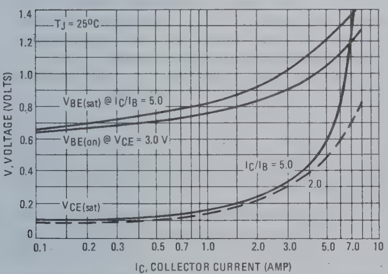


FIGURE 4 – TEMPERATURE COEFFICIENTS

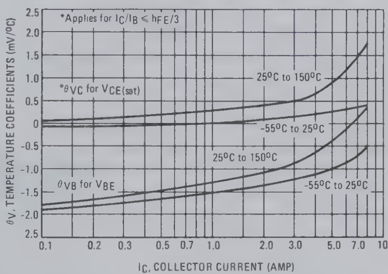


FIGURE 5 – TURN-ON TIME

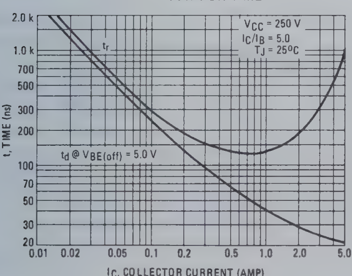
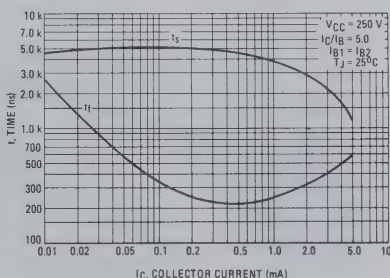


FIGURE 6 – TURN-OFF TIME



1.3

FIGURE 7 — FORWARD BIAS SAFE OPERATING AREA

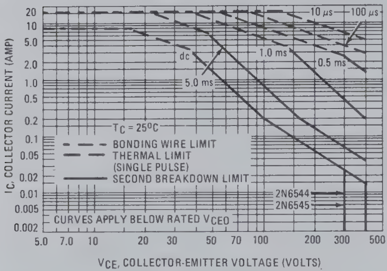


FIGURE 8 — REVERSE BIAS SAFE OPERATING AREA

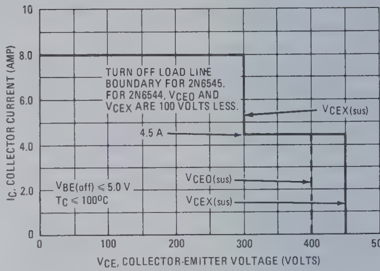
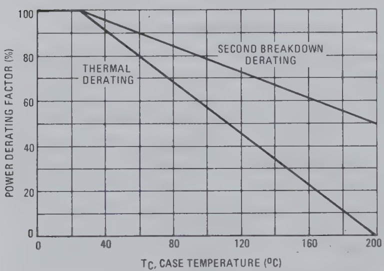


FIGURE 9 — POWER DERATING

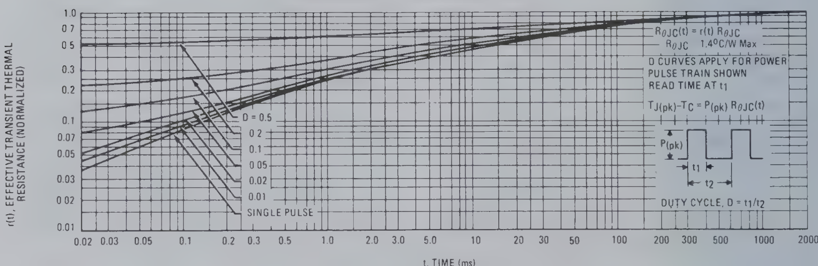


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. The reverse biased safe operating area (Figure 8) is the boundary the load line may traverse during turn-off.

FIGURE 10 — THERMAL RESPONSE



MOTOROLA

2N6546
2N6547

1.3

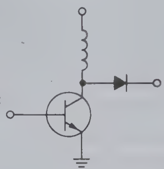
Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The 2N6546 and 2N6547 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features —
High Temperature Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



15 AMPERE
NPN SILICON
POWER TRANSISTORS

300 and 400 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

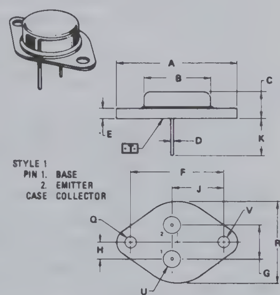
*MAXIMUM RATINGS

Rating	Symbol	2N6546	2N6547	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	350	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	850	Vdc
Emitter Base Voltage	V_{EB}	9.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 30		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 20		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	25 50		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	175 100 1.0		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. T IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

⌖	∅.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS

⌖	∅.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0 055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5 46 BSC		0.215 BSC	
J	16 89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0 190	0.210
V	3.81	4.19	0.150	0 165

CASE 1-05
TO-204AA

1.3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 100 mA, I_B = 0)	2N6546 2N6547	$V_{CEO(sus)}$	300 400	– –	Vdc
Collector-Emitter Sustaining Voltage (I_C = 8.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	2N6546 2N6547	$V_{CEX(sus)}$	350 450	– –	Vdc
(I_C = 15 A, V_{clamp} = Rated V_{CEO} – 100 V, T_C = 100°C)	2N6546 2N6547		200 300	– –	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	– –	1.0 4.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)		$I_{S/b}$	0.2	–	Adc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 10 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	12 6.0	60 30	–
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) (I_C = 15 Adc, I_B = 3.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	– – –	1.5 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C		$V_{BE(sat)}$	– –	1.6 1.6	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	6.0	28	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)		C_{ob}	125	500	pF
SWITCHING CHARACTERISTICS					
Resistive Load					
Delay Time	(V_{CC} = 250 V, I_C = 10 A, I_{B1} = I_{B2} = 2.0 A, t_p = 100 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.05	μs
Rise Time		t_r	–	1.0	μs
Storage Time		t_s	–	4.0	μs
Fall Time		t_f	–	0.7	μs
Inductive Load, Clamped					
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_s	–	5.0	μs
Fall Time		t_f	–	1.5	μs
			Typical		
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_s	2.0		μs
Fall Time		t_f	0.09		μs

*Indicates JEDEC Registered Data.
(1) Puse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

1.3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

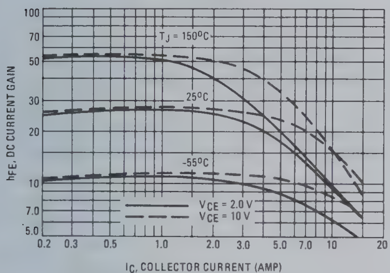


FIGURE 2 — COLLECTOR SATURATION REGION

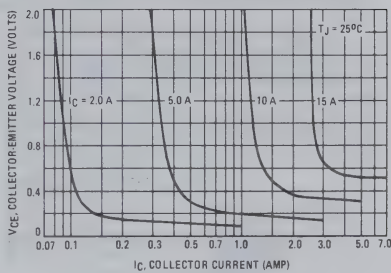


FIGURE 3 — "ON" VOLTAGE

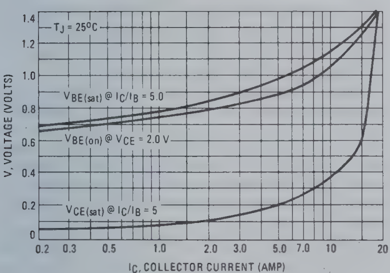


FIGURE 4 — TEMPERATURE COEFFICIENTS

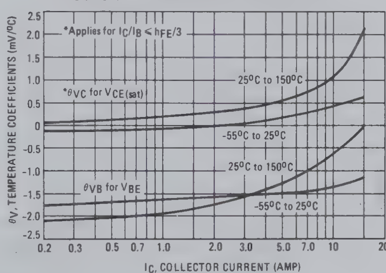


FIGURE 5 — TURN-ON TIME

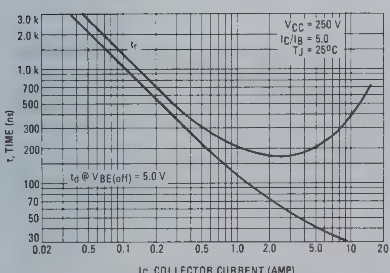
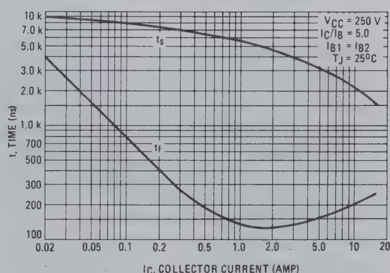


FIGURE 6 — TURN-OFF TIME



MAXIMUM RATED SAFE OPERATING AREAS

FIGURE 7 — FORWARD BIAS SAFE OPERATING AREA

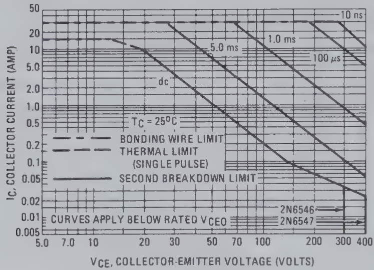


FIGURE 8 — REVERSE BIAS SAFE OPERATING AREA

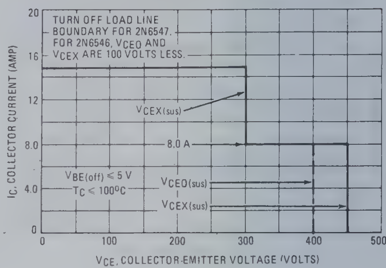
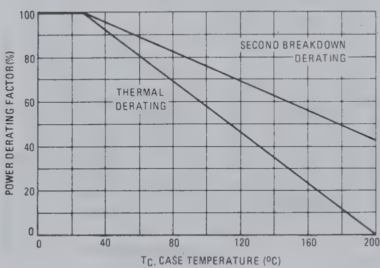


FIGURE 9 — POWER DERATING

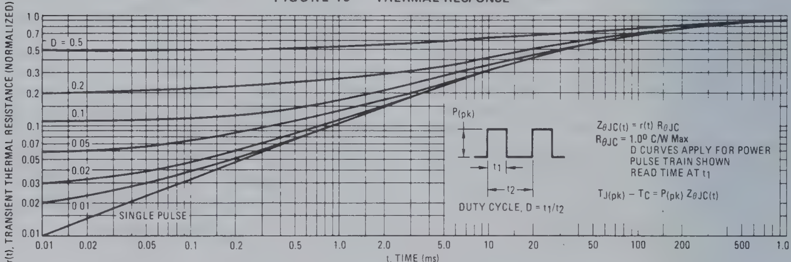


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 10 — THERMAL RESPONSE



MOTOROLA

2N6548
2N6549

1.3

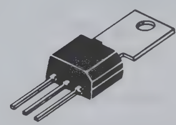
NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for amplifier and driver applications where high gain is an essential requirement, low power lamp and relay drivers and power drivers for high-current applications such as voltage regulators.

- High DC Current Gain —
  h_{FE} = 25,000 (Min) @ I_C = 200 mAdc — 2N6548
  = 15,000 (Min) @ I_C = 500 mAdc — 2N6548
- Collector-Emitter Breakdown Voltage —
  BV_{CES} = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 1.0 Adc
- Duowatt Package —
  2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS



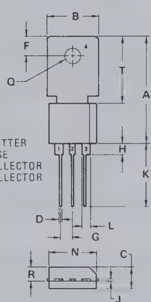
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
*Collector-Base Voltage	V_{CBO}	50	Vdc
*Emitter-Base Voltage	V_{EBO}	12	Vdc
*Collector Current — Continuous	I_C	2.0	Adc
*Base Current — Continuous	I_B	100	mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C
*Solder Temperature, 1/16″ from Case for 10 Seconds	—	260	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.



STYLE 1.
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	-
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-04
TO-202AC

1.3

***ELECTRICAL CHARACTERISTICS** ($T_A = 25^oC$ unless otherwise noted.)

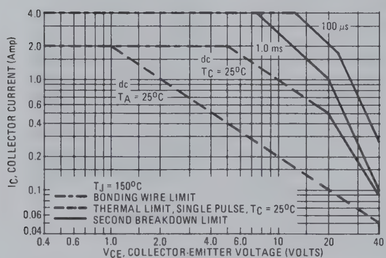
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage(1) ($I_C = 100\ \mu Adc$, $V_{BE} = 0$)	BV_{CES}	40	–	Vdc
Collector-Base Breakdown Voltage ($I_C = 100\ \mu Adc$, $I_E = 0$)	BV_{CBO}	50	–	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\ \mu Adc$, $I_C = 0$)	BV_{EBO}	12	–	Vdc
Collector Cutoff Current ($V_{CB} = 30$ Vdc, $I_E = 0$)	I_{CBO}	–	100	nAdc
Emitter Cutoff Current ($V_{EB} = 10$ Vdc, $I_C = 0$)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
($I_C = 200$ mAdc, $V_{CE} = 5.0$ Vdc) 2N6548		25,000	150,000	
2N6549		15,000	150,000	
($I_C = 500$ mAdc, $V_{CE} = 5.0$ Vdc) 2N6548		15,000	–	
2N6549		10,000	–	
($I_C = 1.0$ Adc, $V_{CE} = 5.0$ Vdc) 2N6548		5,000	–	
2N6549		3,000	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
($I_C = 1.0$ Adc, $I_B = 2.0$ mAdc)		–	1.5	
($I_C = 2.0$ Adc, $I_B = 4.0$ mAdc)		–	2.0	
Base-Emitter Saturation Voltage ($I_C = 1.0$ Adc, $I_B = 2.0$ mAdc)	$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter On Voltage ($I_C = 1.0$ Adc, $V_{CE} = 5.0$ Vdc)	$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS				
High Frequency Current Gain ($I_C = 200$ mAdc, $V_{CE} = 5.0$ Vdc, f = 100 MHz)	$\|h_{fe}\|$	1.0	–	–
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, f = 1.0 MHz)	C_{ob}	–	7.0	pF
Small-Signal Current Gain	h_{fe}			–
($I_C = 50$ mAdc, $V_{CE} = 5.0$ Vdc, f = 1.0 kHz) 2N6548		20,000	–	
2N6549		15,000	-	

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

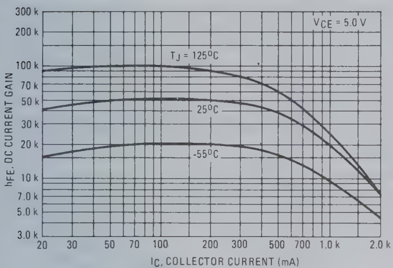


FIGURE 3 – "ON" VOLTAGES

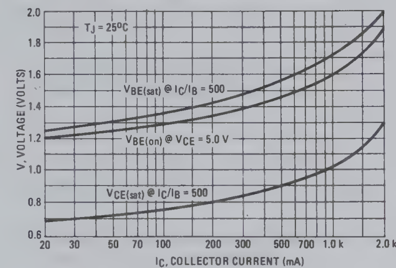


FIGURE 4 – COLLECTOR SATURATION REGION

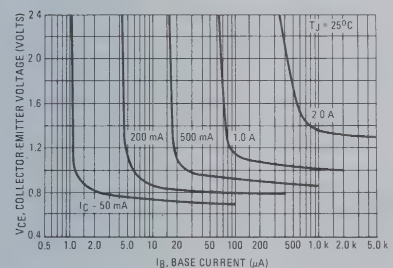


FIGURE 5 – TEMPERATURE COEFFICIENT

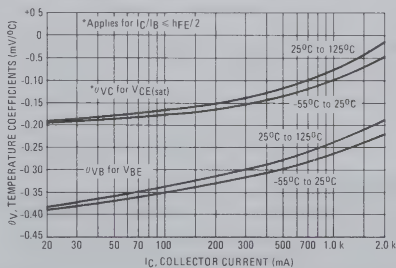
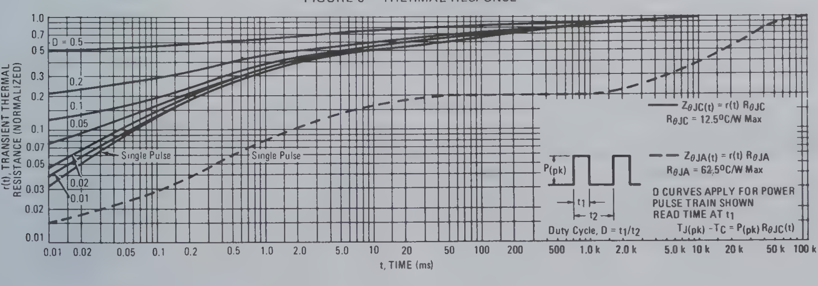


FIGURE 6 – THERMAL RESPONSE



2N6551
2N6552
2N6553

MOTOROLA

1.3

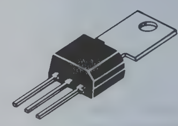
NPN SILICON ANNULAR AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- High Collector-Emitter Breakdown Voltage – BV_{CEO} = 100 Vdc (Min) @ I_C = 1.0 mAdc – 2N6553
- Duowatt Package – 2 Watts Free Air Dissipation @ $T_A = 25^oC$
- Complements to PNP 2N6554/5/6

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



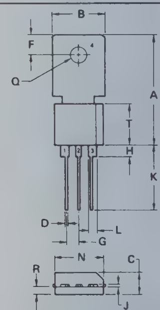
MAXIMUM RATINGS

Rating	Symbol	2N6551	2N6552	2N6553	Unit
*Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
*Collector-Base Voltage	V_{CBO}	60	80	100	Vdc
*Emitter-Base Voltage	V_{EBO}	5.0			Vdc
*Collector Current – Continuous – Peak (1)	I_C	1.0 2.0			Adc
*Base Current	I_B	100			mAdc
*Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	2.0 16			Watts $mW/^oC$
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	10 80			Watts $mW/^oC$
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			^oC
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^oC/W$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^oC/W$

*Indicates JEDEC Registered Data.
(1) ≤10 ms, ≤ 50% Duty Cycle



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04
TO-202AC

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage	BV_{CEO}			Vdc
(I_C = 1.0 mAdc, I_B = 0) 2N6551		60	–	
2N6552		80	–	
2N6553		100	–	
Collector-Base Breakdown Voltage	BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0) 2N6551		60	–	
2N6552		80	–	
2N6553		100	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current	I_{CBO}			nAdc
(V_{CB} = 40 Vdc, I_E = 0) 2N6551		–	100	
(V_{CB} = 60 Vdc, I_E = 0) 2N6552		–	100	
(V_{CB} = 80 Vdc, I_E = 0) 2N6553		–	100	
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)		60	–	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)		80	300	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		60	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		25	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)		–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)		–	1.0	
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)	f_T	75	375	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	18	pF

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN – BANDWIDTH PRODUCT

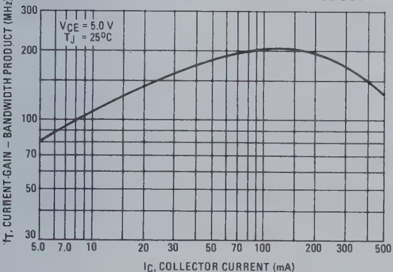
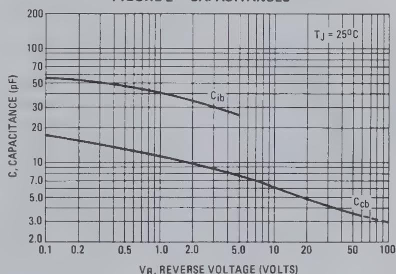


FIGURE 2 – CAPACITANCES



TYPICAL CHARACTERISTICS (continued)

FIGURE 3 — DC CURRENT GAIN

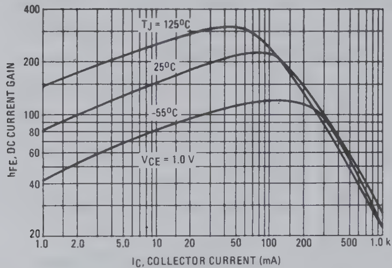


FIGURE 4 — "ON" VOLTAGE

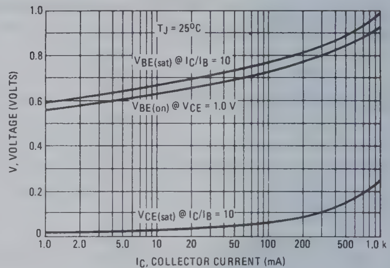


FIGURE 5 — COLLECTOR SATURATION REGION

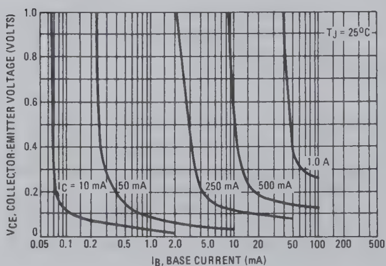


FIGURE 6 — TEMPERATURE COEFFICIENTS

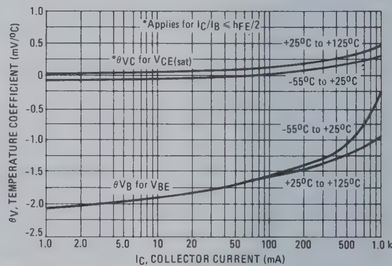


FIGURE 7 — COLLECTOR CHARACTERISTICS

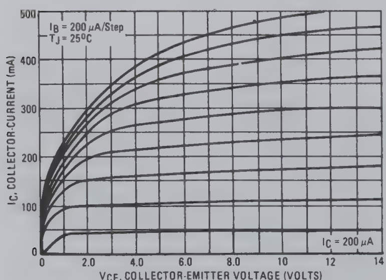
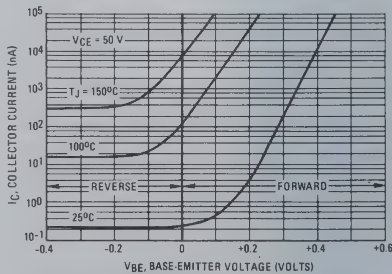


FIGURE 8 — COLLECTOR CUTOFF REGION



TYPICAL CHARACTERISTICS (continued)

FIGURE 9 — THERMAL RESPONSE

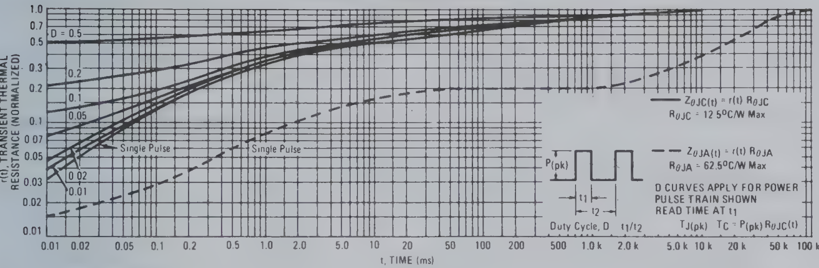
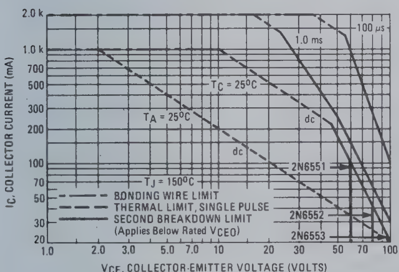


FIGURE 10 — ACTIVE-REGION SAFE-OPERATING AREA

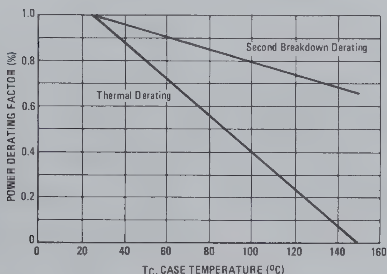


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 — POWER DERATING



2N6554
2N6555
2N6556

MOTOROLA

1.3

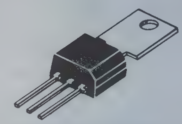
PNP SILICON ANNULAR AMPLIFIER TRANSISTORS

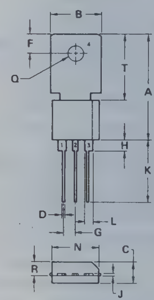
. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 100 Vdc (Min) @ I_C = 1.0 mAdc — 2N6556
- Duowatt Package — 2 Watts Free Air Dissipation @ T_A = 25°C
- Complements to NPN 2N6551/2/3

DUOWATT

PNP SILICON AMPLIFIER TRANSISTORS





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21 84	22 35	0 860	0 880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0 175
D	0.61	0.71	0.024	0 028
F	3.68	3.94	0.145	0 155
G	2.41	2.67	0.095	0 105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0 080
N	9.91	10.16	0.390	0.400
Q	3.56	.3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-04
TO-202AC

MAXIMUM RATINGS

Rating	Symbol	2N6554	2N6555	2N6556	Unit
*Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
*Collector-Base Voltage	V_{CBO}	60	80	100	Vdc
*Emitter-Base Voltage	V_{EBO}	5.0			Vdc
*Collector Current — Continuous Peak	I_C	1.0 2.0			Adc
*Base Current	I_B	100			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C
*Solder Temperature, 1/16″ from Case for 10 Seconds	—	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.

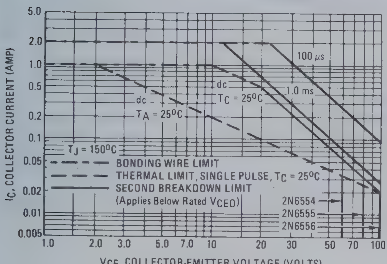
*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	2N6554	BV_{CEO}	60	–	Vdc
	2N6555		80	–	
	2N6556		100	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	2N6554	BV_{CBO}	60	–	Vdc
	2N6555		80	–	
	2N6556		100	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	2N6554	I_{CBO}	–	100	nAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N6555		–	100	
(V_{CB} = 80 Vdc, I_E = 0)	2N6556		–	100	
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)		I_{EBO}		100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 1.0 Vdc)		h_{FE}	60	–	–
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			80	300	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			60		
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			25	–	
Collector-Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 10 mAdc)		$V_{CE(sat)}$	–	0.5	Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$		1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)		f_T	75	375	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	18	pF

* Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 — ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

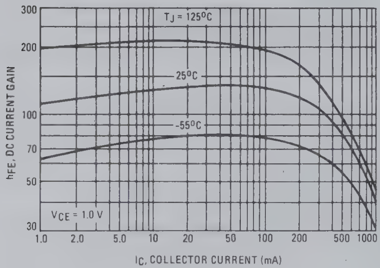


FIGURE 3 – "ON" VOLTAGE

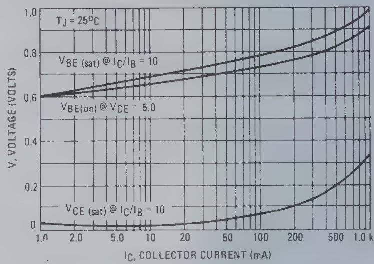


FIGURE 4 – COLLECTOR SATURATION REGION

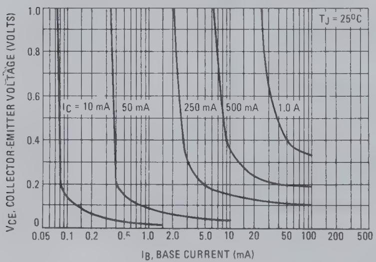


FIGURE 5 – TEMPERATURE COEFFICIENT

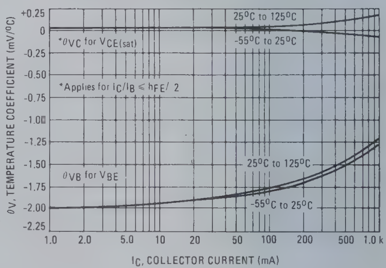
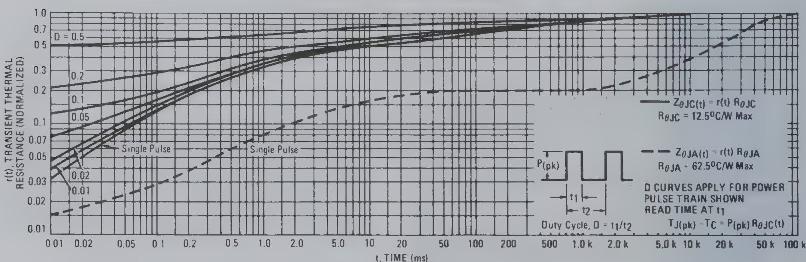


FIGURE 6 – THERMAL RESPONSE



2N6557
2N6558
2N6559

MOTOROLA

1.3

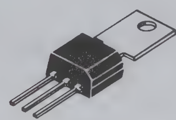
NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 350 Vdc (Min) @ I_C = 1.0 mAdc — 2N6559
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance — C_{cb} = 3.0 pF (Max) @ V_{CB} = 20 Vdc
- Duowatt Package — 2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



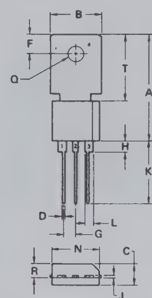
MAXIMUM RATINGS

Rating	Symbol	2N6557	2N6558	2N6559	Unit
*Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
*Collector-Base Voltage	V_{CBO}	250	300	350	Vdc
*Emitter-Base Voltage	V_{EBO}	6.0			Vdc
*Collector Current — Continuous Peak	I_C	0.5 0.7			Adc
*Base Current	I_B	250			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	—	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.



STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-04
TO-202AC

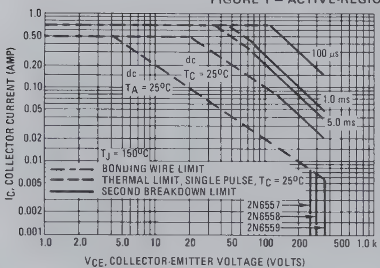
***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage		BV_{CEO}			Vdc
(I_C = 1.0 mAdc, I_B = 0)	2N6557		250	–	
	2N6558		300	–	
	2N6559		350	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	2N6557		250	–	
	2N6558		300	–	
	2N6559		350	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	6.0	–	Vdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 150 Vdc, I_E = 0)	2N6557		–	0.2	
(V_{CB} = 200 Vdc, I_E = 0)	2N6558		–	0.2	
(V_{CB} = 250 Vdc, I_E = 0)	2N6559		–	0.2	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)			25	–	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)			40	180	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 30 mAdc, I_B = 3.0 mAdc)			–	0.6	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			–	1.5	
Base-Emitter On Voltage (I_C = 30 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	0.85	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	45	200	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	3.0	pF

* Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

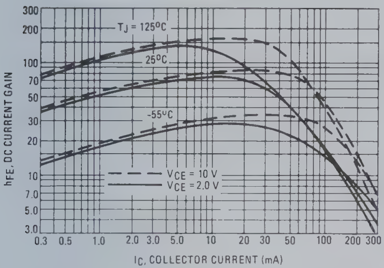


FIGURE 3 – "ON" VOLTAGES

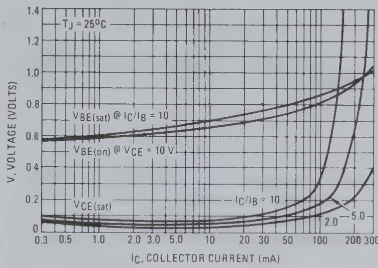


FIGURE 4 – COLLECTOR SATURATION REGION

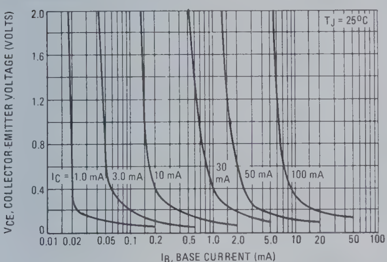


FIGURE 5 – TEMPERATURE COEFFICIENTS

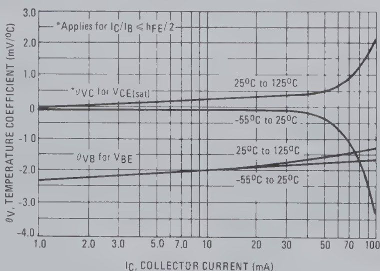
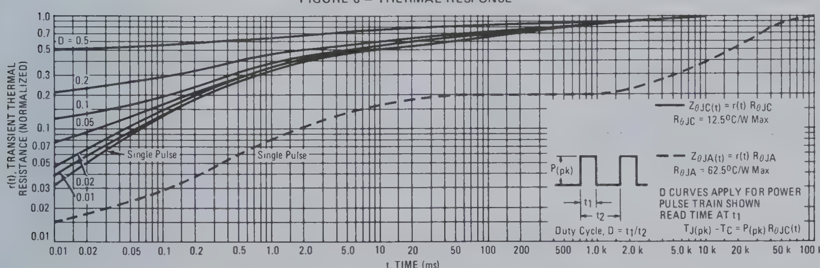


FIGURE 6 – THERMAL RESPONSE



MOTOROLA

1.3

NPN SILICON POWER TRANSISTOR

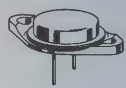
The 2N6569 is a general-purpose, EPIBASE power transistor designed for low voltage amplifier and power switching applications.

- Low Cost
- Safe Operating Area — Full Power Rating to 40 V
- EPIBASE Performance in Gain and Speed
- Metal Can Reliability — TO-3 Package
- All-Purpose Replacement for Industry Standard 2N3055

12 AMPERE

POWER TRANSISTOR
NPN SILICON

40 VOLTS
100 WATTS

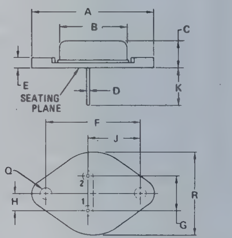


*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	40	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	12 24	Adc
Base Current — Continuous — Peak	I_B	5.0 10	Adc
Emitter Current — Continuous — Peak	I_E	17 34	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	100 0.572	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case fo 10s.	T_L	265	^oC



NOTE:
1. DIM "Q" IS DIA.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

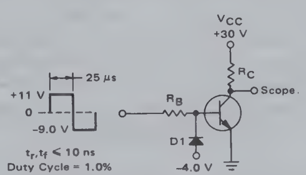
Collector connected to case.
CASE 11-01
(TO-3)

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	–	Vdc
Collector Cutoff Current	I_{CEV}			mAdc
(V_{CEV} = 45 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		–	1.0	
(V_{CEV} = 45 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	10	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s (non-repetitive))	$I_{S/b}$	2.5	–	Adc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		15	200	
(I_C = 12 Adc, V_{CE} = 4.0 Vdc)		5.0	100	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 0.4 Adc)		–	1.5	
(I_C = 12 Adc, I_B = 2.4 Adc)		–	4.0	
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 0.4 Adc)	$V_{BE(sat)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 0.5 MHz)	f_T	1.5	15	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)	C_{ob}	75	750	pF
SWITCHING CHARACTERISTICS				
RESISTIVE LOAD				
Delay Time (V_{CC} = 30 Vdc, I_C = 2.0 Adc, I_{B1} = 0.2 Adc, t_p = 25 μs, Duty Cycle ≤ 1.0%)	t_d	–	0.4	μs
Rise Time (V_{CC} = 30 Vdc, I_C = 2.0 Adc, I_{B1} = 0.2 Adc, t_p = 25 μs, Duty Cycle ≤ 1.0%)	t_r	–	1.5	μs
Storage Time (V_{CC} = 30 Vdc, I_C = 2.0 Adc, I_{B1} = I_{B2} = 0.2 Adc, t_p = 25 μs, Duty Cycle ≤ 1.0%)	t_s	–	5.0	μs
Fall Time (V_{CC} = 30 Vdc, I_C = 2.0 Adc, I_{B1} = I_{B2} = 0.2 Adc, t_p = 25 μs, Duty Cycle ≤ 1.0%)	t_f	–	1.5	μs

*Indicates JEDEC Registered Data.

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



R_B and R_C Varied to Obtain Desired Current Levels
D1 must be fast recovery type.

1.3

FIGURE 2 — THERMAL RESPONSE

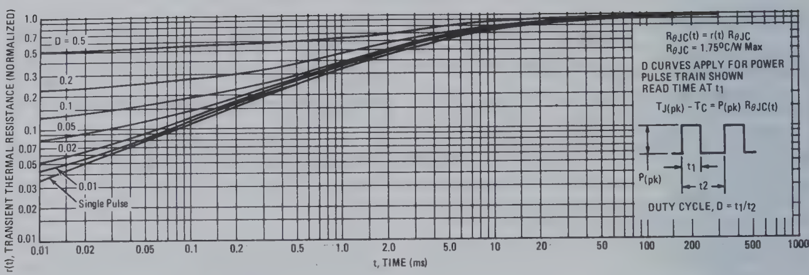
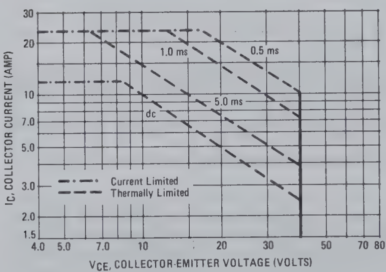


FIGURE 3 — SAFE OPERATING AREA



Safe operating area curves indicate I_C-V_{CE} limits of the transistor being observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. This transistor is thermally limited over its entire operation area. Figure 4 may be used to derate the curves shown or an effective $R_{\theta JC(t)}$ may be computed from Figure 2 for pulsed operation.

FIGURE 4 — POWER DERATING

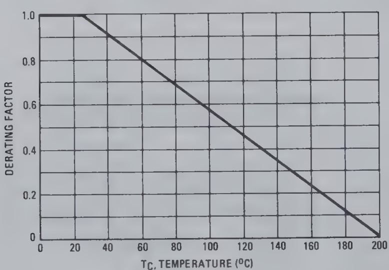


FIGURE 5 – DC CURRENT GAIN

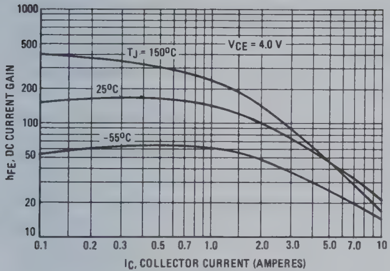


FIGURE 6 – COLLECTOR SATURATION REGION

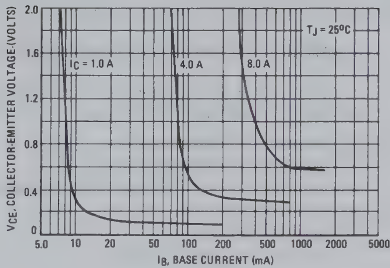


FIGURE 7 – "ON" VOLTAGES

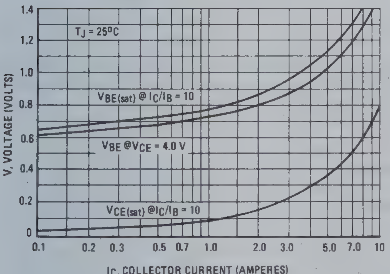
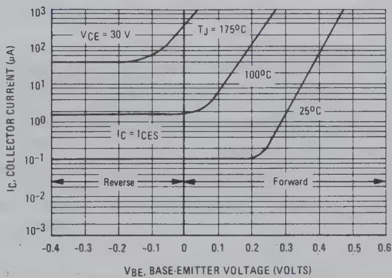


FIGURE 8 – COLLECTOR CUT-OFF REGION



2N6576
2N6577
2N6578

MOTOROLA

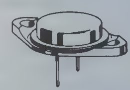
1.3

NPN SILICON POWER DARLINGTON TRANSISTORS

General-purpose EpiBase power darlington transistors, suitable for linear and switching applications.

- Replacement for 2N3055 and Driver
- High Gain Darlington Performance
- Built-In Diode Protection for Reverse Polarity Protection
- Can Be Driven from Low-Level Logic
- Popular Voltage Range
- Operating Range — −65 to +200°C

15 AMPERE
POWER TRANSISTORS
NPN SILICON
DARLINGTON
60, 90, 120 VOLTS
120 WATTS



*MAXIMUM RATINGS

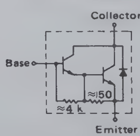
Rating	Symbol	2N6576	2N6577	2N6578	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current — Continuous — Peak	I_C	← 15 → ← 30 →			Adc
Base Current — Continuous — Peak	I_B	← 0.25 → ← 0.50 →			Adc
Emitter Current — Continuous — Peak	I_E	← 15.25 → ← 30.5 →			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 120 → ← 0.685 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +200 →			°C

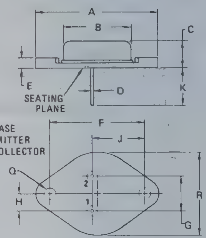
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.46	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16″ from Case for 10s.	T_L	265	°C

*Indicates JEDEC Registered Data

DARLINGTON SCHEMATIC





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03
TO-3

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^oC$ unless otherwise noted.)

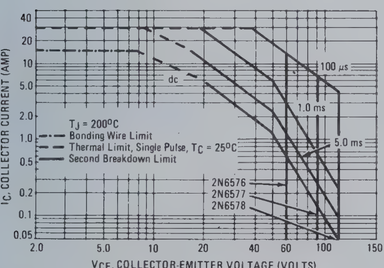
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage(1) (I_C = 200 mAdc, I_B = 0) 2N6576	$V_{CEO(sus)}$	60	–	Vdc
2N6577		90	–	
2N6578		120	–	
Collector Cutoff Current (V_{CE} = Rated Value)	I_{CEO}	–	1.0	mAdc
Collector Cutoff Current (V_{CER} = Rated $V_{CEO(sus)}$ Value, R_{BE} = 10 kΩ, $T_C = 150^oC$)	I_{CER}	–	5.0	mAdc
Collector Cutoff Current V_{CEX} = Rated $V_{CEO(sus)}$ Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	5.0	mAdc
Collector Cutoff Current (V_{CB} = Rated Value)	I_{CBO}	–	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 15 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	100	–	–
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)		500	5,000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		2000	20,000	
(I_C = 0.4 Adc, V_{CE} = 3.0 Vdc)		200	–	
Collector-Emitter Saturation Voltage (I_C = 15 Adc, I_B = 0.15 Adc)	$V_{CE(sat)}$	–	4.0	Vdc
(I_C = 10 Adc, I_B = 0.1 Adc)		–	2.8	
Base-Emitter Saturation Voltage (I_C = 15 Adc, I_B = 0.15 Adc)	$V_{BE(sat)}$	–	4.5	Vdc
(I_C = 10 Adc, I_B = 0.1 Adc)		–	3.5	
Collector-Emitter Diode Voltage Drop (I_{EC} = 15 Adc)	V_F	–	4.5	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common-Emitter Small-Signal Short-Circuit Current Transfer Ratio (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$\|h_{fe}\|$	10	200	–

SWITCHING CHARACTERISTICS
RESISTIVE LOAD (Figure 2)

Characteristic	Conditions	Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.15	μs
Rise Time		t_r	–	1.0	μs
Storage Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, $I_{B1} = I_{B2}$ = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_s	–	2.0	μs
Fall Time		t_f	–	7.0	μs

*Indicates JEDEC Registered Data
(1) Pulse test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — RATED FORWARD BIASED SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%.

$T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 — DC CURRENT GAIN

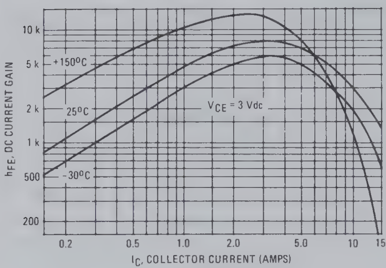


FIGURE 3 — COLLECTOR-SATURATION REGION

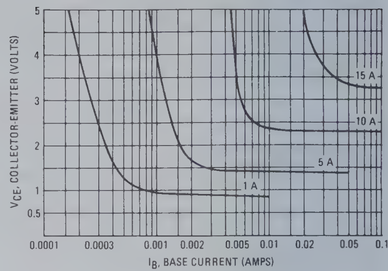


FIGURE 4 — COLLECTOR SATURATION VOLTAGE

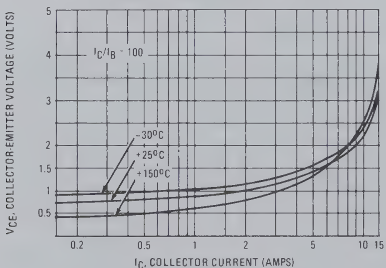


FIGURE 5 — BASE-EMITTER VOLTAGE

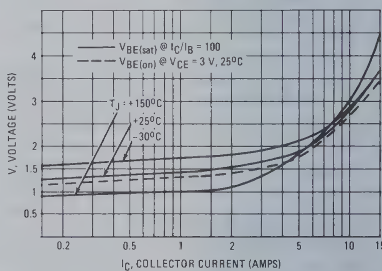
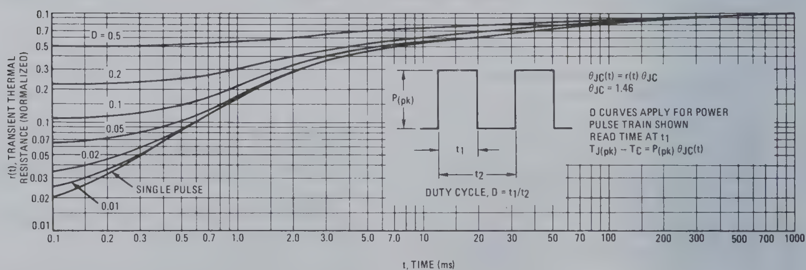


FIGURE 6 — THERMAL RESPONSE



![MOTOROLA]

MOTOROLA

2N6591
2N6592
2N6593

1.3

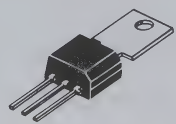
NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for horizontal drive applications, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 250 Vdc (Min) @ I_C = 1.0 mAdc — 2N6593
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 200 mAdc
- Duowatt Package — 2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



MAXIMUM RATINGS

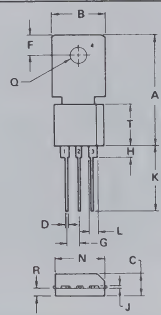
Rating	Symbol	2N6591	2N6592	2N6593	Unit
*Collector-Emitter Voltage	V_{CEO}	150	200	250	Vdc
*Collector-Base Voltage	V_{CBO}	150	200	250	Vdc
*Emitter-Base Voltage	V_{EBO}	5.0	5.0	5.0	Vdc
*Collector Current — Continuous	I_C	0.5	0.5	0.5	Adc
Peak (1)		1.0	1.0	1.0	
*Base Current	I_B	100	100	100	mAdc
*Total Power Dissipation @ T_A = 25°C	P_D	2.0	2.0	2.0	Watts
Derate above 25°C		16	16	16	mW/°C
Total Power Dissipation @ T_C = 25°C	P_D	10	10	10	Watts
Derate above 25°C		80	80	80	mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	-55 to +150	-55 to +150	°C
*Solder Temperature, 1/16" from Case for 10 Seconds	—	260	260	260	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 1.0 ms, Duty Cycle ≤ 50%.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04
TO-202AC

1.3

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	2N6591	BV_{CEO}	150	–	Vdc
	2N6592		200	–	
	2N6593		250	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	2N6591	BV_{CBO}	150	–	Vdc
	2N6592		200	–	
	2N6593		250	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	2N6591	I_{CBO}	–	0.2	μAdc
(V_{CB} = 150 Vdc, I_E = 0)	2N6592		–	0.2	
(V_{CB} = 200 Vdc, I_E = 0)	2N6593		–	0.2	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc)	2N6591	h_{FE}	40	250	–
	2N6592		30	250	
	2N6593		30	250	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)	2N6591		40	200	
	2N6592		40	200	
	2N6593		30	200	
Collector-Emitter Saturation Voltage (I_C = 200 mAdc, I_B = 20 mAdc)		$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	35	300	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	12	pF

* Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN – BANDWIDTH PRODUCT

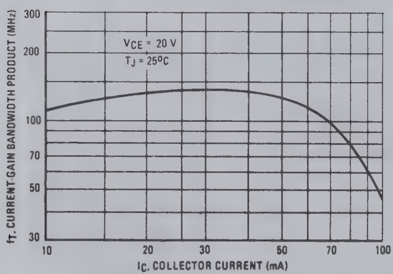
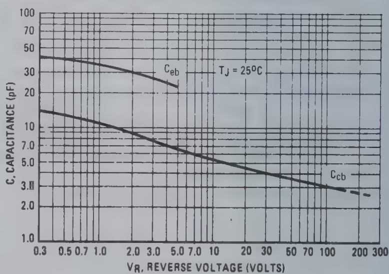


FIGURE 2 – CAPACITANCE



1.3

TYPICAL CHARACTERISTICS (Continued)

FIGURE 3 – DC CURRENT GAIN

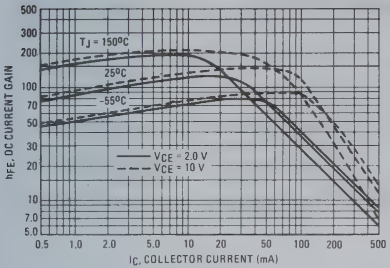


FIGURE 4 – "ON" VOLTAGE

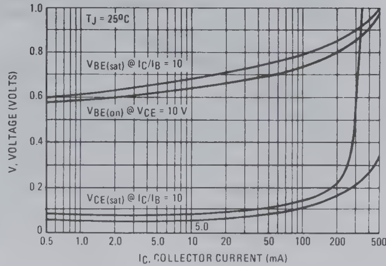


FIGURE 5 – COLLECTOR SATURATION REGION

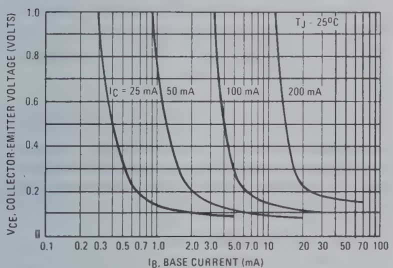


FIGURE 6 – TEMPERATURE COEFFICIENTS

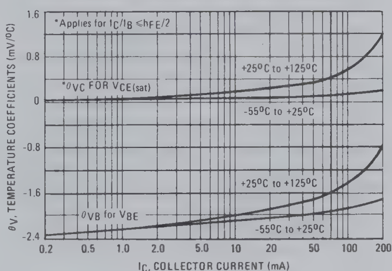


FIGURE 7 – COLLECTOR CHARACTERISTICS

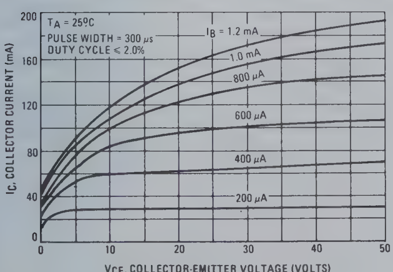
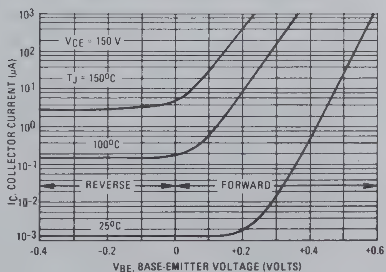


FIGURE 8 – COLLECTOR CUTOFF REGION



TYPICAL CHARACTERISTICS (Continued)

FIGURE 9 – THERMAL RESPONSE

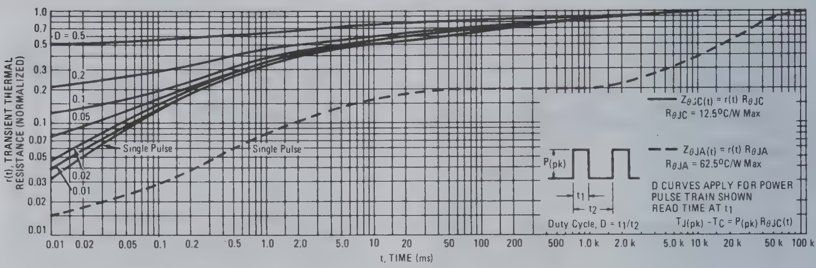
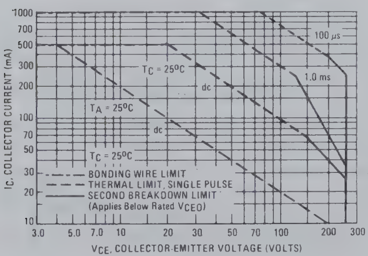


FIGURE 10 – ACTIVE REGION SAFE-OPERATING AREA

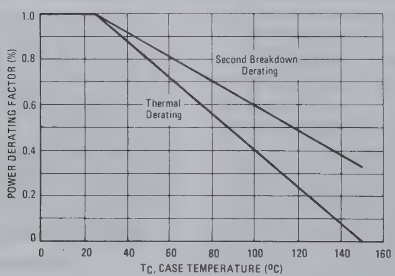


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING



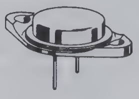
MOTOROLA

PNP SILICON POWER TRANSISTOR

The 2N6594 is a general-purpose, EPI-BASE power transistor designed for low voltage amplifier and power switching applications. It is a complement to the NPN 2N6569.

- Safe Operating Area — Full Power Rating to 40 V
- EPI-BASE Performance in Gain and Speed
- Lower Voltage, Economical Complement to the 2N3055

12 AMPERE
POWER TRANSISTOR
PNP SILICON
40 VOLTS
100 WATTS

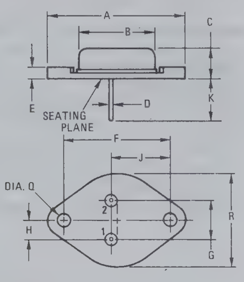


*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	40	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current — Continuous — Peak	I_C	12 24	Adc
Base Current — Continuous — Peak	I_B	5 10	Adc
Emitter Current — Continuous — Peak	I_E	17 34	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	100 0.572	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/16″ from Case for 10 seconds	T_L	265	^oC



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

1.3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

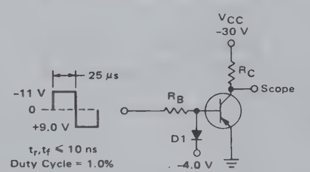
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	–	Vdc
Collector Cutoff Current	I_{CEV}			mAdc
(V_{CEV} = 45 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		–	1	
(V_{CEV} = 45 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	10	
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	5	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1 s (non-repetitive))	$I_{S/b}$	2.5	–	Adc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 4 Adc, V_{CE} = 3 Vdc)		15	200	
(I_C = 12 Adc, V_{CE} = 4 Vdc)		5	100	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 4 Adc, I_B = 0.4 Adc)		–	1.5	
(I_C = 12 Adc, I_B = 2.4 Adc)		–	4	
Base-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{BE(sat)}$	–	2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 4 Vdc, f_{test} = 0.5 MHz)	f_T	2.5	25	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	100	1000	pF

SWITCHING CHARACTERISTICS
RESISTIVE LOAD

Characteristic	Conditions	Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 30 Vdc, I_C = 2 Adc, I_{B1} = 0.2 Adc, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	–	0.4	μs
Rise Time		t_r	–	1.5	μs
Storage Time	(V_{CC} = 30 Vdc, I_C = 2 Adc, I_{B1} = I_{B2} = 0.2 Adc, t_p = 25 μs, Duty Cycle ≤ 1%)	t_s	–	5	μs
Fall Time		t_f	–	1.5	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test, PW = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



R_B and R_C Varied to Obtain Desired Current Levels
D1 must be fast recovery type.

1.3

FIGURE 2 – THERMAL RESPONSE

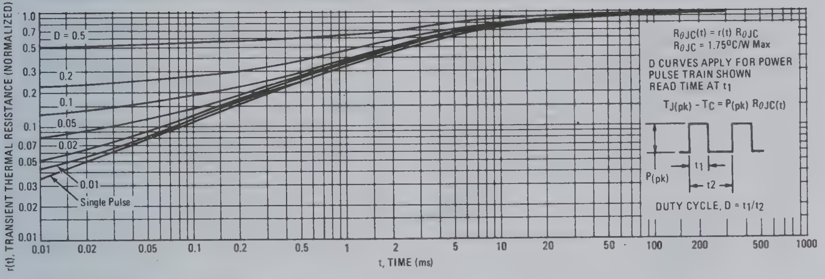
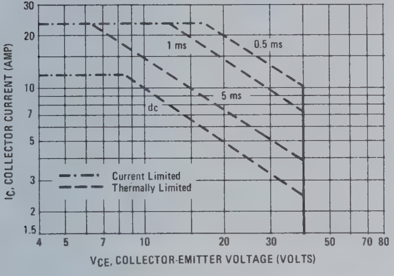
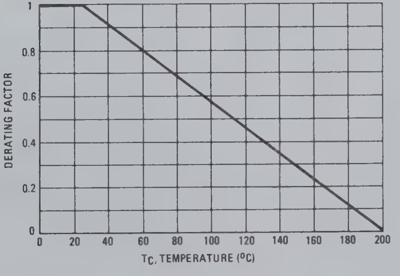


FIGURE 3 – SAFE OPERATING AREA



Safe operating area curves indicate I_C-V_{CE} limits of the transistor being observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. Figure 4 may be used to derate the curves shown or an effective $R_{\theta JC(t)}$ may be computed from Figure 2 for pulsed operation.

FIGURE 4 – POWER DERATING



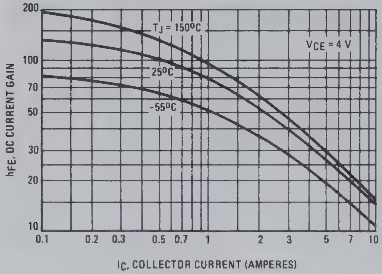


FIGURE 5 – DC CURRENT GAIN

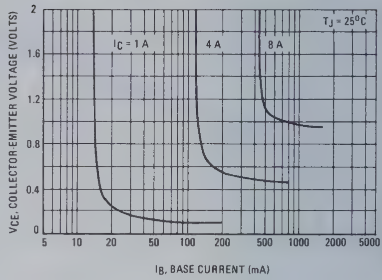


FIGURE 6 – COLLECTOR SATURATION REGION

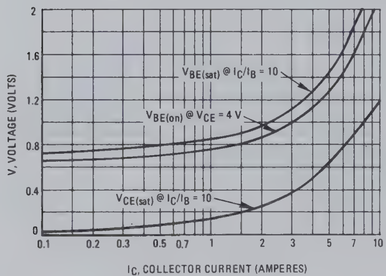


FIGURE 7 – "ON" VOLTAGES

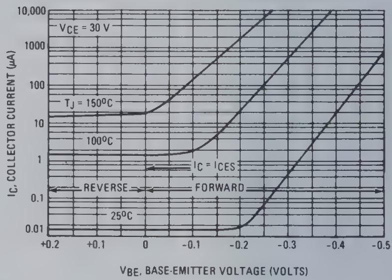


FIGURE 8 – COLLECTOR CUT-OFF REGION

PLASTIC MEDIUM-POWER SILICON TRANSISTORS

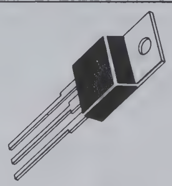
. . . designed for general-purpose amplifier and low speed switching applications.

- High DC Current Gain —
  h_{FE} = 3500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 200 mAdc
  $V_{CEO(sus)}$ = 40 Vdc (Min) — 2N6666
  = 60 Vdc (Min) — 2N6667
  = 80 Vdc (Min) — 2N6668
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc — 2N6666
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 5.0 Adc — 2N6667, 2N6668
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- Complementary to 2N6386, 2N6387, 2N6388

DARLINGTON
8 AND 10 AMPERE

PNP SILICON
POWER TRANSISTORS

40-60-80 VOLTS
65 WATTS



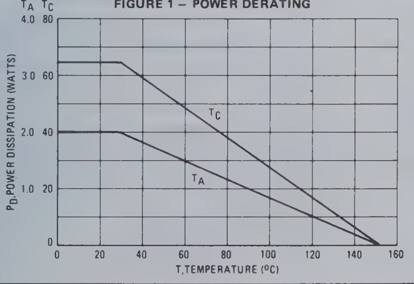
*MAXIMUM RATINGS

Rating	Symbol	2N6666	2N6667	2N6668	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	8.0 15	10 15	10 15	Adc
Base Current	I_B	← 250 →			mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 65 → ← 0.52 →			Watts W/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 0.016 →			Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

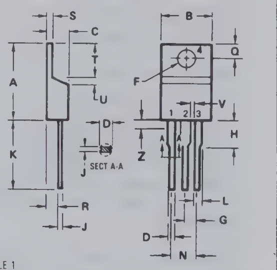
THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 — POWER DERATING



*Indicates JEDEC Registered Data



STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES
1. DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6666		40	—	
	2N6667		60	—	
	2N6668		80	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6666		—	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6667		—	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N6668		—	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6666		—	300	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6667		—	300	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6668		—	300	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6666		—	3.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6667		—	3.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6668		—	3.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	2N6666		1000	20000	
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6667, 2N6668		1000	20000	
(I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)	2N6666		100	—	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6667, 2N6668		100	—	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 0.006 Adc)	2N6666		—	2.0	
(I_C = 5.0 Adc, I_B = 0.01 Adc)	2N6667, 2N6668		—	2.0	
(I_C = 8.0 Adc, I_B = 0.08 Adc)	2N6666		—	3.0	
(I_C = 10 Adc, I_B = 0.1 Adc)	2N6667, 2N6668		—	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	2N6666		—	2.8	
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6667, 2N6668		—	2.8	
(I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)	2N6666		—	4.5	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6667, 2N6668		—	4.5	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)		$\|h_{fe}\|$	20	—	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	200	pF
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	1000	—	—

*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

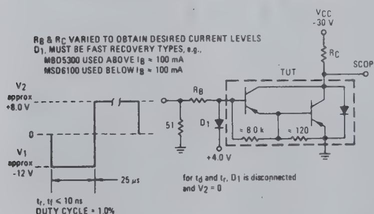


FIGURE 3 — SWITCHING TIMES

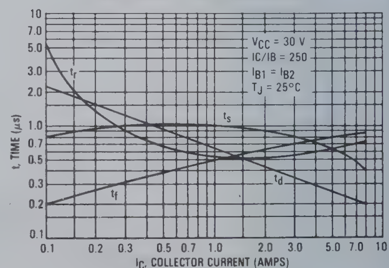


FIGURE 4 — THERMAL RESPONSE

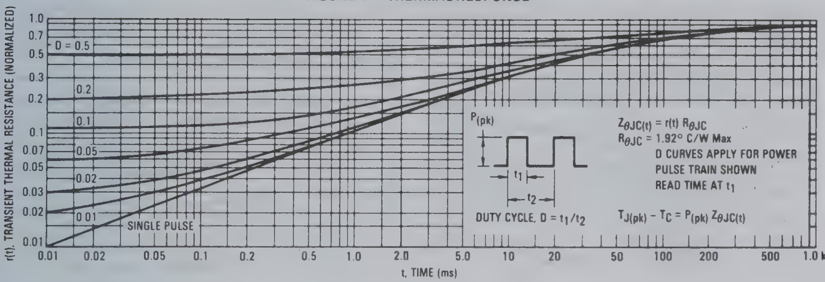
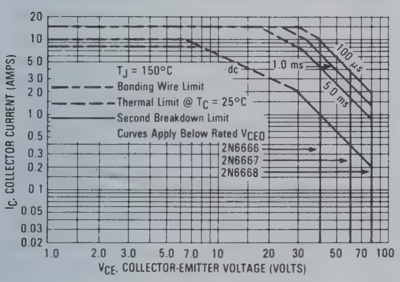


FIGURE 5 — SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — SMALL-SIGNAL CURRENT GAIN

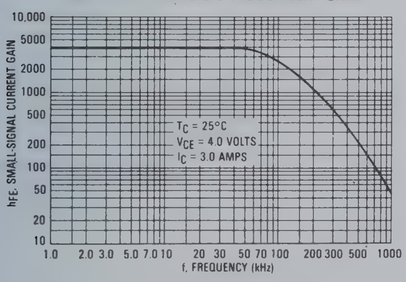


FIGURE 7 — CAPACITANCE

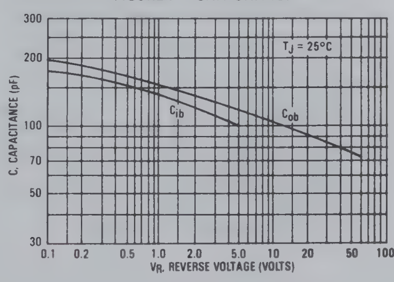


FIGURE 8 — DC CURRENT GAIN

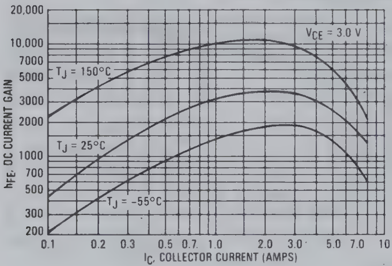


FIGURE 9 — COLLECTOR SATURATION REGION

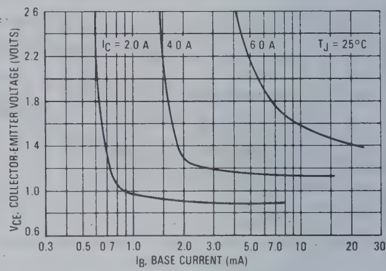


FIGURE 10 — "ON" VOLTAGES

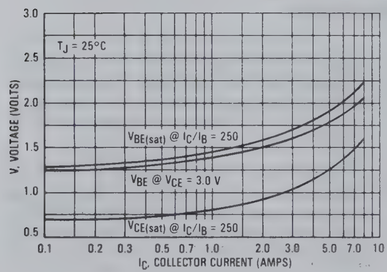


FIGURE 11 — TEMPERATURE COEFFICIENTS

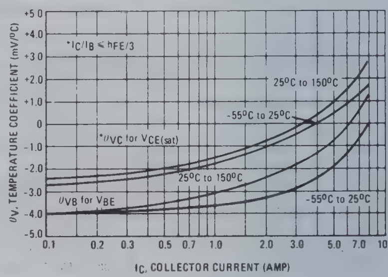


FIGURE 12 – COLLECTOR CUT-OFF REGION

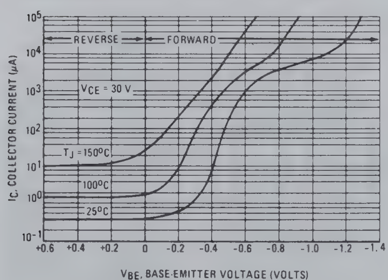
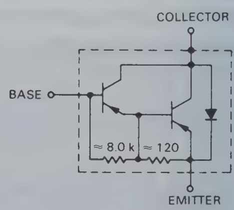


FIGURE 13 – DARLINGTON SCHEMATIC



2N6676
2N6677
2N6678

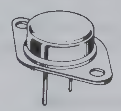
MOTOROLA

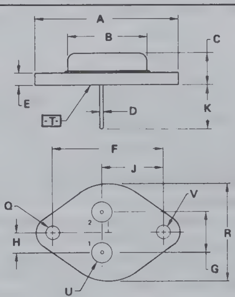
1.3

15 AMPERE

NPN SILICON POWER TRANSISTORS

300, 350, 400 VOLTS
175 WATTS





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

NPN SILICON POWER TRANSISTORS

The 2N6676, 2N6677 and 2N6678 transistors are designed for high voltage switching applications such as:

- Off-Line Power Supplies
- Converter Circuits
- Pulse Width Modulated Regulators

Specification Features —
- High Voltage Capability
- Fast Switching Speeds
- Low Saturation Voltages
- High SOA Ratings

MAXIMUM RATINGS

Rating	Symbol	2N6676	2N6677	2N6678	Unit
Collector Emitter Voltage	V_{CEV}	450	550	650	Vdc
Collector Emitter Voltage	V_{CEX}	350	400	450	Vdc
Collector Emitter Voltage	V_{CEO}	300	350	400	Vdc
Emitter Base Voltage	V_{EBO}		8		Vdc
Collector Current - cont - peak	I_C I_{CM}		15 20		Adc
Base Current - cont	I_B		5		Adc
Power Dissipation $T_C = 25°C$ Derate above 25°C	P_T		175 1		Watts W/°C
Operating and Storage Junction	T_J; T_{stg}		-65 to 200		°C
Thermal Resistance Junction to Case	$R_{\theta JC}$		1.0		°C/W
Maximum Lead Temperature At Distance > 1/16 in. (1.58 mm) from seating plane for 10 s max.			235		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Cutoff Current	I_{CEV}			mA
(V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = −1.5 Vdc)		—	0.1	
(V_{CE} = Rated V_{CEV}, $V_{BE(off)}$, TC = 100°C)		—	1.0	
Emitter Cutoff Current (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mA
Collector-Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0)	$V_{CEO(sus)}$			Vdc
2N6676		300	—	
2N6677		350	—	
2N6678		400	—	
Collector-Emitter Sustaining Voltage (I_C = 15 A, V_{clamp} = Rated V_{CEX})	$V_{CEX(sus)}$			Vdc
2N6676		350	—	
2N6677		400	—	
2N6678		450	—	
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 1		
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 2		
ON CHARACTERISTICS				
DC Current Gain (I_C = 15 A, V_{CE} = 3.0 V)	h_{FE}	8.0	—	—
Base Emitter Saturation Voltage (I_C = 15 A, I_B = 3.0 A)	$V_{BE(sat)}$	—	1.5	Vdc
Collector-Emitter, Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 15 A, I_B = 3.0 A)		—	1.5	
(I_C = 15 A, I_B = 3.0 A, T_C = 100°C)		—	2.0	
DYNAMIC CHARACTERISTICS				
Current Gain (I_C = 1.0 A, V_{CE} = 10 Vdc, f = 5.0 MHz)	$\|h_{fe}\|$	3.0	10	MHz
Output Capacitance (I_C = 1.0 A, V_{CB} = 10 Vdc, f = 0.1 MHz)	C_{ob}	150	500	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Max	Unit
Resistive Load						
Delay Time	V_{CC} = 200 V, I_C = 15 A, I_{B1} = I_{B2} = 3.0 A, t_p = 20 μs, Duty Cycle ≤ 2.0%, V_{BB} ≃ 6.0 V, R_L ≃ 13.5 Ω (See Figure 3)	T_C = 25°C	t_d	—	0.1	μs
Rise Time			t_r	—	0.6	
Storage Time			t_s	—	2.5	
Fall Time			t_f	—	0.5	
Delay Time		T_C = 100°C	t_d	—	0.4	
Rise Time			t_r	—	1.0	
Storage Time			t_s	—	4.0	
Fall Time			t_f	—	1.0	
Inductive Load						
Cross Over Time	L = 50 μH, V_{clamp} = Rated V_{CEX} (See Figure 3)	T_C = 25°C	t_c	—	0.5	μs
		T_C = 100°C		—	0.8	

FIGURE 1 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

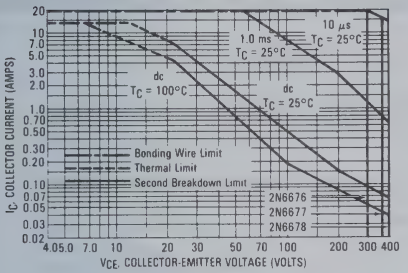
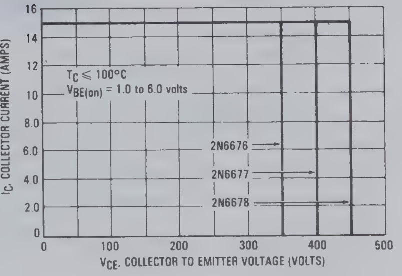


FIGURE 2 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

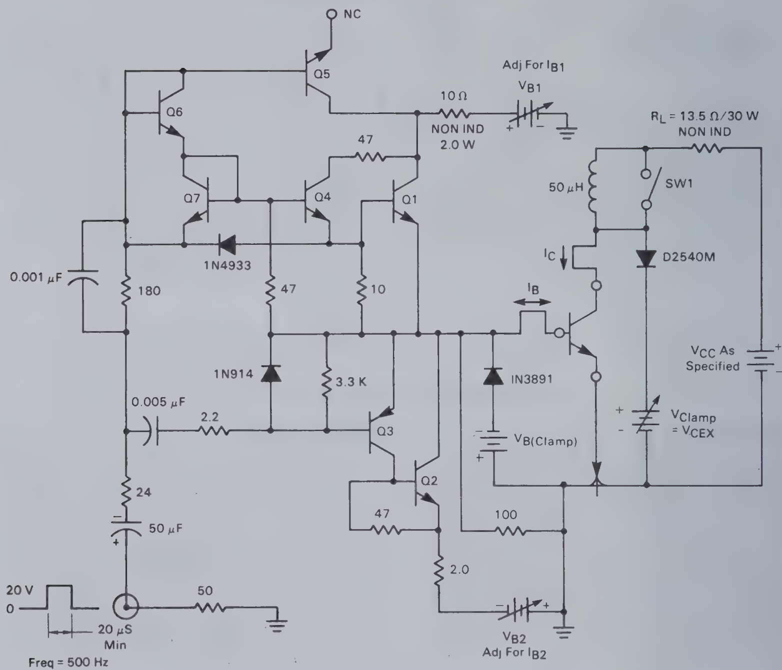
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant$ 25°C. Second breakdown limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 2 gives the RBSOA characteristics.

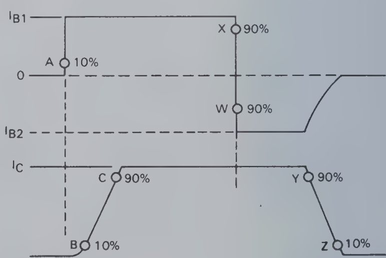
FIGURE 3 — SWITCHING TIME MEASUREMENTS
FOR 2N6676, 2N6677, AND 2N6678



Q_1, Q_2 = 2N6350
Q3 = 2N3762
Q4, Q5, Q6, Q7 = CA3725 Quad Transistor Array

NOTE: Battery symbols V_{CC}, V_{B1}, V_{B2}, $V_{B(clamp)}$ indicate rigorously filtered voltage sources at the circuit terminals to accommodate the fast rise and fall times and high currents present in the circuit.

NOTE: SW1 closed for t_r, t_s, t_f. SW1 open for t_c.



t_d = A–B
T_r = B–C
t_s = X–Y
t_f = Y–Z
$t_{transition}$ = X–W

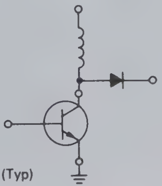
NOTE: TRANSITION TIME FROM 90% IB1 to 90% IB2 MUST BE LESS THAN 0.5 µs

Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:



- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  - 50 ns Inductive Fall Time — 75°C (Typ)
  - 70 ns Inductive Crossover Time — 75°C (Typ)
  - 500 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +150°C
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

5.0 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
80 and 125 WATTS

MAXIMUM RATINGS

Rating	Symbol	2N6833	2N6834	Unit
Collector-Emitter Voltage*	$V_{CEO(sus)}$	450		Vdc
Collector-Emitter Voltage*	V_{CEV}	850		Vdc
Emitter Base Voltage*	V_{EB}	6.0		Vdc
Collector Current — Continuous* — Peak (1)	I_C I_{CM}	5.0 10		Adc
Base Current — Continuous* — Peak (1)	I_B I_{BM}	4.0 8.0		Adc
Total Power Dissipation @ T_C = 25°C* @ T_C = 100°C* Derate above 25°C*	P_D	80 32 0.64	125 71.5 0.714	Watts W/°C
Operating and Storage Junction Temperature Range*	T_J, T_{stg}	-65 to +150	-65 to +200	°C

THERMAL CHARACTERISTICS

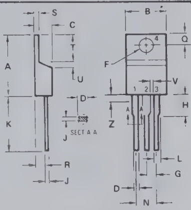
Characteristic	Symbol	2N6833	2N6834	Unit
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	1.56	1.40	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds*	T_L	275		°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
*Indicate JEDEC Registered Data

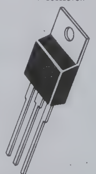
Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

2N6833



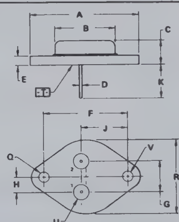
STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

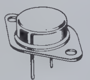


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	-	0.045	-
Z	-	2.03	-	0.080

CASE 221A-02
TO-220AB

2N6834





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67		1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA (Formerly TO-3)

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.25*	
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5*	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0*	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figures 15* and 16*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 17			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)		—	—	1.0	
(I_C = 3.0 Adc, I_B = 0.4 Adc)		—	—	2.5*	
(I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)		—	—	2.5*	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 3.0 Adc, I_B = 0.4 Adc)		—	—	1.5*	
(I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)		—	—	1.5	
DC Current Gain	h_{FE}				—
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)		7.5*	—	30*	
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)		5.0	—	—	
DYNAMIC CHARACTERISTICS (2)					
Current Gain - Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.25 Adc, f_{test} = 10 MHz)	f_T	15*	—	75*	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	20*	—	200*	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 0.8 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100*	ns
Rise Time			t_r	—	100	300*	
Storage Time			t_s	—	1000	3000*	
Fall Time			t_f	—	60	300*	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	400	—	
Fall Time			t_f	—	130	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	500	1600*	ns
Fall Time			t_{fi}	—	100	200*	
Crossover Time			t_c	—	120	250*	
Storage Time		(T_C = 150°C)	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.
(2) $f_T = |h_{fe}| \, f_{test}$
*Indicates JEDEC Registered Limit

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

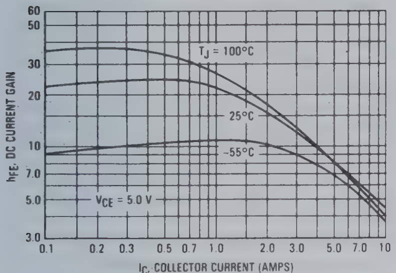


FIGURE 2 — COLLECTOR SATURATION REGION

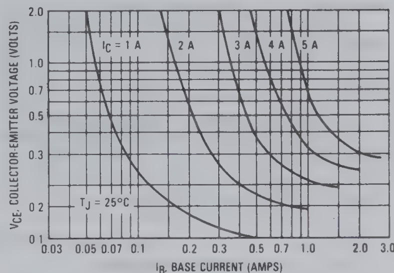


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

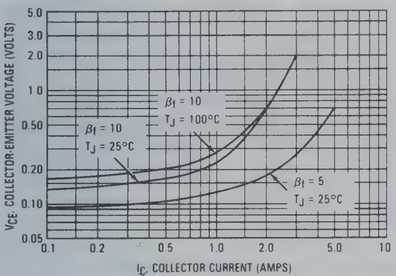


FIGURE 4 — BASE-EMITTER VOLTAGE

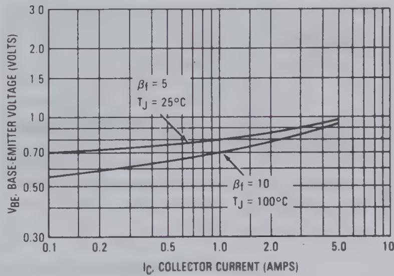


FIGURE 5 — COLLECTOR CUTOFF REGION

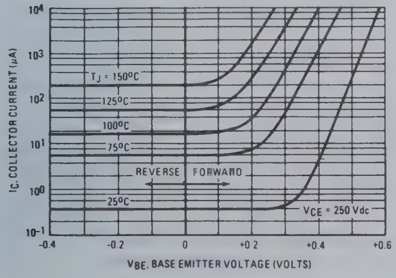
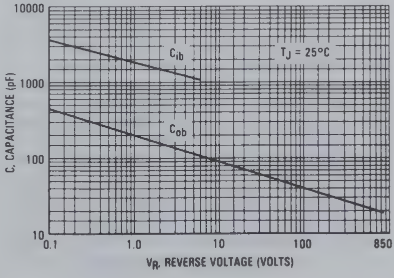


FIGURE 6 — CAPACITANCE



1.3

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

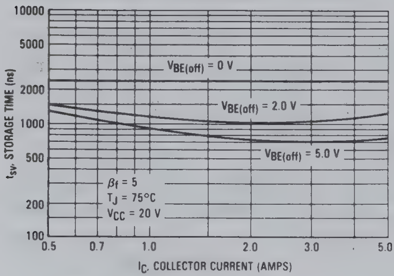


FIGURE 8 — STORAGE TIME

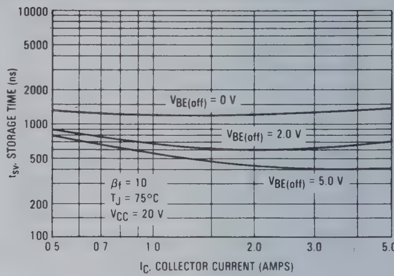


FIGURE 9 — COLLECTOR CURRENT FALL TIME

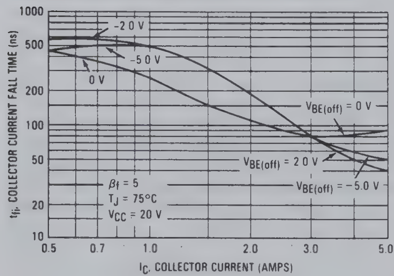


FIGURE 10 — COLLECTOR CURRENT FALL TIME

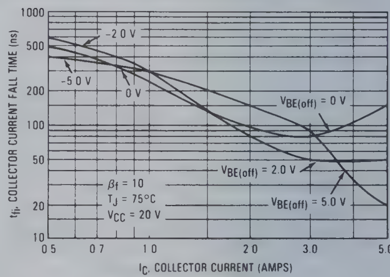


FIGURE 11 — CROSSOVER TIME

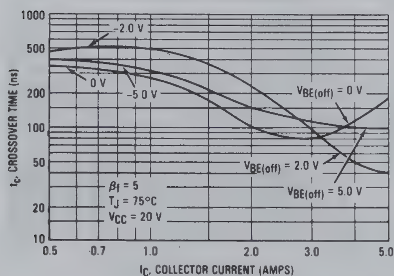


FIGURE 12 — CROSSOVER TIME

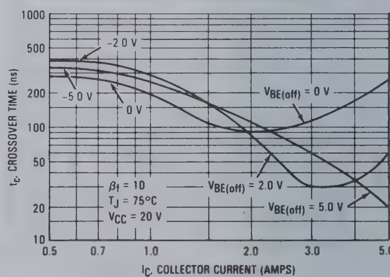


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

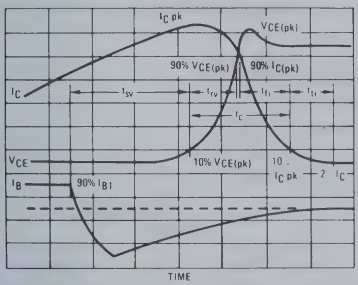
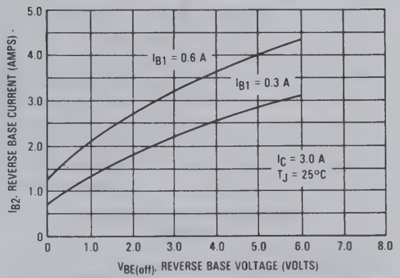


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA (2N6833)

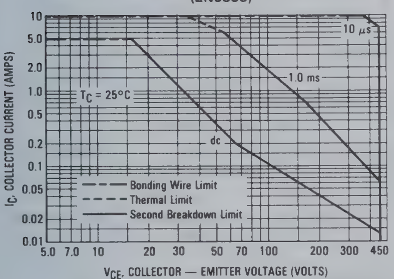
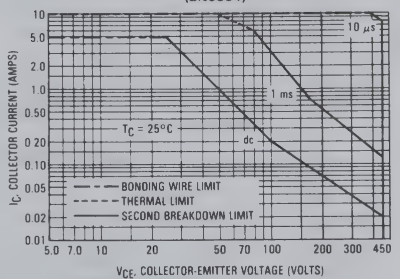


FIGURE 16 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA (2N6834)



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 15 and 16 are based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 15 and 16 may be found at any case temperature by using the appropriate curve on Figures 18 or 19.

$T_{J(pk)}$ may be calculated from the data in Figures 20 or 21. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable putting reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

1.3

FIGURE 17 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA

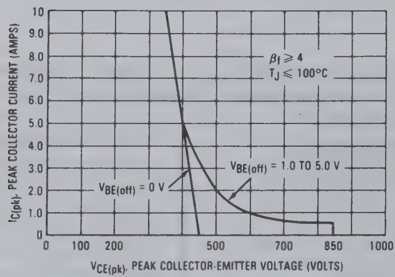


FIGURE 18 — POWER DERATING (2N6833)

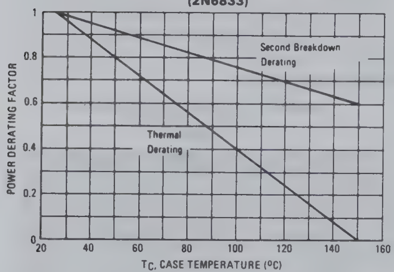


FIGURE 19 — POWER DERATING (2N6834)

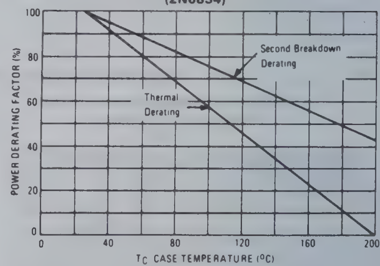
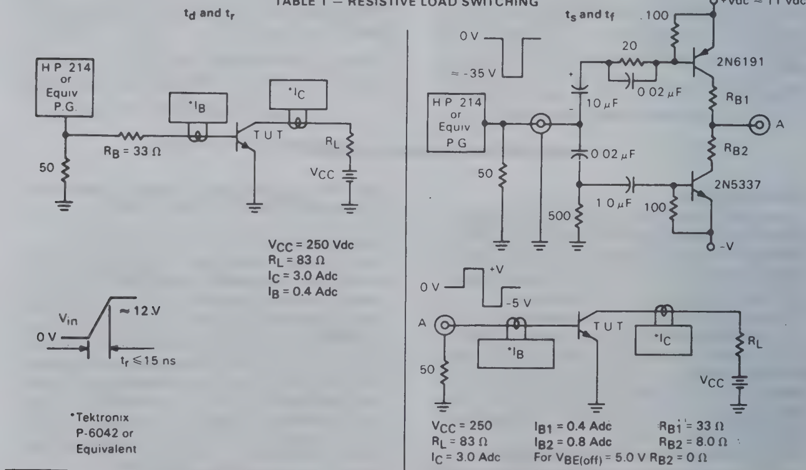
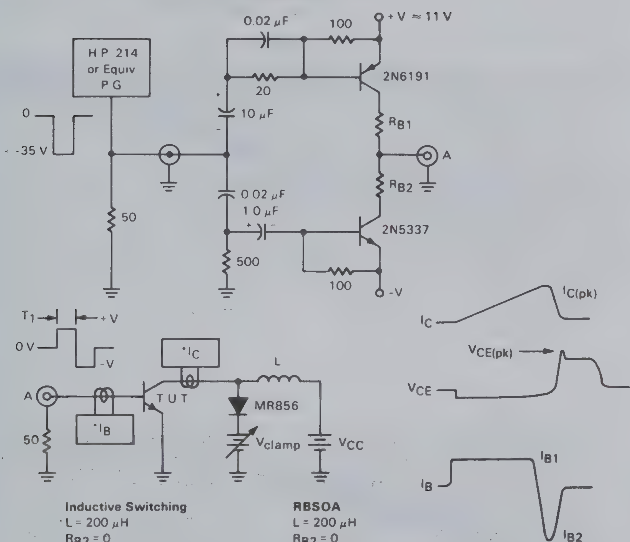


TABLE 1 — RESISTIVE LOAD SWITCHING



*Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



$T_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

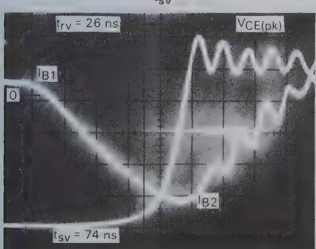
*Tektronix
P-6042 or
Equivalent

Scope - Tektronix
7403 or
Equivalent

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

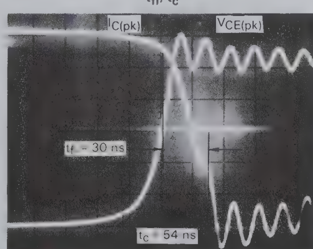
TYPICAL INDUCTIVE SWITCHING WAVEFORMS

t_{sv}



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.4 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base =
20 ns/cm

t_{fi}, t_c



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.4 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base =
20 ns/cm

1.3

THERMAL RESPONSE

FIGURE 20 — 2N6833

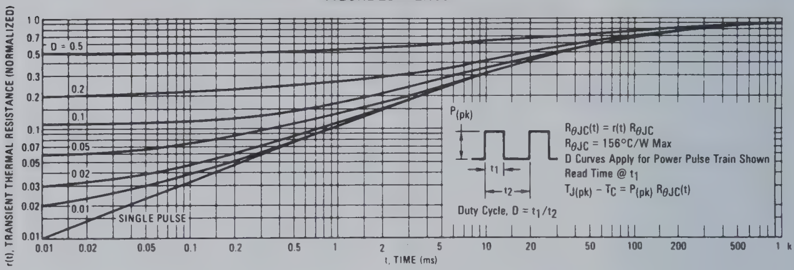
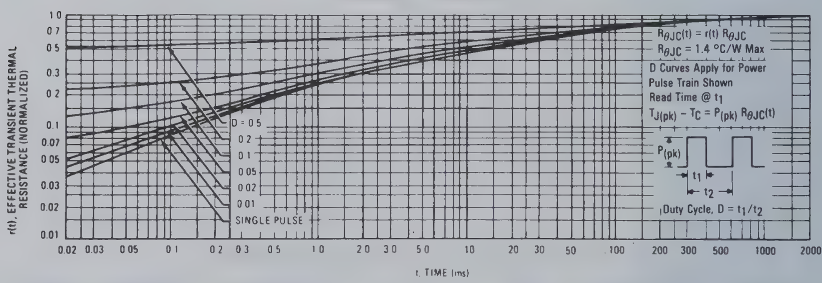


FIGURE 21 — 2N6834



MOTOROLA

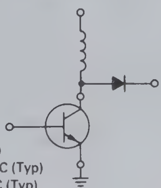
1.3

Designer's Data Sheet

SWITCHMODE III SERIES
ULTRA-FAST NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

- Switching Regulators
- Inverters
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  - 90 ns Inductive Fall Time — 75°C (Typ)
  - 90 ns Inductive Crossover Time — 75°C (Typ)
  - 450 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



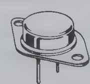
8 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



*MAXIMUM RATINGS

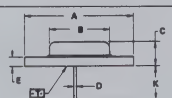
Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8.0 16	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6.0 12	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 85.5 0.86	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*THERMAL CHARACTERISTICS

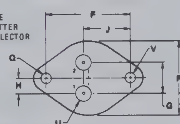
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5.0 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

*Indicate JEDEC Registered Data



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR



NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

⌖	⌀ 13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS

⌖	⌀.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1 550
B	–	21.08	–	0.830
C	6 35	7.62	0 250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0 055	0 070
F	30.15 BSC		1 187 BSC	
G	10 92 BSC		0 430 BSC	
H	5 46 BSC		0 215 BSC	
J	16 89 BSC		0.665 BSC	
K	11 18	12.19	0 440	0 480
Q	3 81	4.19	0 150	0 165
R	–	26.67	–	1,050
U	4 83	5.33	0 190	0.210
V	3.81	4 19	0 150	0.165

CASE 1-05
TO-204AA Type
(TO-3 Type)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.25*	
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5*	
Collector Cutoff Current (V_{CE} = 850 Vdc, $R_{BE(off)}$ = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0*	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 3.0 Adc, I_B = 0.40 Adc)		—	—	1.2	
(I_C = 5.0 Adc, I_B = 0.66 Adc)		—	—	2.5*	
(I_C = 5.0 Adc, I_B = 0.66 Adc, T_C = 100°C)		—	—	3.0*	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 5.0 Adc, I_B = 0.66 Adc)		—	—	1.5*	
(I_C = 5.0 Adc, I_B = 0.66 Adc, T_C = 100°C)		—	—	1.5	
DC Current Gain	h_{FE}				—
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)		7.5*	—	30*	
(I_C = 8.0 Adc, V_{CE} = 5.0 Vdc)		4.0*	—	—	
DYNAMIC CHARACTERISTICS (2)					
Current Gain - Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.25 Adc, f_{test} = 10 MHz)	f_T	10*	—	75*	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	50*	—	350*	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 5.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.66 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 1.3 Adc, R_{B2} = 4.0 Ω)	t_d	—	20	50*	ns
Rise Time			t_r	—	85	250*	
Storage Time			t_s	—	1000	2500*	
Fall Time			t_f	—	70	250*	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	500	—	
Fall Time			t_f	—	100	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 5.0 Adc, I_{B1} = 0.66 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	700	1800*	ns
Fall Time			t_{fi}	—	80	200*	
Crossover Time			t_c	—	150	250*	
Storage Time		(T_C = 150°C)	t_{sv}	—	800	—	
Fall Time			t_{fi}	—	80	—	
Crossover Time			t_c	—	200	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.
(2) $f_T = |h_{fe}| \cdot f_{test}$
*Indicates JEDEC Registered Limit

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

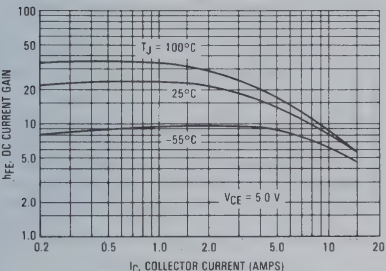


FIGURE 2 — COLLECTOR SATURATION REGION

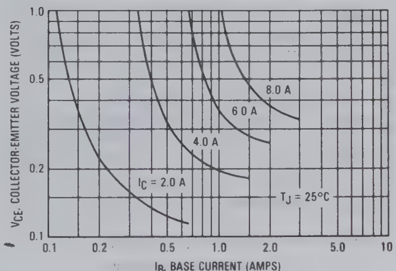


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

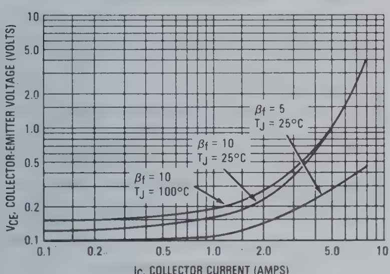


FIGURE 4 — BASE-EMITTER VOLTAGE

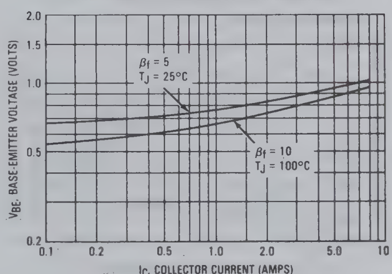


FIGURE 5 — COLLECTOR CUTOFF REGION

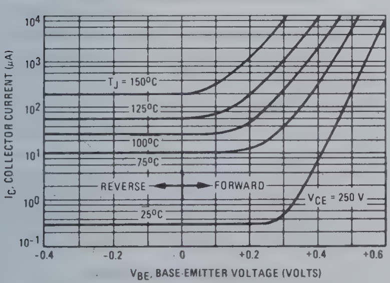
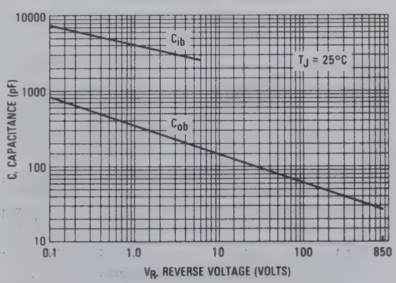


FIGURE 6 — CAPACITANCE



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TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

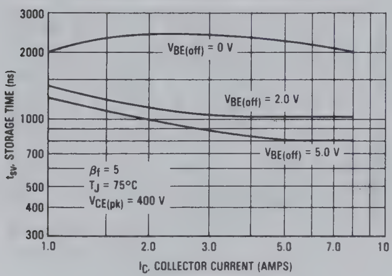


FIGURE 8 — STORAGE TIME

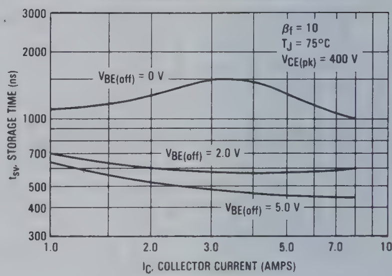


FIGURE 9 — COLLECTOR CURRENT FALL TIME

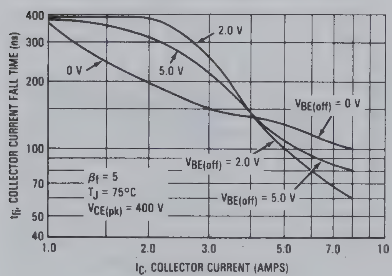


FIGURE 10 — COLLECTOR CURRENT FALL TIME

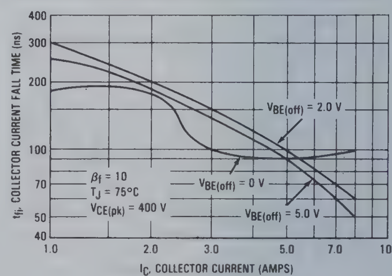


FIGURE 11 — CROSSOVER TIME

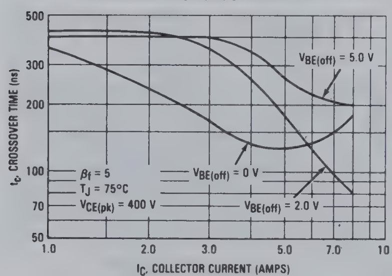


FIGURE 12 — CROSSOVER TIME

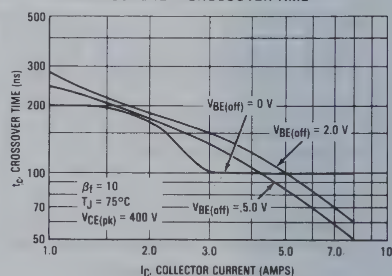


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

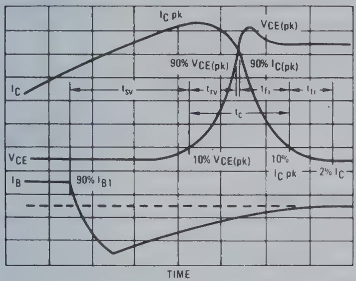
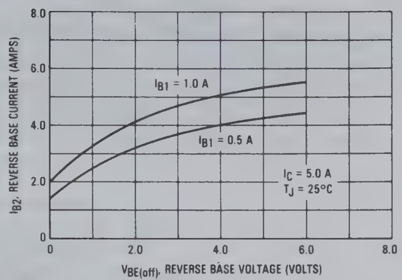


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

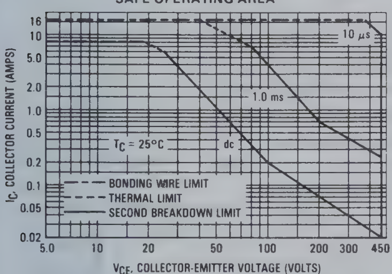
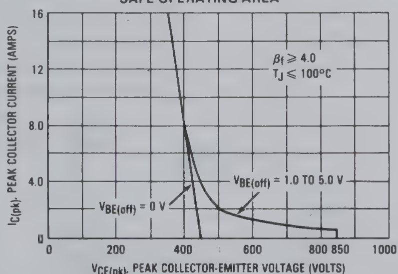


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

1.3

FIGURE 17 — THERMAL RESPONSE

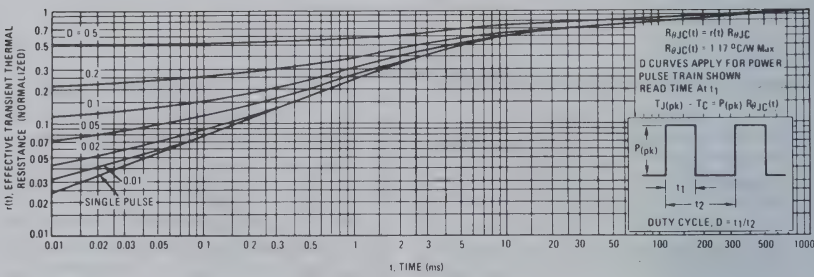


FIGURE 18 — POWER DERATING

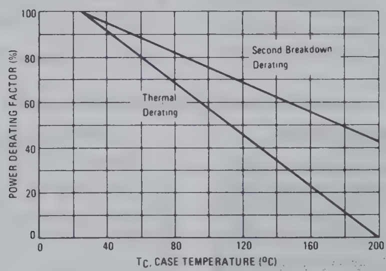
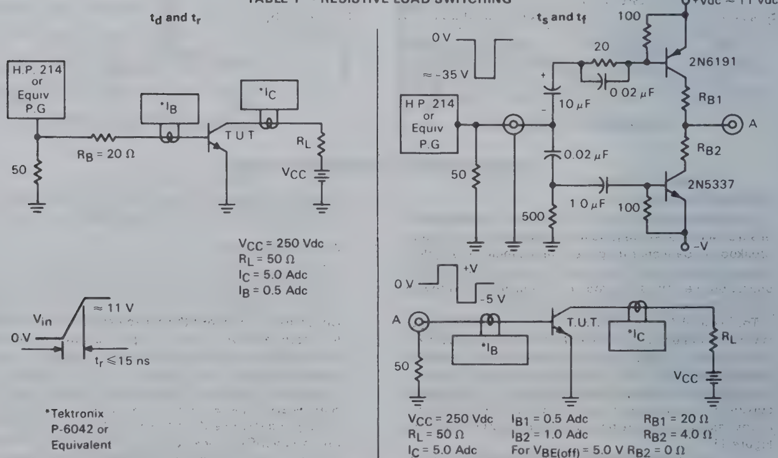
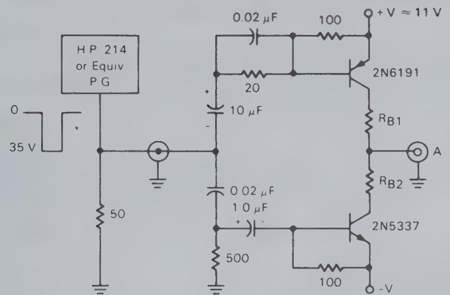


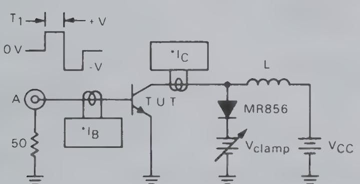
TABLE 1 — RESISTIVE LOAD SWITCHING

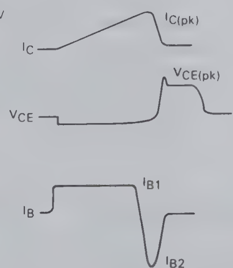


*Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING







$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

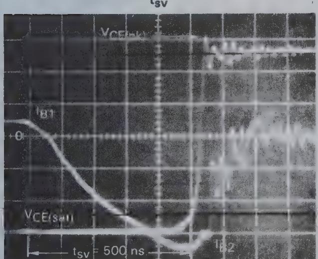
*Tektronix
P-6042 or
Equivalent

Scope - Tektronix
7403 or
Equivalent

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A

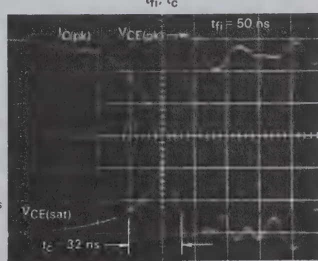
TYPICAL INDUCTIVE SWITCHING WAVEFORMS

t_{sv}



$I_{C(pk)}$ = 5.0 Amps
I_{B1} = 0.5 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base =
100 ns/cm

t_{fi}, t_c



$I_{C(pk)}$ = 5.0 Amps
I_{B1} = 0.5 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base =
20 ns/cm

2N6836

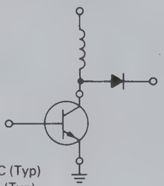
MOTOROLA

1.3

Designer's Data Sheet

SWITCHMODE III SERIES
ULTRA-FAST NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.



- Switching Regulators
- Inverters
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  - 30 ns Inductive Fall Time — 75°C (Typ)
  - 50 ns Inductive Crossover Time — 75°C (Typ)
  - 600 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range −65 to +200°C
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

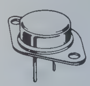
15 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



*MAXIMUM RATINGS

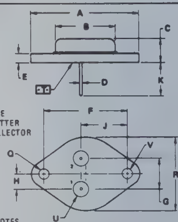
Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5.0 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

*Indicate JEDEC Registered Data



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES.
1. DIMENSIONS Q AND V ARE DATUMS.
2. [-T-] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS
   ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA Type
(TO-3 Type)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)							
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			I_{CEV}	— —	— —	0.25* 1.5*	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	1.0*	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 15*			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 16			
ON CHARACTERISTICS (1)							
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.7 Adc) (I_C = 10 Adc, I_B = 1.3 Adc) (I_C = 10 Adc, I_B = 1.3 Adc, T_C = 100°C)			$V_{CE(sat)}$	— — —	— — —	1.2 2.5* 3.0*	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.3 Adc) (I_C = 10 Adc, I_B = 1.3 Adc, T_C = 100°C)			$V_{BE(sat)}$	— —	— —	1.5* 1.5	Vdc
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)			h_{FE}	7.5* 5.0*	— —	30* —	—
DYNAMIC CHARACTERISTICS (2)							
Current Gain - Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.25 Adc, f_{test} = 10 MHz)			f_T	10*	—	75*	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	50*	—	400*	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.3 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 2.6 Adc, R_{B2} = 1.6 Ω)	t_d	—	20	100*	ns
Rise Time			t_r	—	200	500*	
Storage Time			t_s	—	1200	3000*	
Fall Time			t_f	—	200	350*	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	650	—	
Fall Time			t_f	—	80	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.3 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	800	1800*	ns
Fall Time			t_{fi}	—	50	200*	
Crossover Time			t_c	—	90	250*	
Storage Time		(T_C = 150°C)	t_{sv}	—	1050	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.
(2) $f_T = |h_{fe}| \cdot f_{test}$
*Indicates JEDEC Registered Limit

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

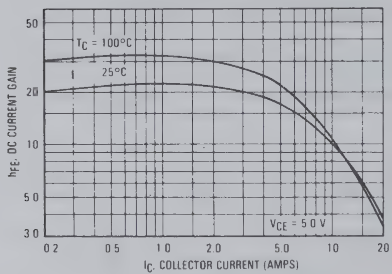


FIGURE 2 — COLLECTOR SATURATION REGION

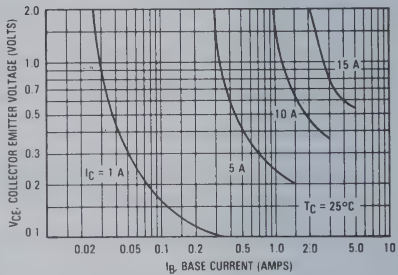


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

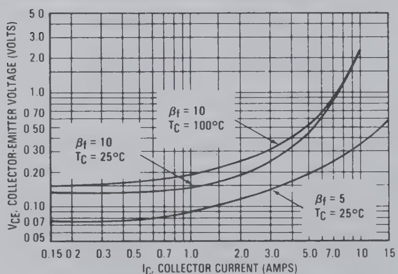


FIGURE 4 — BASE-EMITTER VOLTAGE

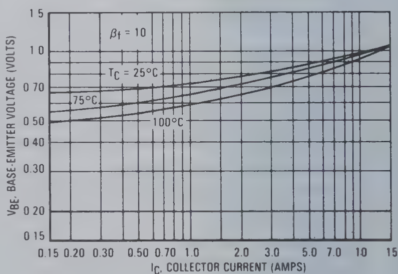


FIGURE 5 — COLLECTOR CUTOFF REGION

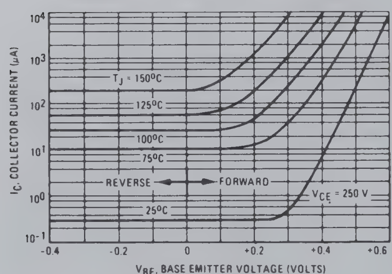
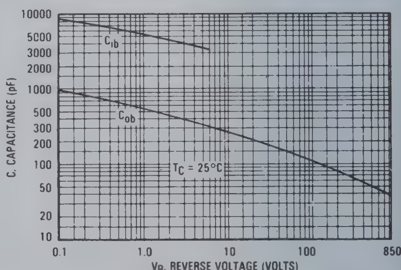


FIGURE 6 — CAPACITANCE



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TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

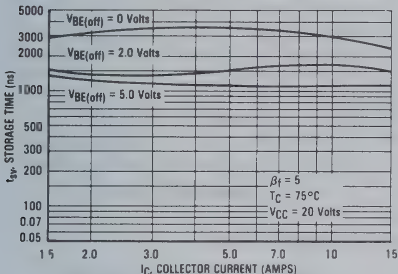


FIGURE 8 — STORAGE TIME

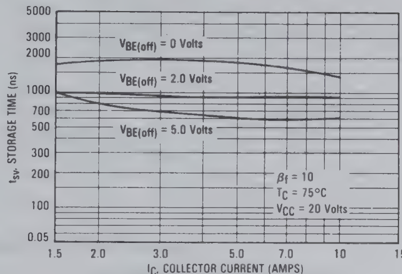


FIGURE 9 — COLLECTOR CURRENT FALL TIME

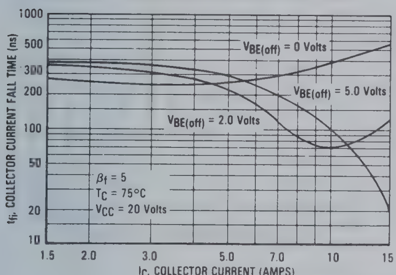


FIGURE 10 — COLLECTOR CURRENT FALL TIME

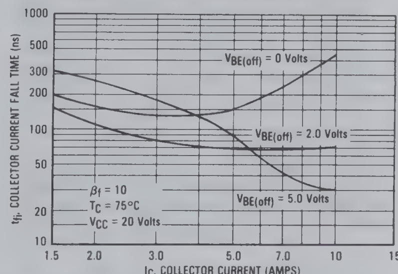


FIGURE 11 — CROSSOVER TIME

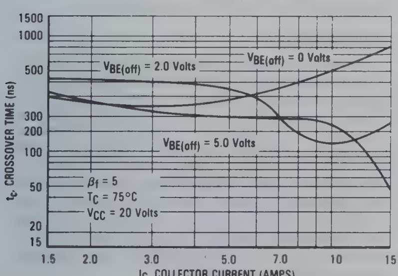


FIGURE 12 — CROSSOVER TIME

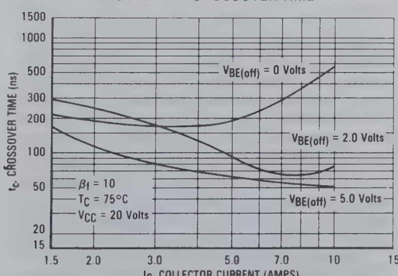


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

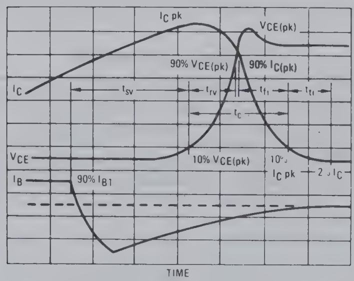
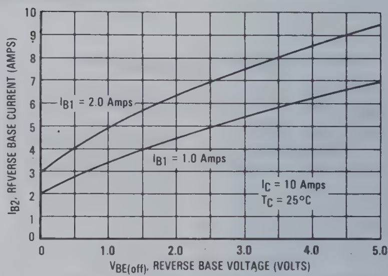


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

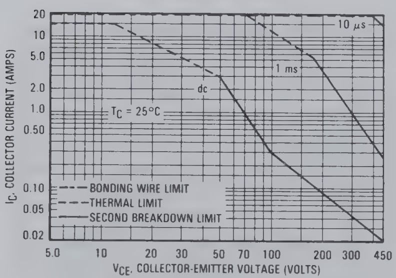
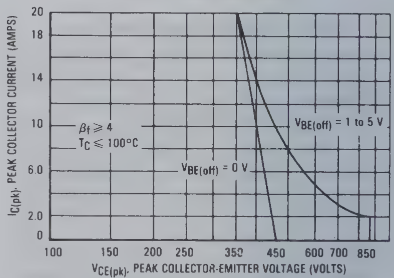


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

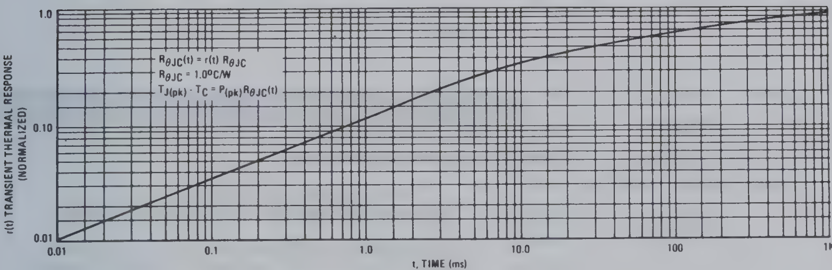


FIGURE 18 — POWER DERATING

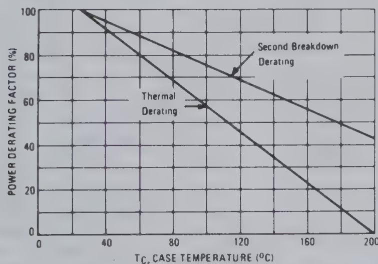
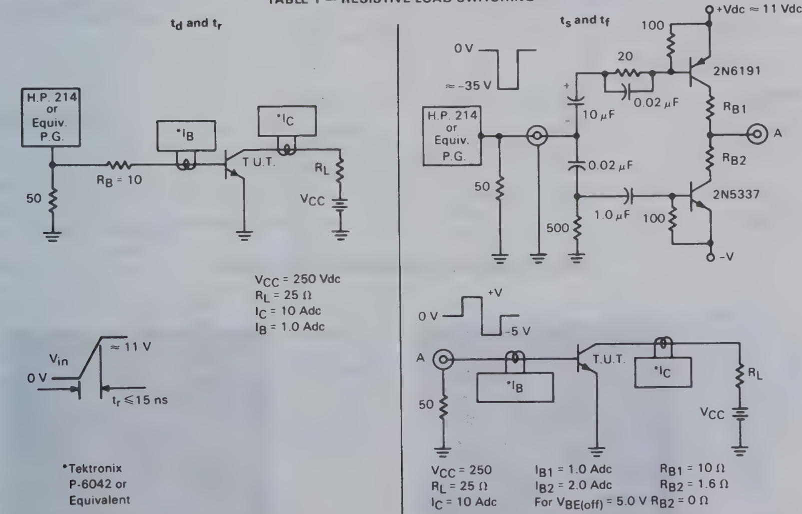


TABLE 1 — RESISTIVE LOAD SWITCHING



*Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

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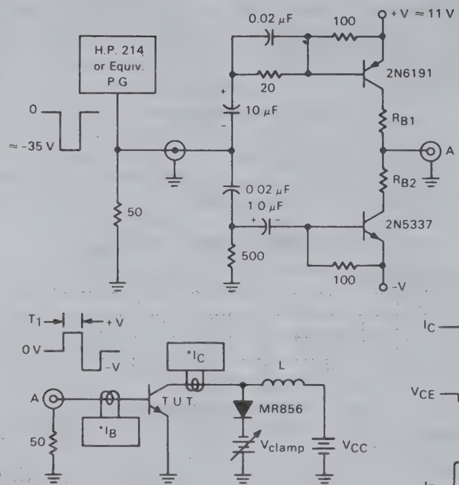
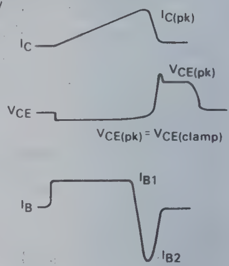
TABLE 2 — INDUCTIVE LOAD SWITCHING





$T_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
$L = 10$ mH
$R_{B2} = \infty$
$V_{CC} = 20$ Volts

Inductive Switching
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

RBSOA
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

*Tektronix
P-6042 or
Equivalent

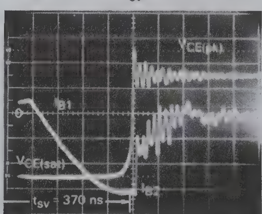
Scope - Tektronix
7403 or
Equivalent

Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

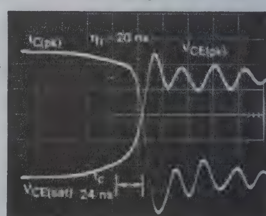
$I_{C(pk)} = 10$ Amps
$I_{B1} = 1.0$ Amp
$V_{BE(off)} = 5.0$ Volts
$V_{CE(pk)} = 400$ Volts
$T_C = 25°C$
Time Base = 100 ns/cm

t_{sv}



$I_{C(pk)} = 10$ Amps
$I_{B1} = 1.0$ Amp
$V_{BE(off)} = 5.0$ Volts
$V_{CE(pk)} = 400$ Volts
$T_C = 25°C$
Time Base = 20 ns/cm

t_{fi}, t_c



MOTOROLA

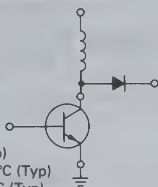
Designer's Data Sheet

SWITCHMODE III SERIES
ULTRA-FAST NPN SILICON POWER TRANSISTORS

This transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  30 ns Inductive Fall Time — 75°C (Typ)
  40 ns Inductive Crossover Time — 75°C (Typ)
  800 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range −65 to +200°C
- 100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents



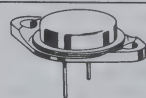
20 AMPERE

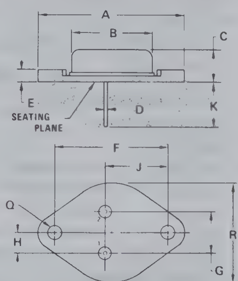
NPN SILICON POWER TRANSISTORS

450 VOLTS
250 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-204AE (Type) Modified TO-3

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage*	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage*	V_{CEV}	850	Vdc
Emitter Base Voltage*	V_{EB}	6.0	Vdc
Collector Current — Continuous* — Peak (1)	I_C I_{CM}	20 30	Adc
Base Current — Continuous* — Peak (1)	I_B I_{BM}	15 20	Adc
Total Power Dissipation @ T_C = 25°C* @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43	Watts W/°C
Operating and Storage Junction* Temperature Range	T_J, T_{stg}	−65 to +200	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering* Purposes: ⅛" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
*Indicate JEDEC Registered Data

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.25*	
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5*	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0*	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 1.2 Adc)		—	—	1.5	
(I_C = 15 Adc, I_B = 2.0 Adc)		—	—	3.0*	
(I_C = 15 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	—	3.0*	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 15 Adc, I_B = 2.0 Adc)		—	—	1.5*	
(I_C = 15 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	—	1.5	
DC Current Gain	h_{FE}				—
(I_C = 15 Adc, V_{CE} = 5.0 Vdc)		7.5*	—	30*	
(I_C = 20 Adc, V_{CE} = 5.0 Vdc)		5.0	—	—	
DYNAMIC CHARACTERISTICS (2)					
Current Gain — Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.25 Adc, f_{test} = 10 MHz)	f_T	10*	—	75*	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	100*	—	500*	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 15 Adc, V_{CC} = 250 Vdc, I_{B1} = 2.0 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I_{B2} = 4.0 Adc, R_{B2} = 1.6 Ω)	t_d	—	20	100*	ns
Rise Time			t_r	—	200	500*	
Storage Time			t_s	—	1200	2700*	
Fall Time			t_f	—	200	350*	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	650	—	
Fall Time			t_f	—	80	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 15 Adc, I_{B1} = 2.0 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	800	2700*	ns
Fall Time			t_{fi}	—	50	200*	
Crossover Time			t_c	—	90	250*	
Storage Time		(T_C = 150°C)	t_{sv}	—	1050	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: PW — 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{FE}| f_{test}$
*Indicates JEDEC Registered Limit

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

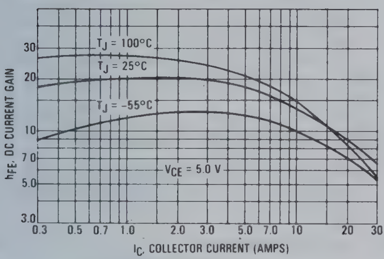


FIGURE 2 — COLLECTOR SATURATION REGION

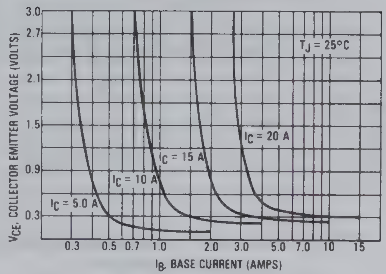


FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION

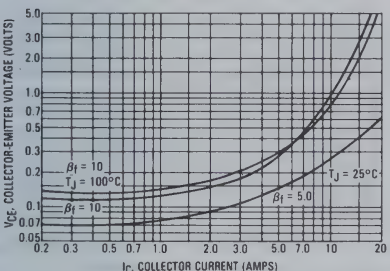


FIGURE 4 — BASE-EMITTER VOLTAGE

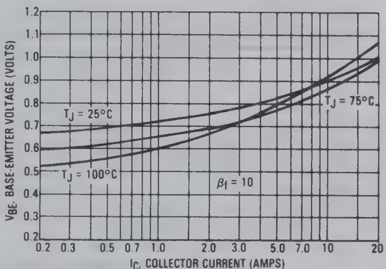


FIGURE 5 — COLLECTOR CUTOFF REGION

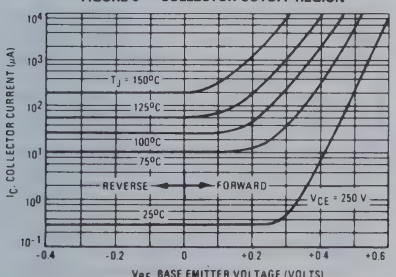
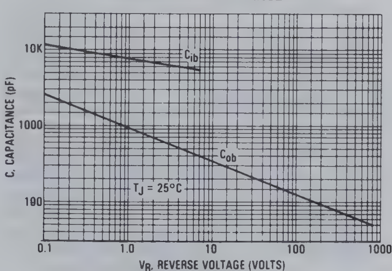


FIGURE 6 — CAPACITANCE



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TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

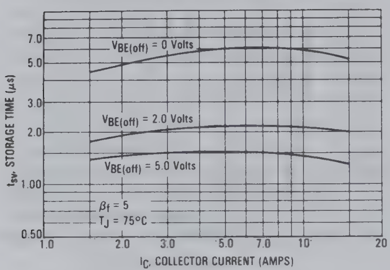


FIGURE 8 — STORAGE TIME

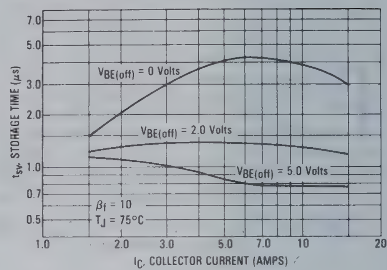


FIGURE 9 — COLLECTOR CURRENT FALL TIME

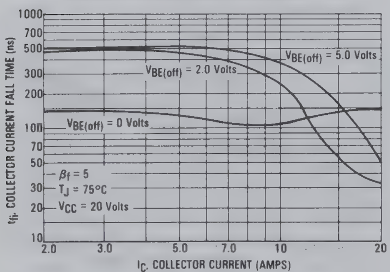


FIGURE 10 — COLLECTOR CURRENT FALL TIME

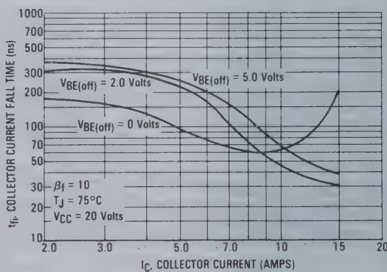


FIGURE 11 — CROSSOVER TIME

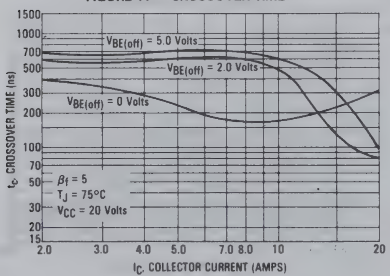


FIGURE 12 — CROSSOVER TIME

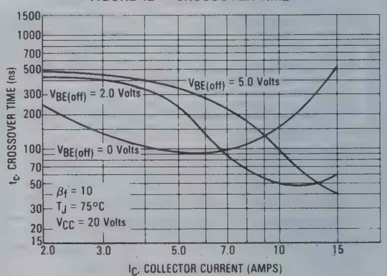


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

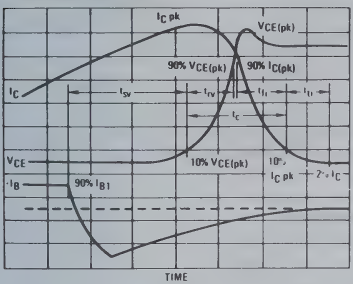
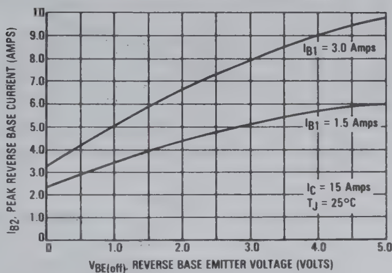


FIGURE 14 — REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

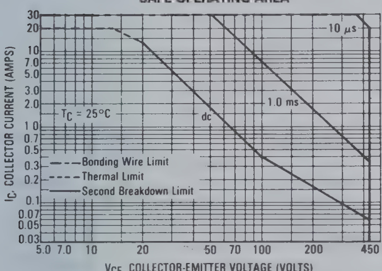
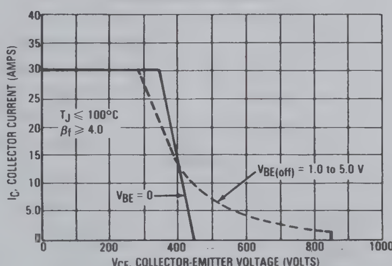


FIGURE 16 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

1.3

FIGURE 17 — THERMAL RESPONSE

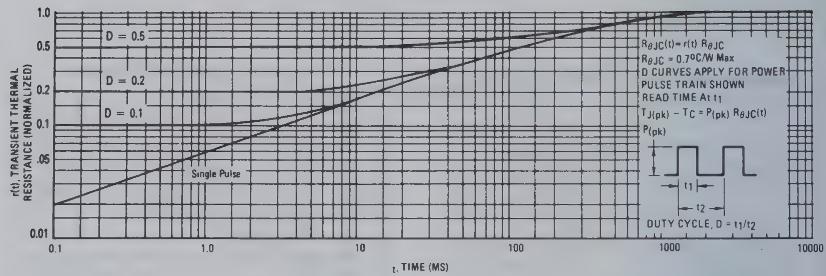


FIGURE 18 — POWER DERATING

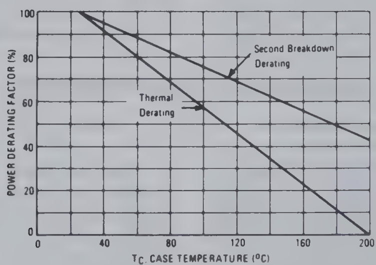
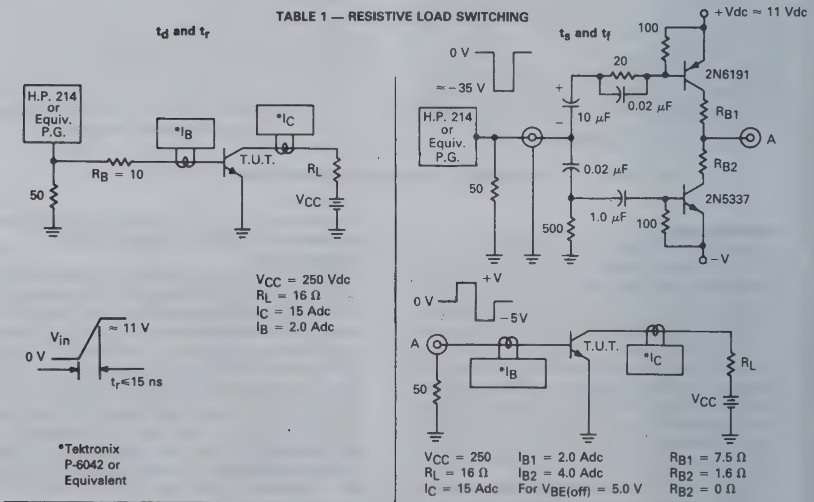
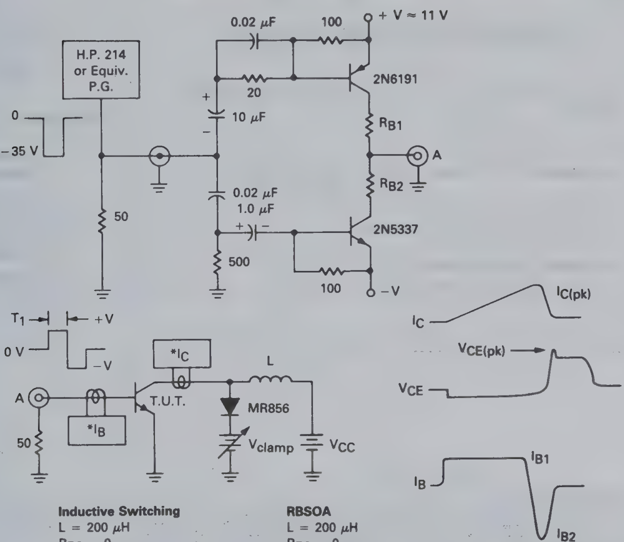


TABLE 1 — RESISTIVE LOAD SWITCHING



*Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



$T_1 \approx \frac{L_{coil}\,(C_{pk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
$L = 10$ mH
$R_{B2} = \infty$
$V_{CC} = 20$ Volts

*Tektronix
P-6042 or
Equivalent

Inductive Switching
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

Scope — Tektronix
7403 or
Equivalent

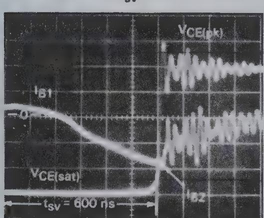
RBSOA
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

Note: Adjust — V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

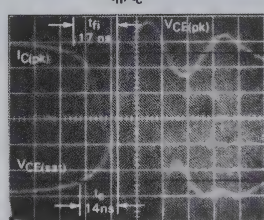
t_{sv}

$I_{C(pk)} = 15$ A
$I_{B1} = 2.0$ A
$V_{BE(off)} = 5.0$ Volts
$V_{CE(pk)} = 400$ Volts
$T_C = 25°C$
Time Base = 200 ns/cm



t_{fi}, t_c

$I_{C(pk)} = 15$ A
$I_{B1} = 2.0$ A
$V_{BE(off)} = 5.0$ Volts
$V_{CE(pk)} = 400$ Volts
$T_C = 25°C$
Time Base = 200 ns/cm



BU204
BU205

MOTOROLA

1.3

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage — V_{CEX} = 1300 Vdc — BU204
  1500 Vdc — BU205
- Glassivated Base-Collector Junction
- Switching Times with Inductive Loads —
  t_f = 0.65 μs (Typ) @ I_C = 2A

2.5 AMPERE

NPN SILICON POWER TRANSISTORS

1300 AND 1500 VOLTS
36 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

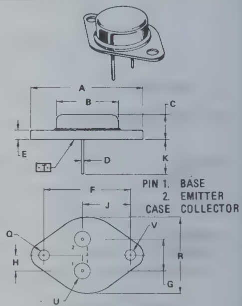
MAXIMUM RATINGS

Rating	Symbol	BU204	BU205	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	600	700	Vdc
Collector-Emitter Voltage	V_{CEX}	1300	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	2.5 3		Adc
Base Current — Peak (1)	I_{BM}	2.5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 90°C Derate above 25°C	P_D	36 10 0.4		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +115		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	∅ 13 (0 005) Ⓜ	T	V Ⓜ

FOR LEADS

⌖	∅.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37		1 550
B		21.08		0 830
C	6.35	7.62	0 250	0 300
D	0.97	1 09	0.038	0 043
E	1.40	1.78	0.055	0 070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3 81	4 19	0.150	0.165
R	-	26.67		1 050
U	4.83	5.33	0.190	0.210
V	3.81	4 19	0.150	0.165

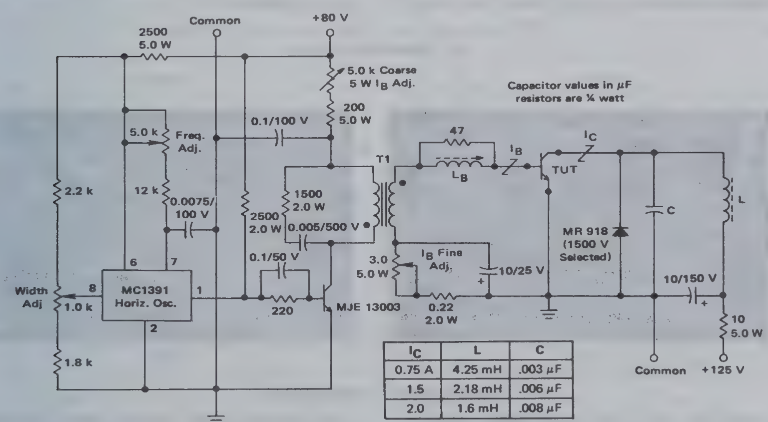
CASE 1-05

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	BU204 BU205	$V_{CEO(sus)}$	600 700	– –	– –	Vdc
Collector Cutoff Current (V_{CE} = 1300 Vdc, V_{BE} = 0) (V_{CE} = 1500 Vdc, V_{BE} = 0)	BU204 BU205	I_{CES}	– –	– –	1.0 1.0	mAdc
Emitter Base Voltage (I_E = 10 mA, I_C = 0)		V_{EBO}	5.0	–	–	Vdc
ON CHARACTERISTICS (1)						
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	–	–	5.0	Vdc
Base Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased		$I_{S/B}$	See Figure 14			
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (1) (I_C =0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)		f_T	–	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	50	–	pF
SWITCHING CHARACTERISTICS						
Fall Time (I_C = 2.0 Adc, I_{B1} = 1.0 Adc, L_B = 25 μH) (See Figure 1)		t_f	–	0.65	–	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 1 — TEST CIRCUIT



I_C	L	C
0.75 A	4.25 mH	.003 μF
1.5	2.18 mH	.006 μF
2.0	1.6 mH	.008 μF

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance — 39 mH. Secondary Inductance — 22 mH, Leakage Inductance with primary shorted — 2.0 μH, Primary 260 turns #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

1.3

BASE DRIVE: The Key to Performance

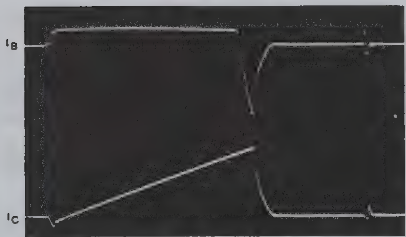
By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1}\ h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1}\ h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation $I_{B1}\ h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

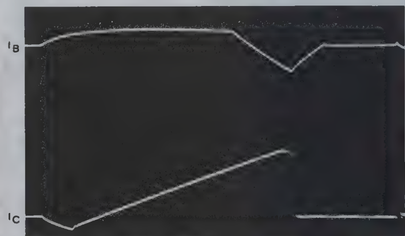
TEST CIRCUIT WAVEFORMS

FIGURE 2



(time)

FIGURE 3



(time)

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 — OPTIMIZING DRIVE @ I_C = 0.75 A

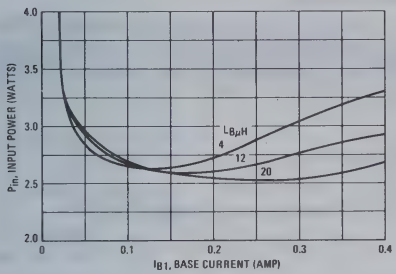


FIGURE 5 — OPTIMIZING DRIVE @ I_C 1.5 A

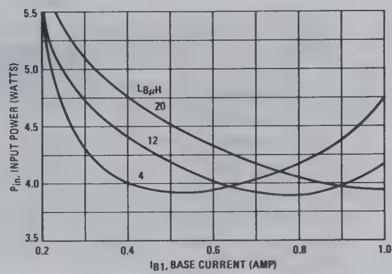


FIGURE 6 — OPTIMIZING DRIVE @ I_C = 2.0 A

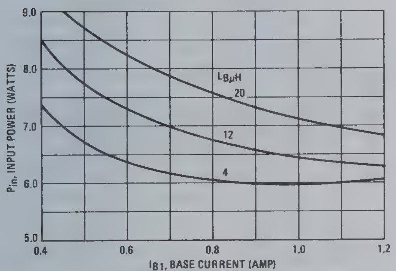


FIGURE 7 — SWITCHING BEHAVIOR versus TEMPERATURE

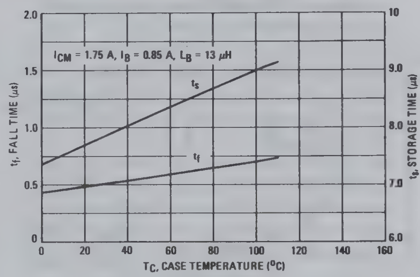


FIGURE 8 — OPTIMUM DRIVE CONDITIONS

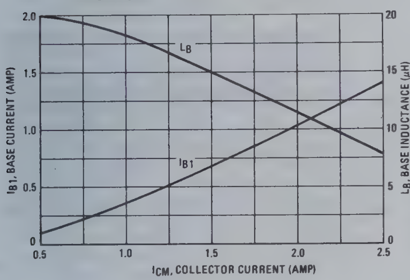
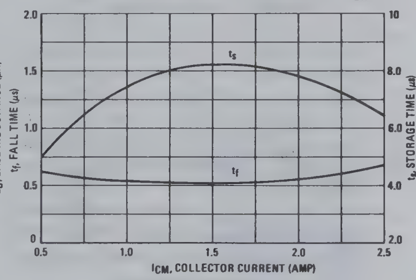


FIGURE 9 — SWITCHING BEHAVIOR versus I_{CM}



1.3

FIGURE 10 – THERMAL RESPONSE

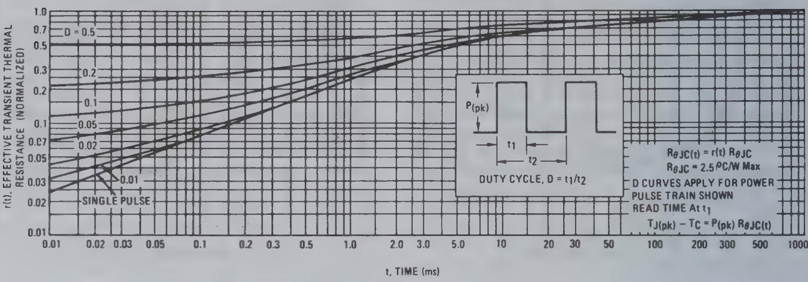


FIGURE 11 – COLLECTOR SATURATION REGION

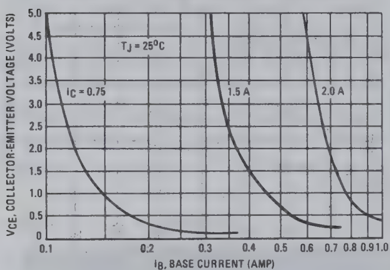


FIGURE 12 – DC CURRENT GAIN

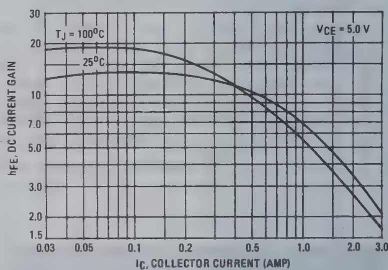


FIGURE 13 – "ON" VOLTAGES

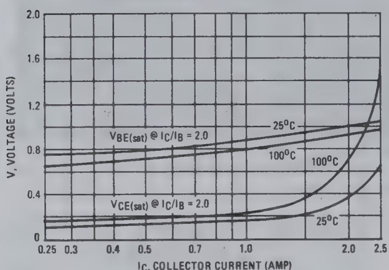
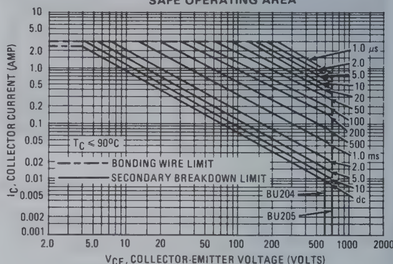


FIGURE 14-MAXIMUM FORWARD BIAS SAFE OPERATING AREA



BU207
BU208

MOTOROLA

1.3

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in large screen color deflection circuits.

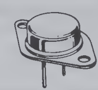
- Collector-Emitter Voltage —
  V_{CEX} = 1300 Vdc — BU207
  1500 Vdc — BU208
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 600 Vdc — BU207
  700 Vdc — BU208
- Switching Times with Inductive Loads, t_f = 0.4 μs (Typ) @ I_C = 4.5 A
- Optimum Drive Condition Curves
- Glass Base-Collector Junction

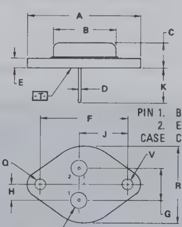
5 AMPERE
NPN SILICON
POWER TRANSISTORS

1300 AND 1500 VOLTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.





PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	·	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

*MAXIMUM RATINGS

Rating	Symbol	BU207	BU208	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	600	700	Vdc
Collector-Emitter Voltage	V_{CEX}	1300	1500	Vdc
Emitter Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	5 7.5		Adc
Base Current — Peak (1)	I_{BM}	4		Adc
Total Power Dissipation @ T_C = 95°C Derate above 95°C	P_D	12.5 0.625		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +115		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.6	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

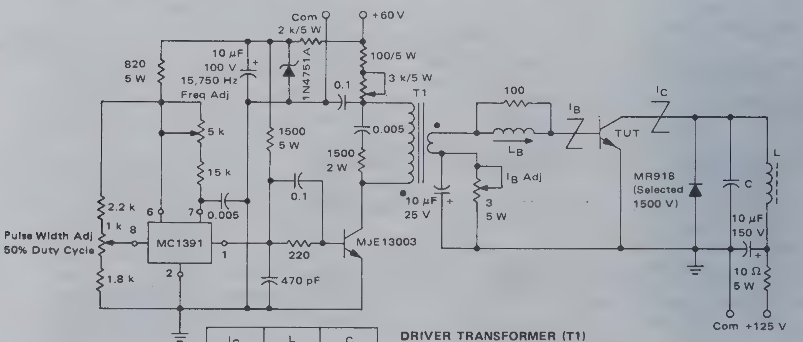
1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^o$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	BU207	$V_{CEO(sus)}$	600	–	–	Vdc
	BU208		700	–	–	
Collector Cutoff Current (V_{CE} = 1300 Vdc, V_{BE} = 0)	BU207	I_{CES}	–	–	1.0	mAdc
(V_{CE} = 1500 Vdc, V_{BE} = 0)	BU208		–	–	1.0	
Emitter Base Voltage (I_E = 10 mA, I_C = 0)		V_{EBO}	5.0	–	–	Vdc
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 4.5 Adc, V_{CE} = 5 Vdc)		h_{FE}	2.25	–	–	–
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)		$V_{CE(sat)}$	–	–	5	Vdc
Base Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)		$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$		See Figure 14		
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1 MHz)		f_T	–	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	125	–	pF
SWITCHING CHARACTERISTICS						
Fall Time	(I_C = 4.5 Adc, I_B = 1.8 Adc, L_B = 10 μH, see Figure 1)	t_f	–	0.6	–	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



I_C A	L mH	C μF
3.5	0.87	0.013
4.5	0.67	0.017

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance — 39 mH, Secondary Inductance — 0.22 mH, Leakage Inductance with primary shorted — 2.0 μH. Primary 260 turns, #28 AWG enamel wire, Secondary .17 turns, #22 AWG enamel wire.

1.3

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1}\ h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1}\ h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor *initiation* of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation $I_{B1}\ h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

TEST CIRCUIT WAVEFORMS

FIGURE 2

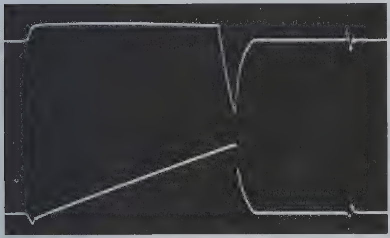
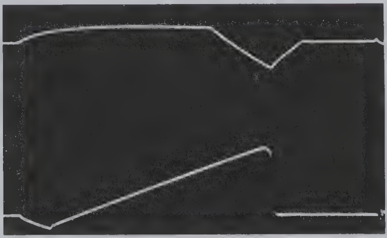


FIGURE 3



TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

1.3

FIGURE 4 – OPTIMIZING DRIVE @ I_C = 3.5 A

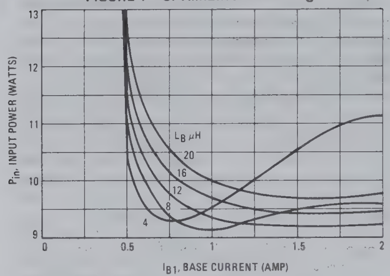


FIGURE 5 – OPTIMIZING DRIVE @ I_C = 4.5 A

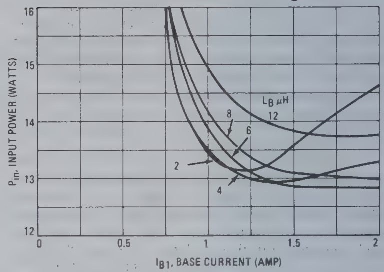


FIGURE 6 – SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 3.5 A, I_B = 1.5 A, L_B = 14 µH

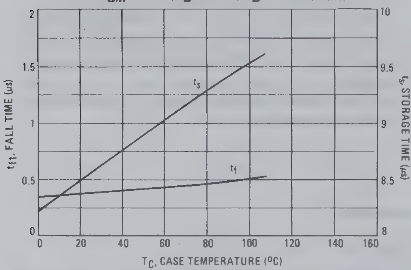


FIGURE 7 – SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 4.5 A, I_B = 1.75 A, L_B = 8 µH

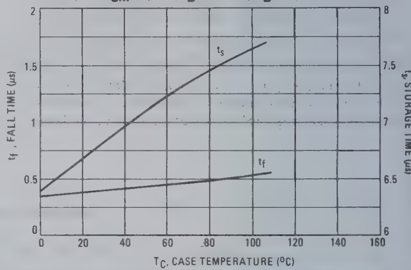


FIGURE 8 – OPTIMUM DRIVE CONDITIONS

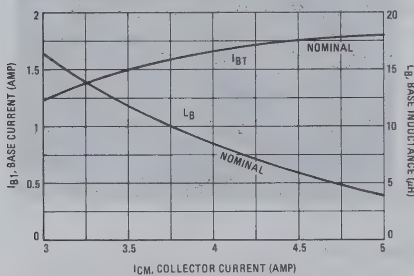


FIGURE 9 – SWITCHING BEHAVIOR versus I_{CM}

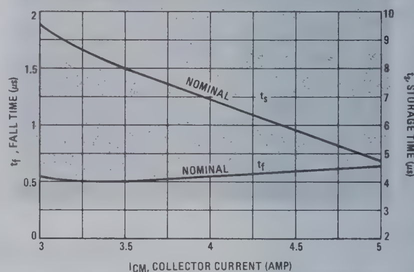


FIGURE 10 – THERMAL RESPONSE

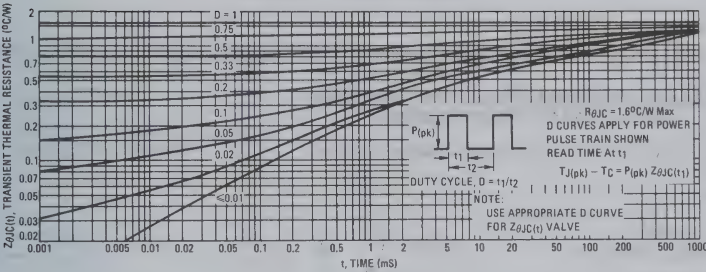


FIGURE 11 – COLLECTOR SATURATION REGION

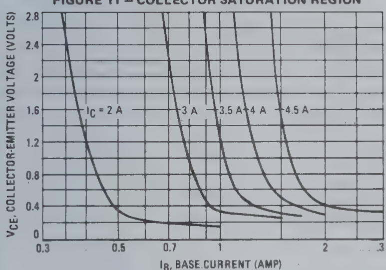


FIGURE 12 – DC CURRENT GAIN

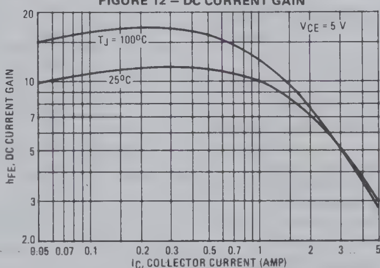


FIGURE 13 – "ON" VOLTAGES

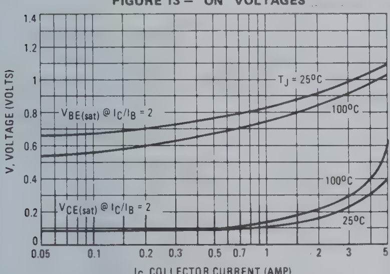
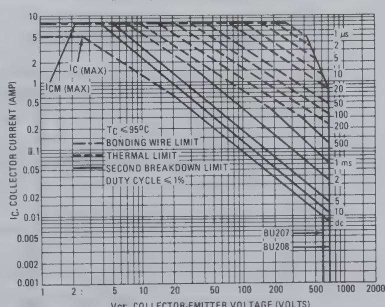


FIGURE 14-MAXIMUM FORWARD BIAS
SAFE OPERATING AREA



BU2208D

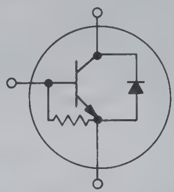
MOTOROLA

1.3

NPN SILICON HORIZONTAL DEFLECTION TRANSISTOR WITH INTEGRATED DAMPER DIODE

. . . specifically designed for use in large screen color deflection circuits

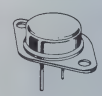
- V_{CES} = 1500 V; $V_{CEO(sus)}$ = 700 V (min)
- Low saturation: $V_{CE(sat)}$ = 1.0 V (max) @ I_C = 4.5 Adc



5 AMPERES

NPN SILICON POWER TRANSISTORS

1500 VOLTS
60 WATTS



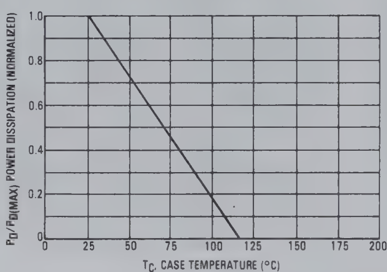
MAXIMUM RATINGS

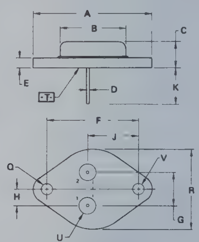
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	700	Vdc
Collector-Emitter Voltage (R_{BE} = 0)	V_{CES}	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C I_{CM}	5.0 7.5	Adc
Base Current — Peak	I_B	3.5	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	60 0.666	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 115	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅0.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA (Type)
(Formerly TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0, L = 25 mH, V_{clamp} = 800 V)		$V_{CEO(sus)}$	700	—	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)		I_{CES}	—	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	300	mAdc
ON CHARACTERISTICS (1)					
Diode Forward Voltage (I_F = 4.0 A)		V_F	—	2.0	Vdc
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2.0 Adc)		$V_{CE(sat)}$	—	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2.0 Adc)		$V_{BE(sat)}$	—	1.5	Vdc
SWITCHING CHARACTERISTICS (Inductive Load)					
Fall Time	(I_C (end) = 4.5 Adc, V_{CC} = 140 Vdc, I_B (end) = 1.8 A, L_C = 0.9 mH, L_B = 10 μH)	t_f	—	0.6 (typ)	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 3%.

BU406
BU407

MOTOROLA

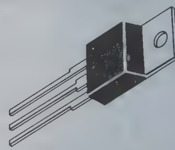
1.3

NPN POWER TRANSISTORS

These devices are high voltage, high speed transistors for horizontal deflection output stages of TV's and CRT's.

- High Voltage:
  V_{CEV} = 330 or 400 V
- Fast Switching Speed:
  t_f = 750 ns (max)
- Low Saturation Voltage:
  $V_{CE(sat)}$ = 1.0 V (max) @ 5.0 A
- Packaged in Compact JEDEC TO-220AB

7.0 AMPERE
NPN SILICON
POWER TRANSISTORS
60 WATTS
150 and 200 VOLTS

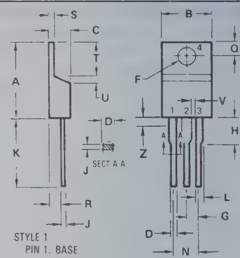


MAXIMUM RATINGS

Rating	Symbol	BU406	BU407	Unit
Collector-Emitter Voltage	V_{CEO}	200	150	Vdc
Collector-Emitter Voltage	V_{CEV}	400	330	Vdc
Collector-Base Voltage	V_{CBO}	400	330	Vdc
Emitter Base Voltage	V_{EBO}	6.0		Vdc
Collector Current — Continuous Peak Repetitive Peak (10 ms)	I_C	7.0 10 15		Adc
Base Current	I_B	4.0		Adc
Total Device Dissipation, T_C = 25°C Derate above T_C = 25°C	P_D	60 0.48		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5.0 Seconds	T_L	275	°C



STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES
1. DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
5. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage(1) (I_C = 100 mAdc, I_B = 0)	BU406 BU407	$V_{CEO(sus)}$	200 150	— —	— —	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, V_{BE} = 0) (V_{CE} = Rated V_{CEO} + 50 Vdc, V_{BE} = 0) (V_{CE} = Rated V_{CEO} + 50 Vdc, V_{BE} = 0, T_C = 150°C)		I_{CES}	— — —	— — —	5.0 0.1 1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	1.0	mAdc
ON CHARACTERISTICS (1)						
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	—	—	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc		$V_{BE(sat)}$	—	—	1.2	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 20 MHz)		f_T	10	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	80	—	pF
SWITCHING CHARACTERISTICS						
Inductive Load Crossover Time (V_{CC} = 40 Vdc, I_C = 5.0 Adc, I_{B1} = I_{B2} = 0.5 Adc, L = 150 μH)		t_c	—	—	0.75	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 1%.

FIGURE 1 — DC CURRENT GAIN

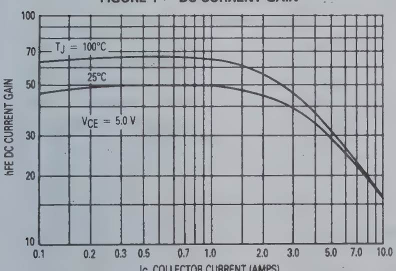
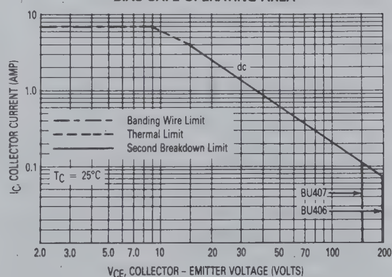


FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



BU806
BU807

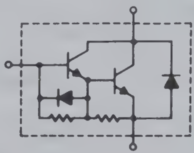
MOTOROLA

1.3

NPN DARLINGTON POWER TRANSISTORS

These Darlington transistors are high voltage, high speed devices for horizontal deflection circuits in TV's and CRT's.

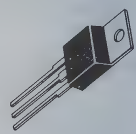
- High Voltage: V_{CEV} = 330 or 400 V
- Fast Switching Speed: t_c = 1.0 μs (max)
- Low Saturation Voltage: $V_{CE(sat)}$ = 1.5 V (max)
- Packaged in JEDEC TO-220AB
- Damper Diode V_F is specified. V_F = 2.0 V (max)

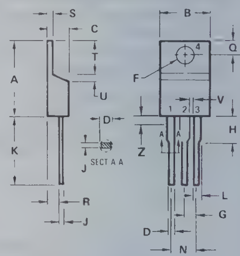


8.0 AMPERE

DARLINGTON NPN POWER TRANSISTORS

60 WATTS
150 and 200 VOLTS





NOTES:
1. DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
5. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	BU806	BU807	Unit
Collector-Emitter Voltage	V_{CEO}	200	150	Vdc
Collector-Emitter Voltage	V_{CEV}	400	330	Vdc
Collector-Base Voltage	V_{CBO}	400	330	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current — Continuous — Peak	I_C	8.0 15		Adc
Emitter-Collector Diode Current	I_F	10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation, T_C = 25°C Derate above T_C = 25°C	P_D	60 0.48		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Lead Temperature for Soldering Purposes, 1/8″ from Case for 5.0 Seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) BU806 (I_C = 100 mAdc, I_B = 0) BU807	$V_{CEO(sus)}$	200 150	— —	— —	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CBO}, V_{BE} = 0)	I_{CES}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 6.0 Vdc)	I_{CEV}	—	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	3.0	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 50 mAdc)	$V_{CE(sat)}$	—	—	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 50 mAdc)	$V_{BE(sat)}$	—	—	2.4	Vdc
Emitter-Collector Diode Forward Voltage (I_F = 4.0 Adc)	V_F	—	—	2.0	Vdc
SWITCHING CHARACTERISTICS					
Turn-On Time (Resistive Load, V_{CC} = 100 Vdc, I_C = 5.0 Adc, I_{B1} = 50 mAdc, I_{B2} = 500 mAdc)	t_{on}	—	0.35	—	μs
Storage Time	t_s	—	0.55	—	μs
Fall Time	t_f	—	0.20	—	μs
Crossover Time (I_C = 5.0 Adc, I_{B1} = 50 mAdc, $V_{BE(off)}$ = 4.0 Vdc, V_{clamp} = 200 Vdc, L = 500 μH)	t_c	—	0.40	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 1%.

FIGURE 1 — DC CURRENT GAIN

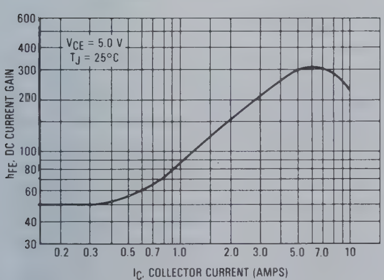
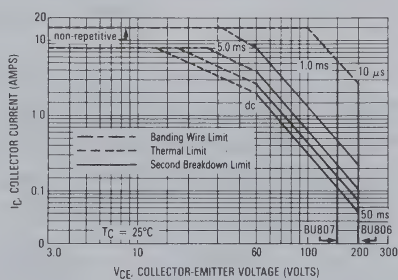


FIGURE 2 — SAFE OPERATING AREA (FBSOA)



D40C1
D40C2
D40C4
D40C5

MOTOROLA

1.3

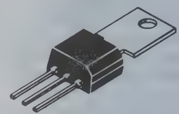
NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for amplifier and driver applications where high gain is an essential requirement, low power lamp and relay drivers and power drivers for high-current applications such as voltage regulators.

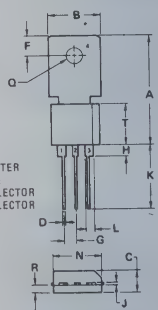
- High DC Current Gain —
  h_{FE} = 40,000 (Min) @ I_C = 200 mAdc — D40C2, 5
- Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 40 Vdc (Min) @ I_C = 10 mAdc — D40C4, 5
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 500 mAdc
- Duowatt Package —
  2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS



Tab forming and TO-5 lead forming available on special request.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

TO-202AC
CASE 306-04

MAXIMUM RATINGS

Rating	Symbol	D40C1,2	D40C4,5	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Emitter Voltage	V_{CES}	30	40	Vdc
Emitter-Base Voltage	V_{EBO}	13		Vdc
Collector Current — Continuous Peak (1)	I_C	0.5 1.0		Adc
Base Current — Continuous	I_B	100		mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C (2)	P_D	1.67 13.3		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	6.25 50		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C
Solder Temperature, 1/16″ from Case for 10 Seconds	—	260		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	°C/W

(1) Pulse Width ≤ 25 ms, Duty Cycle ≤ 50%.
(2) The actual power dissipation capability of Duowatt transistors are 2 W @ T_A = 25°C.

1.3

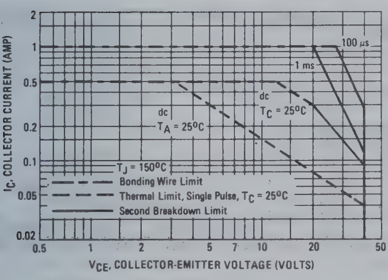
ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, V_{BE} = 0)	D40C1, 2 D40C4, 5	BV_{CEO}	30 40	– –	Vdc
Collector Cutoff Current (V_{CB} = Rated V_{CES}, I_E = 0, T_J = 150°C)		I_{CBO}	–	20	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0)		I_{CES}	–	0.5	μAdc
Emitter Cutoff Current (V_{EB} = 13 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)					
Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	D40C1, 4 D40C2, 5	h_{FE}	10,000 40,000	60,000 –	–
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 0.5 mAdc)		$V_{CE(sat)}$	–	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 0.5 mAdc)		$V_{BE(sat)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	10	pF
High Frequency Current Gain (I_C = 20 mA, V_{CE} = 5 Vdc, f = 100 MHz)		h_{fe}	1.0	–	–
Input Impedance (I_C = 20 mA, V_{CE} = 5 Vdc, f = 1 kHz)		h_{ie}	50	–	Ohms

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

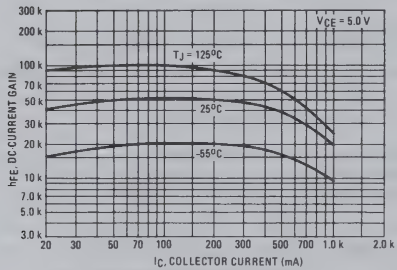


FIGURE 3 – "ON" VOLTAGES

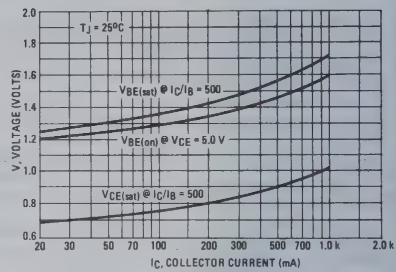


FIGURE 4 – COLLECTOR SATURATION REGION

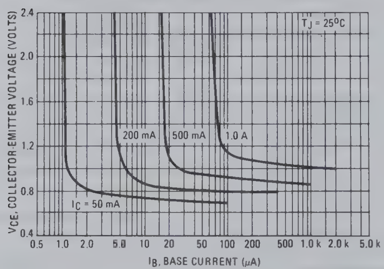


FIGURE 5 – TEMPERATURE COEFFICIENT

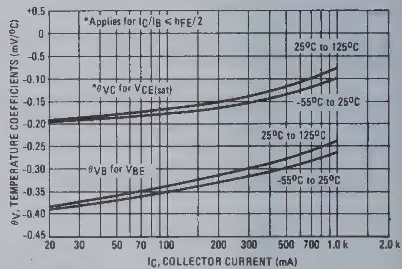
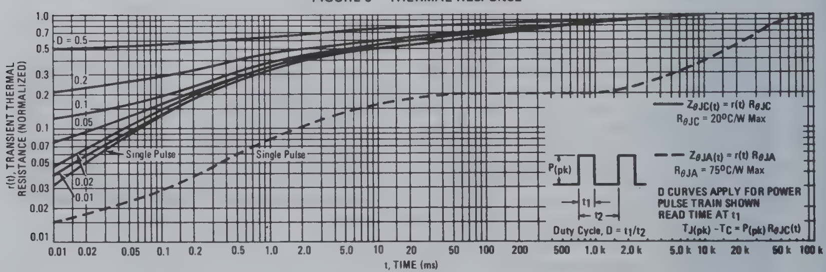


FIGURE 6 – THERMAL RESPONSE



MOTOROLA

NPN
D40D
PNP
D41D

1.3

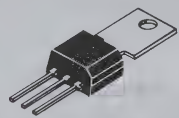
COMPLEMENTARY SILICON ANNULAR AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- Duowatt Package — 2 Watts Free Air Dissipation @ $T_A = 25^oC$

DUOWATT

COMPLEMENTARY SILICON AMPLIFIER TRANSISTORS



Tab forming and TO-5 lead forming available on special request.

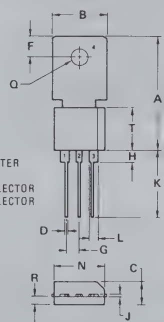
MAXIMUM RATINGS

Rating	Symbol	D40/41D 1,2	D40/41D 4,5	D40/41D 7,8	D40/41D 10,11,13,14	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	60	75	Vdc
Collector-Emitter Voltage	V_{CES}	45	60	75	90	Vdc
Emitter-Base Voltage	V_{EBO}	← 5.0 →				Vdc
Collector Current — Continuous Peak (1)	I_C	← 1.0 → ← 2.0 →				Adc
Base Current	I_B	← 100 →				mAdc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC (2)	P_D	← 1.67 → ← 13.3 →				Watts mW/^oC
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	← 6.25 → ← 50 →				Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −55 to +150 →				^oC
Solder Temperature, 1/16" from Case for 10 Seconds	—	← 260 →				^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^oC/W$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	$^oC/W$

(1) Pulse Test: Pulse Width $\leq$ 300 μs.
(2) The actual power dissipation capability of Duowatt transistors are 2 W @ $T_A = 25^oC$.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

TO-202AC
CASE 306-04

1.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage		BV_{CEO}			Vdc
(I_C = 10 mAdc, I_B = 0)	D40D1,2/D41D1,2		30	–	
	D40D/D41D–4,5		45	–	
	D40D/D41D–7,8		60	–	
	D40D/D41D–10,11,13,14		75	–	
Collector Cutoff Current (V_{CE} = Rated V_{CES})		I_{CES}	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 100 mAdc, V_{CE} = 2.0 Vdc)	D40D/D41D–1,4,7,10,13		50	150	
	D40D/D41D–2,5,8,11,14		120	360	
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	D40D1,4,5,7,8,10,11		10	–	
	D41D1,4,5,7,8,10,11		10	–	
	D40D/D41D–2		20	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)	D40D/D41D–1,2,4,5		–	0.5	
	D40D,7,8,10,11,13,14		–	1.0	
	D41D7,8,10,11,13,14		–	1.0	
Base-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)		$V_{BE(sat)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 20 mA, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	75	375	MHz
Collector-Base Capacitance		C_{cb}			pF
(V_{CB} = 20 Vdc, I_E = 0, f = 1 MHz)	D40D series		–	12	
	D41D series		–	18	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN–BANDWIDTH PRODUCT

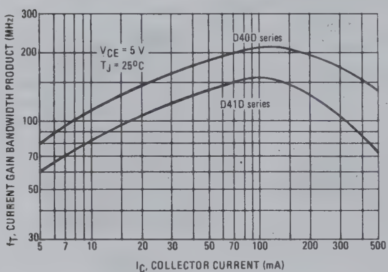
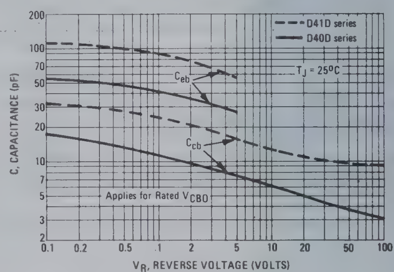


FIGURE 2 – CAPACITANCES



TYPICAL CHARACTERISTICS (continued)

D40D series — FIGURE 3 – DC CURRENT GAIN — D41D series

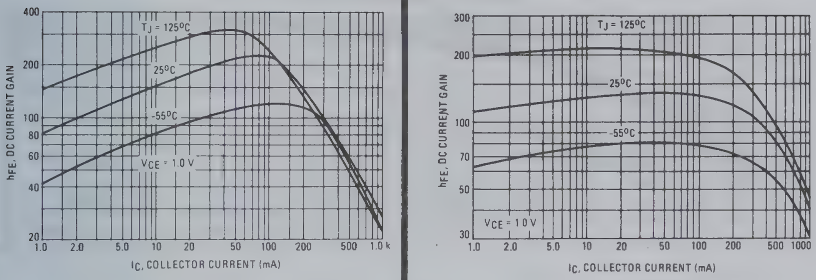


FIGURE 4 – "ON" VOLTAGE

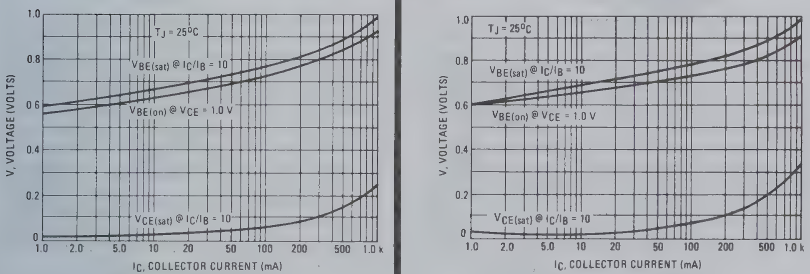
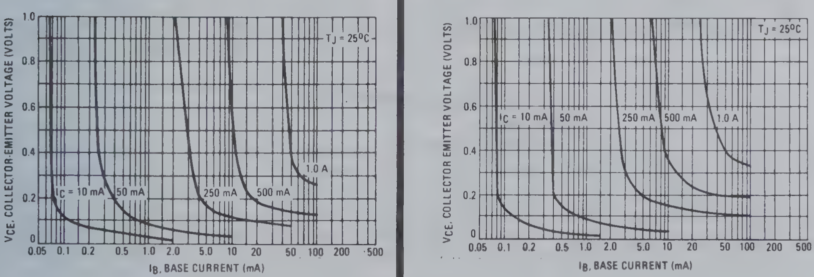


FIGURE 5 – COLLECTOR SATURATION REGION



1.3

TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – THERMAL RESPONSE

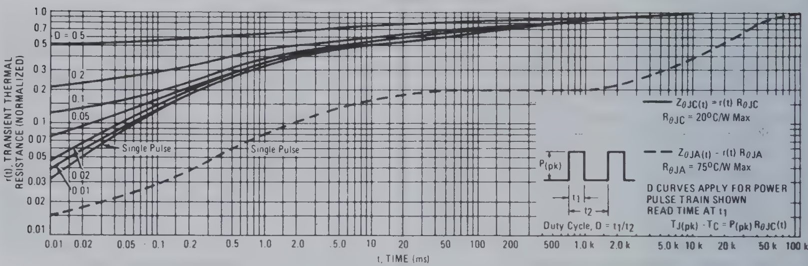
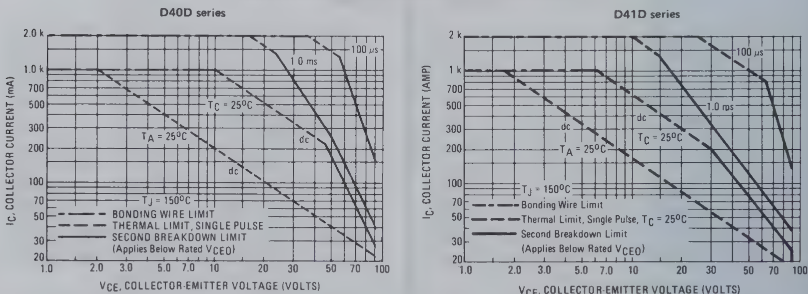


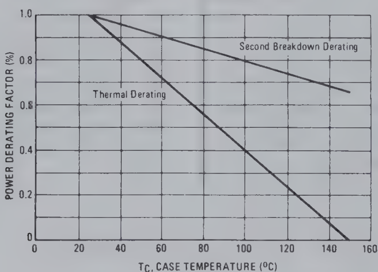
FIGURE 7 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 – POWER DERATING



NPN	PNP
D40E1	D41E1
D40E5	D41E5
D40E7	D41E7

MOTOROLA

1.3

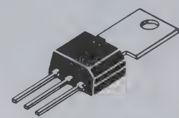
COMPLEMENTARY SILICON ANNULAR AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- Duowatt Package — 2 Watts Free Air Dissipation @ $T_A = 25^oC$

DUOWATT

COMPLEMENTARY SILICON AMPLIFIER TRANSISTORS



Tab forming and TO-5 lead forming available on special request.

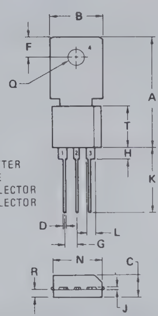
MAXIMUM RATINGS

Rating	Symbol	D40/41E1	D40/41E5	D40/41E7	Unit
Collector-Emitter Voltage	V_{CEO}	30	60	80	Vdc
Collector-Emitter Voltage	V_{CES}	40	70	90	Vdc
Emitter-Base Voltage	V_{EBO}	5.0			Vdc
Collector Current — Continuous Peak (1)	I_C	2 3			Adc
Base Current	I_B	0.5			mAdc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC (2)	P_D	1.67 13.3			Watts mW/^oC
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	8 64			Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	55 to +150			^oC
Solder Temperature, 1/16″ from Case for 10 Seconds	—	260			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^oC/W$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	15.6	$^oC/W$

NOTES 1. Pulse Test: Pulse Width $\leq$ 300 μs.
2. The actual power dissipation capability of Duowatt transistors are 2 W @ $T_A = 25^oC$.



STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

TO-202AC
CASE 306-04

1.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	BV_{CEO}			Vdc
D40E1/D41E1		30	–	
D40E5/D41E5		60	–	
D40E7/D41E7		80	–	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES})	I_{CES}	–	100	nAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
(I_C = 100 mAdc, V_{CE} = 2.0 Vdc)		50	–	
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)		10	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{CE(sat)}$	–	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{BE(sat)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain —Bandwidth Product (I_C = 20 mA, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	75	375	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1 MHz)	C_{cb}			pF
D40E series		–	12	
D41E series		–	18	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT GAIN-BANDWIDTH PRODUCT

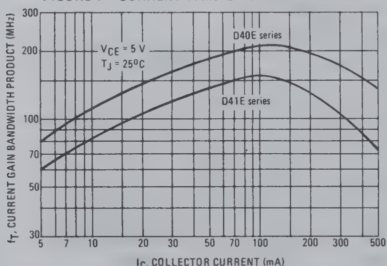
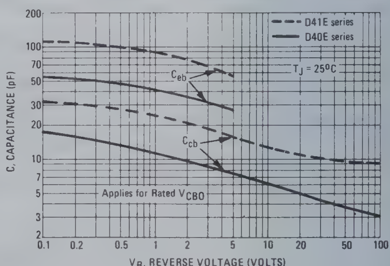


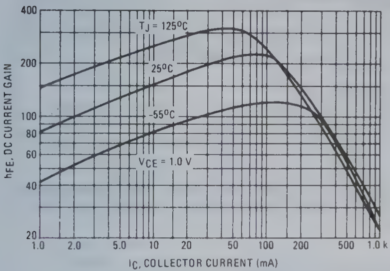
FIGURE 2 – CAPACITANCES



TYPICAL CHARACTERISTICS (continued)

FIGURE 3 — DC CURRENT GAIN

D40E series



D41E series

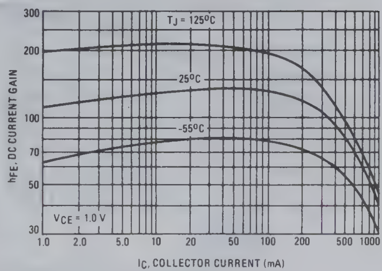
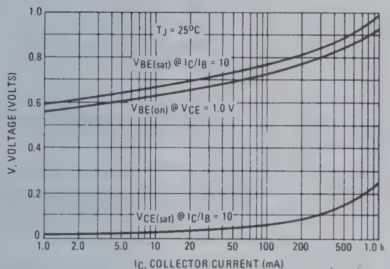


FIGURE 4 — "ON" VOLTAGE



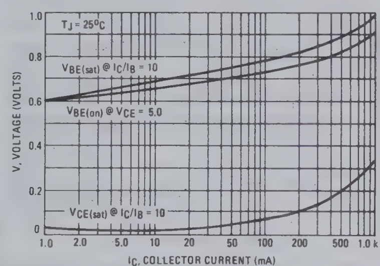
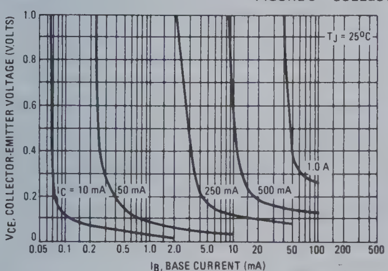
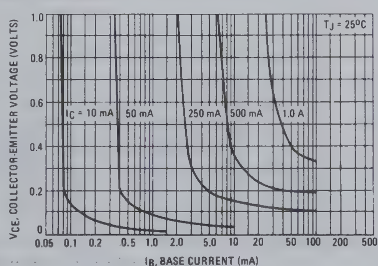


FIGURE 5 — COLLECTOR SATURATION REGION





1.3

TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – THERMAL RESPONSE

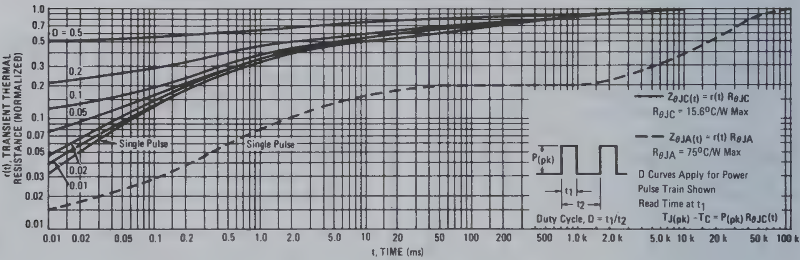
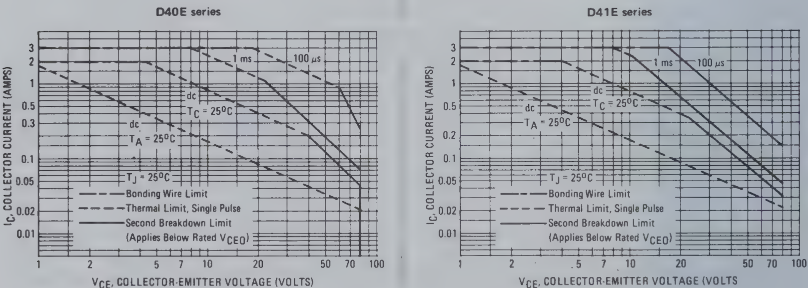


FIGURE 7 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

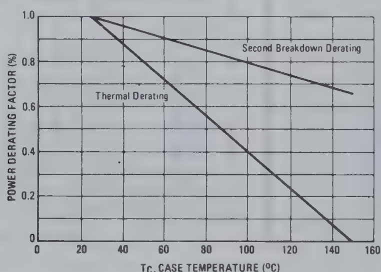


FIGURE 8 – POWER DERATING

MOTOROLA

NPN
D40K
PNP
D41K

1.3

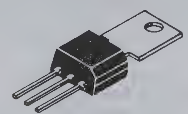
COMPLEMENTARY SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for amplifier and driver applications where high gain is an essential requirement, low power lamp and relay drivers and power drivers for high-current applications such as voltage regulators.

- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 1.5 Adc for D40,41K1,2
- Duowatt Package —
  2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

COMPLEMENTARY SILICON DARLINGTON AMPLIFIER TRANSISTORS



Tab forming and TO-5 lead forming available on special request.

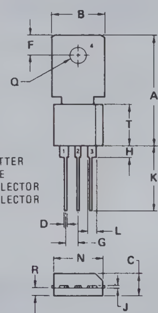
MAXIMUM RATINGS

Rating	Symbol	D40/41K 1,3	D40/41K 2,4	Unit
Collector-Emitter Voltage	V_{CEO}	30	50	Vdc
Collector-Emitter Voltage	V_{CES}	30	50	Vdc
Emitter-Base Voltage	V_{EBO}	13		Vdc
Collector Current — Continuous Peak (1)	I_C	2.0 3.0		Adc
Base Current — Continuous	I_B	100		mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C (2)	P_D	1.67 13.3		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C
Solder Temperature, 1/16″ from Case for 10 Seconds	—	260		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

1. Pulse Width ≤ 25 ms, Duty Cycle ≤ 50%.
2. The actual power dissipation capability of Duowatt transistors are 2 W @ T_A = 25°C.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

TO-202AC
CASE 306-04

1.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc)	D40,41K1,3 D40,41K2,4	BV_{CEO}	30 50	– –	Vdc
Collector Cutoff Current (V_{CB} = Rated V_{CES}, I_E = 0, T_J = 150°C)		I_{CBO}	–	20	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0)		I_{CES}	–	0.5	μAdc
Emitter Cutoff Current (V_{EB} = 13 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	All Devices		10,000	–	
(I_C = 1.5 Adc, V_{CE} = 5.0 Vdc)	D40,41K1,2		1,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	D40,41K3,4		1,000	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 3.0 mAdc)	D40,41K1,2		–	1.5	
(I_C = 1.0 Adc, I_B = 2.0 mA)	D40,41K3,4		–	1.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 3.0 mAdc)	D40,41K1,2		–	2.5	
(I_C = 1.0 Adc, I_B = 2.0 mAdc)	D40,41K3,4		–	2.5	
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	D40K series D41K series	C_{cb}	– –	10 25	pF
High Frequency Current Gain (I_C = 20 mA, V_{CE} = 5 Vdc, f = 100 MHz)		$\|h_{fe}\|$	1.0	–	–

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC SAFE OPERATING AREA

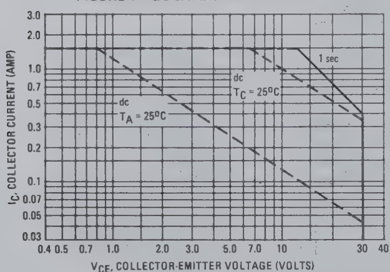
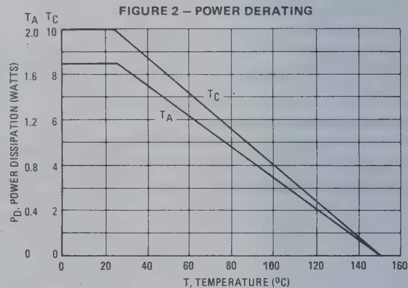


FIGURE 2 – POWER DERATING



TYPICAL CHARACTERISTICS (continued)

DC CURRENT GAIN

FIGURE 3 — (D40K series)

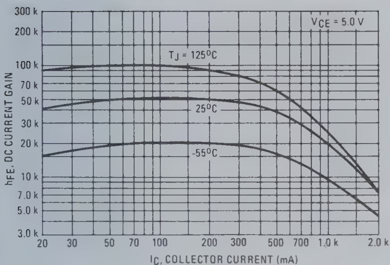
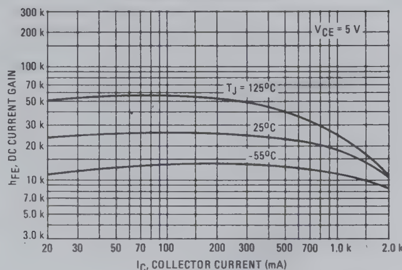


FIGURE 4 — (D41K series)



"ON" VOLTAGES

FIGURE 5 — (D40K series)

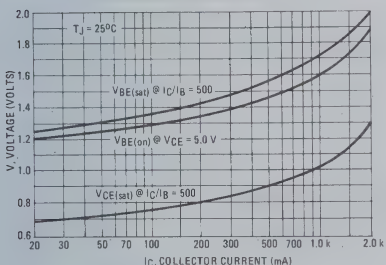


FIGURE 6 — (D41K series)

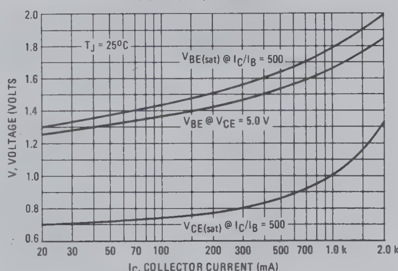
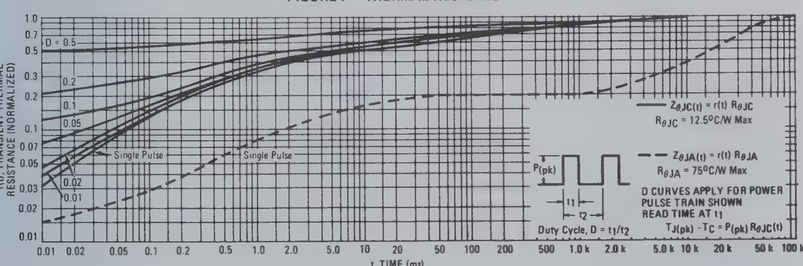


FIGURE 7 — THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

CAPACITANCE

FIGURE 8 — (D40K series)

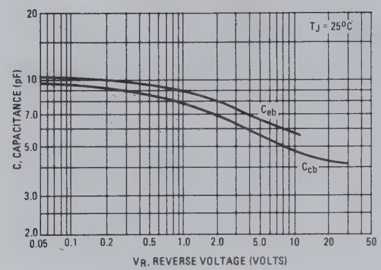
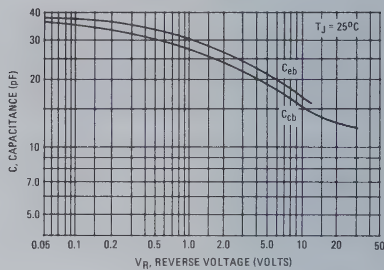


FIGURE 9 — (D41K series)



HIGH FREQUENCY CURRENT GAIN

FIGURE 10 — (D40K series)

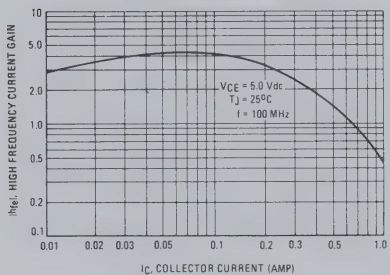
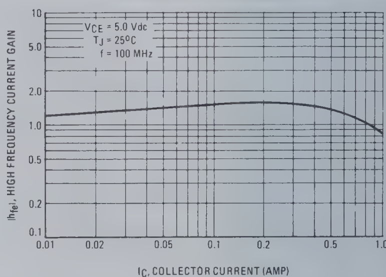


FIGURE 11 — (D41K series)



MOTOROLA

D40N1 D40N3
D40N2 D40N4

1.3

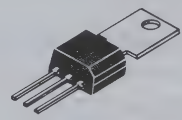
NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage — BV_{CER} = 300 Vdc (Min) @ I_C = 1.0 mAdc — D40N3, 4
- Low Collector-Base Capacitance — C_{cb} = 3.0 pF (Max) @ V_{CB} = 20 Vdc
- Duowatt Package — 2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



Tab forming and TO-5 lead forming available on special request.

MAXIMUM RATINGS

Rating	Symbol	D40N1, 2	D40N3, 4	Unit
Collector-Emitter Voltage (1, 2)	V_{CER}	250	300	Vdc
Collector-Base Voltage	V_{CBO}	250	300	Vdc
Emitter-Base Voltage	V_{EBO}	5.0		Vdc
Collector Current — Continuous — Peak	I_C	0.1 0.7		Adc
Base Current	I_B	250		mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.67 (3) 13.3		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	6.25 50		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C
Solder Temperature, 1/16″ from Case for 10 Seconds	—	260		°C

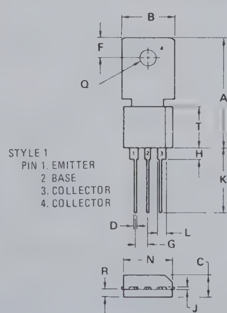
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	°C/W

(1) I_C = 1.0 mAdc, R_{BE} = 10 kΩ.

(2) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2%.

(3) The actual power dissipation capability of Duowatt transistors are 2 W @ T_A = 25°C.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
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R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

TO-202AC
CASE 306-04

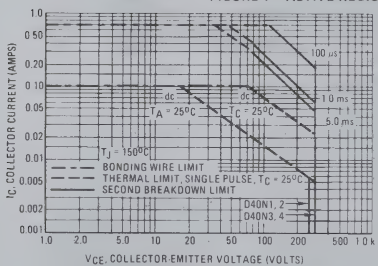
ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1)		BV_{CER}			Vdc
(I_C = 1.0 mAdc, I_B = 0, R_{BE} = 10 kΩ)	D40N1, 2		250	–	
	D40N3, 4		300	–	
Collector Cutoff Current		I_{CBO}			µAdc
(V_{CB} = 250 Vdc, I_E = 0)	D40N1, 2		–	10	
(V_{CB} = 300 Vdc, I_E = 0)	D40N3, 4		–	10	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	10	µAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 4.0 mAdc, V_{CE} = 10 Vdc)	D40N1, 3		20	–	
	D40N2, 4		30	–	
(I_C = 20 mAdc, V_{CE} = 10 Vdc)	D40N1, 3		30	90	
	D40N2, 4		60	180	
(I_C = 40 mAdc, V_{CE} = 10 Vdc)	D40N1, 3		20	–	
	D40N2, 4		30	–	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	50	–	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	3.0	pF

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

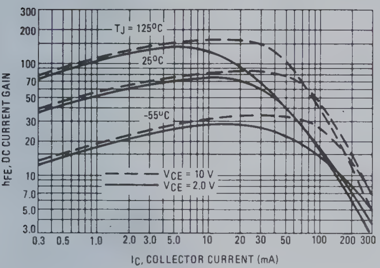


FIGURE 3 – "ON" VOLTAGES

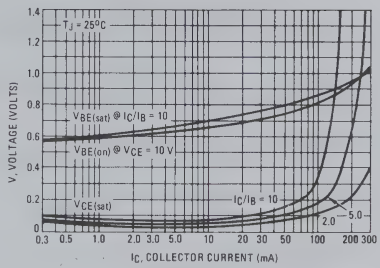


FIGURE 4 – COLLECTOR SATURATION REGION

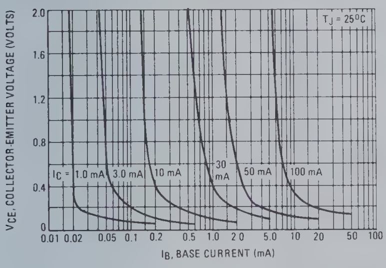


FIGURE 5 – TEMPERATURE COEFFICIENTS

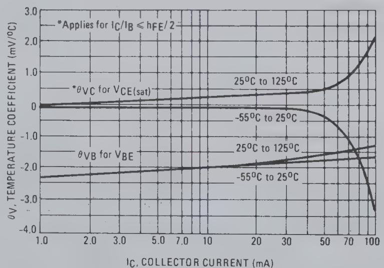
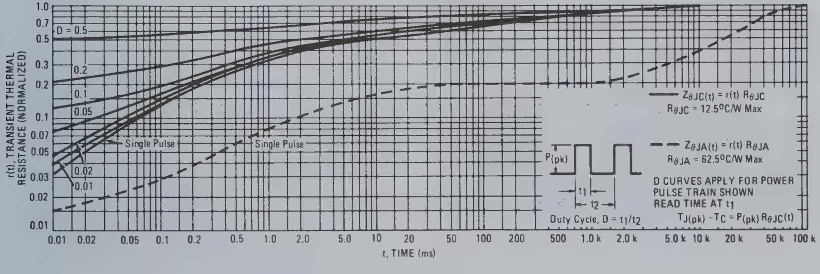


FIGURE 6 – THERMAL RESPONSE



D40P1
D40P3
D40P5

MOTOROLA

1.3

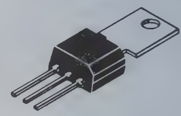
NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for horizontal drive applications, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 225 Vdc (Min) @ I_C = 1.0 mAdc — D40P5
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 100 mAdc
- Duowatt Package — 2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



Tab forming and TO-5 lead forming available on special request.

MAXIMUM RATINGS

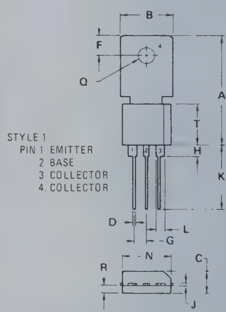
Rating	Symbol	D40P1	D40P3	D40P5	Unit
Collector-Emitter Voltage	V_{CEO}	120	180	225	Vdc
Collector-Base Voltage	V_{CBO}	200	250	300	Vdc
Emitter-Base Voltage	V_{EBO}	7.0			Vdc
Collector Current — Continuous Peak (1)	I_C	0.5 1.0			Adc
Base Current	I_B	100			mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.67 (2) 13.3			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	6.25 50			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C
Solder Temperature, 1/16″ from Case for 10 Seconds	—	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	°C/W

(1) Pulse Test: Pulse Width ≤ 1.0 ms, Duty Cycle ≤ 50%.

(2) The actual power dissipation capability of Duowatt transistors are 2 W @ T_A = 25°C.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

TO-202AC
CASE 306-04

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Character		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	D40P1 D40P3 D40P5	BV_{CEO}	120 180 225	– – –	Vdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0) (V_{CB} = 250 Vdc, I_E = 0) (V_{CB} = 300 Vdc, I_E = 0)	D40P1 D40P3 D40P5	I_{CBO}	– – –	10 10 10	μAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	10	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 80 mAdc, V_{CE} = 10 Vdc) (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)		h_{FE}	40 20	– –	–
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)		$V_{CE(sat)}$	–	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mA)		$V_{BE(sat)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 80 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	50	–	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	6.0	pF
SWITCHING CHARACTERISTICS					
Storage Time ($I_{C(on)}$ = 80 mA, $I_{B(on)}$ = 8.0 mA, $I_{B(off)}$ = 8.0 mA)		t_s	–	2.5	μs

(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 — CURRENT-GAIN — BANDWIDTH PRODUCT

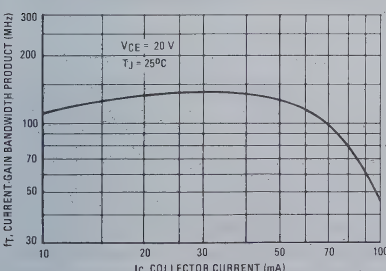
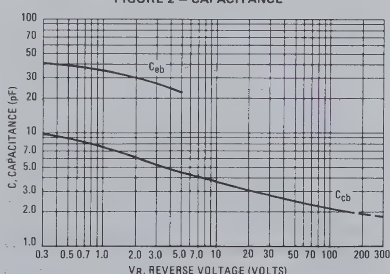


FIGURE 2 — CAPACITANCE



1.3

TYPICAL CHARACTERISTICS (Continued)

FIGURE 3 – DC CURRENT GAIN

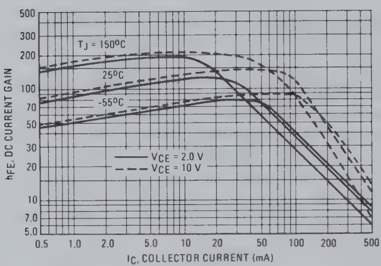


FIGURE 4 – "ON" VOLTAGE

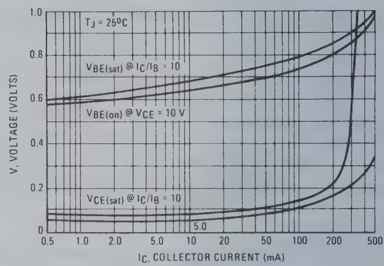


FIGURE 5 – COLLECTOR SATURATION REGION

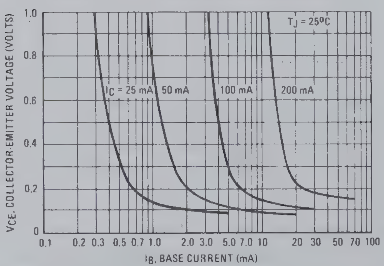


FIGURE 6 – TEMPERATURE COEFFICIENTS

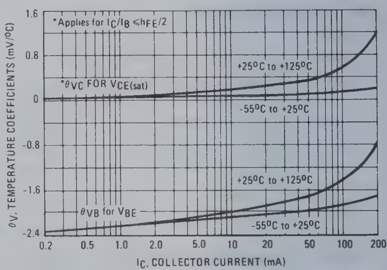


FIGURE 7 – COLLECTOR CHARACTERISTICS

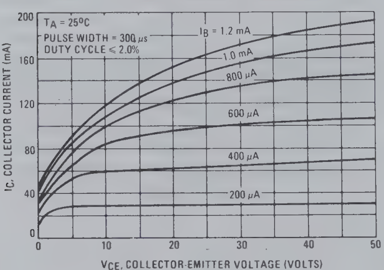
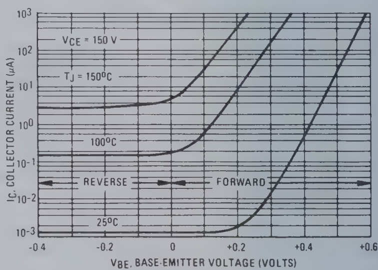


FIGURE 8 – COLLECTOR CUTOFF REGION



1.3

TYPICAL CHARACTERISTICS (Continued)

FIGURE 9 — THERMAL RESPONSE

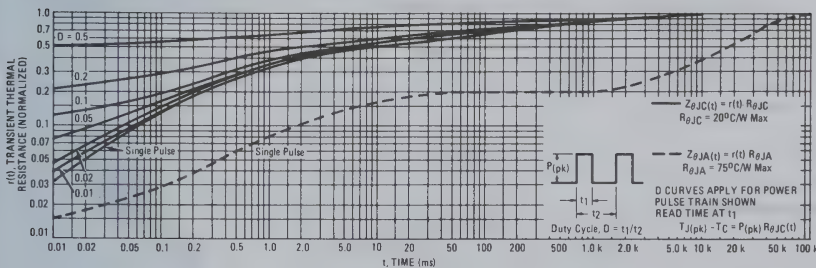
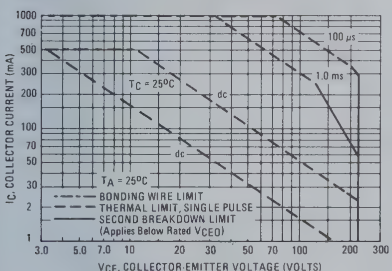


FIGURE 10 — ACTIVE REGION SAFE-OPERATING AREA

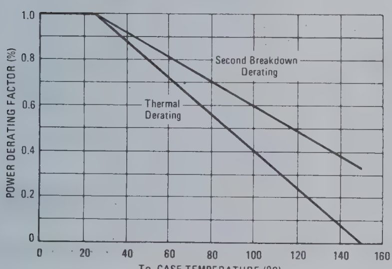


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 — POWER DERATING



NPN
D44C Series
PNP
D45C Series

MOTOROLA

1.3

COMPLEMENTARY SILICON POWER TRANSISTORS

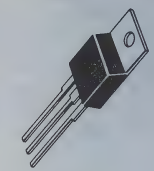
. . . for general purpose driver or medium power output stages in CW or switching applications.

- Low Collector-Emitter Saturation Voltage — 0.5 V (Max)
- High f_t for Good Frequency Response
- Low Leakage Current

4.0 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

30-80 VOLTS



MAXIMUM RATINGS

Rating	Symbol	D44C or D45C 1,2,3	4,5,6	7,8,9	10,11,12	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	60	80	Vdc
Collector-Emitter Voltage	V_{CES}	40	55	70	90	Vdc
Emitter Base Voltage	V_{EB}	5.0				Vdc
Collector Current — Continuous Peak (1)	I_C	4.0 6.0				Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_A = 25°C$	P_D	30 1.67				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150				°C

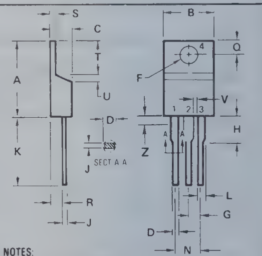
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
DC Current Gain ($V_{CE} = 1.0$ Vdc, $I_C = 0.2$ Adc)	D44C3,6,9,12 D45C3,6,9,12 D45C2,5,8,11	h_{FE}	40	120	—
	D44C2,5,8,11		100	220	
	D44C1,4,7,10 D45C1,4,7,10		25	—	
($V_{CE} = 1.0$ Vdc, $I_C = 1.0$ Adc)	D44C3,6,9,12 D45C3,6,9,12 D44C2,5,8,11		20	—	
($V_{CE} = 1.0$ Vdc, $I_C = 2.0$ Adc)	D45C2,5,8,11		20	—	
	D44C1,4,7,10 D45C1,4,7,10		10	—	



NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-02 (TO-220AB)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0)	I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)	I_{EBO}	—	—	100	μA
ON CHARACTERISTICS					
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 50 mAdc) D44C/D45C2,3,5,6,8,9,11,12 (I_C = 1.0 Adc, I_B = 100 mAdc) D44C/D45C1,4,7,10	$V_{CE(sat)}$	 — —	 — —	 0.5 0.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{BE(sat)}$	—	—	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f = 1.0 MHz) D44C Series D45C Series	C_{cb}	 — —	 100 125	 — —	pF
Gain Bandwidth Product (I_C = 20 mA, V_{CE} = 4.0 Vdc, f = 20 MHz) D44C Series D45C Series	f_T	 — —	 50 40	 — —	MHz
SWITCHING TIMES					
Delay and Rise Times (I_C = 1.0 Adc, I_{B1} = 0.1 Adc) D44C Series D45C Series	$t_d + t_r$	 — —	 100 50	 — —	ns
Storage Time (I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc) D44C Series D45C Series	t_s	 — —	 500 500	 — —	ns
Fall Time (I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc) D44C Series D45C Series	t_f	 — —	 75 50	 — —	ns

FIGURE 1 — DC CURRENT GAIN

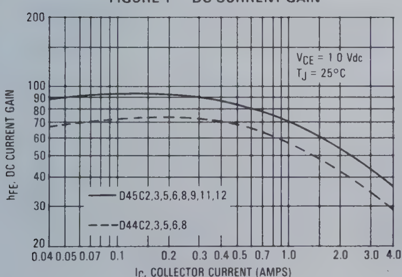
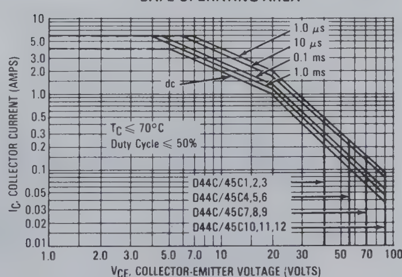


FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



NPN
D44E Series
PNP
D45E Series

MOTOROLA

1.3

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

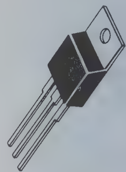
. . . for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 2.0 V (Max) @ 10 A
- High DC Current Gain — 1000 (Min) @ 5.0 Adc
- Complementary Pairs Simplifies Designs

DARLINGTON
10 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40-80 VOLTS
50 WATTS



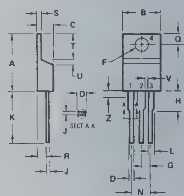
MAXIMUM RATINGS

Rating	Symbol	D44E or D45E 1	2	3	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter Base Voltage	V_{EB}		7.0		Vdc
Collector Current — Continuous Peak (1)	I_C		10 20		Adc
Total Power Dissipation @ T_C = 25°C @ T_A = 25°C	P_D		50 1.67		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.



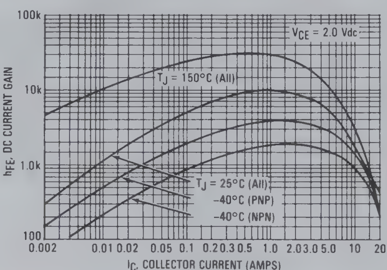
NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3 ONLY.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 1973.
5. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 1.
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-02
(TO-220AB)

FIGURE 1 — TYPICAL DC CURRENT GAIN



1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)	I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 7.0 Vdc)	I_{EBO}	—	—	1.0	μA
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	1000	—	—	—
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 10 mAdc) (I_C = 10 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	 — —	 — —	 1.5 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 10 mAdc)	$V_{BE(sat)}$	—	—	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1.0 MHz) D44E Series D45E Series	C_{CBO}	 — —	 — —	 130 220	pF
SWITCHING CHARACTERISTICS					
Delay and Rise Times (I_C = 10 Adc, I_{B1} = 20 mAdc)	$t_d + t_r$	—	0.6	—	μs
Storage Time (I_C = 10 Adc, I_{B1} = I_{B2} = 20 mAdc)	t_s	—	2.0	—	μs
Fall Time (I_C = 10 Adc, I_{B1} = I_{B2} = 20 mAdc)	t_f	—	0.5	—	μs

SAFE OPERATING AREA INFORMATION

FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (NPN)

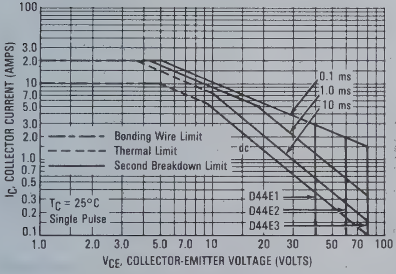
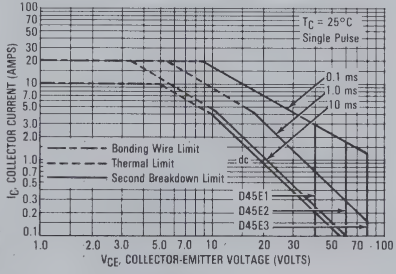


FIGURE 3 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (PNP)



NPN
D44H Series
PNP
D45H Series

MOTOROLA

1.3

COMPLEMENTARY SILICON POWER TRANSISTORS

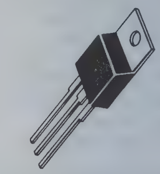
. . . for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

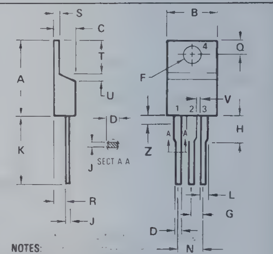
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

10 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

30-80 VOLTS





NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 1.
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-02 (TO-220AB)

MAXIMUM RATINGS

Rating	Symbol	D44H or D45H 1,2	4,5	7,8	10,11	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	60	80	Vdc
Emitter Base Voltage	V_{EB}	5.0				Vdc
Collector Current — Continuous Peak (1)	I_C	10 20				Adc
Total Power Dissipation @ T_C = 25°C @ T_A = 25°C	P_D	50 1.67				Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
DC Current Gain (V_{CE} = 1.0 Vdc, I_C = 2.0 Adc)	D44H1,4,7,10 D45H1,4,7,10	h_{FE}	35	—	—
	D44H2,5,8,11 D45H2,5,8,11		60	—	
(V_{CE} = 1.0 Vdc, I_C = 4.0 Adc)	D44H1,4,7,10 D45H1,4,7,10		20	—	
	D44H2,5,8,11 D45H2,5,8,11		40	—	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)	I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)	I_{EBO}	—	—	100	μA
ON CHARACTERISTICS					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 0.4 Adc) D44H/D45H2,5,8,11		—	—	1.0	
(I_C = 8.0 Adc, I_B = 0.8 Adc) D44H/D45H1,4,7,10		—	—	1.0	
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.8 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1.0 MHz)	C_{cb}				pF
D44H Series		—	130	—	
D45H Series		—	230	—	
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T				MHz
D44H Series		—	50	—	
D45H Series		—	40	—	
SWITCHING TIMES					
Delay and Rise Times (I_C = 5.0 Adc, I_{B1} = 0.5 Adc)	$t_d + t_r$				ns
D44H Series		—	300	—	
D45H Series		—	135	—	
Storage Time (I_C = 5.0 Adc, I_{B1} = I_{B2} = 0.5 Adc)	t_s				ns
D44H Series		—	500	—	
D45H Series		—	500	—	
Fall Time (I_C = 5.0 Adc, I_{B1} = I_{B2} = 0.5 Adc)	t_f				ns
D44H Series		—	140	—	
D45H Series		—	100	—	

FIGURE 1 — NORMALIZED DC CURRENT GAIN

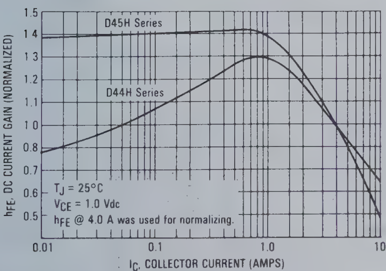
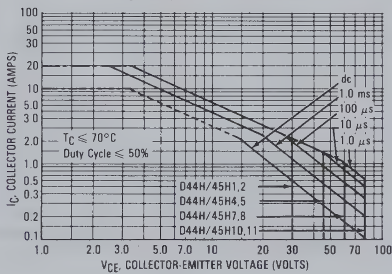


FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



NPN
D44VH Series
PNP
D45VH Series

MOTOROLA

1.3

COMPLEMENTARY SILICON POWER TRANSISTORS

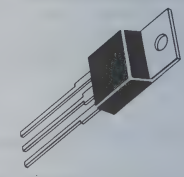
These complementary silicon power transistors are designed for high-speed switching applications, such as switching regulators and high frequency inverters. The devices are also well-suited for drivers for high power switching circuits.

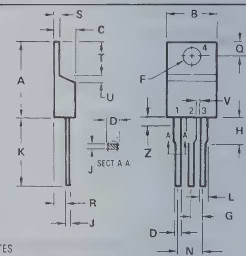
- Fast Switching — t_f = 90 ns (Max)
- Key Parameters Specified @ 100°C
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Complementary Pairs Simplify Circuit Designs

15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

30, 45, 60 and 80 VOLTS
83 WATTS





NOTES
1 DIMENSION H APPLIES TO ALL LEADS.
2 DIMENSION L APPLIES TO LEADS 1 AND 3
3 DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4 DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
5 CONTROLLING DIMENSION INCH

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 1.
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

**CASE 221A-02
(TO-220AB)**

MAXIMUM RATINGS

Rating	Symbol	D44VH or D45VH 1	4	7	10	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	60	80	Vdc
Collector-Emitter Voltage	V_{CEV}	50	70	80	100	Vdc
Emitter Base Voltage	V_{EB}	7.0				Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	15 20				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	83 1.67				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ⩽ 6.0 ms, Duty Cycle ⩽ 50%.

Note 1: All polarities are shown for NPN transistors. For PNP transistors, reverse polarities.
Note 2: See MJE5220/5230 Series data sheet for characteristic curves.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)	$V_{CEO(sus)}$				Vdc
(I_C = 25 mAdc, I_B = 0) D44VH1, D45VH1		30	—	—	
D44VH4, D45VH4		45	—	—	
D44VH7, D45VH7		60	—	—	
D44VH10, D45VH10		80	—	—	
Collector-Emitter Cutoff Current	I_{CEV}				μAdc
(V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc)		—	—	10	
(V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc, T_C = 100°C)		—	—	100	
Emitter Base Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				—
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)		35	—	—	
(I_C = 4.0 Adc, V_{CE} = 1.0 Vdc)		20	—	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 0.4 Adc) D44VH Series		—	—	0.4	
(I_C = 8.0 Adc, I_B = 0.8 Adc) D45VH Series		—	—	1.0	
(I_C = 15 Adc, I_B = 3.0 Adc, T_C = 100°C) D44VH Series		—	—	0.8	
D45VH Series		—	—	1.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 0.4 Adc) D44VH Series		—	—	1.2	
(I_C = 8.0 Adc, I_B = 0.8 Adc) D45VH Series		—	—	1.0	
(I_C = 8.0 Adc, I_B = 0.4 Adc, T_C = 100°C) D44VH Series		—	—	1.1	
(I_C = 8.0 Adc, I_B = 0.8 Adc, T_C = 100°C) D45VH Series		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	—	50	—	MHz
Output Capacitance	C_{cb}				pF
(V_{CB} = 10 Vdc, I_C = 0, f_{test} = 1.0 MHz) D44VH Series		—	120	—	
D45VH Series		—	275	—	
SWITCHING CHARACTERISTICS					
Delay Time (V_{CC} = 20 Vdc, I_C = 8.0 Adc, I_{B1} = I_{B2} = 0.8 Adc)	t_d	—	—	50	ns
Rise Time	t_r	—	—	250	
Storage Time	t_s	—	—	700	
Fall Time	t_f	—	—	90	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

MDS20
MDS21

MOTOROLA

1.3

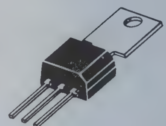
NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, high-voltage drivers and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 300 Vdc (Min) @ I_C = 1.0 mAdc — MDS21
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance —
  C_{cb} = 3.0 pF (Max) @ V_{CB} = 20 Vdc
- Duowatt Package —
  2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS

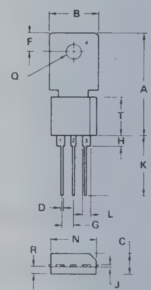


MAXIMUM RATINGS

Rating	Symbol	MDS20	MDS21	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	Vdc
Collector-Base Voltage	V_{CBO}	250	300	Vdc
Emitter-Base Voltage	V_{EBO}	8.0		Vdc
Collector Current — Continuous	I_C	0.5		Adc
Base Current	I_B	0.25		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C
Solder Temperature, 1/16″ from Case for 10 Seconds	—	260		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 1
PIN 1 EMITTER
2 BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9 91	10.41	0.390	0.410
C	4 39	4 65	0.173	0.183
D	0 58	0 74	0.023	0.029
F	3 56	4.06	0.140	0.160
G	2 41	2 67	0.095	0.105
H	1 70	1 96	0 067	0.077
J	0 48	0 66	0.019	0.026
K	12 19	12 95	0 480	0.510
L	1 65	2 03	0.065	0.080
N	9 91	10 16	0 390	0 400
Q	3 56	3 81	0 140	0 150
R	1 07	1.75	0 042	0.069
T	7.87	9 14	0 310	0.360

CASE 306-04
TO-202AC

1.3

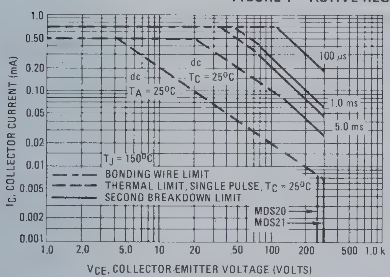
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	MDS20 MDS21	BV_{CEO}	250 300	– –	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	MDS20 MDS21	BV_{CBO}	250 300	– –	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	8.0	–	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0)	MDS20 MDS21	I_{CEO}	– –	0.5 0.5	μAdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0) (V_{CB} = 250 Vdc, I_E = 0)	MDS20 MDS21	I_{CBO}	– –	0.1 0.1	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 30 mAdc, V_{CE} = 10 Vdc)		h_{FE}	40	250	–
Collector-Emitter Saturation Voltage (I_C = 30 mAdc, I_B = 3.0 mAdc)		$V_{CE(sat)}$	–	0.6	Vdc
Base-Emitter On Voltage (I_C = 30 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	0.85	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Prdouct (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	60	–	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	3.0	pF

Note 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

1.3

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

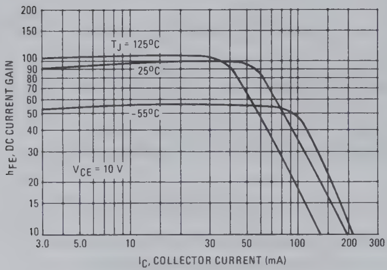


FIGURE 3 – "ON" VOLTAGES

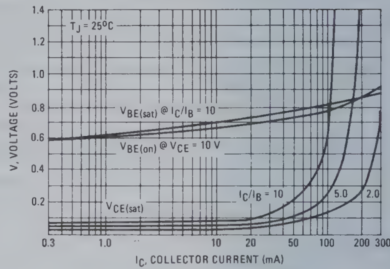


FIGURE 4 – COLLECTOR SATURATION REGION

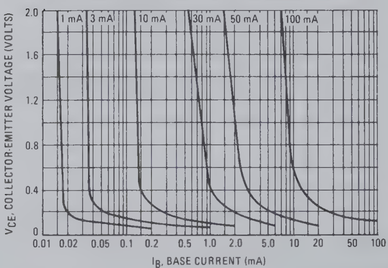


FIGURE 5 – TEMPERATURE COEFFICIENTS

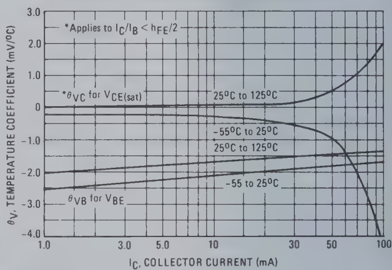
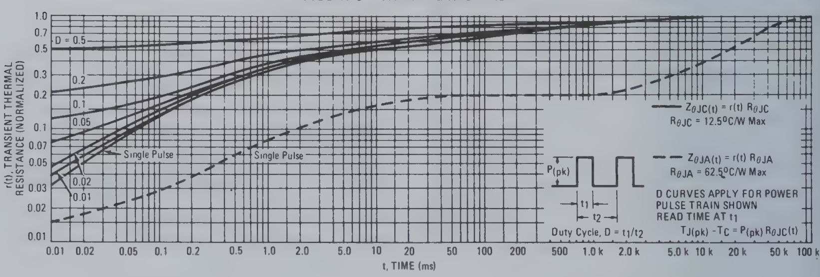


FIGURE 6 – THERMAL RESPONSE



NPN **MDS26** **MDS27**

PNP **MDS76** **MDS77**

MOTOROLA

1.3

COMPLEMENTARY PLASTIC SILICON POWER TRANSISTORS

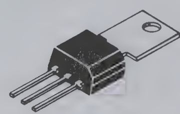
. . . designed for low power audio amplifier and low current, high speed switching applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc — MDS26, MDS76
  = 60 Vdc — MDS27, MDS77
- DC Current Gain —
  h_{FE} = 40 (Min) @ I_C = 0.2 Adc
  = 30 (Min) @ I_C = 1.0 Adc
- Current-Gain — Bandwidth Product —
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages —
  I_{CBO} = 100 nA (Max) @ Rated V_{CB}

DUOWATT
3.0 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40, 60 VOLTS
10 WATTS



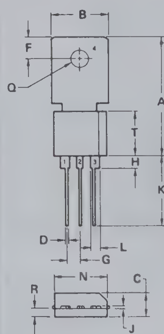
Tab forming and TO-5 lead forming available on special request.

MAXIMUM RATINGS

Rating	Symbol	MDS26 MDS76	MDS27 MDS77	Unit
Collector-Base Voltage	V_{CB}	60	80	Vdc
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous	I_C	3.0		Adc
Peak		5.0		
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_A = 25^oC$	P_D	2.0		Watts
Derate above 25^oC		0.016		$W/^oC$
Total Device Dissipation @ $T_C = 25^oC$	P_D	12.5		Watts
Derate above 25^oC		100		$mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	$^oC/W$
Thermal Resistance, Junction to Ambient	θ_{JA}	62.5	$^oC/W$



STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04
TO-202 AC

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	MDS26,MDS76	$V_{CEO(sus)}$	40	–	Vdc
	MDS27,MDS77		60	–	
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)	MDS26,MDS76	I_{CBO}	–	0.1	μAdc
(V_{CB} = 80 Vdc, I_E = 0)	MDS27,MDS77			0.1	
(V_{CB} = 60 Vdc, I_E = 0, $T_C = 125^oC$)	MDS26,MDS76		–	0.1	mAdc
(V_{CB} = 80 Vdc, I_E = 0, $T_C = 125^oC$)	MDS27,MDS77		–	0.1	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 1.0 Vdc)		h_{FE}	40	200	–
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			30	–	
Collector-Emitter Saturation Voltage (I_C = 200 mAdc, I_B = 20 mAdc)		$V_{CE(sat)}$	–	0.3	Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	0.6	
(I_C = 3.0 Adc, I_B = 600 mAdc)			–	1.7	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	1.8	Vdc
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	50	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MDS26, MDS27	C_{ob}	–	50	pF
	MDS76, MDS77		–	70	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

(2) $f_T = |h_{fe}| \bullet f_{test}$

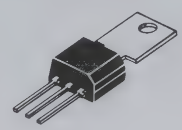
MOTOROLA

PNP SILICON ANNULAR TRANSISTOR

. . . designed for general-purpose applications requiring high breakdown voltages, low saturation voltages and low capacitance.

- Complement to NPN Type 2N6558

DUOWATT PNP SILICON HIGH VOLTAGE TRANSISTOR



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	2.0 16	Watt mW/^oC
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	10 80	Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	^oC

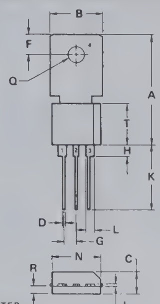
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	$^oC/W$
Thermal Resistance, Junction to Ambient	θ_{JA}	62.5	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Breakdown Voltage(1) (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	300	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	300	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}	–	0.2	μAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	-	0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 30 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 25 30 30	 – –	–
Collector-Emitter Saturation Voltage (I_C = 30 mAdc, I_B = 3.0 mAdc)	$V_{CE(sat)}$	–	0.75	Vdc
Base-Emitter Saturation Voltage (I_C = 30 mAdc, I_B = 3.0 mAdc)	$V_{BE(sat)}$	-	0.9	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 10 MHz)	f_T	45		MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	8.0	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04
TO-202 AC

1.3

FIGURE 1 – DC CURRENT GAIN

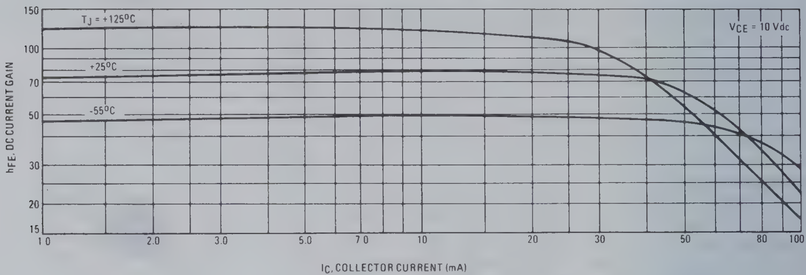


FIGURE 2 – CAPACITANCES

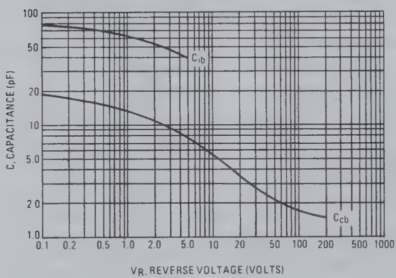


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

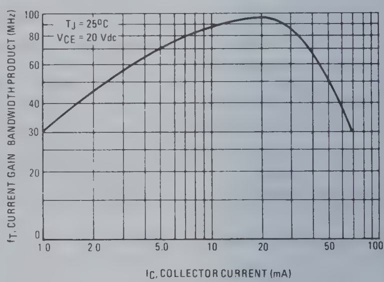


FIGURE 4 – "ON" VOLTAGES

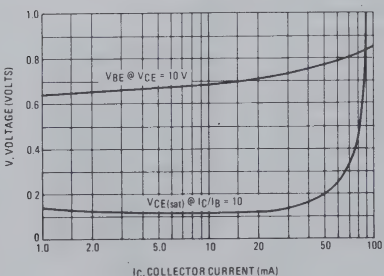
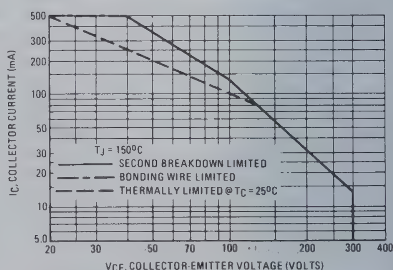


FIGURE 5 – DC SAFE OPERATING AREA



MDS1678

MOTOROLA

NPN SILICON ANNULAR RF TRANSISTOR

. . . designed for use in Citizen-band and other high-frequency communications equipment operating to 30 MHz. Higher breakdown voltages allow a high percentage of up-modulation in AM circuits.

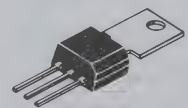
- Output Power = 4 W (Min) @ V_{CC} = 12 Vdc
- Power Gain = 10 dB (Min)
- High Collector-Emitter Breakdown Voltage — $BV_{CER} \geqslant 65$ Vdc

DUOWATT

4 W—27 MHz

RF POWER OUTPUT TRANSISTOR

NPN SILICON



Tab-forming and TO-5 lead-forming available on special request.

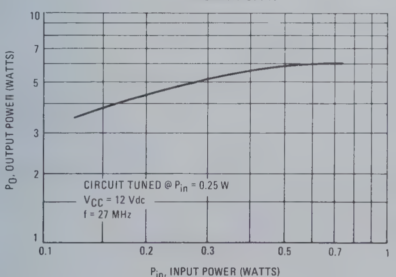
MAXIMUM RATINGS

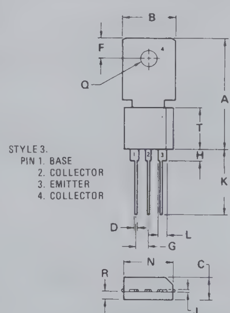
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	65	Vdc
Collector-Emitter Voltage	V_{CER}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector Current — Continuous	I_C	3	Adc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	2 16	Watt mW/^oC
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	10 80	Watt mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Reistance, Junction to Case	θ_{JC}	12.5	$^oC/W$
Thermal Resistance, Junction to Ambient	θ_{JA}	62.5	$^oC/W$

FIGURE 1 — POWER GAIN





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04
TO-202AC

1.3

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) ($I_C = 10$ mAdc, $R_{BE} = 10\ \Omega$)	BV_{CER}	65	–	–	Vdc
Emitter-Base Breakdown Voltage ($I_E = 1$ mAdc, $I_C = 0$)	BV_{EBO}	4	–	–	Vdc
Collector Cutoff Current ($V_{CB} = 30$ Vdc, $I_E = 0$)	I_{CBO}	–	–	0.01	mAdc
ON CHARACTERISTICS					
DC Current Gain (2)	h_{FE}				–
($I_C = 500$ mAdc, $V_{CE} = 5$ Vdc)		15	–	–	
($I_C = 1.5$ Adc, $V_{CE} = 5$ Vdc)		10	–	–	
Collector-Emitter Saturation Voltage ($I_C = 500$ mAdc, $I_B = 50$ mAdc)	$V_{CE(sat)}$	–	–	1	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 12$ Vdc, $I_E = 0$, f = 1 MHz)	C_{ob}	–	–	45	pF
Current-Gain—Bandwidth Product ($I_C = 100$ mAdc, $V_{CE} = 5$ Vdc, f = 20 MHz)	f_T	100	–	–	MHz
FUNCTIONAL TEST (Figure 1)					
Common-Emitter Amplifier Power Gain ($P_{out} = 4$ W, $V_{CC} = 12$ Vdc, f = 27 MHz)	G_{PE}	10	–	–	dB
Output Power ($P_{in} = 400$ mW, $V_{CC} = 12$ Vdc, f = 27 MHz)	P_{out}	4	–	–	Watts
Collector Efficiency (3) ($P_{out} = 4$ W, $V_{CC} = 12$ Vdc, f = 27 MHz)	η	–	70	–	%
Percentage Up-Modulation (4) (f = 27 MHz)	–	–	85	–	%

(1) Pulsed through a 25 mH Inductor.

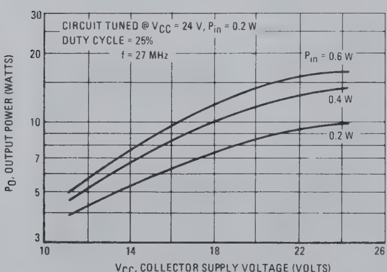
(2) Pulse Test: Pulse Width $\leqslant$ 300 μs, Duty Cycle $\leqslant$ 2.0%.

(3) $\eta = \dfrac{R_F P_{out}}{(V_{CC})(I_C)} \cdot 100$

(4) Percentage Up-Modulation is measured in the test circuit (Figure 3) by setting the Carrier Power (P_c) to 4 Watts with $V_{CC} = 12$ Vdc and noting the power input. Then the Peak Envelope Power (PEP) is noted after doubling the original power input to simulate driver modulation (at a 25% duty cycle for thermal considerations) and raising the V_{CC} to 24 Vdc (to simulate the modulating voltage). Percentage Up-Modulation is then determined by the relation:

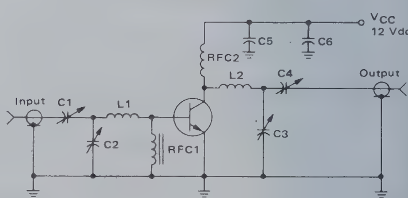
$$\text{Percentage Up-Modulation} = \left[\left(\frac{PEP}{P_c}\right)^{1/2} - 1\right] \bullet 100$$

FIGURE 2 — OUTPUT POWER WITH V_{CC} VARIATIONS



C1, C2 — 9.0-180 pF ARCO 463 or equivalent
C3, C4 — 4.0-80 pF ARCO 462 or equivalent
C5 — 0.02 μF ceramic disc
C6 — 0.1 μF ceramic disc
RFC1 — 4 turns #30 enameled wire wound on ferroxcube bead type 56-590-65/3B
RFC2 — 26 Turns #22 enameled wire (2 layers—13 turns each layer) 1/4'' inner diameter
L1 — 0.22 μH molded choke
L2 — 0.68 μH molded choke

FIGURE 3 — 27 MHz TEST CIRCUIT



MOTOROLA

MJ410
MJ411

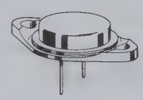
1.3

HIGH VOLTAGE NPN SILICON TRANSISTORS

. . . designed for medium to high voltage inverters, converters, regulators and switching circuits.

- High Collector-Emitter Voltage —
  V_{CEO} = 200 Volts — MJ410
  300 Volts — MJ411
- DC Current Gain Specified @ 1.0 and 2.5 Adc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.8 Vdc @ I_C = 1.0 Adc

5 AMPERE
POWER TRANSISTORS
NPN SILICON
200–300 VOLTS
100 WATTS



MAXIMUM RATINGS

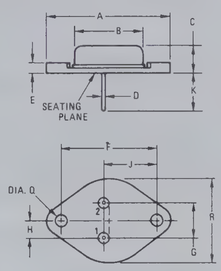
Rating	Symbol	MJ410	MJ411	Unit
Collector-Emitter Voltage	V_{CEO}	200	300	Vdc
Collector-Base Voltage	V_{CB}	200	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	5.0 10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	100 1.33		Watts W/°C
Operating Junction Temperature Range	T_J	-65 to +150		°C
Storage Temperature Range	T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0) MJ410 MJ411	$V_{CEO(sus)}$	 200 300	 – –	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0) MJ410 (V_{CE} = 300 Vdc, I_B = 0) MJ411	I_{CEO}	 – –	 0.25 0.25	mAdc
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) MJ410 (V_{CE} = 300 Vdc, $V_{EB(off)}$ - 1.5 Vdc, T_C = 125°C) MJ411	I_{CEX}	 – –	 0.5 0.5	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 30 10	 90 -	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	-	MHz



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

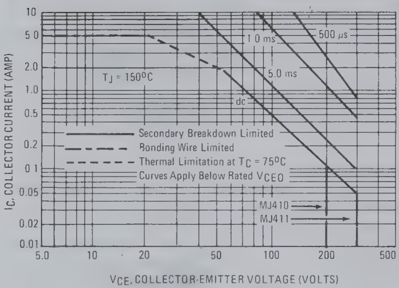
NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	–	1.050

CASE 11-01
TO-3

1.3

FIGURE 1 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 150^oC$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 2 — DC CURRENT GAIN

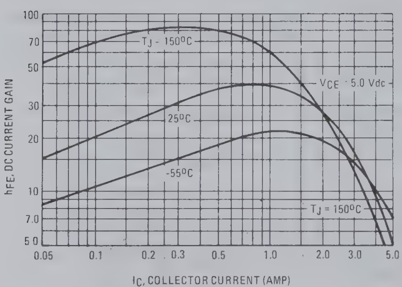


FIGURE 3 — "ON" VOLTAGES

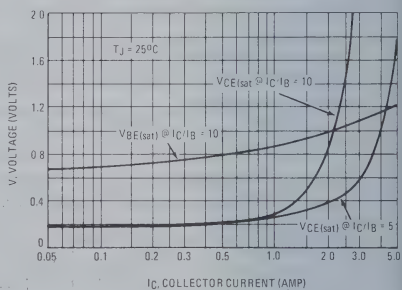


FIGURE 4 — SUSTAINING VOLTAGE TEST LOAD LINE

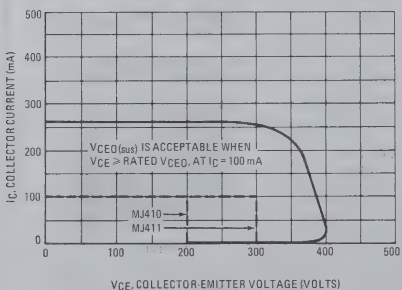
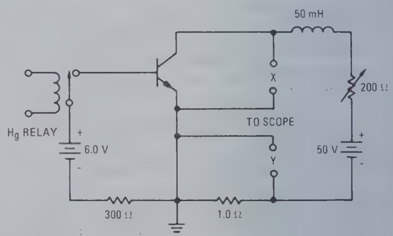


FIGURE 5 — SUSTAINING VOLTAGE TEST CIRCUIT



MOTOROLA

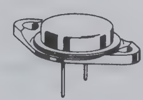
HIGH-VOLTAGE NPN SILICON TRANSISTORS

. . . designed for medium-to-high voltage inverters, converters, regulators and switching circuits.

- High Voltage — V_{CEX} = 400 Vdc
- Gain Specified to 3.5 Amp
- High Frequency Response to 2.5 MHz

**10 AMPERE
POWER TRANSISTORS
NPN SILICON**

**400 VOLTS
125 WATTS**



MAXIMUM RATINGS

Rating	Symbol	MJ413	MJ423	MJ431	Unit
Collector-Emitter Voltage	V_{CEX}	400	400	400	Vdc
Collector-Base Voltage	V_{CB}	400	400	400	Vdc
Emitter-Base Voltage	V_{EB}	5.0	5.0	5.0	Vdc
Collector Current — Continuous	I_C	10	10	10	Adc
Base Current	I_B	2.0	2.0	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		125 1.0		Watts W/°C
Operation Junction Temperature Range	T_J		-65 to +150		°C
Storage Temperature Range	T_{stg}		-65 to +200		°C

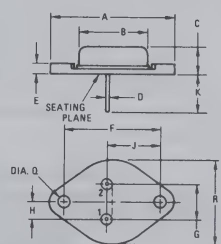
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (1) (I_C = 100 mAdc, I_B = 0)		$BV_{CEO(sus)}$	325	—	Vdc
Collector Cutoff Current (V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	MJ413, MJ423 MJ431	I_{CEX}	— —	0.25 2.5	mAdc
(V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	MJ413, MJ423 MJ431		— —	0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	MJ413, MJ423 MJ431	I_{EBO}	— —	5.0 2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	MJ413	h_{FE}	20	80	—
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)			15	—	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	MJ423		30	90	
(I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)			10	—	
(I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	MJ431		15	35	
(I_C = 3.5 Adc, V_{CE} = 5.0 Vdc)			10	—	
Collector-Emitter Saturation Voltage (1) (I_C = 0.5 Adc, I_B = 0.05 Adc)	MJ413	$V_{CE(sat)}$	—	0.8	Vdc
(I_C = 1.0 Adc, I_B = 0.10 Adc)	MJ423		—	0.8	
(I_C = 2.5 Adc, I_B = 0.5 Adc)	MJ431		—	0.7	
Base-Emitter Saturation Voltage (1) (I_C = 0.5 Adc, I_B = 0.05 Adc)	MJ413	$V_{BE(sat)}$	—	1.25	Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)	MJ423		—	1.25	
(I_C = 2.5 Adc, I_B = 0.5 Adc)	MJ431		—	1.5	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10Vdc, f = 1.0 MHz)		f_T	2.5	—	MHz

(1) PW ≤ 300 μs, Duty Cycle ≤ 2.0%



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-3

FIGURE 1 — ACTIVE-REGION SAFE-OPERATING AREA

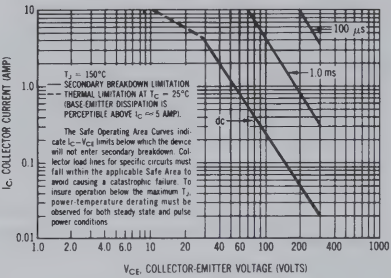


FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

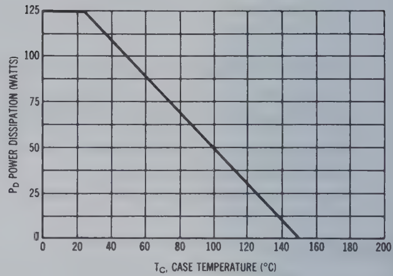


FIGURE 3 — SUSTAINING VOLTAGE TEST LOAD LINE

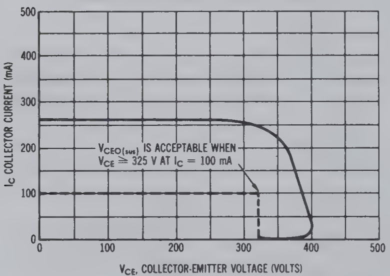


FIGURE 4 — SUSTAINING VOLTAGE TEST CIRCUIT

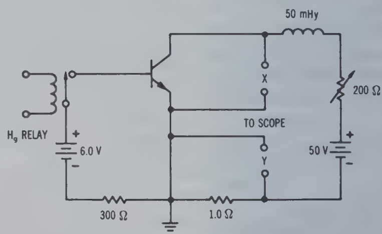


FIGURE 5 — CURRENT GAIN

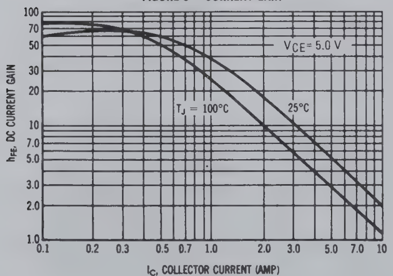
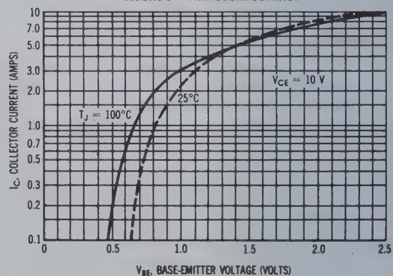


FIGURE 6 — TRANSCONDUCTANCE



MOTOROLA

HIGH-POWER NPN SILICON TRANSISTOR

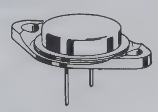
. . . for use as an output device in complementary audio amplifiers to 100-Watts music power per channel.

- High DC Current Gain — h_{FE} = 25–100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the PNP MJ4502

30 AMPERE
POWER TRANSISTOR

NPN SILICON

100 VOLTS
200 WATTS



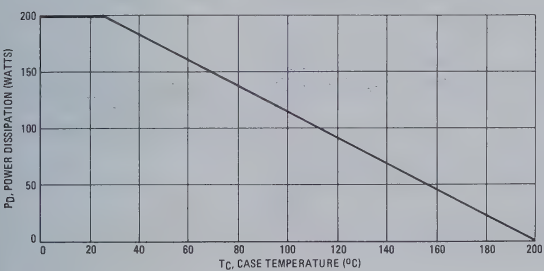
MAXIMUM RATINGS

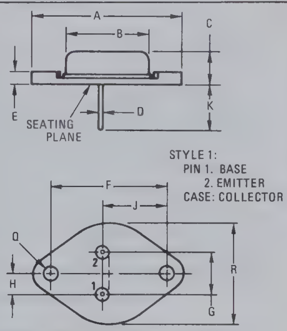
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CER}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Collector-Emitter Voltage	V_{CEO}	90	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	200 1.14	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	$^oC/W$

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	--	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

CASE 11-01
TO-3

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	BV_{CER}	100	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	–	Vdc
Collector-Base Cutoff Current	I_{CBO}			mAdc
(V_{CB} = 100 Vdc, I_E = 0)		–	1.0	
(V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)		–	5.0	
Emitter-Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (1) (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter "On" Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.3	Vdc
Collector-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

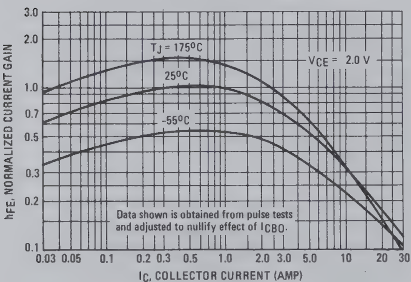


FIGURE 3 – "ON" VOLTAGES

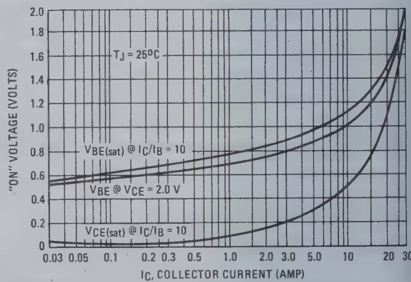
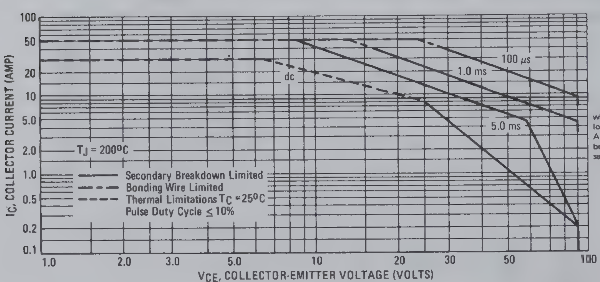


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

MOTOROLA

MJ900, MJ901 PNP
MJ1000, MJ1001 NPN

1.3

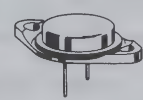
MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain -- h_{FE} = 6000 (Typ) @ I_C = 3.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

8.0 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON

60–80 VOLTS
90 WATTS



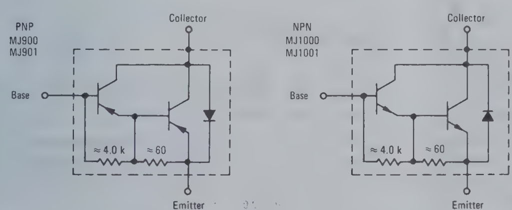
MAXIMUM RATINGS

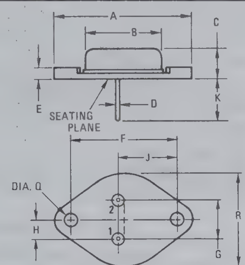
Rating	Symbol	MJ900 MJ1000	MJ901 MJ1001	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	8.0		Adc
Base Current	I_B	0.1		Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	90 0.515		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.94	$^oC/W$

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 100 mAdc, I_B = 0)	MJ900, MJ1000	BV_{CEO}	60	–	Vdc
	MJ901, MJ1001		80	–	
Collector Emitter Leakage Current (V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ900, MJ1000	I_{CER}	–	1.0	mAdc
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ901, MJ1001			1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ900, MJ1000			5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ901, MJ1001			5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		2.0	mAdc
Collector-Emitter Leakage Current (V_{CE} = 30 Vdc, I_B = 0)	MJ900, MJ1000	I_{CEO}	–	500	μAdc
(V_{CE} = 40 Vdc, I_B = 0)	MJ901, MJ1001			500	
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000		–
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			750	-	
Collector-Emitter Saturation Voltage(1) (I_C = 3.0 Adc, I_B = 12 mAdc)		$V_{CE(sat)}$	–	2.0	Vdc
(I_C = 8.0 Adc, I_B = 40 mAdc)			–	4.0	
Base-Emitter Voltage(1) (I_C = 3.0 Adc, V_{CE} – 3.0 Vdc)		V_{BE}		2.5	Vdc

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — DC CURRENT GAIN

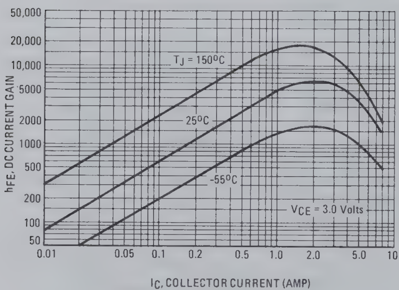


FIGURE 3 — SMALL-SIGNAL CURRENT GAIN

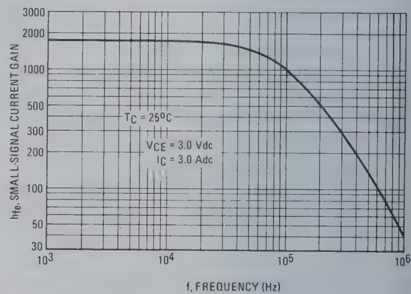


FIGURE 4 — "ON" VOLTAGES

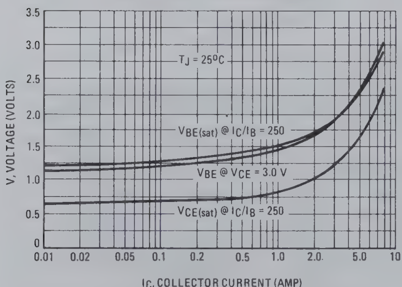
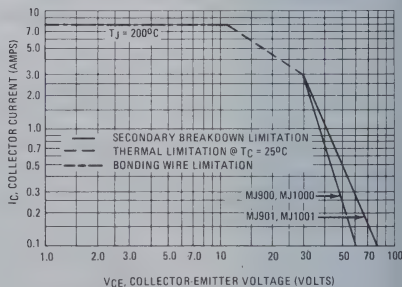


FIGURE 5 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MJ2500, MJ2501 PNP
MJ3000, MJ3001 NPN

MOTOROLA

1.3

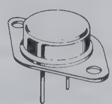
10 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON

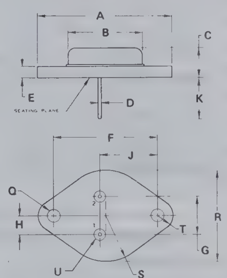
60–80 VOLTS
150 WATTS

MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 4000 (Typ) @ I_C = 5.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1–04

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

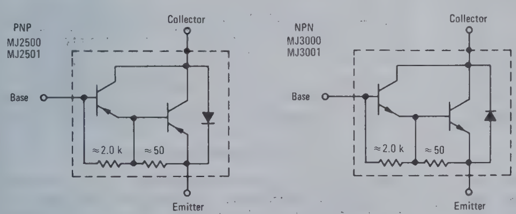
MAXIMUM RATINGS

Rating	Symbol	MJ2500 MJ3000	MJ2501 MJ3001	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	10		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @ $T_C = 25^oC$	P_D	150		Watts
Derate above 25^oC		0.857		$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^oC/W$

FIGURE 1 — DARLINGTON CIRCUIT SCHEMATIC



1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ2500, MJ3000 MJ2501, MJ3001	BV_{CEO}	60 80	– –	Vdc
Collector Emitter Leakage Current (V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm) (V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm) (V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C) (V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	 MJ2500, MJ3000 MJ2501, MJ3001 MJ2500, MJ3000 MJ2501, MJ3001	I_{CER}	 – – – –	 1.0 1.0 5.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
Collector-Emitter Leakage Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	 MJ2500, MJ3000 MJ2501, MJ3001	I_{CEO}	 – –	 1.0 1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	–	–
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 20 mAdc) (I_C = 10 Adc, I_B = 50 mAdc)		$V_{CE(sat)}$	 – –	 2.0 4.0	Vdc
Base-Emitter Voltage (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		V_{BE}	–	3.0	Vdc

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

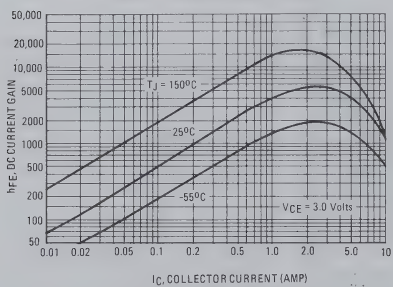


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

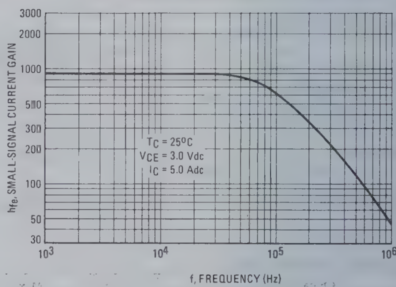


FIGURE 4 – "ON" VOLTAGES

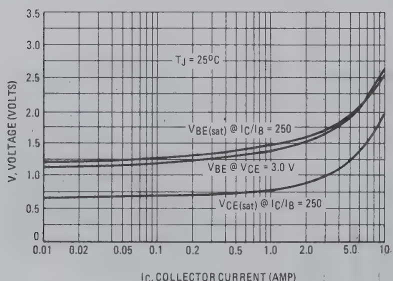
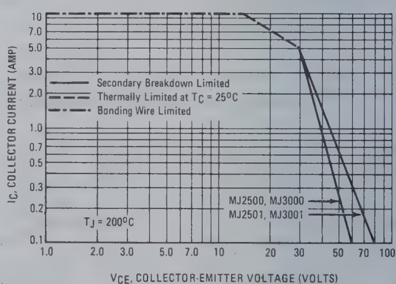


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA

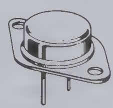
MJ3029
MJ3030

NPN SILICON HIGH-VOLTAGE TRANSISTORS

. . . designed for TV horizontal and vertical deflection amplifier circuits.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 250 Vdc (Min) MJ3029
  325 Vdc (Min) MJ3030
- Fast Fall Time in Horizontal Deflection —
  t_f = 1.0 μs (Max) @ V_{CC} = 80 Vdc — MJ3030
- Excellent Gain Linearity for Vertical Deflection —
  h_{fe} @ 0.4 Adc, h_{fe} @ 0.3 Adc = 0.95 (Min) — MJ3029

5 AMPERE
POWER TRANSISTORS
NPN SILICON
250-325 VOLTS
125 WATTS

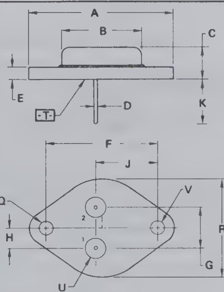


MAXIMUM RATINGS

Rating	Symbol	MJ3029	MJ3030	Unit
Collector-Emitter Voltage	V_{CEO}	250	325	Vdc
Collector-Emitter Voltage	V_{CER}	500	—	Vdc
Collector-Emitter Voltage	V_{CEX}	—	700	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	125 1.0		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	$^oC/W$



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	∅0.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	∅0.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

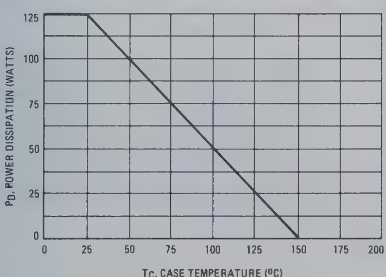
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage(1) (I_C = 0.1 Adc, I_B = 0)	MJ3029 MJ3030	$V_{CEO(sus)}$	250 325	– –	Vdc
Collector Cutoff Current (V_{CE} = 500 Vdc, R_{BE} = 1.5 k Ohms)	MJ3029	I_{CER}		1.0	mAdc
Collector Cutoff Current (V_{CE} = 700 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	MJ3030	I_{CEX}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 5.0 Vdc)(1) (I_C = 0.4 Adc, V_{CE} = 5.0 Vdc)(1)	MJ3029 MJ3029	h_{FE1} h_{FE2}	25 30	– –	–
Gain Linearity	MJ3029	$\frac{h_{FE2}}{h_{FE1}}$	0.95	–	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.8 Adc)	MJ3030	$V_{CE(sat)}$	–	2.0	Vdc
SWITCHING CHARACTERISTICS					
Fall Time (V_{CC} = 80 Vdc, I_C = 3.0 Adc, I_{B1} = 0.8 Adc) Figure 3	MJ3030	t_f	–	1.0	μs

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

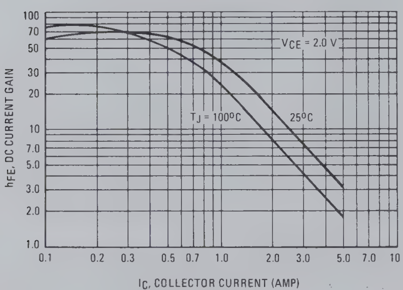
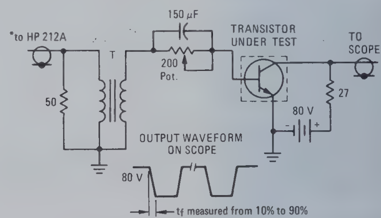
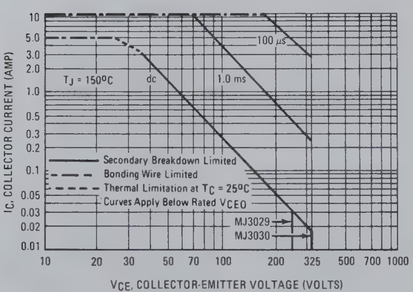


FIGURE 3 – TEST FOR FALL TIME



*HP 212A: Set for 10 μs wide pulses at 2000 pulses per sec. (500 μs intervals). Adjust for I_{B1} = 0.8 A.
Bias: Adjust to 1.5 V on a VTVM across the 200 Ω Pot.
T: Pulse Transformer: Motorola Part No. 25D68782A01.

FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA

MJ3040
MJ3041
MJ3042

1.3

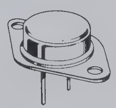
HIGH VOLTAGE SILICON POWER DARLINGTONS

. . . developed for line operated amplifier, series pass and switching regulator applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 300 Vdc (Min) — MJ3040, MJ3041
  = 350 Vdc (Min) — MJ3042
- High DC Current Gain —
  h_{FE} = 100 (Min) @ I_C = 2.5 Adc — MJ3040
  = 250 (Min) @ I_C = 2.5 Adc — MJ3041, MJ3042
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.2 Vdc (Max) @ I_C = 2.5 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON
10 AMPERE
POWER TRANSISTORS
NPN SILICON

300, 350 VOLTS
175 WATTS



MAXIMUM RATINGS

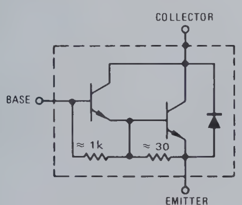
Rating	Symbol	MJ3040	MJ3041	MJ3042	Unit
Collector-Base Voltage	V_{CB}	400	400	500	Vdc
Collector-Emitter Voltage	V_{CEO}	300	300	350	Vdc
Emitter-Base Voltage	V_{EB}	8.0			Vdc
Collector Current — Continuous — Peak (1)	I_C	10 15			Adc
Total Device Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	175 1.0			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200			°C

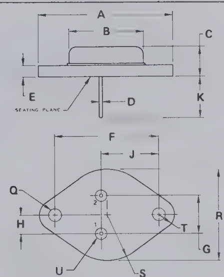
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

(1) Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

DARLINGTON SCHEMATIC





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1–04

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	MJ3040, MJ3041	$V_{CEO(sus)}$	300	–	Vdc
	MJ3042		350	–	
Collector Cutoff Current (V_{CB} = 400 Vdc, I_E = 0)	MJ3040, MJ3041	I_{CBO}	–	1.0	mAdc
(V_{CB} = 500 Vdc, I_E = 0)	MJ3042		–	1.0	
(V_{CB} = 400 Vdc, I_E = 0, T_C = 100°C)	MJ3040, MJ3041		–	5.0	
(V_{CB} = 500 Vdc, I_E = 0, T_C = 100°C)	MJ3042		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	40	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	MJ3040	h_{FE}	100	–	–
	MJ3041, MJ3042		250	–	
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	MJ3040		25	–	
	MJ3041, MJ3042		50		
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 50 mAdc)		$V_{CE(sat)}$	–	2.2	Vdc
(I_C = 5.0 Adc, I_B = 400 mAdc)			–	2.5	
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 400 mAdc)		$V_{BE(sat)}$	–	3.0	Vdc
Base-Emitter On Voltage (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	2.5	Vdc

FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA

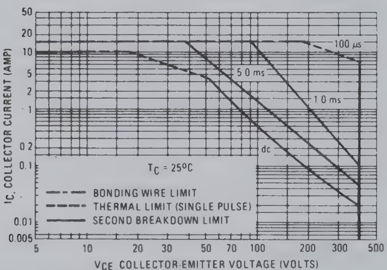
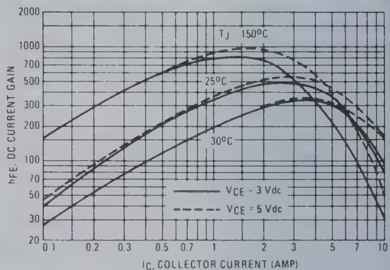


FIGURE 2 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor – average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA

NPN MJ3247 MJ3248 TO-66 PNP MJ3237 MJ3238

MJ4247 MJ4248 TO-3 MJ4237 MJ4238

1.3

COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for use as high-frequency drivers in audio amplifiers.

- DC Current Gain Specified to 4.0 Amperes

  h_{FE} = 40 (Min) @ I_C = 3.0 Adc
  = 20 (Min) @ I_C = 4.0 Adc

- Collector-Emitter Sustaining Voltage -

  $V_{CEO(sus)}$ = 120 Vdc (Min)
  = 150 Vdc (Min)

- High Current Gain - Bandwidth Product

  f_T = 20 MHz (Min) @ I_C = 500 mAdc

8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

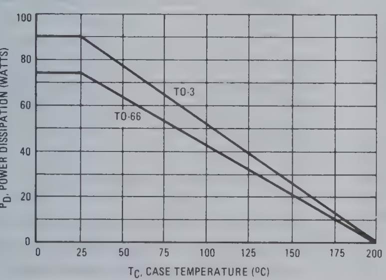
120-150 VOLTS
75 WATTS – TO-66
90 WATTS – TO-3

RATING	Symbol	MJ4247 MJ4237 MJ3247 MJ3237	MJ4248 MJ4238 MJ3248 MJ3238	Unit
Collector-Emitter Voltage	V_{CEO}	120	150	Vdc
Collector-Base Voltage	V_{CB}	120	150	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	8.0 16		Adc
Base Current — Continuous	I_B	2.0		Adc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C
		TO-3	TO-66	
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	90 0.51	75 0.43	Watts W/°C

THERMAL CHARACTERISTICS

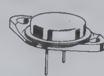
Characteristic	Symbol	TO-3	TO-66	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.94	2.33	°C/W

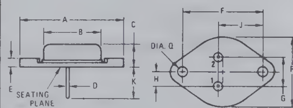
FIGURE 1 – POWER DERATING



MJ4247
MJ4248

MJ4237
MJ4238





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	-	21 08	–	0.830
C	6.35	7 62	0 250	0 300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1 177	1.197
G	10.67	11.18	0 420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0 440	0.480
Q	3.84	4.09	0 151	0 161
R	-	26.67	–	1.050

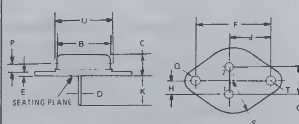
Collector connected to case
CASE 11-01
(TO 3)

STYLE 1
PIN 1 BASE
2. EMITTER
CASE COLLECTOR

NOTE
1. DIM "Q" IS DIA

MJ3247
MJ3248

MJ3237
MJ3238



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11 94	12 70	0 470	0 500
C	6 35	8 64	0 250	0 340
D	0 71	0 86	0 028	0 034
E	1 27	1 91	0.050	0 075
F	24 33	24 43	0 958	0 962
G	4 83	5 33	0 190	0 210
H	2 41	2 67	0 095	0 105
J	14 48	14 99	0 570	0 590
K	9 14	-	0 360	
P	-	1 27	-	0 050
Q	3 61	3 86	0 142	0 152
S	-	8 89		0 350
T		3 68		0 145
U		15 75	-	0 620

All JEDEC Dimensions and and Notes Apply

CASE 80 02
TO-66

STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1)	$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0) MJ4237, MJ4247, MJ3237, MJ3247		120	–	
MJ4238, MJ4248, MJ3238, MJ3248		150	–	
Collector Cutoff Current	I_{CEO}			mAdc
(V_{CE} = 120 Vdc, I_B = 0) MJ4237, MJ4247, MJ3237, MJ3247		–	0.1	
(V_{CE} = 150 Vdc, I_B = 0) MJ4238, MJ4248, MJ3238, MJ3248		–	0.1	
Collector Cutoff Current	I_{CBO}			μAdc
(V_{CB} = 120 Vdc, I_E = 0) MJ4237, MJ4247, MJ3237, MJ3247		–	10	
(V_{CB} = 150 Vdc, I_E = 0) MJ4238, MJ4248, MJ3238, MJ3248		–	10	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	10	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
(I_C = 0.1 Adc, V_{CE} = 2.0 Vdc)		40	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)		40	–	
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)		40	–	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)		20	–	
DC Current Gain Linearity	h_{FE}	Typ		
(V_{CE} From 2.0V to 20V, I_C From 0.1A to 3A)		2		
(NPN TO PNP)		3		
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	20	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 — CAPACITANCES

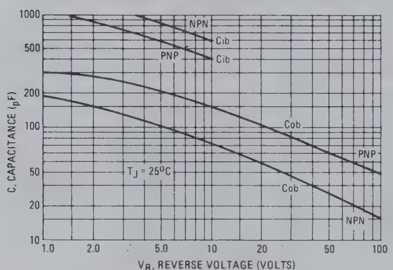


FIGURE 3 — CURRENT GAIN BANDWIDTH PRODUCT

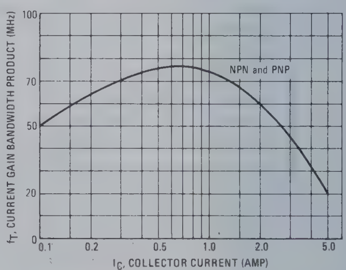


FIGURE 4 — THERMAL RESPONSE (TO-66)

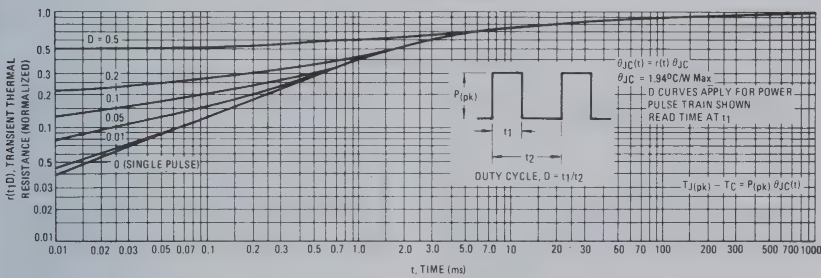
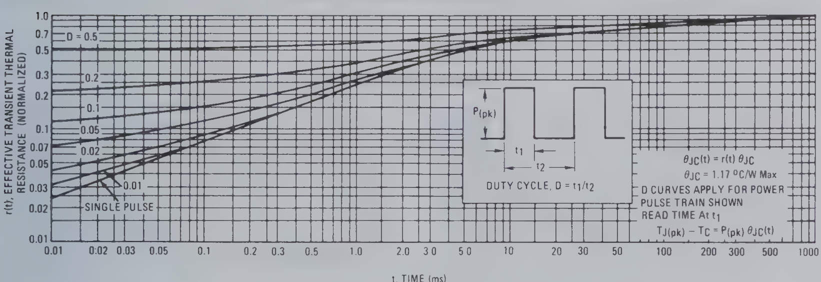


FIGURE 5 — THERMAL RESPONSE (TO-3)



FORWARD BIAS SAFE OPERATING AREA

FIGURE 6 — MJ3237, 38/MJ3247, 48

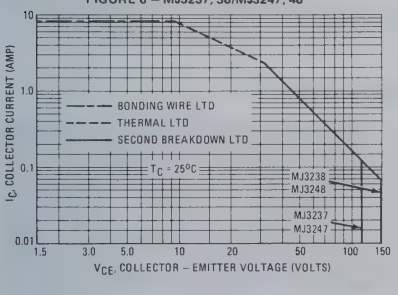
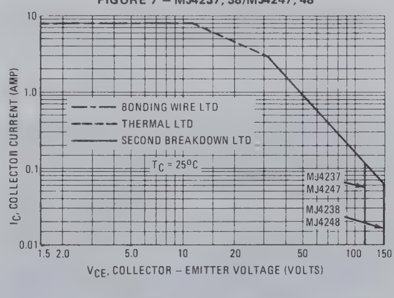


FIGURE 7 — MJ4237, 38/MJ4247, 48



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Second breakdown pulse limits are valid for duty cycles to 10%. At high case temperatures, thermal limitations may reduce the power that can be handled to values less than the limitations imposed by second breakdown.

1.3

FIGURE 8 – DC CURRENT GAIN

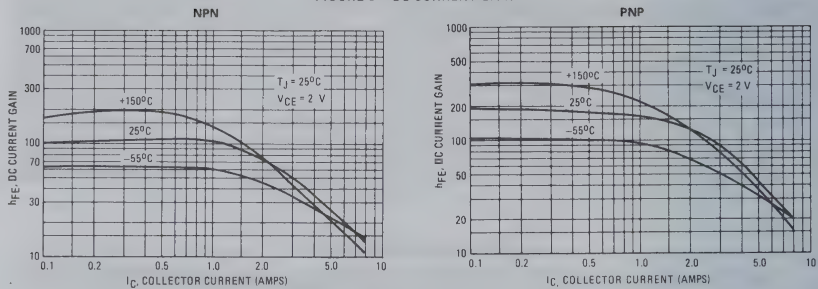


FIGURE 9 – "ON" VOLTAGE

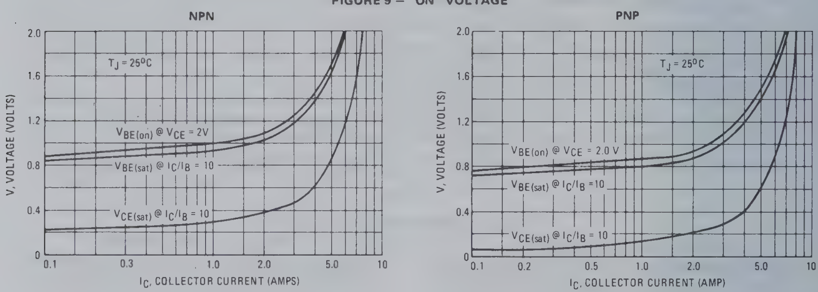
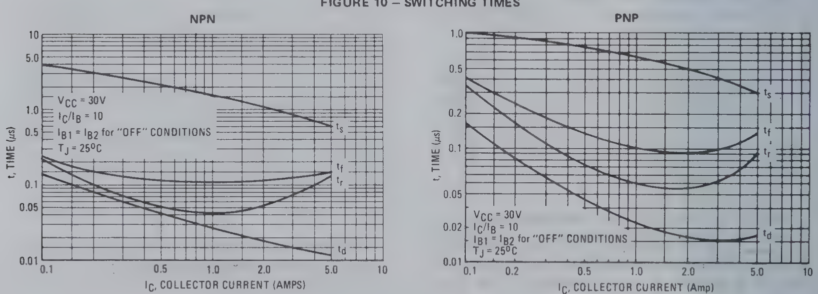


FIGURE 10 – SWITCHING TIMES



MJ4030, MJ4031, MJ4032 PNP
MJ4033, MJ4034, MJ4035 NPN

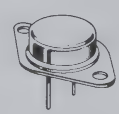
MOTOROLA

MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 3500 (Typ) @ I_C = 10 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor

16 AMPERE
DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON
60–100 VOLTS
150 WATTS

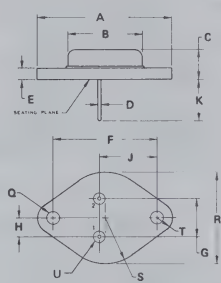


MAXIMUM RATINGS

Rating	Symbol	MJ4030 MJ4033	MJ4031 MJ4034	MJ4032 MJ4035	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current	I_C	16			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W



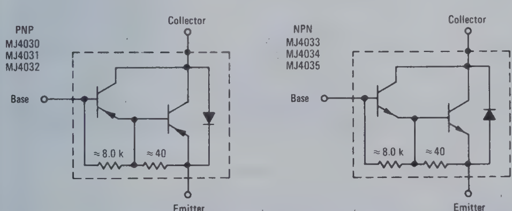
STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1–04

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

FIGURE 1 — DARLINGTON CIRCUIT SCHEMATIC



1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ4030, MJ4033 MJ4031, MJ4034 MJ4032, MJ4035	BV_{CEO}	60 80 100	– –	Vdc
Collector Emitter Leakage Current (V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ4030, MJ4033	I_{CER}	–	1.0	mAdc
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ4031, MJ4034			1.0	
(V_{CB} = 100 Vdc, R_{BE} = 1.0 k ohm)	MJ4032, MJ4035			1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4030, MJ4033			5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4031, MJ4034			5.0	
(V_{CB} = 100 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4032, MJ4035			5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		5.0	mAdc
Collector-Emitter Leakage Current (V_{CE} = 30 Vdc, I_B = 0)	MJ4030, MJ4033	I_{CEO}		3.0	mAdc
(V_{CE} = 40 Vdc, I_B = 0)	MJ4031, MJ4034			3.0	
(V_{CE} = 50 Vdc, I_B = 0)	MJ4032, MJ4035			3.0	
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	–	
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 40 mAdc) (I_C = 16 Adc, I_B = 80 mAdc)		$V_{CE(sat)}$		2.5 4.0	Vdc
Base-Emitter Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		V_{BE}		3.0	Vdc

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

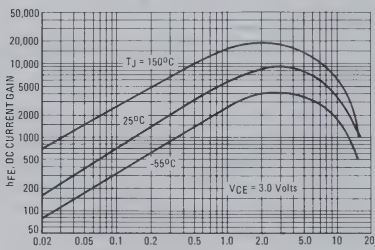


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

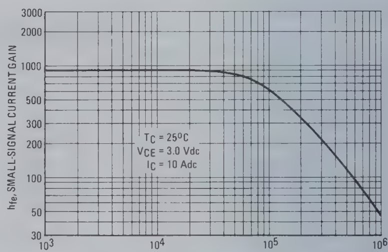


FIGURE 4 – "ON" VOLTAGES

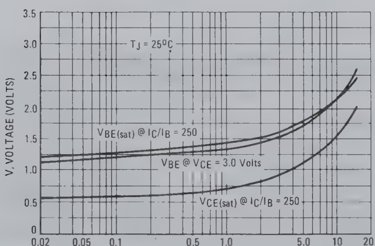
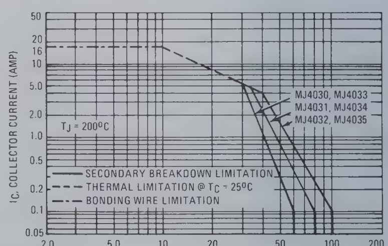


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA

HIGH-POWER PNP SILICON TRANSISTOR

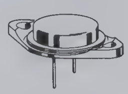
. . . for use as an output device in complementary audio amplifiers to 100-Watts music power per channel.

- High DC Current Gain — h_{FE} = 25–100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the NPN MJ802

30 AMPERE POWER TRANSISTOR

PNP SILICON

100 VOLTS
200 WATTS



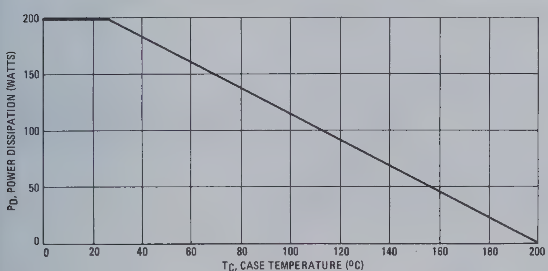
MAXIMUM RATINGS

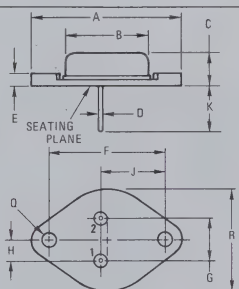
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CER}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Collector-Emitter Voltage	V_{CEO}	90	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-3

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	BV_{CER}	100	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	– –	1.0 5.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter "On" Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.3	Vdc
Collector-Emitter Saturation Voltage (I_C = 7.5 Adc, I_R = 0.75 Adc)	$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

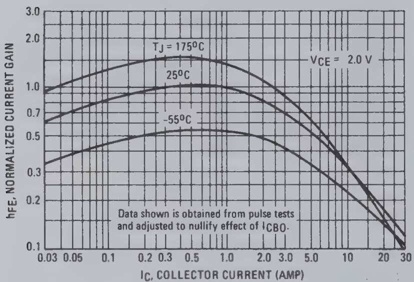


FIGURE 3 – "ON" VOLTAGES

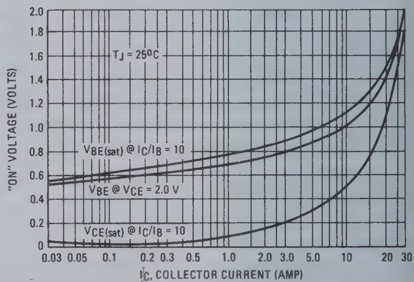
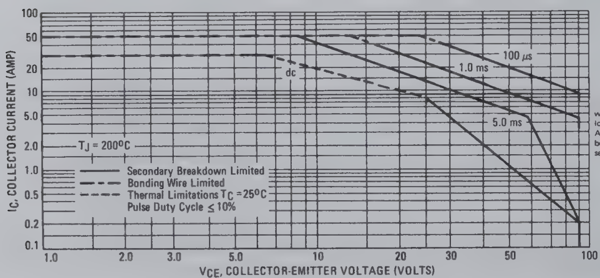


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



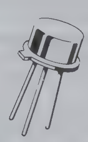
The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

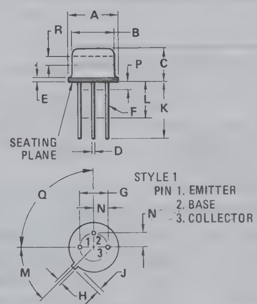
PNP SILICON POWER TRANSISTORS

. . . designed for high-voltage amplifier and saturated switching applications at collector currents to one Ampere. Ideally suited for applications of dc-to-dc converters, relay and hammer drivers, motor controls, and servo and pulse amplifiers. High-voltage ratings permit direct-line operation.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)} = < 1.5$ Vdc (Max) @ $I_C = 500$ mAdc
- High Collector-Emitter Breakdown Voltage — $BV_{CEO} = 200, 300,$ and 400 Vdc (Min)
- DC Current Gain Specified — 10 mAdc to 500 mAdc

1.0 AMPERE
POWER TRANSISTORS
PNP SILICON
200-300-400 VOLTS
5 WATTS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

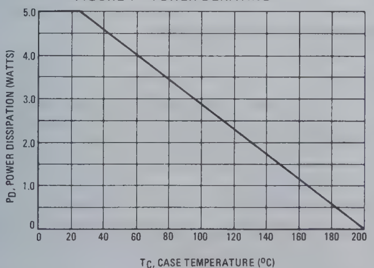
MAXIMUM RATINGS

Rating	Symbol	MJ4645	MJ4646	MJ4647	Unit
Collector-Emitter Voltage	V_{CEO}	200	300	400	Vdc
Collector-Base Voltage	V_{CB}	200	300	400	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 0.5 → ← 1.0 →			Adc
Total Device Dissipation @ $T_C = 25°C$	P_D	← 5.0 →			Watts
Derate above 25°C		← 28.6 →			mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	35	°C/W

FIGURE 1 — POWER DERATING



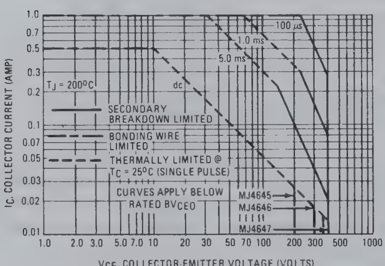
1.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0) MJ4645 MJ4646 MJ4647	BV_{CEO}	 200 300 400	 – – –	 – – –	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0) MJ4645 MJ4646 MJ4647	BV_{CBO}	 200 300 400	 – – –	 – – –	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	5.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 0.5 Vdc)	I_{CEX}	–	–	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 100 mAdc, V_{CE} = 10 Vdc) (1) (I_C = 500 mAdc, V_{CE} = 10 Vdc) (1)	h_{FE}	 20 25 20	 – – –	 – – –	–
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 100 mAdc) MJ4645 MJ4646 MJ4647	$V_{CE(sat)}$	 – – –	 0.5 0.6 0.75	 1.0 1.2 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 70 mAdc, V_{CE} = 20 Vdc, f = 20 MHz) MJ4645, MJ4646 MJ4647,	f_T	 40 30	 – –	 –	MHz
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 100 kHz) MJ4645 MJ4646, MJ4647	C_{ob}	 – –	 – –	 80 60	pF
SWITCHING CHARACTERISTICS					
Delay Time (V_{CC} = 100 Vdc, I_C = 500 mAdc,	t_d	–	–	100	ns
Rise Time I_{B1} = 50 mAdc, $V_{BE(off)}$ = 5.0 Vdc)	t_r		–	100	ns
Turn-Off Time (V_{CC} = 100 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc, Pulse Width = 1.0 μs)	t_{off}	–	–	720	ns

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant$ 200°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJ6502
MJ6503

MOTOROLA

Designers Data Sheet

SWITCHMODE SERIES
PNP SILICON POWER TRANSISTORS

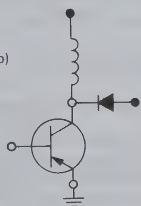
The MJ6502 and MJ6503 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
  100 ns Inductive Fall Time @ 25°C (Typ)
  125 ns Inductive Crossover Time @ 25°C (Typ)

Operating Temperature Range −65 to +200°C

100°C Performance Specified for:
  Reversed Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents



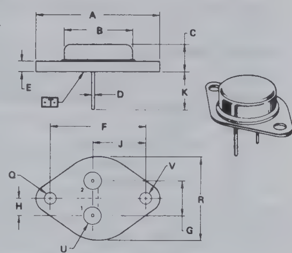
8 AMPERE

PNP SILICON
POWER TRANSISTORS

250 AND 400 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1 187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1,050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

CASE 1-05

MAXIMUM RATINGS

Rating	Symbol	MJ6502	MJ6503	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	400	Vdc
Collector-Emitter Voltage	V_{CEV}	300	450	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	8.0 16		Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	4.0 8.0		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	125 71.5 0.714		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 10 mA, I_B = 0)	MJ6502 MJ6503	$V_{CEO(sus)}$	250 400	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	 – –	 – –	 0.5 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5 Vdc)		h_{FE}	15		–	–
Collector-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 1.0 Adc) (I_C = 8 Adc, I_B = 3.0 Adc) (I_C = 4 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	 – – –	 – – –	 1.5 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 1.0 Adc) (I_C = 4 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{BE(sat)}$	 – –	 –	 1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	100	–	400	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, t_p = 50 μs, Duty Cycle ≤ 2%)	t_d		0.025	0.1	μs
Rise Time		t_r	–	0.100	0.5	μs
Storage Time	(V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%)	t_s		0.60	2.0	μs
Fall Time		t_f	–	0.11	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 4 A(pk), V_{CE}(pk) = 250 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	0.8	3.0	μs
Crossover Time		t_c		0.4	1.5	μs
Fall Time		t_{fi}	–	0.1	–	μs
Storage Time	(I_C = 4 A(pk), V_{CE}(pk) = 250 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}		0.5		μs
Crossover Time		t_c	–	0.125	–	μs
Fall Time		t_{fi}		0.1	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

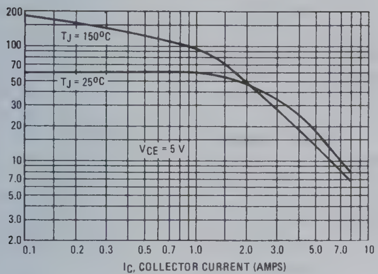


FIGURE 2 – COLLECTOR SATURATION REGION

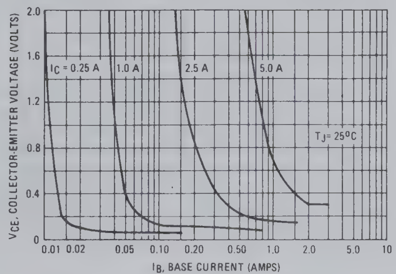


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

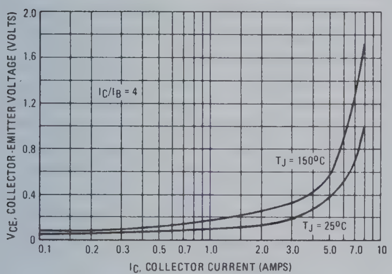


FIGURE 4 – BASE-EMITTER VOLTAGE

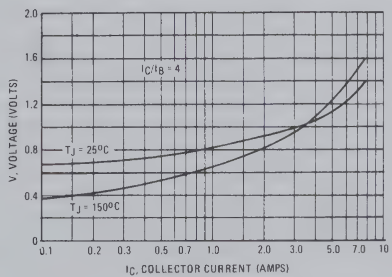


FIGURE 5 – COLLECTOR CUTOFF REGION

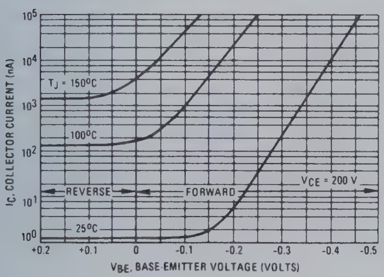
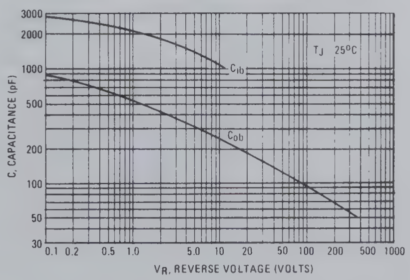


FIGURE 6 – CAPACITANCE



1.3

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

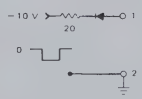
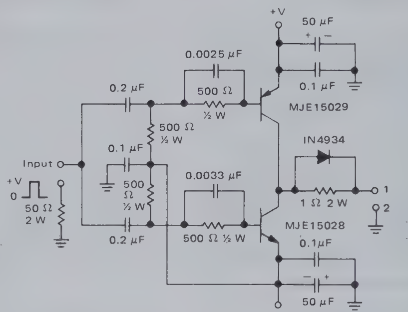
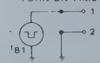
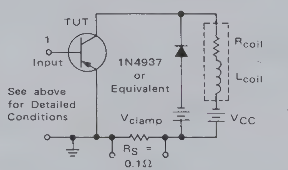
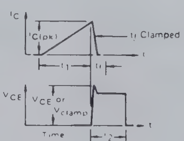
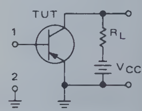
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C 100 mA	 −V adjusted to obtain desired I_{B1} +V adjusted to obtain desired $V_{BE(off)}$	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} 180 μH R_{coil} 0.05 Ω V_{CC} 20 V V_{clamp} = 250 V R_B adjusted to attain I_{B1}	V_{CC} = 250 V R_L = 62 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

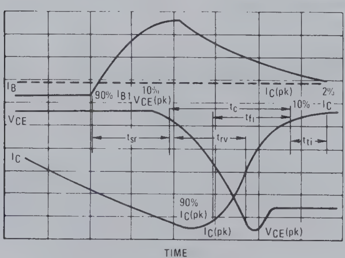
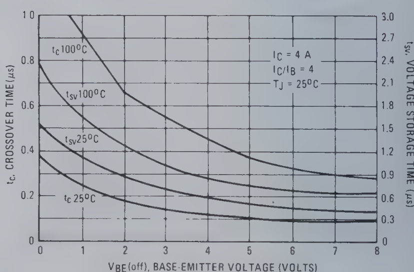


FIGURE 8 – INDUCTIVE SWITCHING TIMES



1.3

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE}(pk)$
t_{rv} = Voltage Rise Time, 10–90% $V_{CE}(pk)$
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% $V_{CE}(pk)$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 9 — TURN-ON SWITCHING TIMES

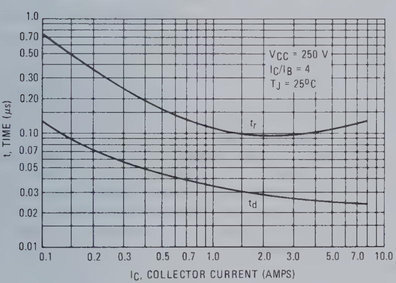


FIGURE 10 — TURN-OFF SWITCHING TIMES

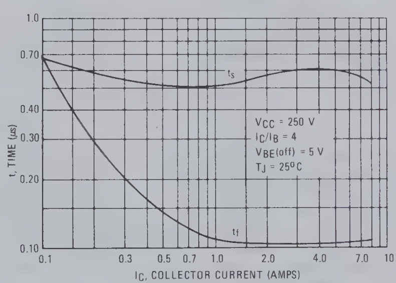
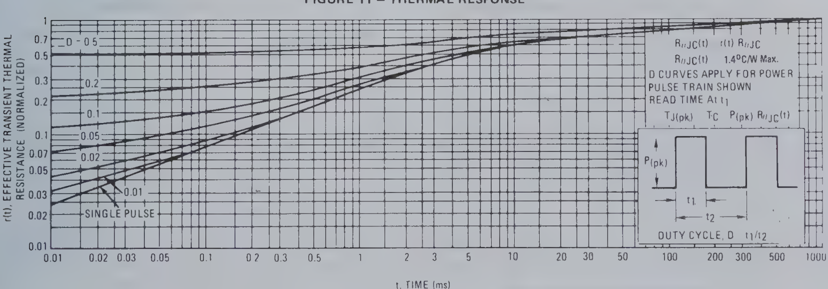


FIGURE 11 — THERMAL RESPONSE



1.3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

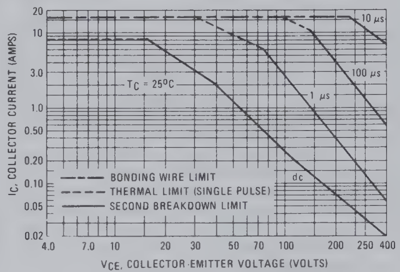
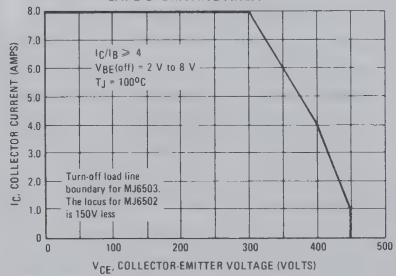


FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

FIGURE 14 PEAK REVERSE BASE CURRENT

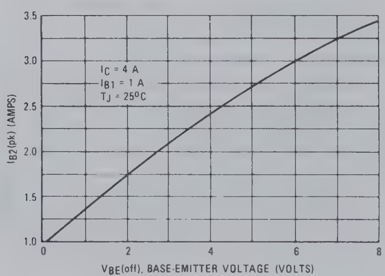
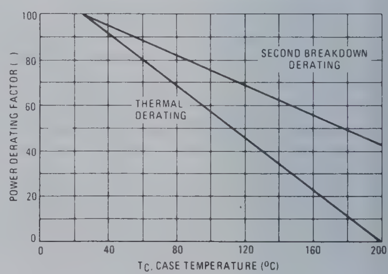


FIGURE 15 POWER DERATING



MOTOROLA

1.3

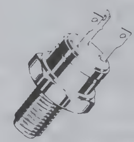
MEDIUM-POWER PNP SILICON TRANSISTORS

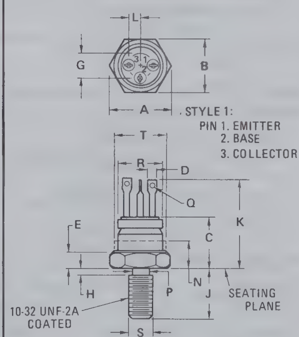
. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 7.0 Adc
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact, High Dissipation TO-59 Case
- Isolated Collector Configuration — 700 V Breakdown

7 AMPERE
POWER TRANSISTORS
PNP SILICON

60 VOLTS
60 WATTS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	10.77	11.10	0.424	0.437
C	8.13	11.89	0.320	0.468
E	2.29	3.81	0.090	0.150
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	10.16	11.56	0.400	0.455
K	14.48	19.38	0.570	0.763
L	2.29	2.79	0.090	0.110
N	–	6.35	–	0.250
P	4.14	4.80	0.163	0.189
Q	1.02	1.65	0.040	0.065
R	8.08	9.65	0.318	0.380
S	4.212	4.310	0.1658	0.1697
T	9.65	11.10	0.380	0.437

All JEDEC dimensions and notes apply
Collector isolated from case.

CASE 160-03
(TO-59)

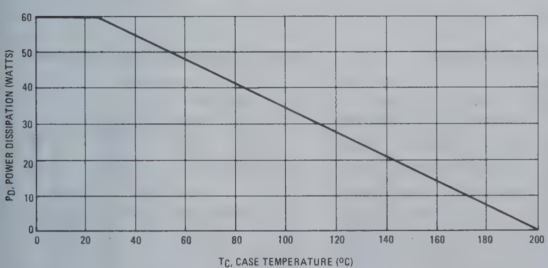
MAXIMUM RATINGS

Rating	Symbol	MJ6700	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	7.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 343	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.91	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2. All limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

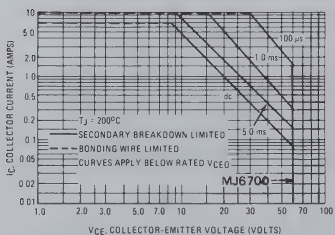
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage [1] (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 55 Vdc, I_B = 0)	I_{CEO}	–	100	μAdc
Collector Cutoff Current (V_{CE} = 55 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	10	μAdc
(V_{CE} = 55 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	1.0	mAdc
Collector Cutoff Current (V_{CB} = 60Vdc, I_E = 0)	I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS [1]				
DC Current Gain	h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)		25	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)		25	180	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)		15	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)		–	0.7	
(I_C = 7.0 Adc, I_B = 0.7 Adc)		–	1.2	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)		–	1.2	
(I_C = 7.0 Adc, I_B = 0.7 Adc)		–	2.0	
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)	f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	300	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)	C_{ib}	–	1250	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 40 Vdc, $V_{BE(off)}$ = 4.0 Vdc,	t_d	–	100	ns
Rise Time	I_C = 2.0 Adc, I_{B1} = 200 mAdc)	t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	t_s	–	1.0	μs
Fall Time	I_{B1} = I_{B2} = 200 mAdc)	t_f	–	150	ns

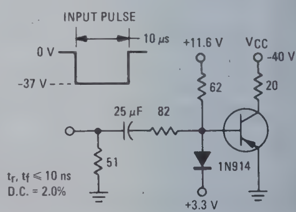
[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 3 – SWITCHING TIME TEST CIRCUIT



MOTOROLA

MEDIUM-POWER PNP SILICON TRANSISTORS

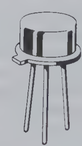
. . . designed for switching and wide band amplifier applications.

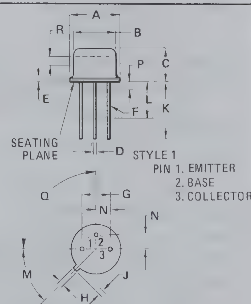
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 5.0 Amp
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-39 Case for Critical Space-Limited Applications.

5 AMPERE POWER TRANSISTORS

PNP SILICON

60 VOLTS
10 WATTS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70		0.500	–
L	6.35	–	0.250	–
M	45^o NOM		45^o NOM	
P	–	1.27	-	0.050
Q	90^o NOM		90^o NOM	
R	2.54		0.100	

All JEDEC dimensions and notes apply.
CASE 79-02
TO-39

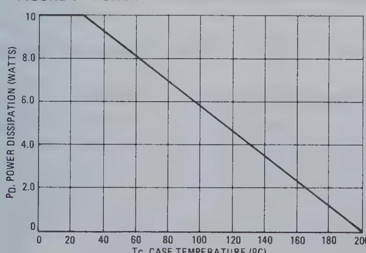
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	5.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	10 57.2	Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	17.5	$^oC/W$

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2. All limits are applicable and must be observed.

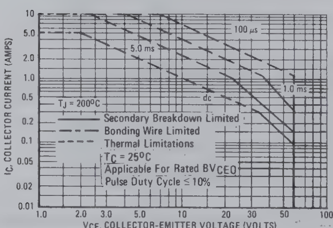
1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage [1] (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 55 Vdc, I_B = 0)	I_{CEO}	–	100	µAdc
Collector Cutoff Current (V_{CE} = 55 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	10	µAdc
(V_{CE} = 55 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	1.0	mAdc
Collector Cutoff Current (V_{CB} = 60 V, I_E = 0)	I_{CBO}	–	10	µAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	100	µAdc
ON CHARACTERISTICS [1]				
DC Current Gain	h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)		25	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)		25	180	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)		15	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)		–	0.7	
(I_C = 5.0 Adc, I_B = 0.5 Adc)		–	1.2	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)		–	1.2	
(I_C = 5.0 Adc, I_B = 0.5 Adc)		–	1.8	
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 10 MHz)	f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	300	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)	C_{ib}	–	1250	pF
SWITCHING CHARACTERISTICS				
Delay Time (V_{CC} = 40 Vdc, $V_{BE(off)}$ = 4.0 Vdc,	t_d	–	100	ns
Rise Time I_C = 2.0 Adc, I_{B1} = 0.2 Adc)	t_r	–	100	ns
Storage Time (V_{CC} = 40 Vdc, I_C = 2.0 Adc,	t_s	–	1.0	µs
Fall Time I_{B1} = I_{B2} = 0.2 Adc)	t_f	–	150	ns

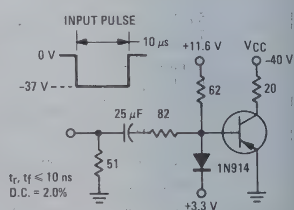
[1] Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 3 – SWITCHING TIME TEST CIRCUIT



MJ8500
MJ8501

MOTOROLA

1.3

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ8500 and MJ8501 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 300 ns Inductive Fall Time — 25°C (Typ)
- 500 ns Inductive Crossover Time — 25°C (Typ)
- 900 ns Inductive Storage Time — 25°C (Typ)

Operating Temperature Range −65 to +200°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

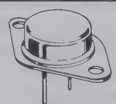
2.5 AMPERE

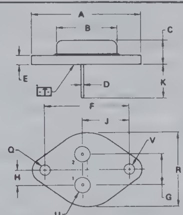
NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS
2. $\boxed{-T-}$ IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

⌖	⌀.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS

⌖	⌀.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1 BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37	–	1.550
B	–	21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

MAXIMUM RATINGS

Rating	Symbol	MJ8500	MJ8501	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	2.5 5.0	2.5 5.0	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	2.0 4.0	2.0 4.0	Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	125 71 0.71	125 71 0.71	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) MJ8500 (I_C = 100 mA, I_B = 0) MJ8501	$V_{CEO(sus)}$	700 800	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 – –	 – –	 0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	7.5	–	–	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.33 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 1.0 Adc, I_B = 0.33 Adc, T_C = 100°C)	$V_{CE(sat)}$	 – – –	 – – –	 2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.33 Adc) (I_C = 1.0 Adc, I_B = 0.33 Adc, TC = 100°C)	$V_{BE(sat)}$	 – –	 – –	 1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	50	–	250	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — (V_{CC} = 500 Vdc, I_C = 1.0 A, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.045	0.20	μs
Rise Time	t_r	–	0.2	2.0	μs
Storage Time	t_s	–	1.0	4.0	μs
Fall Time	t_f	–	0.5	2.0	μs
Inductive Load, Clamped (Table 1)					
Storage Time — (I_C = 1.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	1.3	4.0	μs
Crossover Time	t_c	–	0.6	2.0	μs
Storage Time — (I_C = 1.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	0.9	–	μs
Crossover Time	t_c	–	0.5	–	μs
Fall Time	t_{fi}	–	0.3	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

1.3

FIGURE 1 — DC CURRENT GAIN

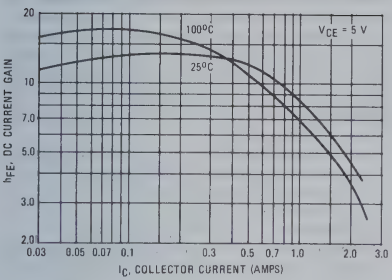


FIGURE 2 — COLLECTOR SATURATION REGION

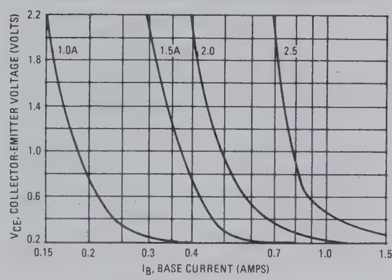


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

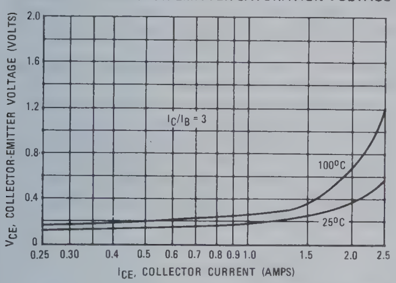


FIGURE 4 — BASE-EMITTER VOLTAGE

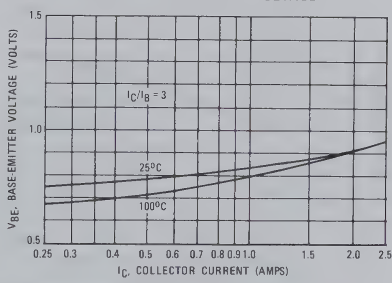


FIGURE 5 — COLLECTOR CUTOFF REGION

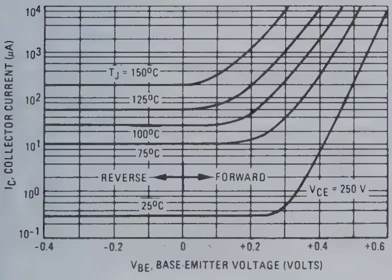


FIGURE 6 — CAPACITANCE

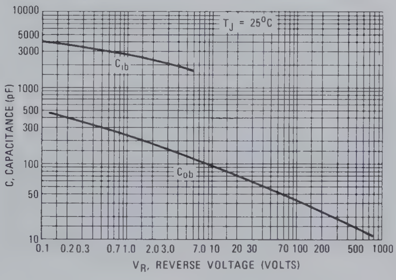


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FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

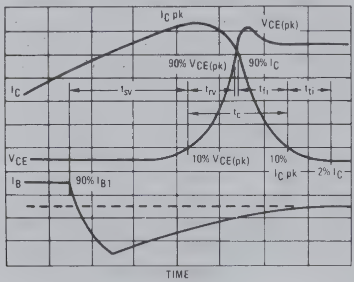
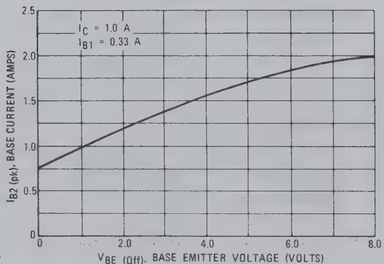


FIGURE 8 — PEAK REVERSE BASE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE\ (pk)}$
t_{rv} = Voltage Rise Time, 10–90% $V_{CE\ (pk)}$
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% $V_{CE\ (pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 — TURN - ON SWITCHING TIMES

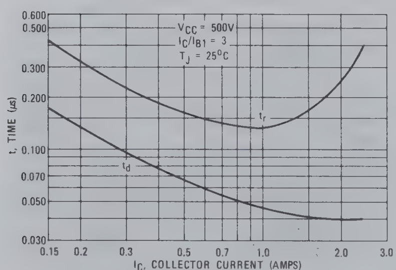


FIGURE 10 — TURN - OFF SWITCHING TIMES

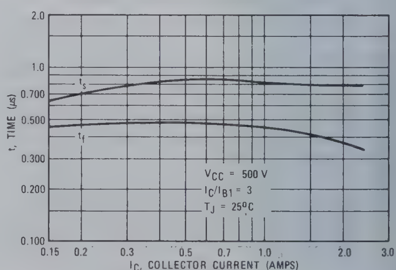


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

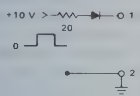
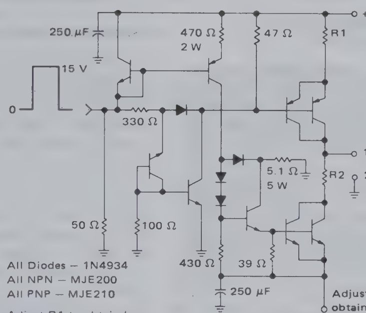
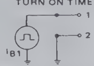
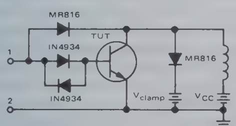
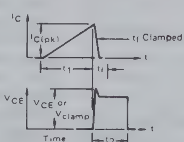
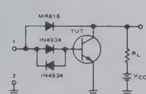
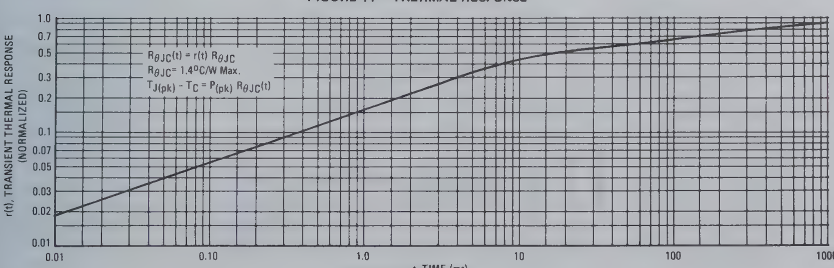
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞ Adjust to obtain $V_{BE(off)}$ = –5.0 V	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 500 V	V_{CC} = 500 V R_L = 500 Ω Pulse Width = 50 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 11 – THERMAL RESPONSE



1.3

FIGURE 12 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

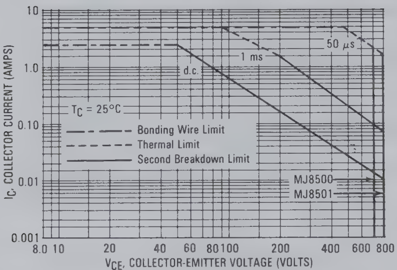
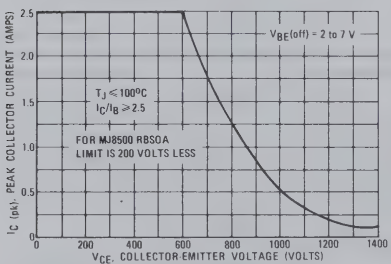


FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

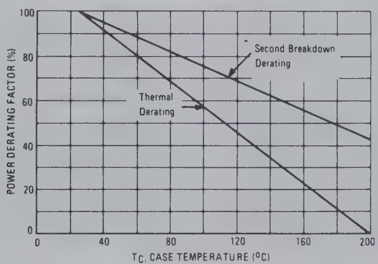
The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 — POWER DERATING



MJ8502
MJ8503

MOTOROLA

1.3

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ8502 and MJ8503 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

150 ns Inductive Fall Time—25°C (Typ)
400 ns Inductive Crossover Time—25°C (Typ)
1200 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range −65 to + 200°C

100°C Performance Specified for:

Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

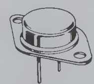
5.0 AMPERE

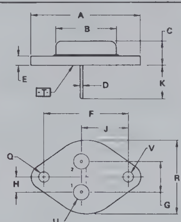
NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	⌀.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	⌀.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B		21.08	–	0 830
C	6 35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3 81	4.19	0.150	0.165
R		26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4 19	0.150	0 165

CASE 1-05 TO-3

MAXIMUM RATINGS

Rating	Symbol	MJ8502	MJ8503	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	5.0 10	5.0 10	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	4.0 8.0	4.0 8.0	Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	150 86 0.85	150 86 0.85	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.16	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

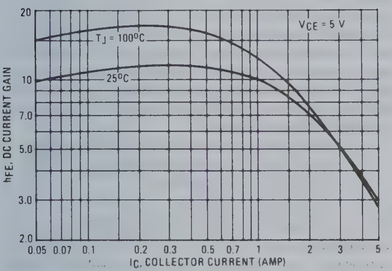
1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) MJ8502 (I_C = 100 mA, I_B = 0) MJ8503		$V_{CEO(sus)}$	700 800	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	– –	– –	0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	7.5	–	–	–
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 2.0 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	– – –	– – –	2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{BE(sat)}$	– –	– –	1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	60	–	300	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 500 Vdc, IC = 2.5A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.040	0.20	μs
Rise Time		t_r	–	0.125	2.0	μs
Storage Time		t_s	–	1.2	4.0	μs
Fall Time		t_f	–	0.65	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 2.5 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, TC = 100°C)	t_{sv}	–	1.6	5.0	μs
Crossover Time		t_c	–	0.60	2.0	μs
Storage Time	(I_C = 2.5 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	1.2	–	μs
Crossover Time		t_c	–	0.4	–	μs
Fall Time		t_{fi}	–	0.15	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 — DC CURRENT GAIN



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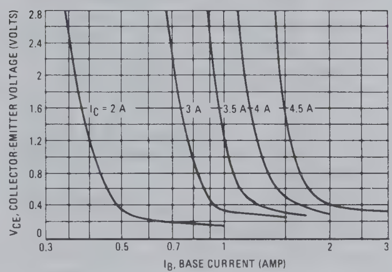

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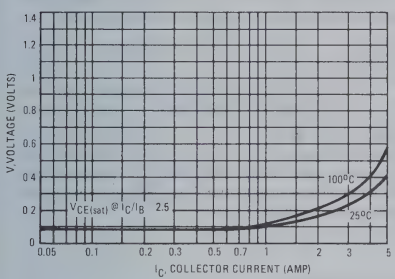
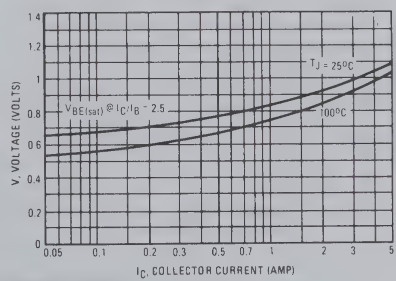


FIGURE 4 — BASE-EMITTER VOLTAGE



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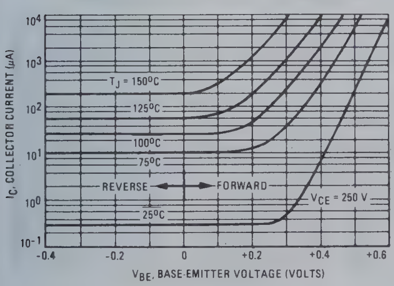

FIGURE 6 — CAPACITANCE

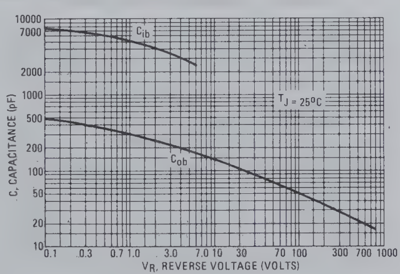

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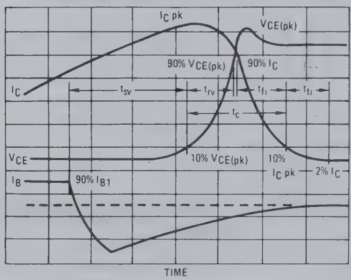
FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS



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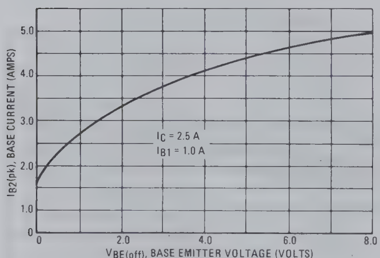

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RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 — TURN-ON SWITCHING TIMES

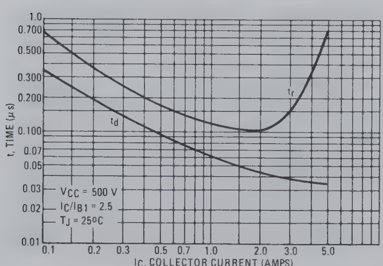


FIGURE 10 — TURN-OFF SWITCHING TIMES

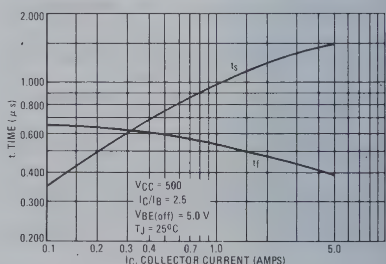


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

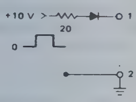
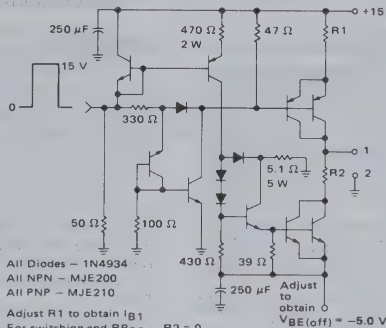
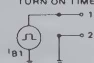
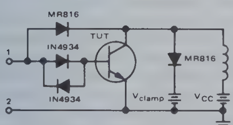
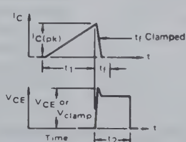
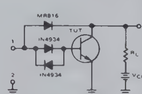
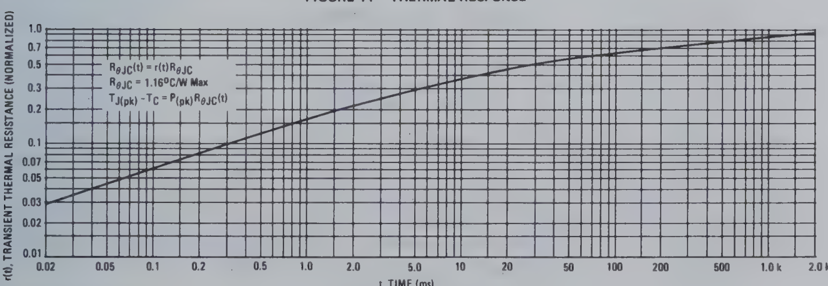
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 500 V	V_{CC} = 500 V R_L = 200 Ω Pulse Width = 50 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 11 – THERMAL RESPONSE



1.3

SAFE OPERATING AREA INFORMATION

FIGURE 12 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA

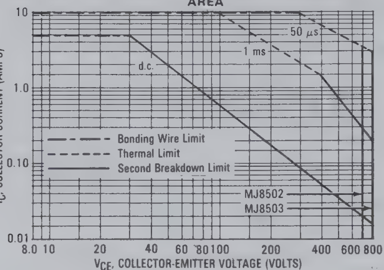
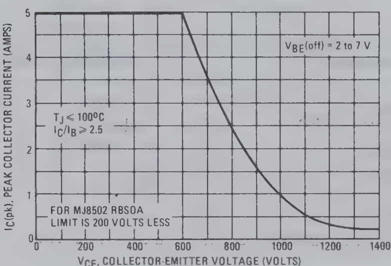


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

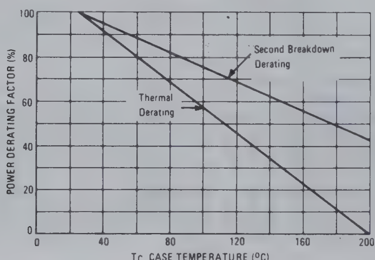
The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



MJ8504
MJ8505

MOTOROLA

1.3

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ8504 and MJ8505 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 75 ns Inductive Fall Time $-25^{\circ}C$ (typ)
- 150 ns Inductive Crossover Time $-25^{\circ}C$ (typ)
- 1.25 μs Inductive Storage Time $-25^{\circ}C$ (typ)

Operating Temperature Range -65 to $+200^{\circ}C$

$100^{\circ}C$ Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

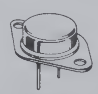
10 AMPERE

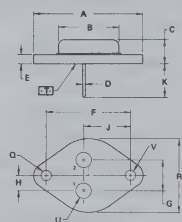
NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.





NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. -T- IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q.
   ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37		1.550
B	–	21 08	–	0 830
C	6 35	7.62	0 250	0.300
D	0.97	1 09	0.038	0 043
E	–	3 43		0 135
F	30 15 BSC		1 187 BSC	
G	10.92 BSC		0.430 BSC	
H	5 46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0 440	0 480
Q	3.81	4.19	0 150	0 165
R	–	26 67	–	1.050
U	4 83	5 33	0 190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

MAXIMUM RATINGS

Rating	Symbol	MJ8504	MJ8505	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	10 15	10 15	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	8 12	8 12	Adc
Total Power Dissipation @ $T_C = 25^{\circ}C$ @ $T_C = 100^{\circ}C$ Derate above $25^{\circ}C$	P_D	175 100 1.0	175 100 1.0	Watts $W/^{\circ}C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to $+200$		$^{\circ}C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^{\circ}C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^{\circ}C$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq$ 10%.

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ8504		$V_{CEO(sus)}$	700	–	–	Vdc
MJ8505			800	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 1.5 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	7.5	–	–	–
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5.0 Adc, I_B = 2.0 Adc)			–	–	2.0	
(I_C = 10 Adc, I_B = 4.0 Adc)			–	–	5.0	
(I_C = 5.0 Adc, I_B = 2.0 Adc, T_C = 100°C)			–	–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 5.0 Adc, I_B = 2.0 Adc)			–	–	1.5	
(I_C = 5.0 Adc, I_B = 2.0 Adc, T_C = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	90	–	450	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 500 Vdc, I_C = 5.0 A, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.050	0.20	μs
Rise Time		t_r	–	0.175	2.0	μs
Storage Time		t_s	–	1.25	4.0	μs
Fall Time		t_f	–	0.60	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc. T_C = 100°C	t_{sv}	–	1.75	5.5	μs
Crossover Time		t_c	–	0.400	2.0	μs
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	1.25	–	μs
Crossover Time		t_c	–	0.150	–	μs
Fall Time		t_{fi}	–	0.075	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – DC CURRENT GAIN

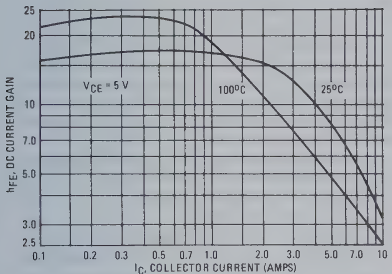


FIGURE 2 – COLLECTOR SATURATION REGION

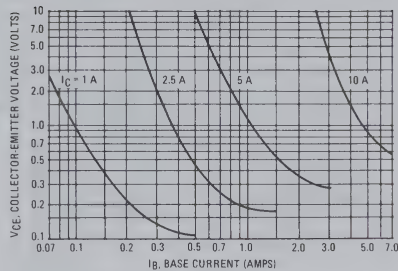


FIGURE 3 – COLLECTOR-EMITTER SATURATION REGION

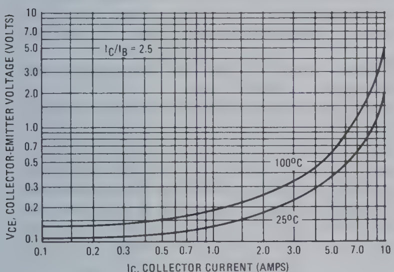


FIGURE 4 – BASE EMITTER VOLTAGE

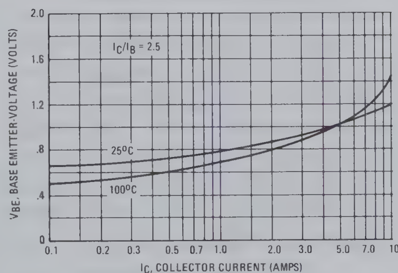


FIGURE 5 – COLLECTOR CUTOFF REGION

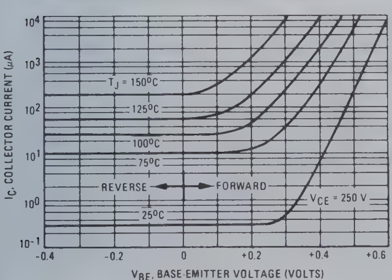
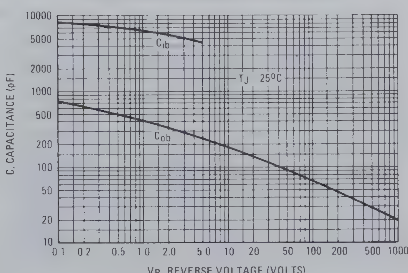


FIGURE 6 – CAPACITANCE



1.3

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

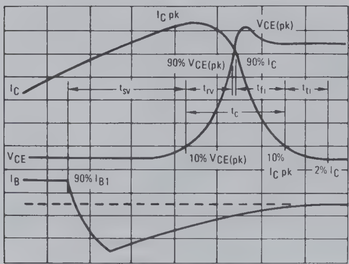
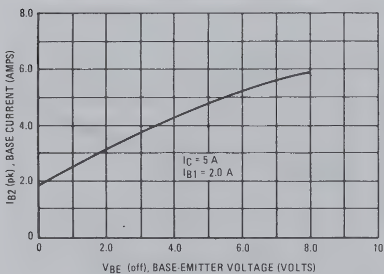


FIGURE 8 — PEAK REVERSE BASE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$
t_{rv} = Voltage Rise Time, 10–90% $V_{CE(pk)}$
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 — TURN-ON SWITCHING TIMES

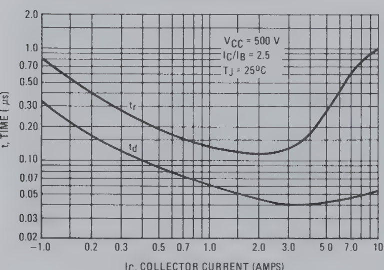
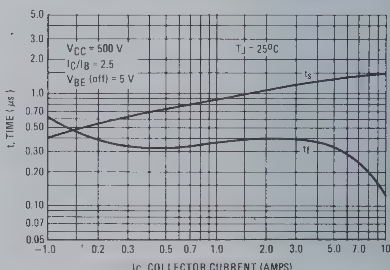


FIGURE 10 — TURN-OFF SWITCHING TIMES



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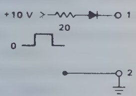
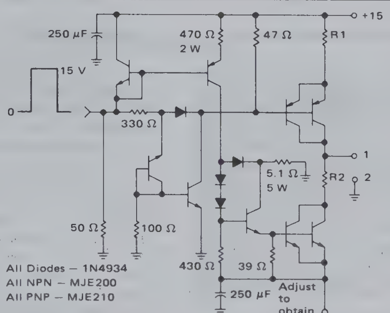
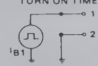
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
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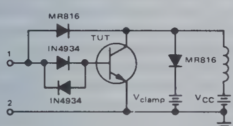
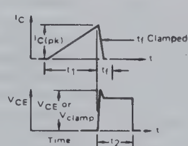
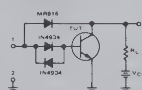
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

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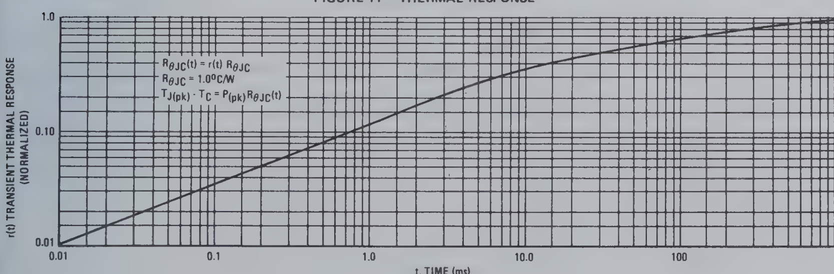

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FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

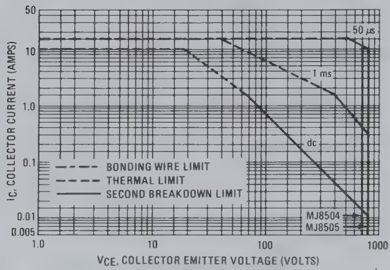
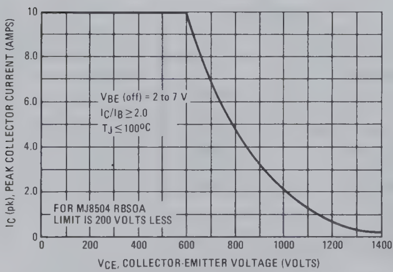


FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

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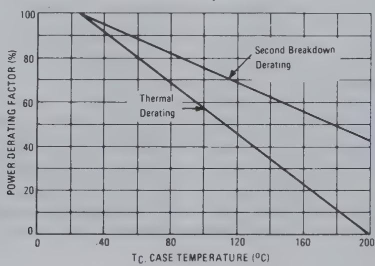


MJ10000
MJ10001

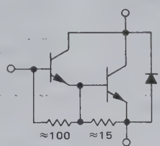
MOTOROLA

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10000 and MJ10001 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

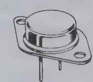


100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times With Inductive Loads — 210 ns Inductive Fall Time (Typ)
- Saturation Voltages
- Leakage Currents

20 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
350 and 400 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



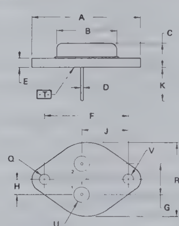
MAXIMUM RATINGS

Rating	Symbol	MJ10000	MJ10001	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ $T_C = 25^\circ C$ @ $T_C = 100^\circ C$ Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10000	$V_{CEO(sus)}$	350	–	–	Vdc
MJ10001		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) I_C = 2 A, V_{clamp} = Rated V_{CEX}, $T_C = 100^oC$ MJ10000	$V_{CEX(sus)}$	400	–	–	Vdc
MJ10001		450	–	–	
I_C = 10 A, V_{clamp} = Rated V_{CEX}, $T_C = 100^oC$ MJ10000		275	–	–	
MJ10001		325	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	0.25	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150^oC$)		–	–	5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, $T_C = 100^oC$)	I_{CER}	–	–	5	mAdc
Emitter Cutoff Current (V_{EB} = 8 Vdc, I_C = 0)	I_{EBO}	–	–	150	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			Adc
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)	h_{FE}	50	–	600	–
(I_C = 10 Adc, V_{CE} = 5 Vdc)		40	–	400	
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 400 mAdc)	$V_{CE(sat)}$	–	–	1.9	Vdc
(I_C = 20 Adc, I_B = 1 Adc)		–	–	3	
(I_C = 10 Adc, I_B = 400 mAdc, $T_C = 100^oC$)		–	–	2	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 400 mAdc)	$V_{BE(sat)}$	–	–	2.5	Vdc
(I_C = 10 Adc, I_B = 400 mAdc, $T_C = 100^oC$)		–	–	2.5	
Diode Forward Voltage (1) (I_F = 10 Adc)	V_f	–	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	$\|h_{fe}\|$	10		–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	100		325	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%).	t_d	–	0.12	0.2	μs
Rise Time	t_r	–	0.20	0.6	μs
Storage Time	t_s	–	1.5	3.5	μs
Fall Time	t_f	–	1.1	2.4	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, $T_C = 100^oC$)	t_{sv}	–	3.5	5.5	μs
Crossover Time	t_c	–	1.5	3.7	μs
Storage Time (I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, $T_C = 25^oC$)	t_{sv}	–	1.0	–	μs
Crossover Time	t_c	–	0.7	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

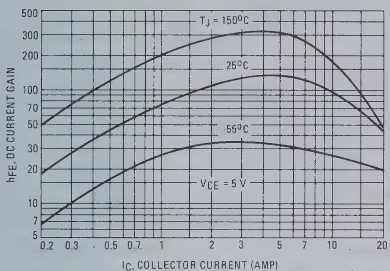


FIGURE 2 — COLLECTOR SATURATION REGION

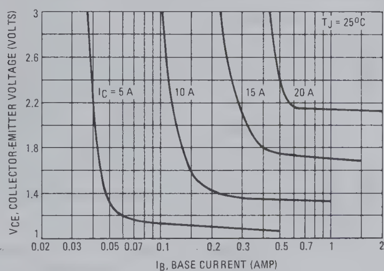


FIGURE 3 — COLLECTOR EMMITTER SATURATION VOLTAGES

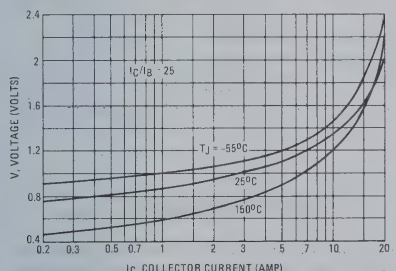


FIGURE 4 — BASE-EMITTER VOLTAGE

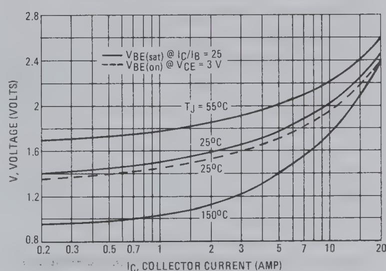


FIGURE 5 — COLLECTOR CUTOFF REGION

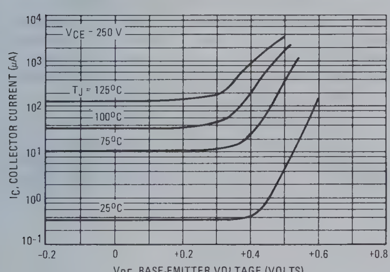
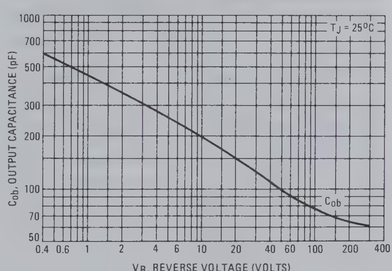


FIGURE 6 — OUTPUT CAPACITANCE



1.3

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

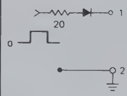
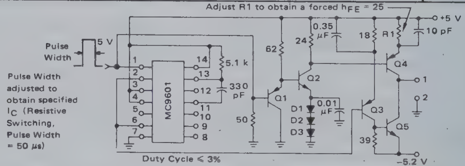
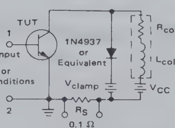
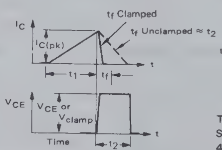
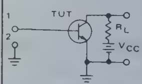
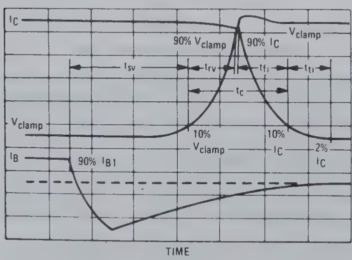
	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA	 Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 µs)	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above For Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope-Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c)\, f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

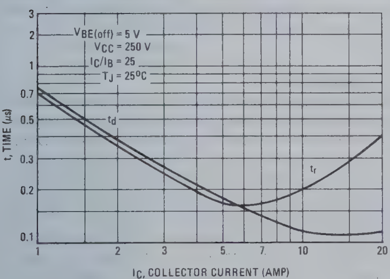


FIGURE 9 — TURN-OFF TIME

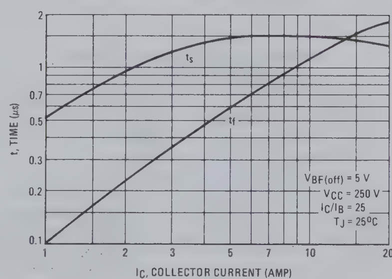
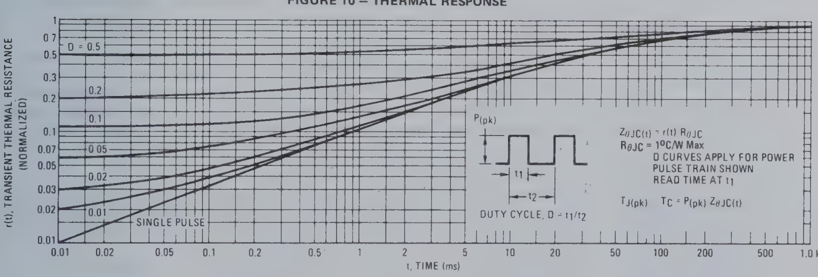


FIGURE 10 — THERMAL RESPONSE



1.3

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATING AREA

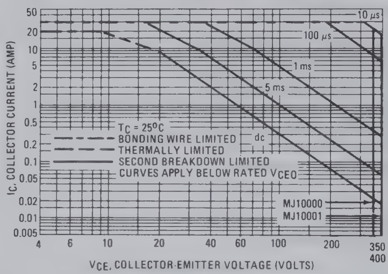
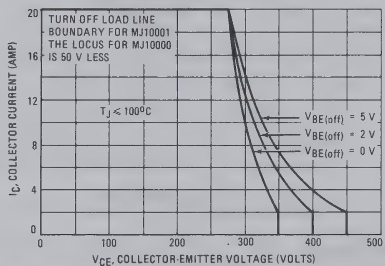


FIGURE 12 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

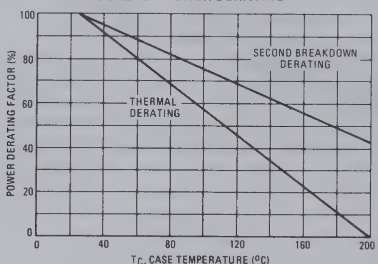
The data of Figure 11 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 — POWER DERATING



MOTOROLA

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10002 and MJ10003 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

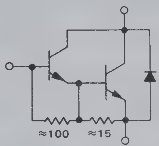
100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads

Switching Times with Inductive Loads — 140 ns Inductive Fall Time (Typ)

Saturation Voltages

Leakage Currents



10 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
350 and 400 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

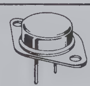
MAXIMUM RATINGS

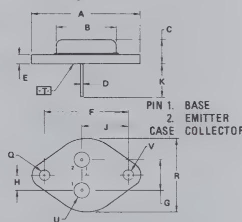
Rating	Symbol	MJ10002	MJ10003	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 20		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5.0		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25°C	P_D	150 100 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

   | ⌖ | ⌀.13 (0.005) Ⓜ | T | V Ⓜ |

   FOR LEADS:

   | ⌖ | ⌀.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10002	$V_{CEO(sus)}$	350	–	–	Vdc
MJ10003		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) (I_C = 1.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10002	$V_{CEX(sus)}$	400	–	–	Vdc
MJ10003		450	–	–	
(I_C = 5.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10002		275	–	–	
MJ10003		325	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	0.25	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–		5.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–		5.0	mAdc
Emitter Cutoff Current (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			Adc
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	–	500	–
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)		30	–	300	
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 250 mAdc)	$V_{CE(sat)}$	–		1.9	Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)		–	–	2.9	
(I_C = 5.0 Adc, I_B = 250 mAdc, T_C = 100°C)		–		2.0	
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 250 mAdc)	$V_{BE(sat)}$	–	–	2.5	Vdc
(I_C = 5.0 Adc, I_B = 250 mAdc, T_C = 100°C)		–	–	2.5	
Diode Forward Voltage (1) (I_F = 5.0 Adc)	V_f	–	3.0	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	$\|h_{fe}\|$	10	–		
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	60	–	275	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — (V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%).	t_d		0.05	0.2	μs
Rise Time	t_r	–	0.25	0.6	μs
Storage Time	t_s	–	1.2	3.0	μs
Fall Time	t_f	–	0.6	1.5	μs
Inductive Load, Clamped (Table 1)					
Storage Time — (I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_{sv}	–	2.1	5.0	μs
Crossover Time	t_c	–	1.3	3.3	μs
Storage Time — (I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_{sv}	–	0.92	–	μs
Crossover Time	t_c	–	0.5	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

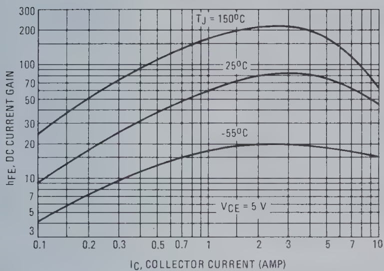


FIGURE 2 — COLLECTOR SATURATION REGION

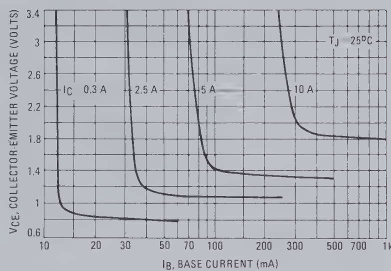


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

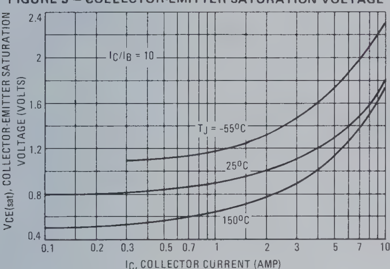


FIGURE 4 — BASE-EMITTER VOLTAGE

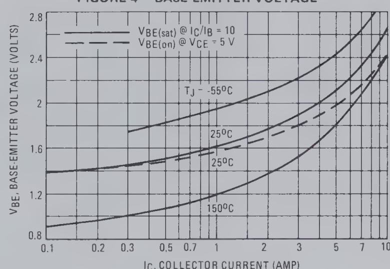


FIGURE 5 — COLLECTOR CUT-OFF REGION

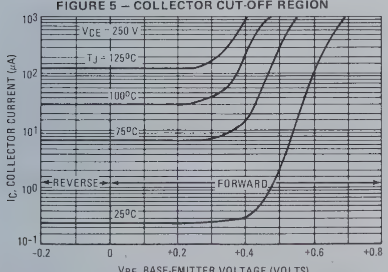
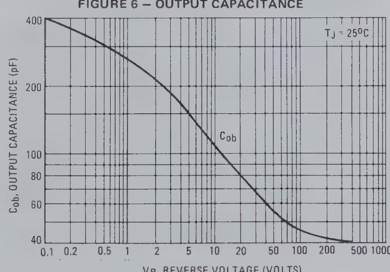


FIGURE 6 — OUTPUT CAPACITANCE



1.3

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

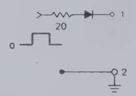
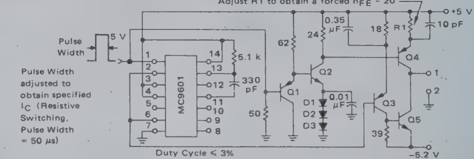
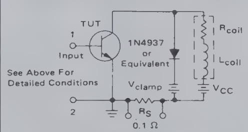
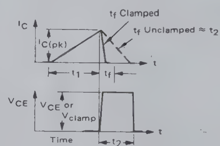
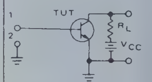
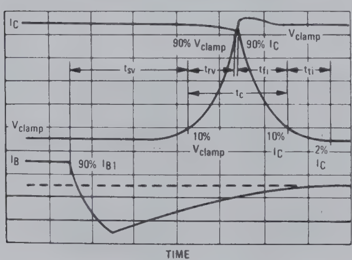
	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA	Adjust R1 to obtain a forced h_{FE} = 20  Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 μs) Duty Cycle ≤ 3%	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above For Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope-Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

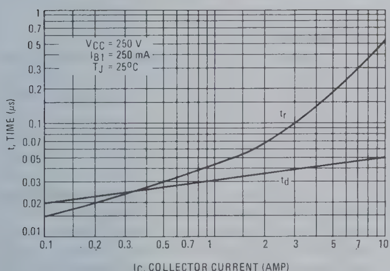


FIGURE 9 — TURN-OFF TIME

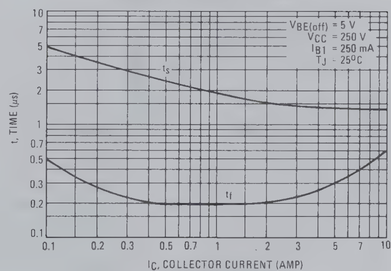
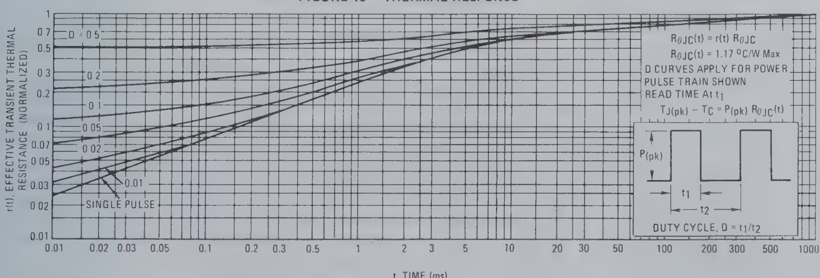


FIGURE 10 — THERMAL RESPONSE



1.3

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – ACTIVE-REGION SAFE OPERATING AREA

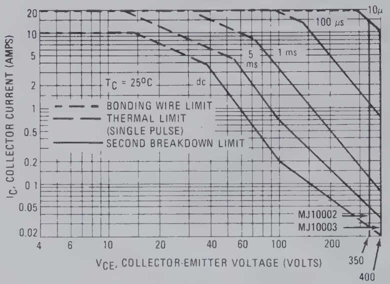
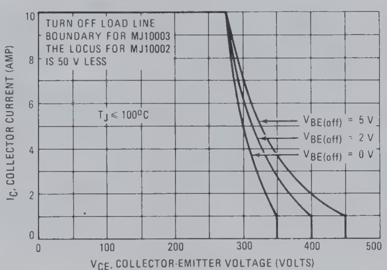


FIGURE 12 – REVERSE BIASED SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

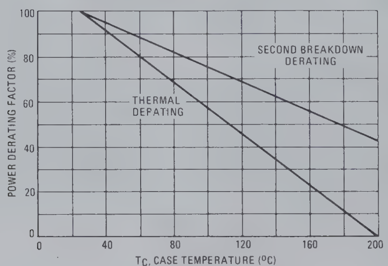
The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



MJ10004
MJ10005

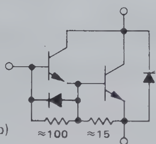
MOTOROLA

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The MJ10004 and MJ10005 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
- 40 ns Inductive Fall Time – 25°C (Typ)
- 650 ns Inductive Storage Time – 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

20 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
350 and 400 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

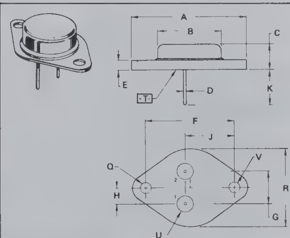
MAXIMUM RATINGS

Rating	Symbol	MJ10004	MJ10005	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	20 30		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2.5 5.0		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25°C	P_D	175 100 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	⌀.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	⌀.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

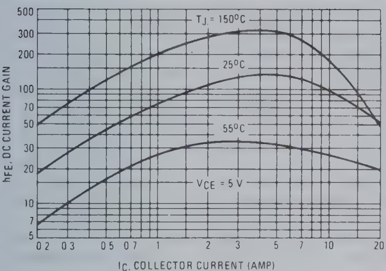
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1)	$V_{CEO(sus)}$				Vdc
(I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10004		350	–	–	
MJ10005		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)	$V_{CEX(sus)}$				Vdc
(I_C = 2.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10004		400	–	–	
MJ10005		450	–	–	
(I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10004		275	–	–	
MJ10005		325	–	–	
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	–	5.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)					
DC Current Gain	h_{FE}				–
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)		50	–	600	
(I_C = 10 Adc, V_{CE} = 5.0 Vdc)		40	–	400	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 400 mAdc)		–	–	1.9	
(I_C = 20 Adc, I_B = 2.0 Adc)		–	–	3.0	
(I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)		–	–	2.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 400 mAdc)		–	–	2.5	
(I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)		–	–	2.5	
Diode Forward Voltage (1) (I_F = 10 Adc)	V_f	–	3.0	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	$\|h_{fe}\|$	10	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	100	–	325	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 400 mA, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%).	t_d	–	0.12	0.2	μs
Rise Time	t_r	–	0.2	0.6	μs
Storage Time	t_s	–	0.6	1.5	μs
Fall Time	t_f	–	0.15	0.5	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_{sv}	–	1.0	2.5	μs
Crossover Time	t_c	–	0.4	1.5	μs
Storage Time (I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_{sv}	–	0.65	–	μs
Crossover Time	t_c	–	0.2	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN



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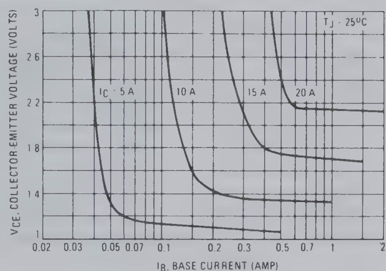
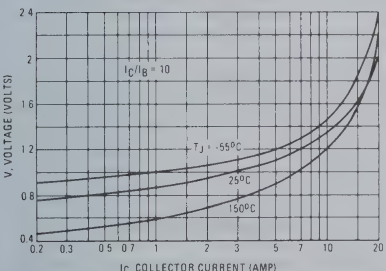


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE



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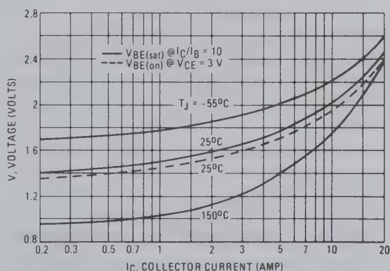

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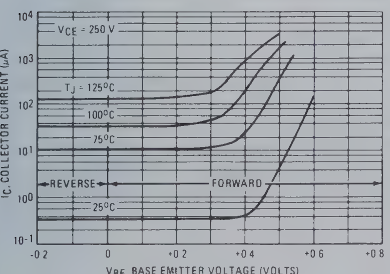

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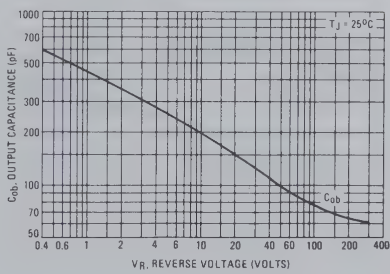

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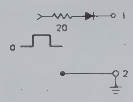
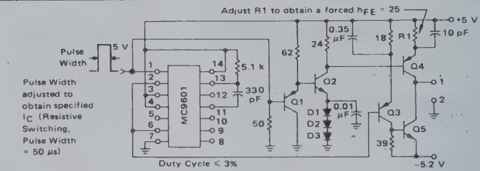
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA	Adjust R1 to obtain a forced h_{FE} = 25  Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 µs)	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
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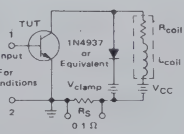
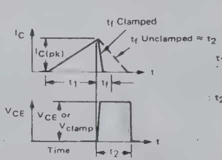
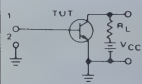
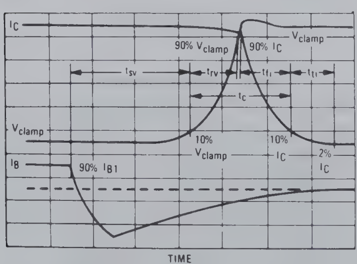
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above For Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



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t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

TYPICAL CHARACTERISTICS

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

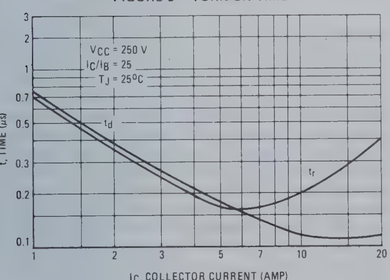


FIGURE 9 — TURN-OFF TIME

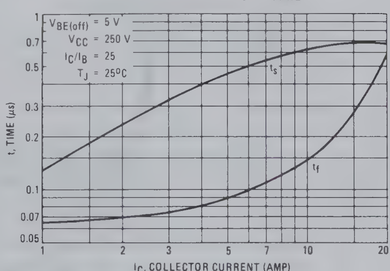
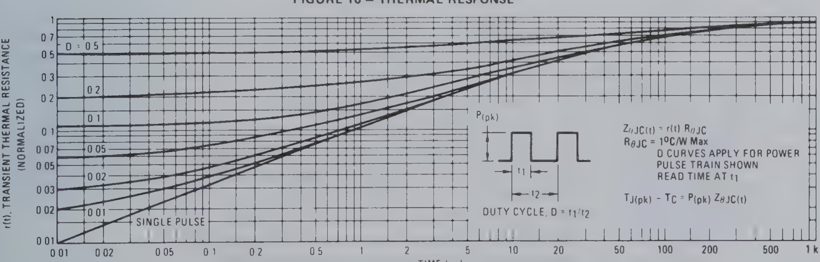


FIGURE 10 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

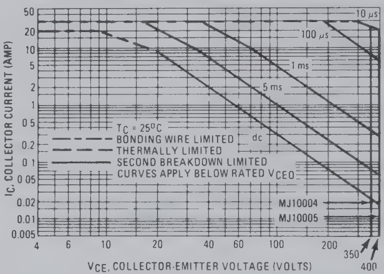
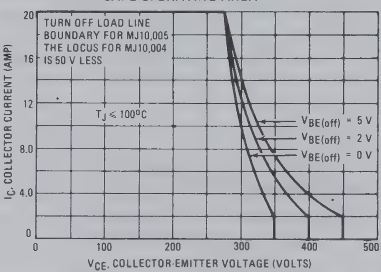


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

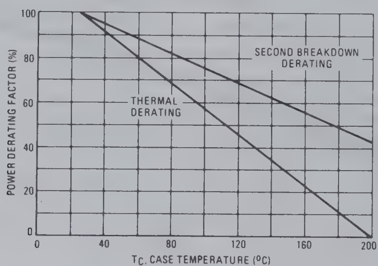
The data of Figure 11 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



MJ10006
MJ10007

MOTOROLA

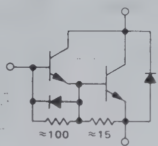
1.3

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10006 and MJ10007 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
  30 ns Inductive Fall Time – 25°C (Typ)
  500 ns Inductive Storage Time – 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:
  Reversed Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents

10 AMPERE

NPN SILICON

POWER DARLINGTON TRANSISTORS

350 AND 400 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

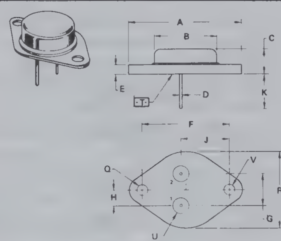
MAXIMUM RATINGS

Rating	Symbol	MJ10006	MJ10007	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	10 20		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2.5 5.0		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	150 100 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES.
1. DIMENSIONS Q AND V ARE DATUMS
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q.

⌖	⌀.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS

⌖	⌀.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21 08		0 830
C	6 35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10 92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0 165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10006 / MJ10007	$V_{CEO(sus)}$	350 / 400	– / –	– / –	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) (I_C = 1 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10006 / MJ10007; (I_C = 5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10006 / MJ10007	$V_{CEX(sus)}$	400 / 450 / 275 / 325	– / – / – / –	– / – / – / –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	– / –	– / –	0.25 / 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40 / 30	– / –	500 / 300	–
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 250 mAdc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 250 mAdc, T_C = 100°C)	$V_{CE(sat)}$	– / – / –	– / – / –	1.9 / 2.9 / 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 250 mAdc) (I_C = 5.0 Adc, I_B = 250 mAdc, T_C = 100°C)	$V_{BE(sat)}$	– / –	– / –	2.5 / 2.5	Vdc
Diode Forward Voltage (1) (I_F = 5.0 Adc)	V_f	–	3.0	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	$\lvert h_{fe} \rvert$	10	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	60	–	275	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — (V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%).	t_d	–	0.05	0.2	μs
Rise Time	t_r	–	0.25	0.6	μs
Storage Time	t_s	–	0.5	1.5	μs
Fall Time	t_f	–	0.06	0.5	μs
Inductive Load, Clamped (Table 1)					
Storage Time — (I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_{sv}	–	0.8	2.0	μs
Crossover Time	t_c	–	0.6	1.5	μs
Storage Time — (I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_{sv}	–	0.5	–	μs
Crossover Time	t_c	–	0.3	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

1.3

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

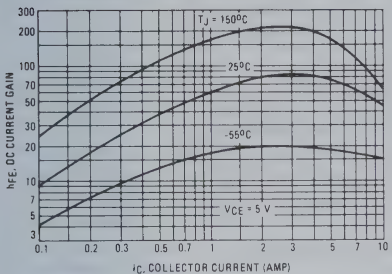


FIGURE 2 — COLLECTOR SATURATION REGION

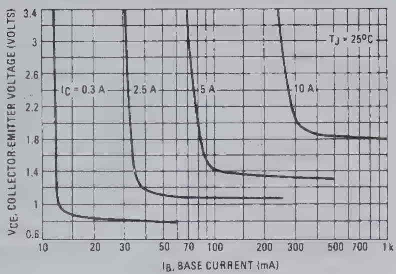


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

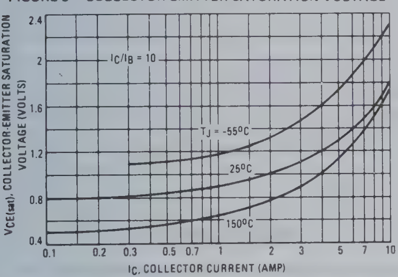


FIGURE 4 — BASE-EMITTER VOLTAGE

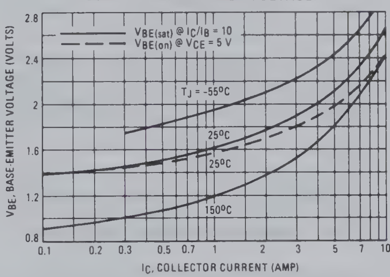


FIGURE 5 — COLLECTOR CUTOFF REGION

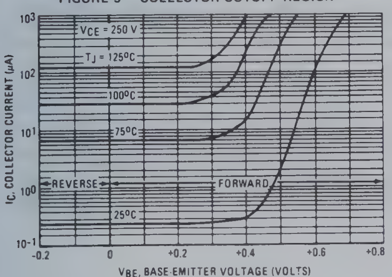
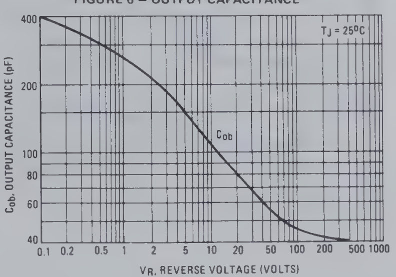


FIGURE 6 — OUTPUT CAPACITANCE



1.3

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

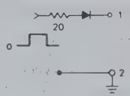
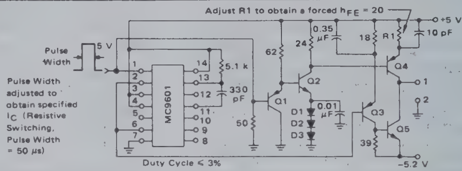
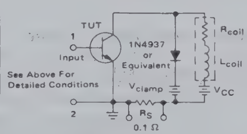
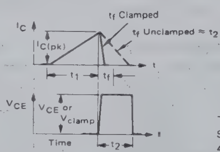
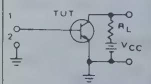
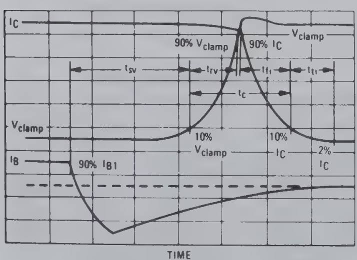
	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA	 Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914	
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V f_o = 500 kHz V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 50 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above For Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope-Tektronix 475 or Equipment	RESISTIVE TEST CIRCUIT 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

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t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

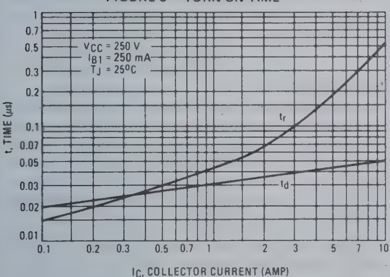


FIGURE 9 – TURN-OFF TIME

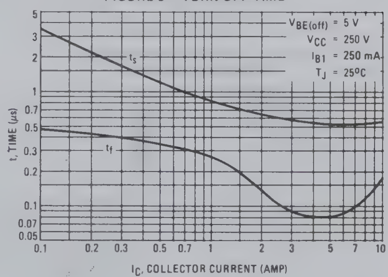
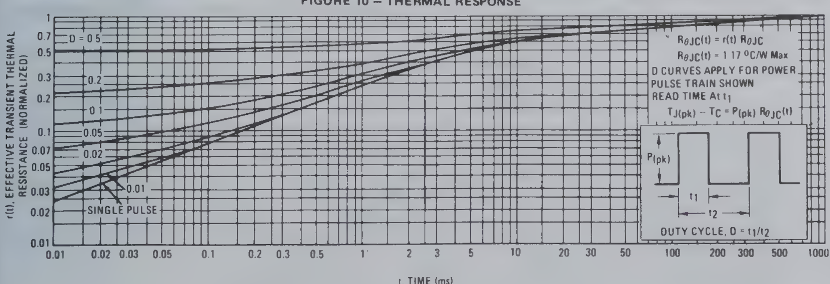


FIGURE 10 – THERMAL RESPONSE



1.3

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

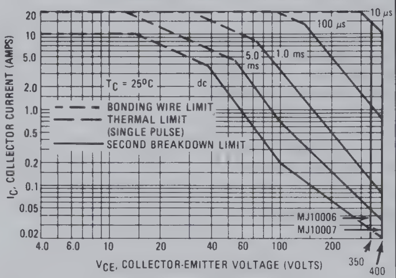
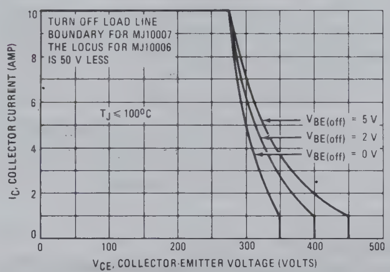


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

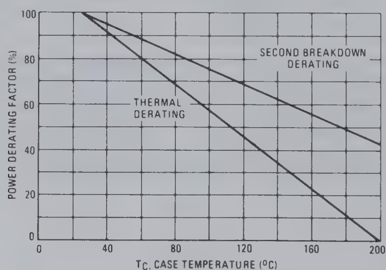
The data of Figure 11 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



MOTOROLA

MJ10008
MJ10009

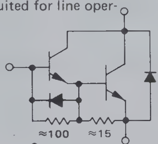
1.3

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10008 and MJ10009 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
 1.6 μs (max) Inductive Crossover Time — 10 A, 100°C
 3.5 μs (max) Inductive Storage Time — 10 A, 100°C

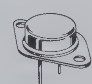
Operating Temperature Range −65 to +200°C

100°C Performance Specified for:
 Reversed Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents

20 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
450 and 500 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



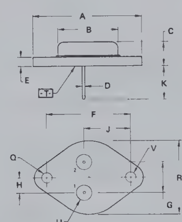
MAXIMUM RATINGS

Rating	Symbol	MJ10008	MJ10009	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	500	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	450	500	Vdc
Collector-Emitter Voltage	V_{CEV}	650	700	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ⩽ 10%.



STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37		1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10008	$V_{CEO(sus)}$	450	–	–	Vdc
MJ10009		500	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) (I_C = 2 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C, $V_{BE(off)}$ = 5 V) MJ10008	$V_{CEX(sus)}$	450	–	–	Vdc
MJ10009		500	–	–	
(I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C, $V_{BE(off)}$ = 5 V) MJ10008		325	–	–	
MJ10009		375	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	0.25	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	–	5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)	h_{FE}	40	–	400	–
(I_C = 10 Adc, V_{CE} = 5 Vdc)		30	–	300	
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 500 mAdc)	$V_{CE(sat)}$	–	–	2	Vdc
(I_C = 20 Adc, I_B = 2 Adc)		–	–	3.5	
(I_C = 10 Adc, I_B = 500 mAdc, T_C = 100°C)		–	–	2.5	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 500 mAdc)	$V_{BE(sat)}$	–	–	2.5	Vdc
(I_C = 10 Adc, I_B = 500 mAdc, T_C = 100°C)		–	–	2.5	
Diode Forward Voltage (1) (I_F = 10 Adc)	V_f	–	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	$\|h_{fe}\|$	8	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	100	–	325	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 25 μs Duty Cycle ≤ 2%)	t_d	–	0.12	0.25	μs
Rise Time	t_r	–	0.5	1.5	μs
Storage Time	t_s	–	0.8	2.0	μs
Fall Time	t_f	–	0.2	0.6	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_C = 10 A(pk), V_{clamp} = 250 V, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	1.5	3.5	μs
Crossover Time	t_c	–	0.36	1.6	μs
Storage Time (I_C = 10 A(pk), V_{clamp} = 250 V, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc)	t_{sv}	–	0.8	–	μs
Crossover Time	t_c	–	0.18	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

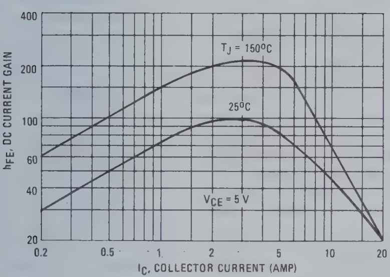


FIGURE 2 – COLLECTOR SATURATION REGION

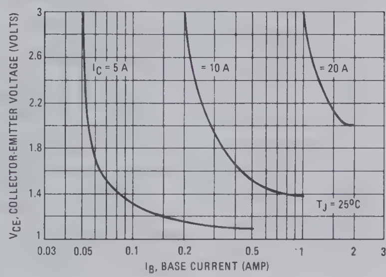


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

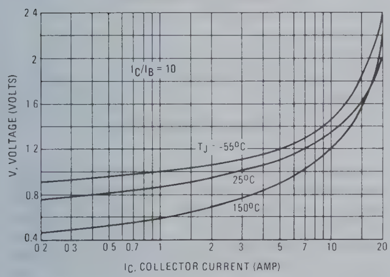


FIGURE 4 – BASE-EMITTER VOLTAGE

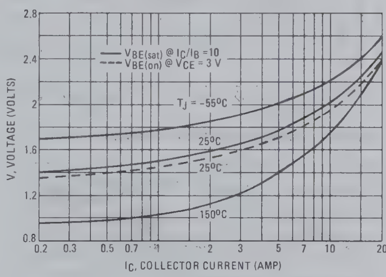


FIGURE 5 – COLLECTOR CUTOFF REGION

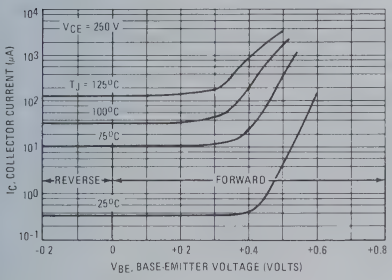
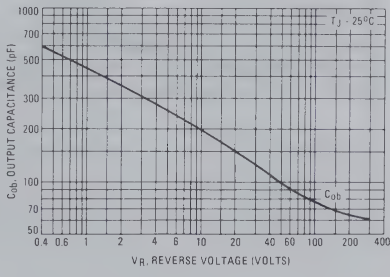
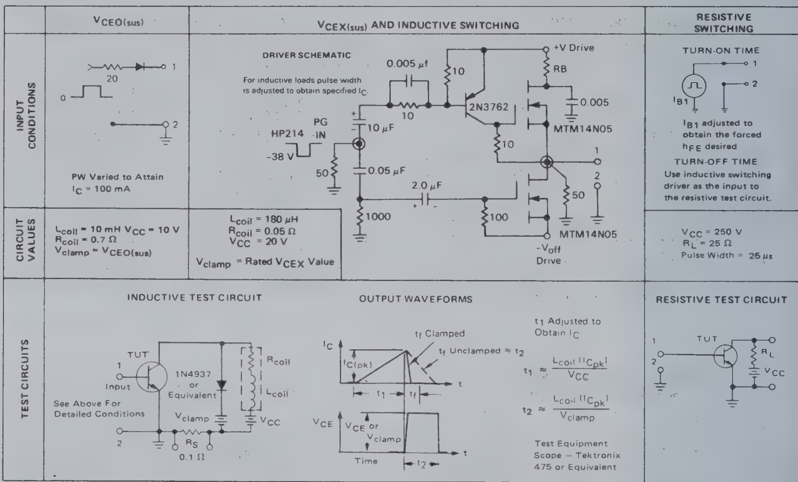


FIGURE 6 – OUTPUT CAPACITANCE



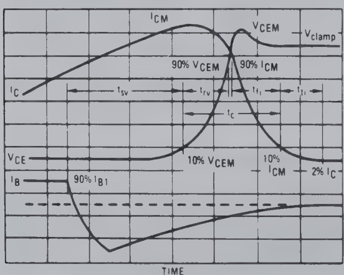
1.3

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust –V such that $V_{BE(off)}$ = 5 V except as required for RB SOA (Figure 12).

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

— continued —

TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 7. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at $T_C = 25^oC$ and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at $T_C = 100^oC$.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

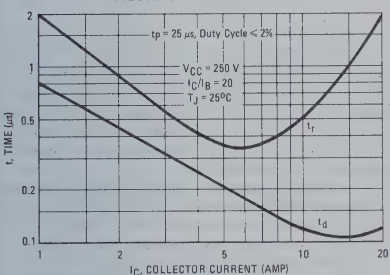


FIGURE 9 — TURN-OFF TIME

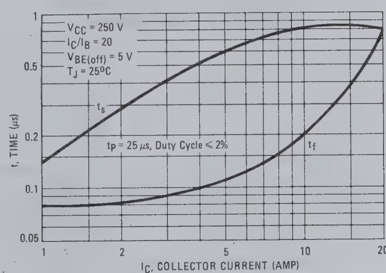
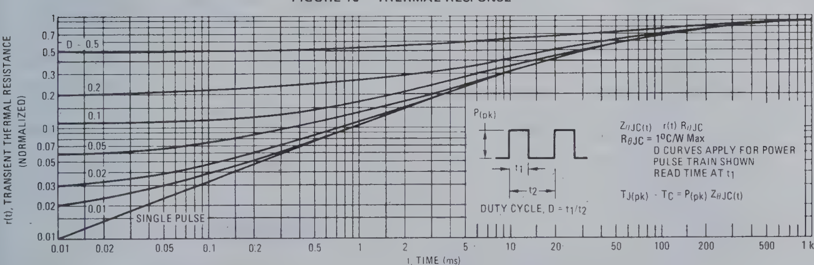


FIGURE 10 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATING AREA

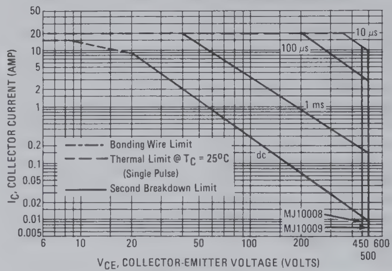
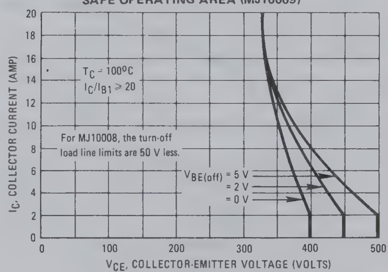


FIGURE 12 — REVERSE BIAS SWITCHING SAFE OPERATING AREA (MJ10009)



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics. See Table 1 for circuit conditions.

FIGURE 13 — POWER DERATING

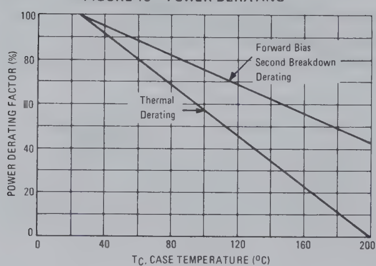
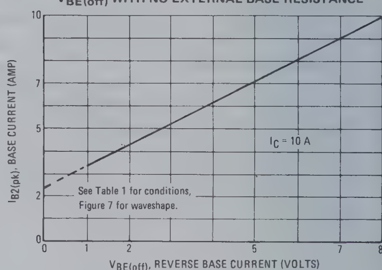


FIGURE 14 — REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE

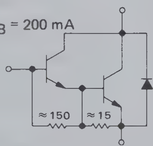


MOTOROLA

DARLINGTON HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in deflection circuits.

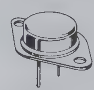
- $V_{CE(sat)}$ = 3.0 Volts (Max) @ I_C = 4.0 Amps, I_B = 200 mA
- Built-In Damper Diode
- V_{CEX} = 1400 Volts
- Glassivated Base-Collector Junction
- Safe Operating Area @ 50 μs = 25 A, 200 V



8.0 AMPERE

NPN SILICON DARLINGTON POWER TRANSISTOR

1400 VOLTS
80 WATTS



MAXIMUM RATINGS

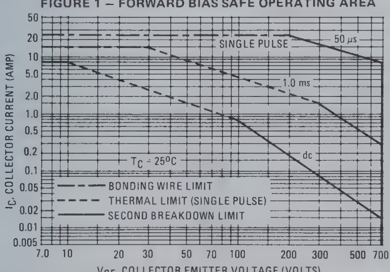
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEX}	1400	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	8.0 16	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	2.0 4.0	Adc
Emitter Current — Continuous Peak (1)	I_E I_{EM}	10 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.6	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

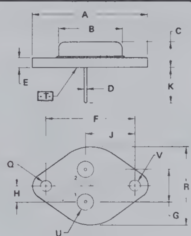
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1.8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 1.0 ms, Duty Cycle ≤ 10%.

FIGURE 1 — FORWARD BIAS SAFE OPERATING AREA





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

| ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ |

FOR LEADS:

| ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

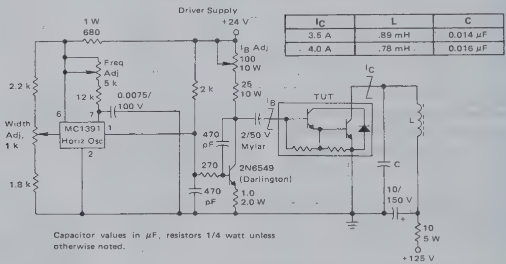
CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	700	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1400 Vdc, V_{BE} = 0)	I_{CES}	–	–	0.25	mAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	–	50	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 3.5 Adc, I_B = 0.15 Adc)		–	–	3.0	
(I_C = 4.0 Adc, I_B = 0.2 Adc)		–	–	3.0	
Base Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 3.5 Adc, I_B = 0.15 Adc)		–	–	2.0	
(I_C = 4.0 Adc, I_B = 0.2 Adc)		–	–	2.0	
Forward Diode Voltage (I_F = 4.0 Adc)	V_f	–	1.2	2.0	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 1			
SWITCHING CHARACTERISTICS					
Fall Time (See Figure 2) (I_C = 4.0 Adc, I_{B1} = 0.2 Adc)	t_f	–	0.65	1.0	μs

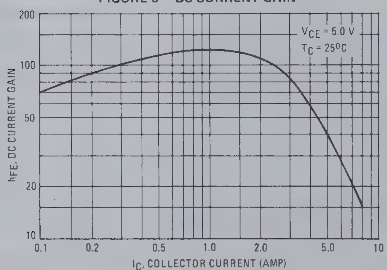
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 2 — FALL TIME TEST CIRCUIT



Capacitor values in μF, resistors 1/4 watt unless otherwise noted.

FIGURE 3 — DC CURRENT GAIN

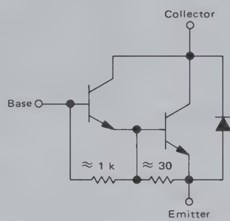


MOTOROLA

NPN SILICON POWER DARLINGTON TRANSISTOR

The MJ10012 is a high-voltage, high-current darlington transistor designed for automotive ignition, switching regulator and motor control applications.

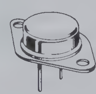
- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 400 Vdc (Min)
- 175 Watts Capability at 50 Volts
- Automotive Functional Tests



10 AMPERE

POWER TRANSISTOR DARLINGTON NPN SILICON

400 VOLTS
175 WATTS



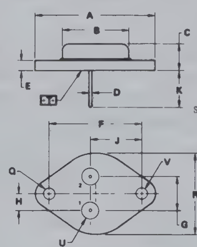
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage (R_{BE} = 27 Ω)	V_{CER}	550	Vdc
Collector-Base Voltage	V_{CBO}	600	Vdc
Emitter-Base Voltage	V_{EBO}	8.0	Vdc
Collector Current — Continuous — Peak (1)	I_C	10 15	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%..



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. $\boxed{\text{-T-}}$ IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

⌖	∅.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	∅.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

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D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
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J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67	–	1.050
U	4.83	5 33	0.190	0.210
V	3 81	4 19	0.150	0.165

CASE 1-05
TO-204AA

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Figure 1) (I_C = 200 mAdc, I_B = 0, V_{clamp} = Rated V_{CEO})	$V_{CEO(sus)}$	400	–	–	Vdc
Collector-Emitter Sustaining Voltage (Figure 1) (I_C = 200 mAdc, R_{BE} = 27 Ohms, V_{clamp} = Rated V_{CER})	$V_{CER(sus)}$	425	–	–	Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 27 Ohms)	I_{CER}	–	–	1.0	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	–	40	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 6.0 Vdc) (I_C = 6.0 Adc, V_{CE} = 6.0 Vdc) (I_C = 10 Adc, V_{CE} = 6.0 Vdc)	h_{FE}	 300 100 20	 550 350 150	 – 2000 –	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 6.0 Adc, I_B = 0.6 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	 – – –	 – – –	 1.5 2.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 0.6 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	 – –	 – –	 2.5 3.0	Vdc
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 6.0 Vdc)	$V_{BE(on)}$	–	–	2.8	Vdc
Diode Forward Voltage (I_F = 10 Adc)	V_f	–	2.0	3.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	–	165	350	pF
SWITCHING CHARACTERISTICS					
Storage Time (V_{CC} = 12 Vdc, I_C = 6.0 Adc, I_{B1} = I_{B2} = 0.3 Adc) Figure 2	t_s	–	7.5	15	μs
Fall Time (V_{CC} = 12 Vdc, I_C = 6.0 Adc, I_{B1} = I_{B2} = 0.3 Adc) Figure 2	t_f	–	5.2	15	μs
FUNCTIONAL TESTS					
Second Breakdown Collector Current with Base-Forward Biased	$I_{S/B}$	See Figure 10			–
Pulsed Energy Test (See Figure 12)	$\frac{I_C^2 L}{2}$	–	–	180	mJ

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – SUSTAINING VOLTAGE TEST CIRCUIT

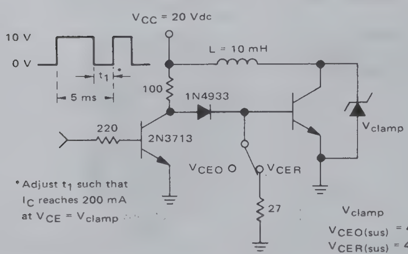


FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

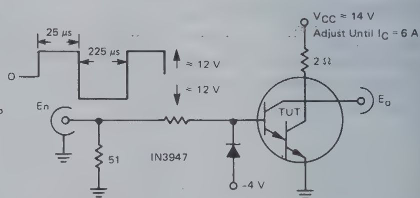


FIGURE 3 — DC CURRENT GAIN

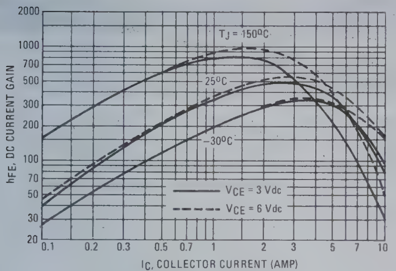


FIGURE 4 — COLLECTOR-SATURATION REGION

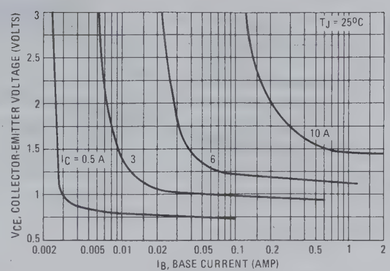


FIGURE 5 — COLLECTOR-EMITTER SATURATION VOLTAGE

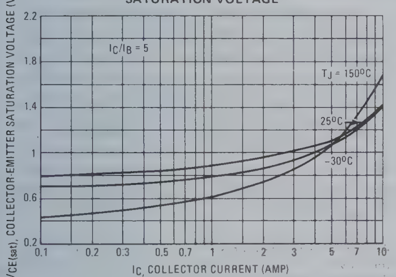


FIGURE 6 — BASE-EMITTER VOLTAGE

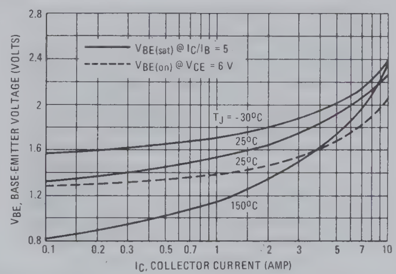


FIGURE 7 — TURN-OFF SWITCHING TIME

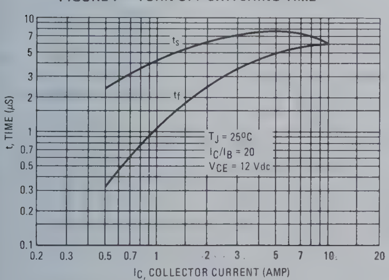


FIGURE 8 — COLLECTOR CUTOFF REGION

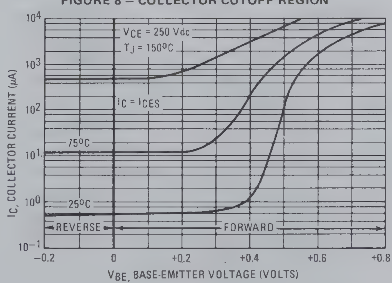


FIGURE 9 — THERMAL RESPONSE

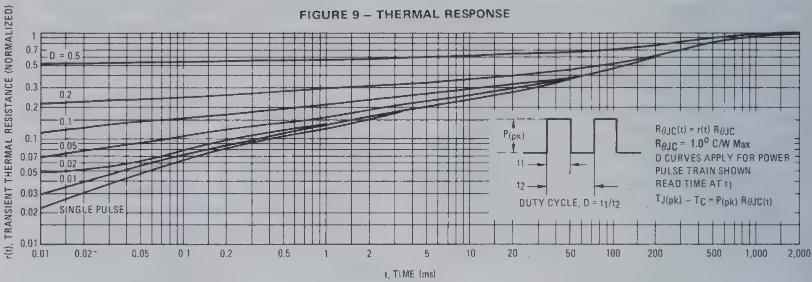
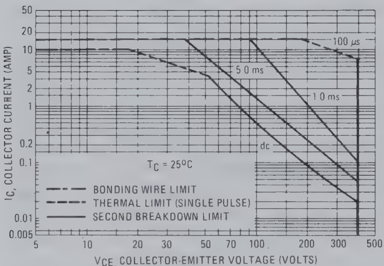


FIGURE 10 — FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 — POWER DERATING

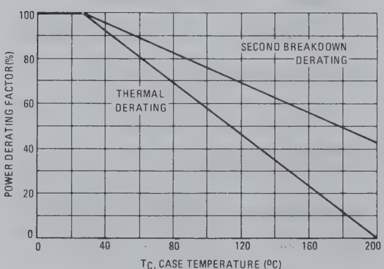
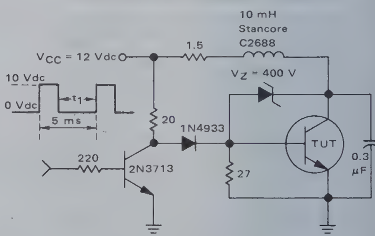


FIGURE 12 — USAGE TEST CIRCUIT



t_1 to be selected such that I_C reaches 6 Adc before switch-off.

NOTE:

"Usage Test," Figure 12 specifies energy handling capabilities in an automotive ignition circuit.

MOTOROLA

MJ10013
MJ10014

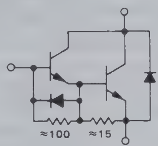
1.3

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10013 and MJ10014 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



- Fast Turn-Off Times
  - 250 ns Inductive FAll Time—25°C (Typ)
  - 500 ns Inductive Crossover Time—25°C (Typ)
  - 1.4 μs Inductive Storage Time—25°C (Typ)
- Operating Temperature Range: −65 to +200°C
- 100°C Performance Specified for:
  - Reversed Biased SOA With Inductive Loads
  - Switching Times With Inductive Loads
  - Saturation Voltages
  - Leakage Currents

10 AMPERE

NPN SILICON

POWER DARLINGTON TRANSISTORS

550 AND 600 VOLTS
175 WATTS

Designers Data for "Worst-Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristic boundaries—are given to facilitate "worst-case" design.

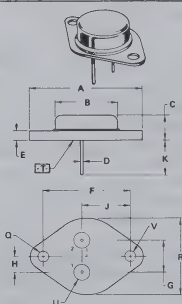
MAXIMUM RATINGS

Rating	Symbol	MJ10013	MJ10014	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	550	600	Vdc
Collector-Emitter Voltage	V_{CEV}	650	700	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 15		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	7 10		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%



NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. -T- IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

| ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ |

FOR LEADS.

| ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5 46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3 81	4 19	0.150	0.165
R	–	26 67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJ10013 MJ10014	$V_{CEO(sus)}$	550 600	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	– –	– –	0.3 5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)		I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (2)						
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc) (I_C = 10 Adc, V_{CE} = 5 Vdc)		h_{FE}	20 10	– –	500 250	–
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)		$V_{CE(sat)}$	– –	– –	2.5 2.6	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)		$V_{BE(sat)}$	– –	– –	3 3	Vdc
Diode Forward Voltage (1) (I_F = 10 Adc)		V_f	–	3	5	Vdc
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		$\|h_{fe}\|$	10	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	100	–	350	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%).	t_d	–	0.02	0.2	μs
Rise Time		t_r	–	0.9	2	μs
Storage Time		t_s	–	0.95	4	μs
Fall Time		t_f	–	0.22	1	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_s	–	2.3	6	μs
Crossover Time		t_c	–	1	3	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_s	–	1.4	–	μs
Crossover Time		t_c	–	0.5	–	μs
Fall Time		t_{fi}	–	0.25	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.
(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

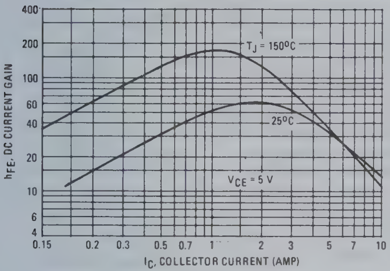


FIGURE 2 — COLLECTOR SATURATION REGION

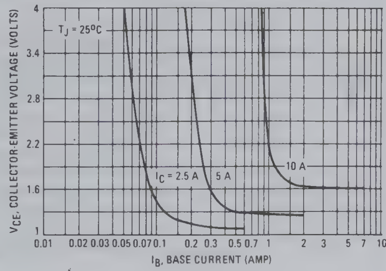


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

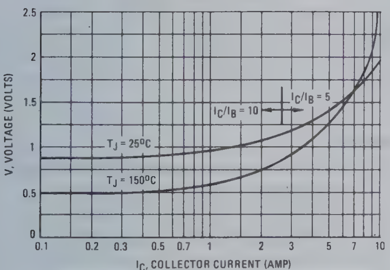


FIGURE 4 — BASE-EMITTER VOLTAGE

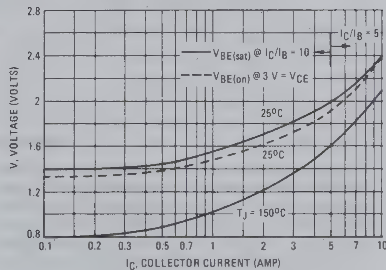


FIGURE 5 — COLLECTOR CUTOFF REGION

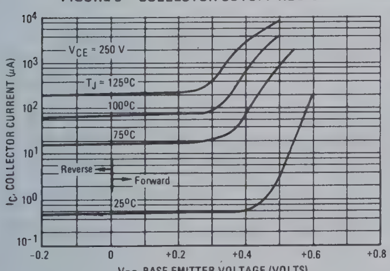
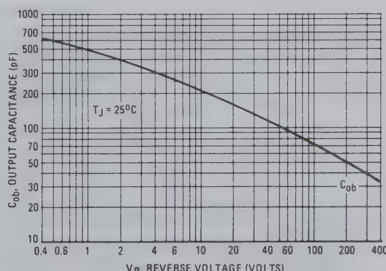
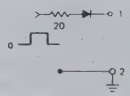
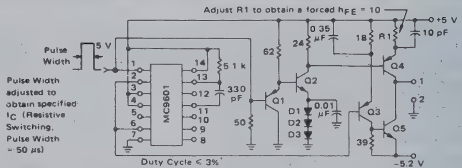
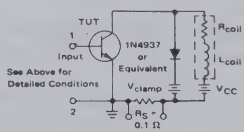
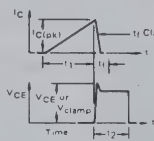
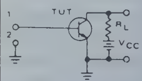


FIGURE 6 — OUTPUT CAPACITANCE



1.3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA		Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

SWITCHING TIME NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

— continued —

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

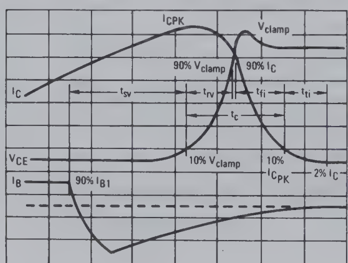
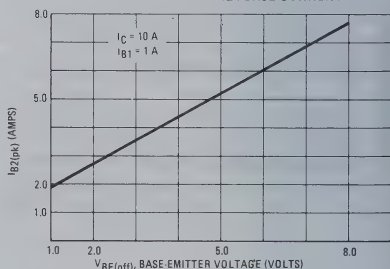


FIGURE 8 — PEAK REVERSE CURRENT



TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON TIME

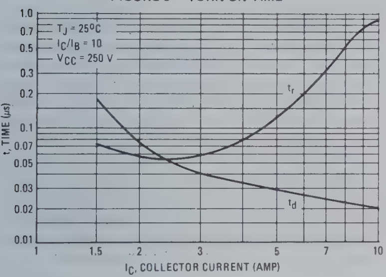


FIGURE 10 – TURN-OFF TIME

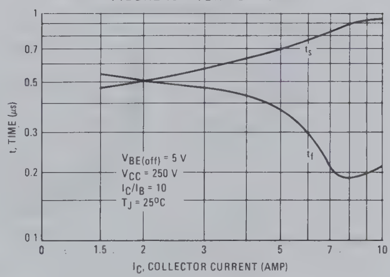
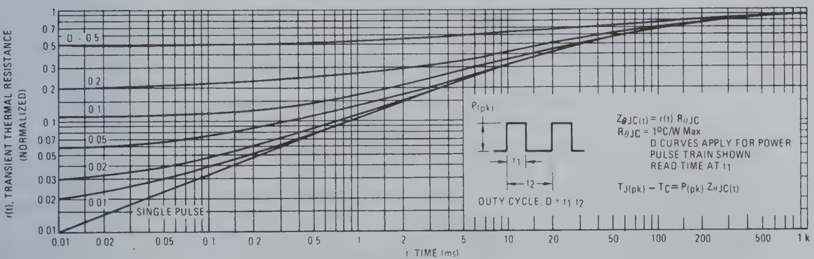


FIGURE 11 – THERMAL RESPONSE



1.3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for theses devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

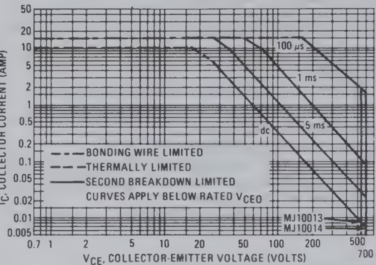
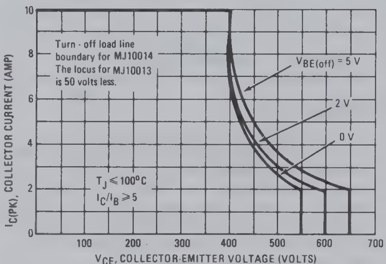


FIGURE 13 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

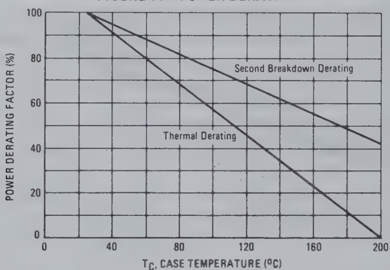
The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 — POWER DERATING



MJ10015
MJ10016

MOTOROLA

1.3

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

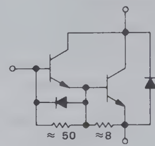
The MJ10015 and MJ10016 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

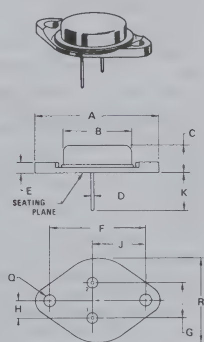
- Switching Regulators
- Motor Controls
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  1.0 μs (max) Inductive Crossover Time — 20 Amps
  2.5 μs (max) Inductive Storage Time — 20 Amps
- Operating Temperature Range −65 to +200°C
- Performance Specified for
  Reversed Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents

50 AMPERE

NPN SILICON
POWER DARLINGTON
TRANSISTORS

400 and 500 VOLTS
250 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO-3

MAXIMUM RATINGS

Rating	Symbol	MJ10015	MJ10016	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	500	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	50 75		Adc
Base Current — Continous — Peak (1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10015	$V_{CEO(sus)}$	400	–	–	Vdc
MJ10016		500	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	0.25	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)	I_{EBO}	–	–	350	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 7			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 8			
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				–
(I_C = 20 Adc, V_{CE} = 5.0 Vdc)		25	–	–	
(I_C = 40 Adc, V_{CE} = 5.0 Vdc)		10	–	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 20 Adc, I_B = 1.0 Adc)		–	–	2.2	
(I_C = 50 Adc, I_B = 10 Adc)		–	–	5.0	
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	–	–	2.75	Vdc
Diode Forward Voltage (2) (I_F = 20 Adc)	V_f	–	2.5	5.0	Vdc
DYNAMIC CHARACTERISTIC					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	–	–	750	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 20 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5 Vdc, t_p = 25 μs Duty Cycle ≤ 2%).	t_d	–	0.14	0.3	μs
Rise Time		t_r	–	0.3	1.0	μs
Storage Time		t_s	–	0.8	2.5	μs
Fall Time		t_f	–	0.3	1.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 20 A(pk), V_{clamp} ≈ 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc)	t_{sv}	–	1.0	2.5	μs
Crossover Time		t_c	–	0.36	1.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

(2) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

1.3

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

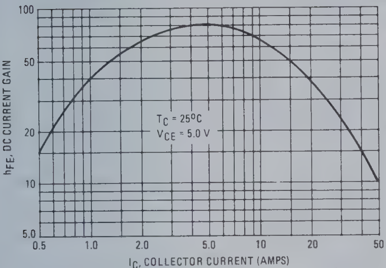


FIGURE 2 — COLLECTOR-EMITTER SATURATION VOLTAGE

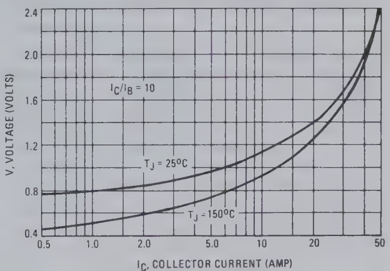


FIGURE 3 — BASE-EMITTER SATURATION VOLTAGE

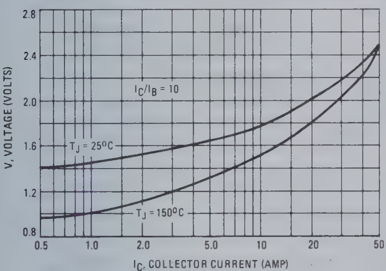


FIGURE 4 — COLLECTOR CUTOFF REGION

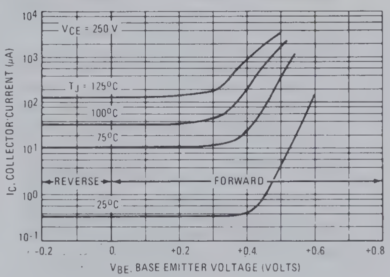
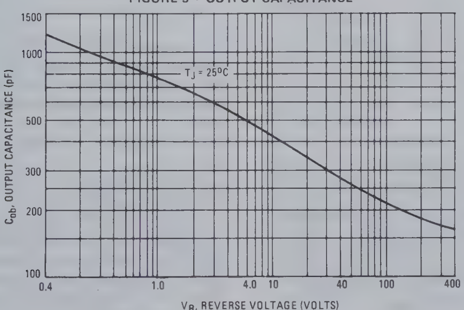
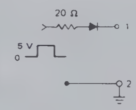
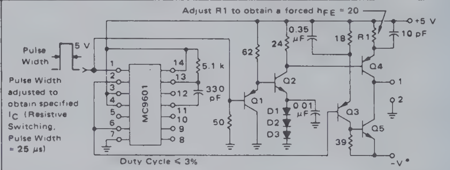
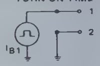
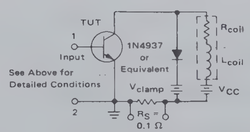
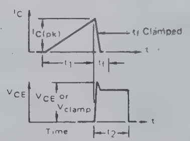
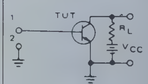


FIGURE 5 — OUTPUT CAPACITANCE



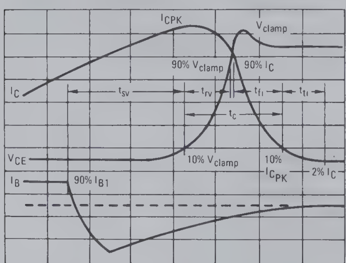
1.3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	V_{CEX} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	Adjust R1 to obtain a forced h_{FE} = 20  Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 25 μs) Duty Cycle ≤ 3%	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching circuit as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V Q1 2N2907 Q5 MJE200 Q2 2N2222 D1 1N914 Q3 2N3762 D2 1N914 Q4 MJE210 D3 1N914	V_{CC} = 250 V R_L = 12.5 Ω Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

*Adjust −V such that $V_{BE(off)}$ = 5 V except as required for RB SOA (Figure 8).

FIGURE 6 — INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed.

The Safe Operating Area figures shown in Figures 7 and 8 are specified ratings for these devices under the test conditions shown.

FIGURE 7 — FORWARD BIAS SAFE OPERATING AREA

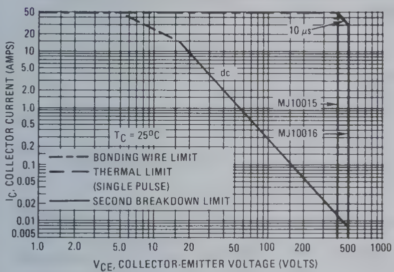
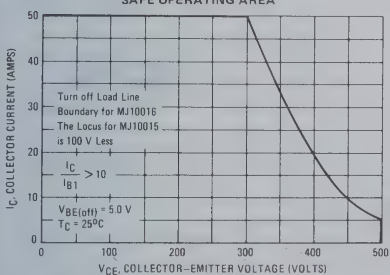


FIGURE 8 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the complete RBSOA characteristics.

FIGURE 9 — POWER DERATING

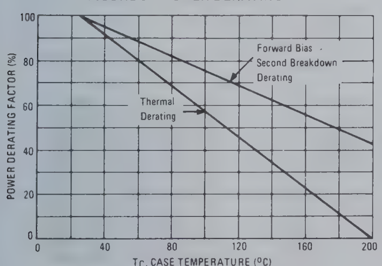
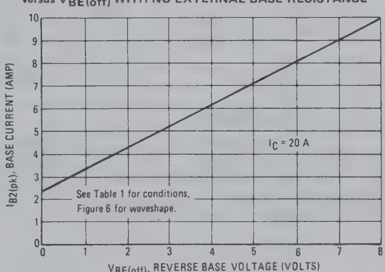


FIGURE 10 — TYPICAL REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



MJ10020
MJ10021

MOTOROLA

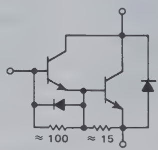
1.3

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The MJ10020 and MJ10021 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  - 150 ns Inductive Fall Time at 25°C (Typ)
  - 750 ns Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range −65 to +200°C
- 100°C Performance Specified for:
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



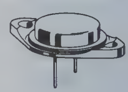
60 AMPERE

NPN SILICON POWER DARLINGTON TRANSISTORS

200 and 250 VOLTS
250 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



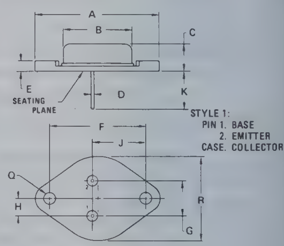
MAXIMUM RATINGS

Rating	Symbol	MJ10020	MJ10021	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	200	250	Vdc
Collector-Emitter Voltage	V_{CEV}	300	350	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	60 100		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	20 30		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) MJ10020 (I_C = 100 mA, I_B = 0) MJ10021	$V_{CEO(sus)}$	200 250	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 – –	 – –	 0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 13		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 14		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 15 Adc, V_{CE} = 5.0 V)	h_{FE}	75	–	1000	–
Collector-Emitter Saturation Voltage (I_C = 30 Adc, I_B = 1.2 Adc) (I_C = 60 Adc, I_B = 4.0 Adc) (I_C = 30 Adc, I_B = 1.2 Adc, T_C = 100°C)	$V_{CE(sat)}$	 – – –	 – – –	 2.2 4.0 2.4	Vdc
Base-Emitter Saturation Voltage (I_C = 30 Adc, I_B = 1.2 Adc) (I_C = 30 Adc, I_B = 1.2 Adc, T_C = 100°C)	$V_{BE(sat)}$	 – –	 – –	 3.0 3.5	Vdc
Diode Forward Voltage (I_F = 30 Adc)	V_f	–	2.5	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	175	–	700	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 175 Vdc, I_C = 30 A, I_{B1} = 1.2 Adc, $V_{BE(off)}$ = 5.0 V, t_p = 25 μs Duty Cycle ≤ 2.0%).	t_d	–	0.02	0.2	μs
Rise Time		t_r	–	0.30	1.0	μs
Storage Time		t_s	–	1.0	3.5	μs
Fall Time		t_f	–	0.07	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	I_{CM} = 30 A(pk), V_{CEM} = 200 V, I_{B1} = 1.2 A, $V_{BE(off)}$ = 5 V, T_C = 100°C)	t_{sv}	–	1.2	3.5	μs
Crossover Time		t_c	–	0.45	2.0	μs
Storage Time	(I_{CM} = 30 A(pk), V_{CEM} = 200 V, I_{B1} = 1.2 A, $V_{BE(off)}$ = 5 V, T_C = 25°C)	t_{sv}	–	0.75	–	μs
Crossover Time		t_c	–	0.25	–	μs
Fall Time		t_{fi}	–	0.15	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%

1.3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

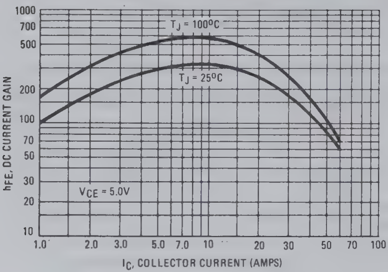


FIGURE 2 – COLLECTOR SATURATION REGION

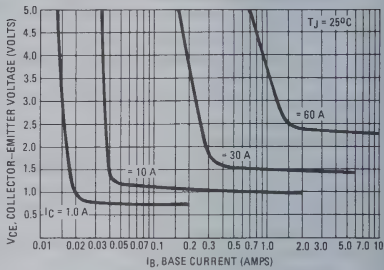


FIGURE 3 – COLLECTOR–EMITTER SATURATION VOLTAGE

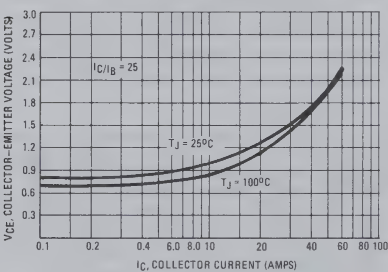


FIGURE 4 – BASE–EMITTER VOLTAGE

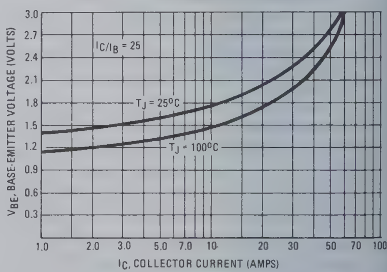


FIGURE 5 – COLLECTOR CUTOFF REGION

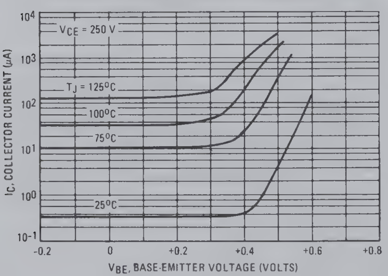
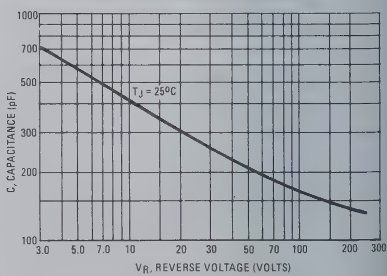
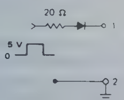
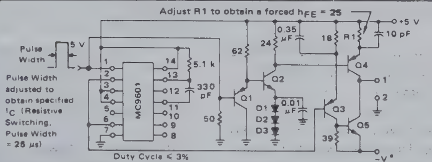
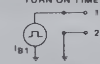
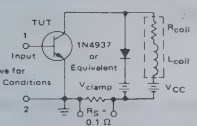
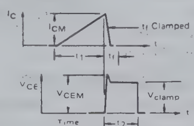
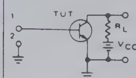


FIGURE 6 – OUTPUT CAPACITANCE



1.3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching circuit as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V Q1 2N2907 Q5 MJE15028 Q2 2N2222 D1 1N914 Q3 2N3762 D2 1N914 Q4 MJE15029 D3 1N914	V_{CC} = 175 V R_L = 5.6 Ω Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

*Adjust —V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

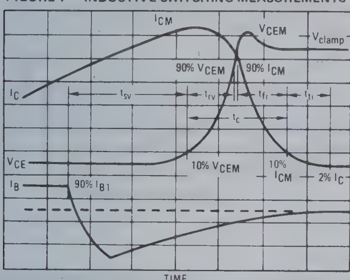


FIGURE 8 — TYPICAL PEAK REVERSE BASE CURRENT

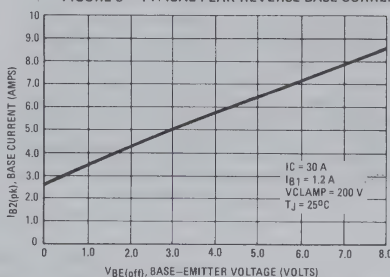
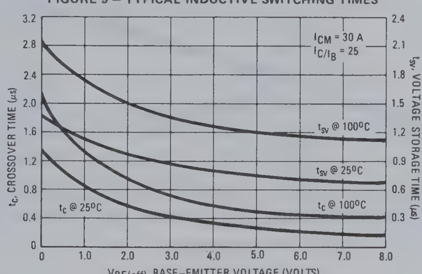


FIGURE 9 — TYPICAL INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10 – 90% V_{CEM}
t_{fi} = Current Fall Time, 90 – 10% I_{CM}
t_{ti} = Current Tail, 10 – 2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

FIGURE 10 – TYPICAL TURN-ON SWITCHING TIMES

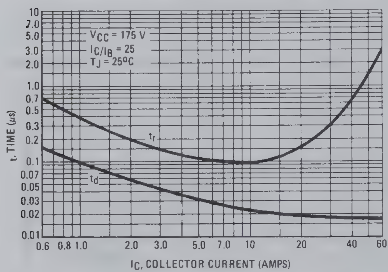


FIGURE 11 – TYPICAL TURN-OFF SWITCHING TIMES

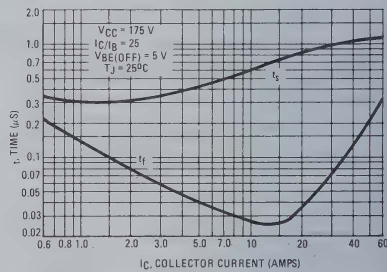
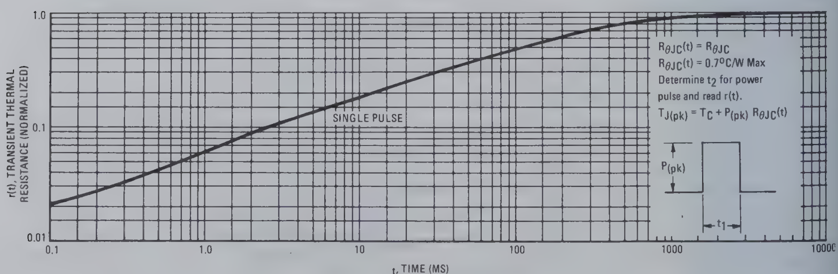


FIGURE 12 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

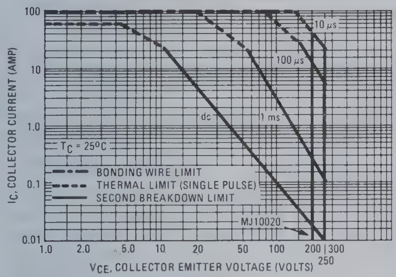
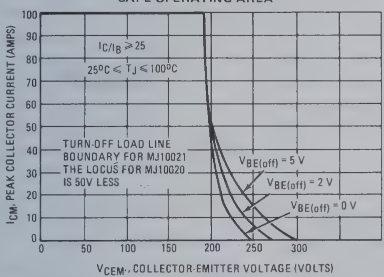


FIGURE 14 — MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

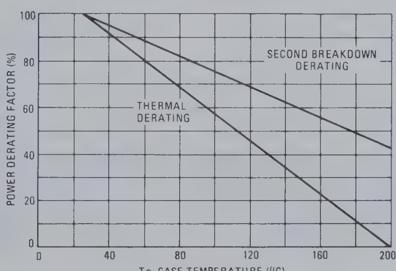
The data of Figure 13 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^o$ C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

FIGURE 15 — POWER DERATING



MJ10022
MJ10023

MOTOROLA

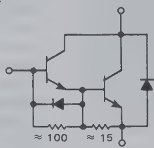
1.3

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The MJ10022 and MJ10023 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  150 ns Inductive Fall Time @ 25°C (Typ)
  300 ns Inductive Storage Time @ 25°C (Typ)
- Operating Temperature Range –65 to +200°C
- 100°C Performance Specified for:
  Reversed Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents



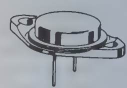
40 AMPERE

NPN SILICON POWER DARLINGTON TRANSISTORS

350 and 400 VOLTS
250 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



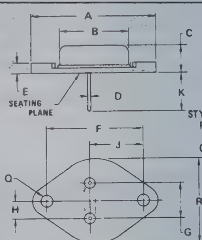
MAXIMUM RATINGS

Rating	Symbol	MJ10022	MJ10023	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	450	600	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	40 80		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	20 40		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO-3

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) MJ10022 (I_C = 100 mA, I_B = 0) MJ10023	$V_{CEO(sus)}$	350 400	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 — —	 — —	 0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 13		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 14		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 V)	h_{FE}	50	—	600	—
Collector-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc) I_C = 40 Adc, I_B = 5.0 Adc) (I_C = 20 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 2.2 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.2 Adc) (I_C = 20 Adc, I_B = 1.2 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 2.5 2.5	Vdc
Diode Forward Voltage (I_F = 20 Adc)	V_f	—	2.5	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	150	—	600	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 250 Vdc, I_C = 20 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5.0 V, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	—	0.03	0.2	μs
Rise Time	t_r	—	0.4	1.2	μs
Storage Time	t_s	—	0.9	2.5	μs
Fall Time	t_f	—	0.3	0.9	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_{CM} = 20 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 V, T_C = 100°C)	t_{sv}	—	1.9	4.4	μs
Crossover Time	t_c	—	0.6	2.0	μs
Fall Time	t_{fi}	—	0.3	—	μs
Storage Time (I_{CM} = 20 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 V, T_C = 25°C)	t_{sv}	—	1.0	—	μs
Crossover Time	t_c	—	0.3	—	μs
Fall Time	t_{fi}	—	0.15	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

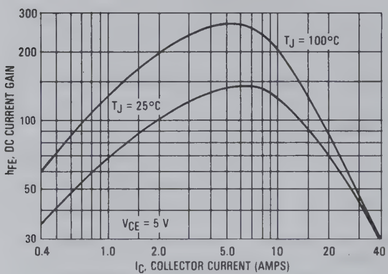


FIGURE 2 — COLLECTOR SATURATION REGION

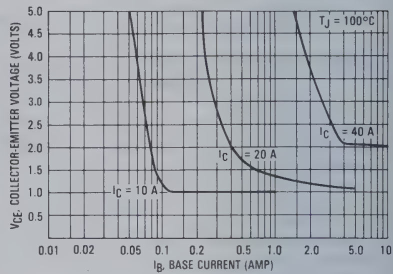


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

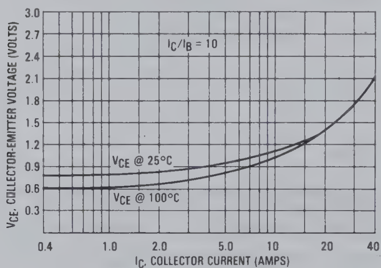


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

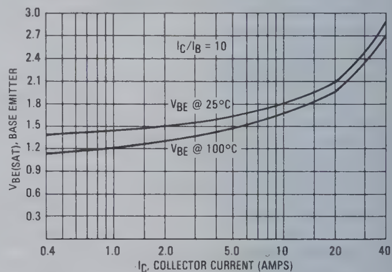


FIGURE 5 — COLLECTOR CUTOFF REGION

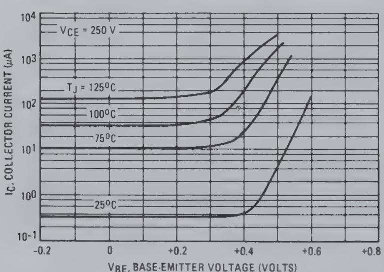
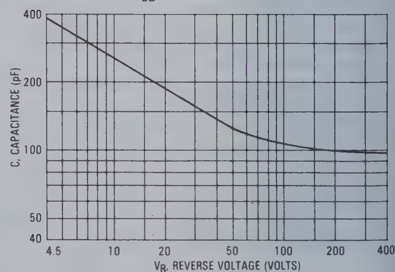


FIGURE 6 — C_{ob}, OUTPUT CAPACITANCE



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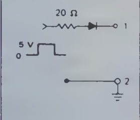
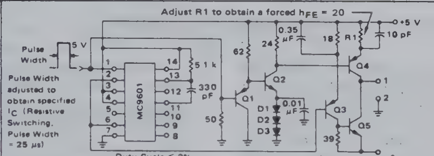
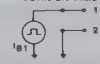
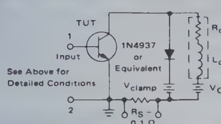
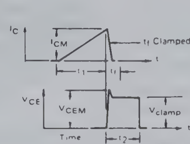
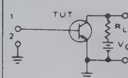
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 25 μs) Duty Cycle ≤ 3%	TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching circuit as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V Q1 2N2907 Q5 MJE15028 Q2 2N2222 D1 1N914 Q3 2N3762 D2 1N914 Q4 MJE15029 D3 1N914	V_{CC} = 250 V R_L = 12.5 Ω Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

*Adjust — V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

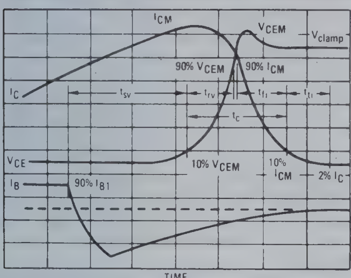


FIGURE 8 — TYPICAL PEAK REVERSE BASE CURRENT

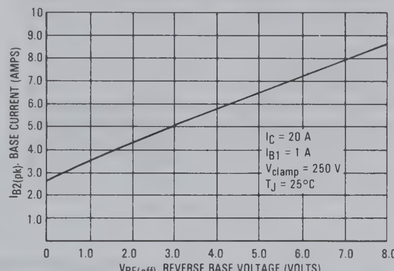
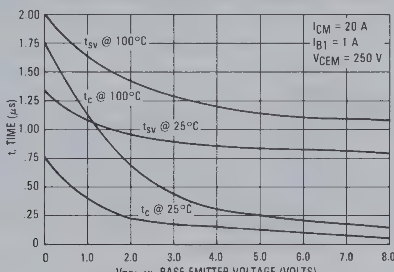


FIGURE 9 — TYPICAL INDUCTIVE SWITCHING TIMES



1.3

SWITCHING TIMES NOTE

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t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user orinented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 10 — TYPICAL TURN-ON SWITCHING TIMES

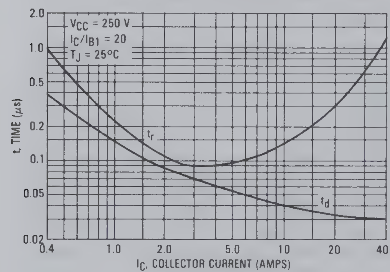


FIGURE 11 — TYPICAL TURN-OFF SWITCHING TIMES

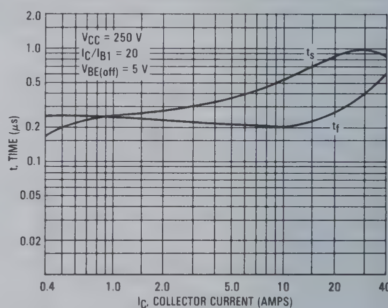
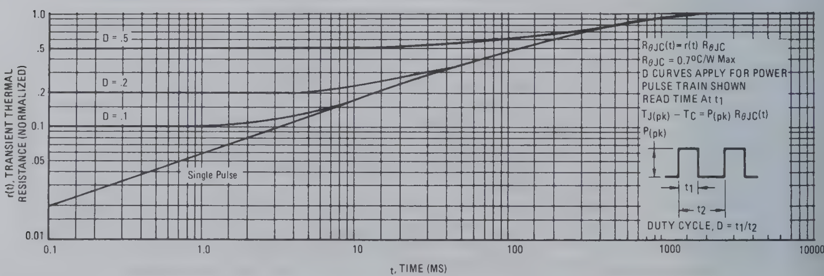


FIGURE 12 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

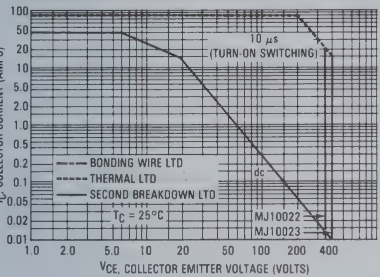
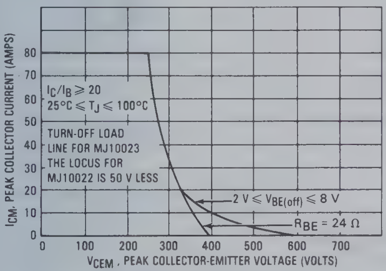


FIGURE 14 — MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

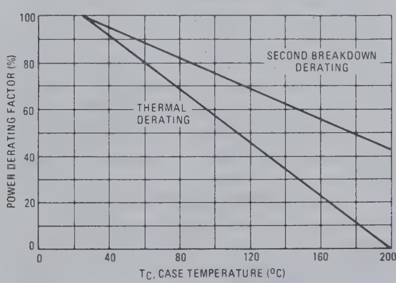
The data of Figure 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

FIGURE 15 — POWER DERATING



MJ10024
MJ10025

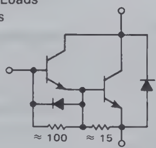
MOTOROLA

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10024 and MJ10025 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Operating Temperature Range −65 to +200°C
- 100°C Performance Specified for:
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



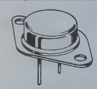
20 AMPERE

NPN SILICON POWER DARLINGTON TRANSISTORS

750 and 850 VOLTS
250 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



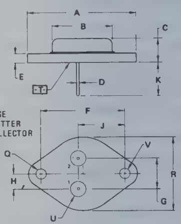
MAXIMUM RATINGS

Rating	Symbol	MJ10024	MJ10025	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	750	850	Vdc
Collector-Emitter Voltage	V_{CEV}	1000	1200	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 40		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 20		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

| ⌖ | ∅ 0.13 (0.005) Ⓜ | T | V Ⓜ |

FOR LEADS

| ⌖ | ∅ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39 37		1 550
B		21 08	–	0.830
C	6.35	7.62	0.250	0 300
D	0 97	1 09	0 038	0.043
E	1 40	1.78	0 055	0 070
F	30.15 BSC		1.187 BSC	
G	10 92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26 67	–	1.050
U	4 83	5 33	0.190	0.210
V	3 81	4 19	0.150	0.165

CASE 1-05

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) MJ10024 (I_C = 100 mA, I_B = 0) MJ10025		$V_{CEO(sus)}$	750 850	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)		I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$		See Figure 14		
Clamped Inductive SOA with base reverse biased		RBSOA		See Figure 15		
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 V)		h_{FE}	50	—	600	—
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) I_C = 20 Adc, I_B = 5.0 Adc) (I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	— — —	— — —	2.2 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{BE(sat)}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage (I_F = 10 Adc)		V_f	—	1.25	4.0	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	110	—	500	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time Rise Time Storage Time Fall Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5.0 V, t_p = 50 μs, Duty Cycle ⩽ 2.0%)	t_d t_r t_s t_f	— — — —	0.03 0.6 2.0 0.6	0.3 1.8 5.0 1.8	μs
Inductive Load, Clamped (Table 1)						
Storage Time Crossover Time	(I_{CM} = 10 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 V, T_C = 100°C)	t_{sv} t_c	— —	2.9 1.0	7.0 3.3	μs
Storage Time Crossover Time	(I_{CM} = 10 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, R_{BE} = 24 Ω, T_C = 100°C	t_{sv} t_c	— —	21 9.0	50 25	μs
Storage Time Crossover Time	(I_{CM} = 10 A, V_{CEM} = 250 V, $V_{BE(off)}$ = 5.0 V, I_{B1} Baker Clamped [1 Ampere Source], T_C = 100°C)	t_{sv} t_c	— —	2.2 0.5	— —	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ⩽ 2%

FIGURE 1 — DC CURRENT GAIN

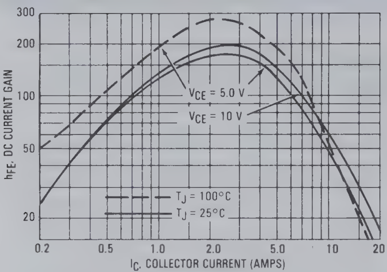


FIGURE 2 — COLLECTOR SATURATION REGION

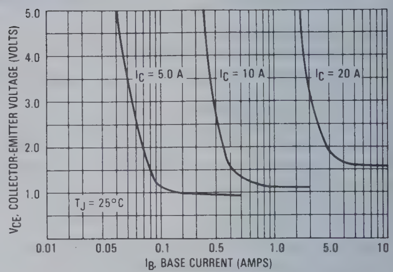


FIGURE 3 — COLLECTOR SATURATION VOLTAGE

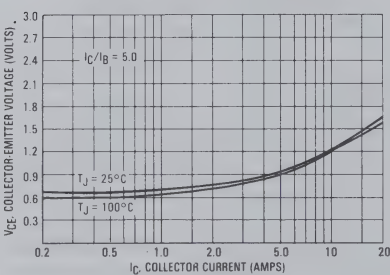


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

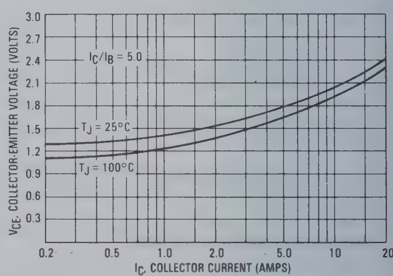


FIGURE 5 — COLLECTOR CUTOFF REGION

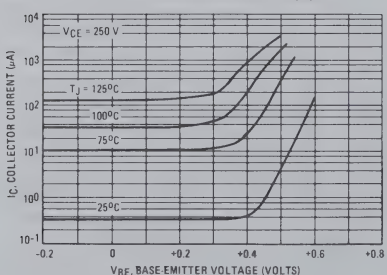


FIGURE 6 — C_{ob}, OUTPUT CAPACITANCE

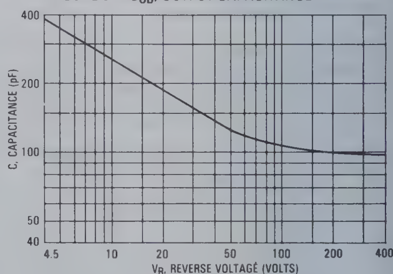
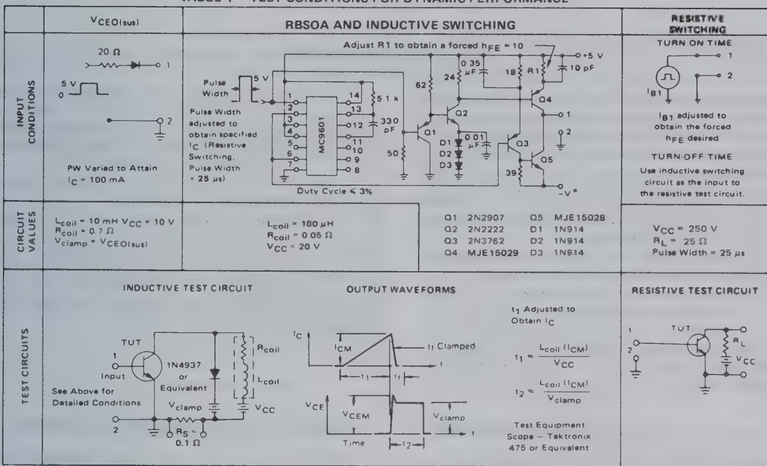


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust — V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

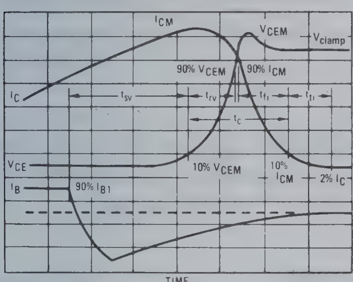


FIGURE 8 — TYPICAL PEAK REVERSE BASE CURRENT

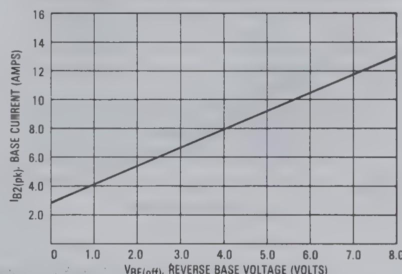


FIGURE 9 — TYPICAL INDUCTIVE SWITCHING TIMES

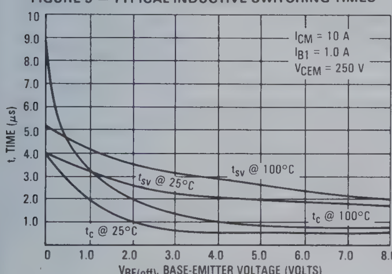
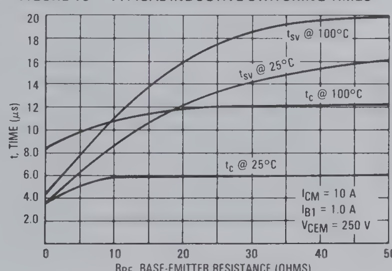


FIGURE 10 — TYPICAL INDUCTIVE SWITCHING TIMES



1.3

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user orinented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 11 — TYPICAL TURN-ON SWITCHING TIMES

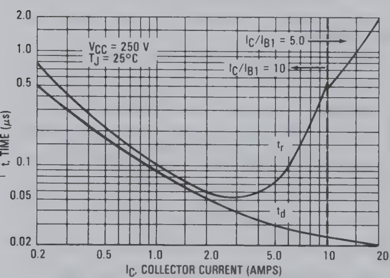


FIGURE 12 — TYPICAL TURN-OFF SWITCHING TIMES

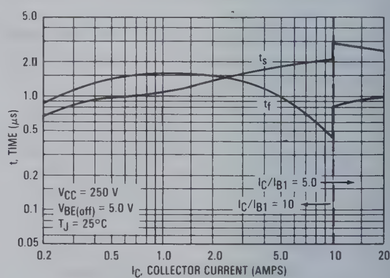
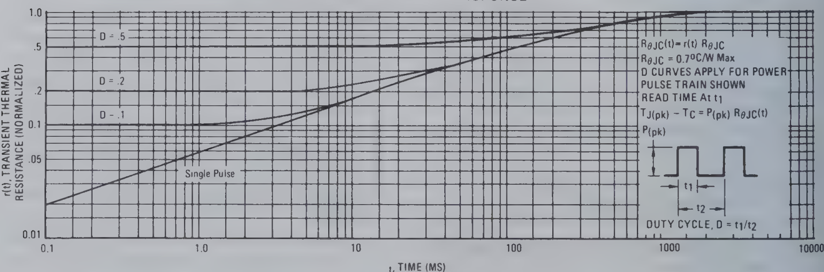


FIGURE 13 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 14 and 15 are specified for these devices under the test conditions shown.

FIGURE 14 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

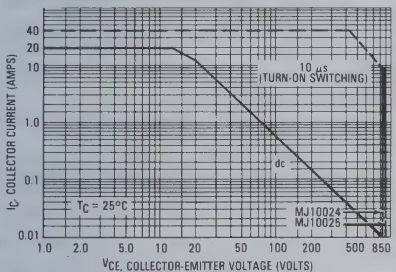
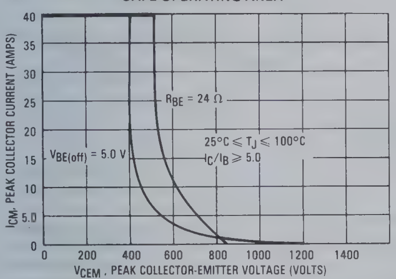


FIGURE 15 — MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

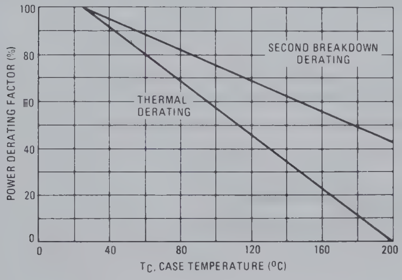
The data of Figure 14 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 14 may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

FIGURE 16 — POWER DERATING



MJ10041
MJ10044
MJ10047

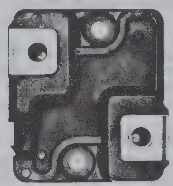
MOTOROLA

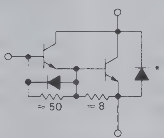
1.3

Designer's Data Sheet

25 kVA ENERGY MANAGEMENT SERIES SWITCHMODE DARLINGTON TRANSISTORS 25, 50 and 100 Ampere Operating Current

These Darlington transistors are designed for industrial service under practical operating environments requiring fast switching speed for highly efficient systems operating at high frequency such as inverters, PWM controllers and other high frequency systems operating from 120, 230 and 460 V lines.





*Emitter-Collector Diode is a fast recovery high power diode.
Note: The 8 ohm resistor is not included in the MJ10044 and MJ10047.

25, 50, and 100 AMPERE
NPN SILICON POWER DARLINGTON TRANSISTOR
250, 450 and 850 VOLTS
250 WATTS

Designer's Data for "Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst-case" design.

MAXIMUM RATINGS

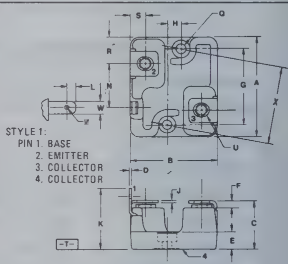
Mechanical Ratings		
Rating	**Value**	**Unit**
Mounting Torque (To heat sink with 6-32 Screw) (Note 1)	8.0	in.-lb
Lead Torque (Lead to bus with 5 mm Screw) (Note 2)	20	in.-lb
Per Unit Weight	41	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.5	°C/W

Mica Insulators available as separate items.
0.003" thick. Motorola Part Number 14CSB12387B003.

Notes:
1. A Belleville washer of 0.281" O.D., 0.138" I.D., 0.013" thick and 43 pounds flat is recommended.
2. The maximum penetration of the screw should be limited to 0.50".
3. To adapt the collector and emitter terminals to quick connect terminals, AMP 250 Series Faston tab P/N 61499-1 is suggested.
4. The mounting holes of this package are compatible with TO-204 (formerly TO-3) mounting holes.



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ Ø 0.25 (0.010) Ⓜ T A Ⓜ B Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
4. CONTROLLING DIMENSION: INCH EXCEPT FOR METRICALLY THREADED INSERTS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	39.11	40.13	1.540	1.580
B	33.93	34.95	1.336	1.376
C	–	20.32	–	0.800
D	0.68	0.83	0.027	0.033
E	8.30	8.81	0.327	0.347
F	–	4.44	–	0.175
G	29.67 BSC		1.168 BSC	
H	5.08 BSC		0.200 BSC	
J	0.93	1.09	0.037	0.043
K	—	25.40	–	1.000
L	2.92	3.30	0.115	0.130
N	17.14	17.39	0.675	0.685
Q	3.73	3.88	0.147	0.153
R	10.41	10.79	0.410	0.425
S	5.84	6.35	0.230	0.250
U	M5 .8 (METRIC THRD)			
V	1.27	1.52	0.050	0.060
W	4.69	4.85	0.185	0.191
X	30.15 BSC		1.187 BSC	

CASE 353-01

MAXIMUM RATINGS (Continued) (T_C = 25°C unless otherwise noted.)

Rating	Symbol	MJ10041	MJ10044	MJ10047	Unit
Collector-Emitter Voltage (I_B = 0)	V_{CEO}	850	450	250	Vdc
Collector-Emitter Voltage (R_{BE} = 10 Ohms)	V_{CER}	900	500	300	Vdc
Collector-Base Voltage	V_{CB}	900	500	300	Vdc
Emitter-Base Voltage	V_{EB}		8.0		Vdc
Collector Current — Operating (T_C = 115°C) (T_C = 85°C) (T_C = 85°C)	$I_{C(op)}$	25 — —	— 50 —	— — 100*	A
Collector Current — Continuous — Peak Repetitive — Peak Nonrepetitive	I_C	37.5 75 125	75 150 250	100 300 500	A
Base Current — Continuous — Peak Nonrepetitive	I_B		25 50		A
Total Device Dissipation Derate above T_C = 25°C For 1-minute overload	P_D		250 2.0 333		Watts W/°C Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}		–55 to +150 –55 to 200		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 125 mAdc) MJ10041 MJ10044 MJ10047	$V_{CEO(sus)}$	850 450 250	— — —	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	— —	2.0 10	mA
Collector Cutoff Current (V_{CE} = Rated V_{CER}, R_{BE} = 10 Ω, T_C = 100°C)	I_{CER}	—	10	mA
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0) MJ10041 MJ10044 – MJ10047	I_{EBO}	— —	500 2.5	mA
SAFE OPERATING AREA				
Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figures 32, 34 & 36		
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figures 33, 35 & 37		
Overload Safe Operating Area	OLSOA	See Figures 38, 39, 40, 41, 42 & 43		
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	2000	pF

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤ 2.0%.
*This rating is with a 50% duty cycle, and is limited by power dissipation. Higher operating currents are allowable at lower duty cycles.

1.3

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
MJ10041				
DC Current Gain	h_{FE}			
(I_C = 25 Adc, V_{CE} = 5.0 Vdc)		25	—	
(I_C = 25 Adc, V_{CE} = 10 Vdc)		40	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.0 Adc)		—	2.0	
(I_C = 37.5 Adc, I_B = 7.5 Adc)		—	5.0	
(I_C = 25 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.0 Adc)		—	3.0	
(I_C = 25 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	3.0	
MJ10044				
DC Current Gain	h_{FE}			
(I_C = 50 Adc, V_{CE} = 5.0 Vdc)		50	—	
(I_C = 50 Adc, V_{CE} = 10 Vdc)		60	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 50 Adc, I_B = 1.67 Adc)		—	2.0	
(I_C = 75 Adc, I_B = 6.0 Adc)		—	3.3	
(I_C = 50 Adc, I_B = 1.67 Adc, T_C = 100°C)		—	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 50 Adc, I_B = 1.67 Adc)		—	3.0	
(I_C = 50 Adc, I_B = 1.67 Adc, T_C = 100°C)		—	3.0	
MJ10047				
DC Current Gain	h_{FE}			
(I_C = 100 Adc, V_{CE} = 5.0 Vdc)		75	—	
(I_C = 100 Adc, V_{CE} = 10 Vdc)		90	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 100 Adc, I_B = 2.75 Adc)		—	2.0	
(I_C = 100 Adc, I_B = 2.75 Adc, T_C = 100°C)		—	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 100 Adc, I_B = 2.75 Adc)		—	3.5	
(I_C = 100 Adc, I_B = 2.75 Adc, T_C = 100°C)		—	3.5	

(1) Pulse Test: Pulse width of 300 μs, duty cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted.)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
MJ10041							
Resistive Load							
Delay Time	(V_{CC} = 300 Vdc, I_C = 25 A, I_{B1} = 2.5 A, $V_{BE(OFF)}$ = 5.0 V, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.03	0.25	μs
Rise Time			t_r	—	1.2	5.0	
Storage Time			t_s	—	3.3	10	
Fall Time			t_f	—	1.5	5.0	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 25 A, V_{CEM} = 300 V, $V_{BE(OFF)}$ = 5.0 V, I_{B1} = 2.5 A)	T_J = 100°C	t_{sv}	—	5.0	15	μs
Crossover Time			t_c	—	3.0	10	
Storage Time		T_J = 25°C	t_{sv}	—	3.5	10	
Crossover Time			t_c	—	1.5	5.0	

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted.)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
MJ10044							
Resistive Load							
Delay Time	(V_{CC} = 250 Vdc, I_C = 50 A, I_{B1} = 1.67 A, $V_{BE(OFF)}$ = 5.0 V, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.03	0.25	μs
Rise Time			t_r	—	0.9	3.0	
Storage Time			t_s	—	1.5	3.8	
Fall Time			t_f	—	0.4	1.3	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 50 A, V_{CEM} = 250 V, $V_{BE(OFF)}$ = 5.0 V, I_{B1} = 1.67 A)	T_J = 100°C	t_{sv}	—	2.5	7.5	μs
Crossover Time			t_c	—	0.8	3.0	
Storage Time		T_J = 25°C	t_{sv}	—	1.5	3.8	
Crossover Time			t_c	—	0.5	1.5	
MJ10047							
Resistive Load							
Delay Time	(V_{CC} = 150 Vdc, I_C = 100 A, I_{B1} = 2.75 A, $V_{BE(OFF)}$ = 5.0 V, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.035	0.25	μs
Rise Time			t_r	—	1.2	4.0	
Storage Time			t_s	—	1.4	4.0	
Fall Time			t_f	—	0.25	1.0	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 100 A, V_{CEM} = 150 V, $V_{BE(OFF)}$ = 5.0 V, I_{B1} = 2.75 A)	T_J = 100°C	t_{sv}	—	2.8	8.0	μs
Crossover Time			t_c	—	1.4	4.0	
Storage Time		T_J = 25°C	t_{sv}	—	2.2	6.5	
Crossover Time			t_c	—	1.0	3.0	
C-E DIODE CHARACTERISTICS							
Power Dissipation (I_B = 0)			P_D	—	—	125	W
Single Cycle Surge Current (60 Hz)			I_{FSM}	—	—	250	Apk
Forward Voltage (1)			V_F				Vdc
(I_F = 25 Adc)		MJ10041		—	2.7	5.0	
(I_F = 50 Adc)		MJ10044		—	1.7	5.0	
(I_F = 100 Adc)		MJ10047		—	2.5	5.0	
Reverse Recovery Time			t_{rr}				μs
(I_F = 25 Adc, di/dt = 25 A/μs)		MJ10041		—	0.2	1.0	
(I_F = 50 Adc, di/dt = 50 A/μs)		MJ10044		—	0.4	1.0	
(I_F = 100 Adc, di/dt = 100 A/μs)		MJ10047		—	0.4	1.0	
Reverse Recovery Current			$I_{RM(rec)}$				A
(I_F = 25 A, di/dt = 25 A/μs)		MJ10041		—	3.5	12.5	
(I_F = 50 A, di/dt = 50 A/μs)		MJ10044		—	10	25	
(I_F = 100 A, di/dt = 100 A/μs)		MJ10047		—	25	50	
Forward Turn-On Time (Compliance Voltage = 250 V)			t_{on}				μs
(I_F = 25 Adc)		MJ10041		—	0.1	1.0	
(I_F = 50 Adc)		MJ10044		—	0.1	0.5	
(I_F = 100 Adc)		MJ10047		—	0.4	1.0	

(1) Pulse Test: Pulse width of 300 μs, duty cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

MJ10041

FIGURE 1 — DC CURRENT GAIN

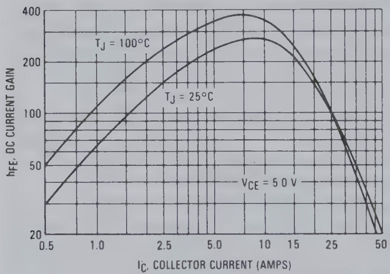
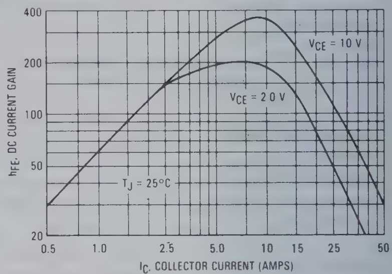


FIGURE 2 — DC CURRENT GAIN



MJ10044

FIGURE 3 — DC CURRENT GAIN

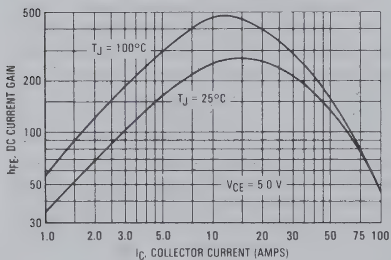
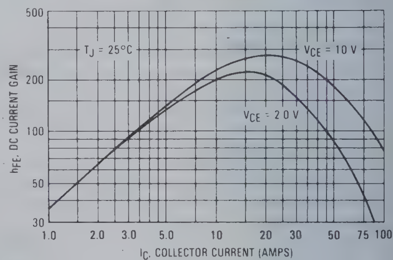


FIGURE 4 — DC CURRENT GAIN



MJ10047

FIGURE 5 — DC CURRENT GAIN

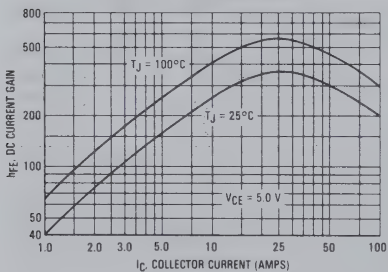
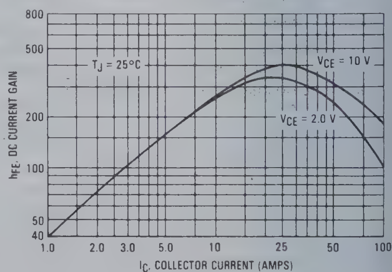


FIGURE 6 — DC CURRENT GAIN



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10041

FIGURE 7 — DC CURRENT GAIN

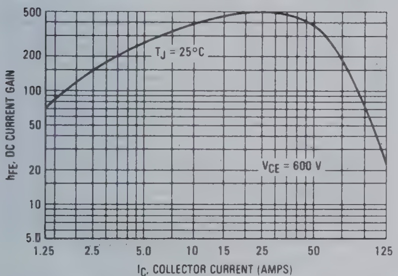
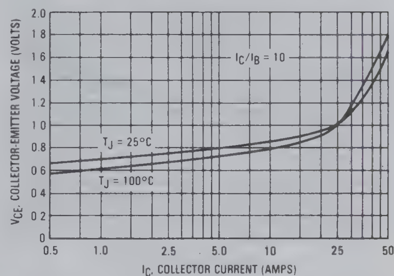


FIGURE 8 — COLLECTOR SATURATION VOLTAGE



MJ10044

FIGURE 9 — DC CURRENT GAIN

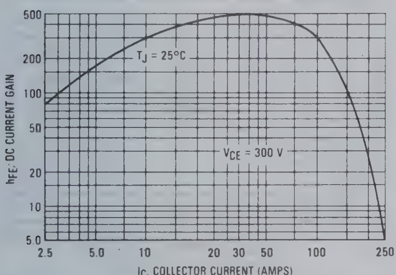
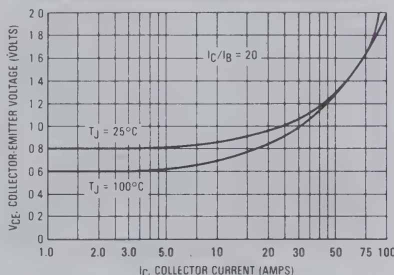


FIGURE 10 — COLLECTOR SATURATION REGION



MJ10047

FIGURE 11 — DC CURRENT GAIN

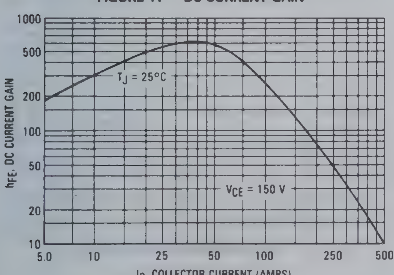
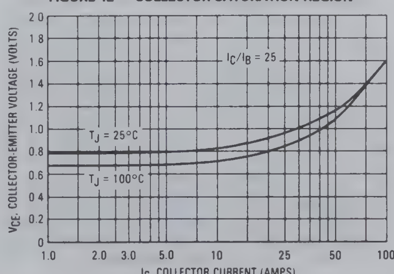


FIGURE 12 — COLLECTOR SATURATION REGION



1.3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10041

FIGURE 13 — BASE-EMITTER SATURATION VOLTAGE

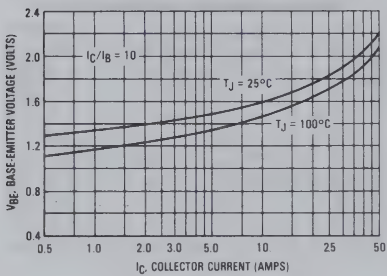
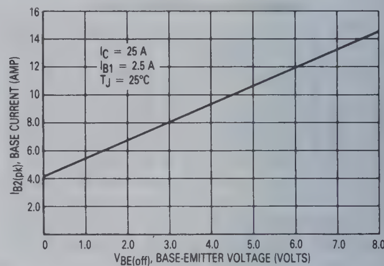


FIGURE 14 — PEAK REVERSE BASE CURRENT



MJ10044

FIGURE 15 — BASE-EMITTER SATURATION VOLTAGE

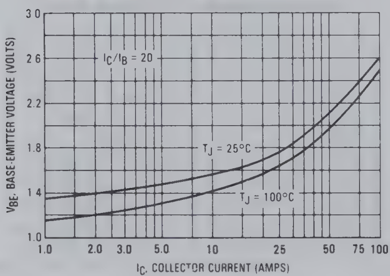
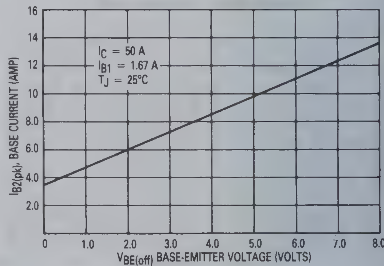


FIGURE 16 — PEAK REVERSE BASE CURRENT



MJ10047

FIGURE 17 — BASE-EMITTER SATURATION VOLTAGE

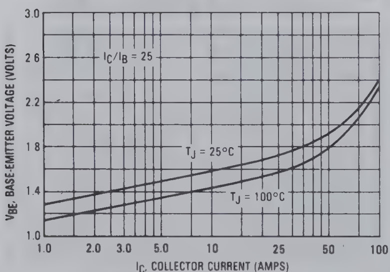
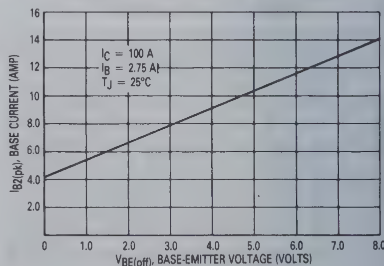


FIGURE 18 — PEAK REVERSE BASE CURRENT



1.3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10041

FIGURE 19 — TYPICAL INDUCTIVE SWITCHING TIMES

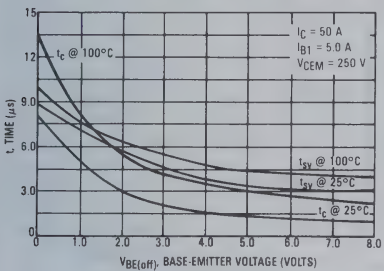
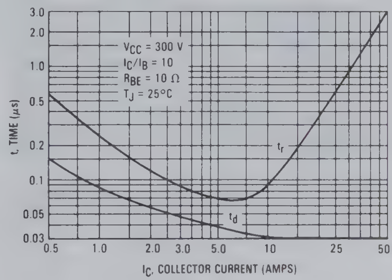


FIGURE 20 — TYPICAL TURN-ON SWITCHING TIMES



MJ10044

FIGURE 21 — TYPICAL INDUCTIVE SWITCHING TIMES

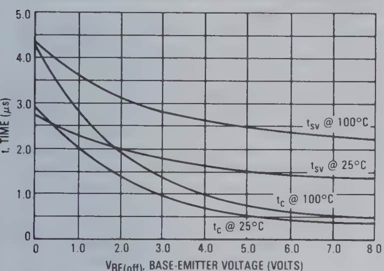
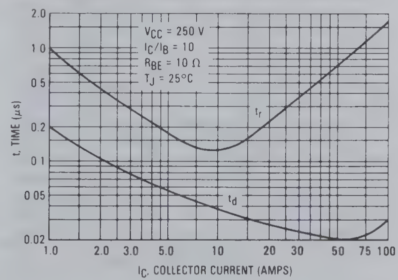


FIGURE 22 — TYPICAL TURN-ON SWITCHING TIMES



MJ10047

FIGURE 23 — TYPICAL INDUCTIVE SWITCHING TIMES

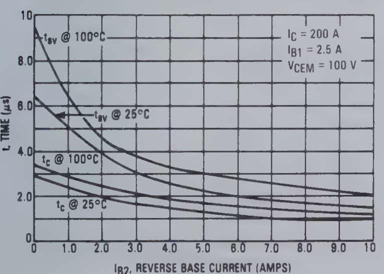
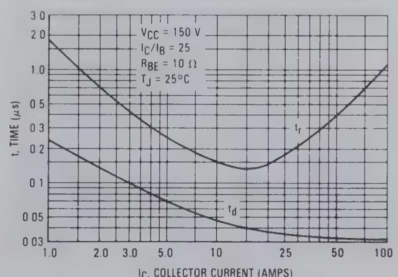


FIGURE 24 — TYPICAL TURN-ON SWITCHING TIMES



1.3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 25 — TYPICAL TURN-OFF SWITCHING TIMES MJ10041

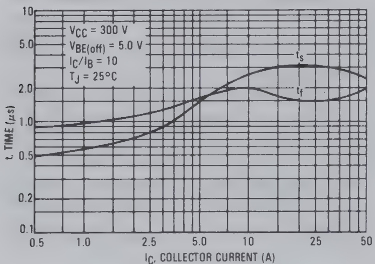


FIGURE 26 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE

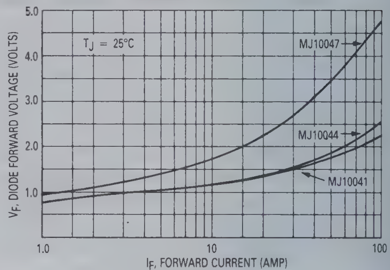


FIGURE 27 — TYPICAL TURN-OFF SWITCHING TIMES MJ10044

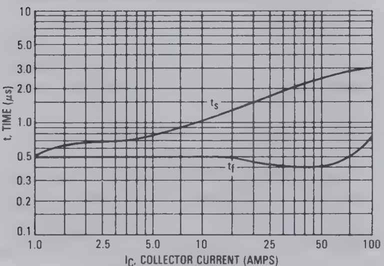


FIGURE 28 — POWER DERATING

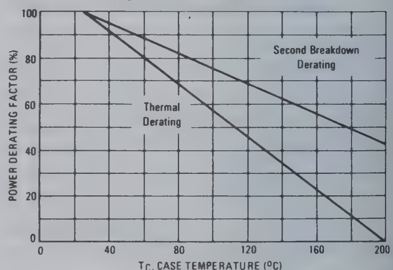


FIGURE 29 — TYPICAL TURN-OFF SWITCHING TIMES MJ10047

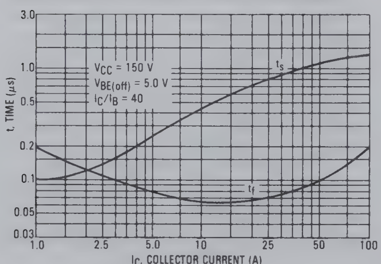
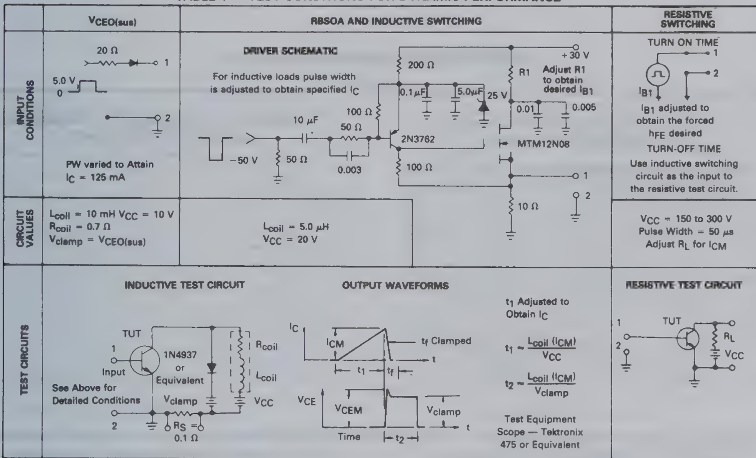


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust — V such that $V_{BE(off)} = 5.0$ V except as required for RBSOA

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
t_{fi} = Current Fall Time, 90–10% I_{CM}
t_{ti} = Current Tail, 10–2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 30 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = \tfrac{1}{2} V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 30 — INDUCTIVE SWITCHING MEASUREMENTS

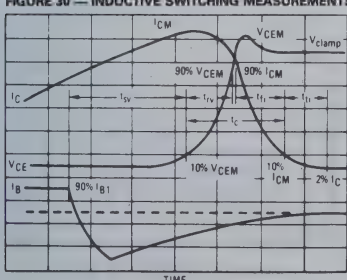
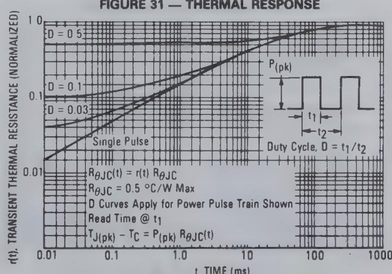


FIGURE 31 — THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

MJ10041

FIGURE 32 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

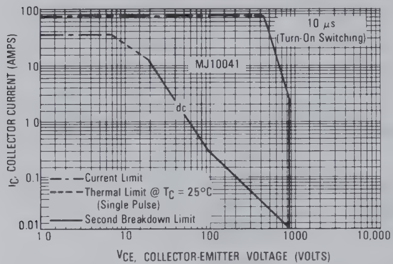
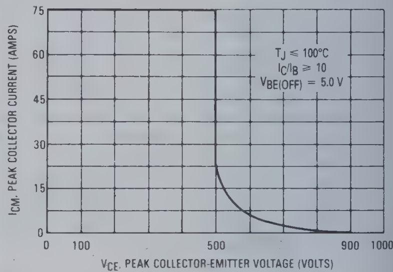


FIGURE 33 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



MJ10044

FIGURE 34 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

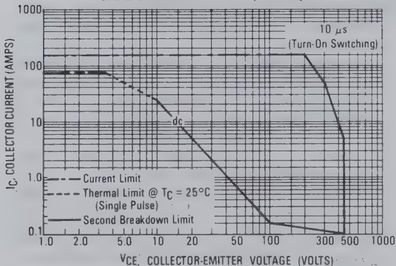
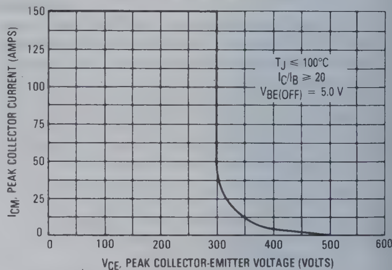


FIGURE 35 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



MJ10047

FIGURE 36 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

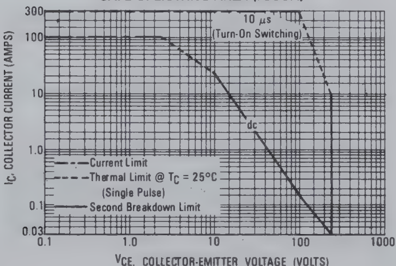
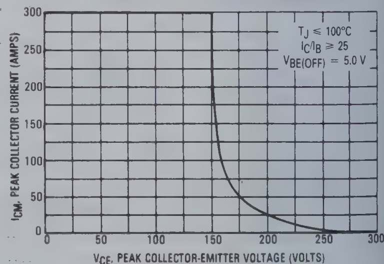


FIGURE 37 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



OVERLOAD CHARACTERISTICS

MJ10041

FIGURE 38 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

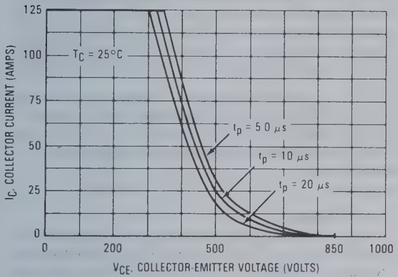
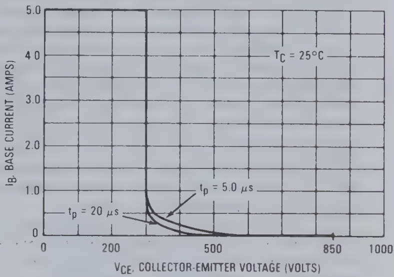


FIGURE 39 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



MJ10044

FIGURE 40 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

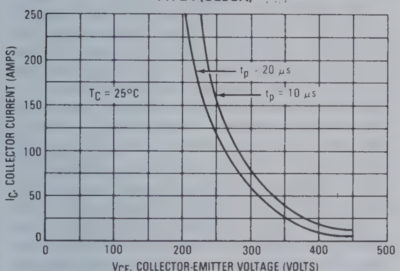
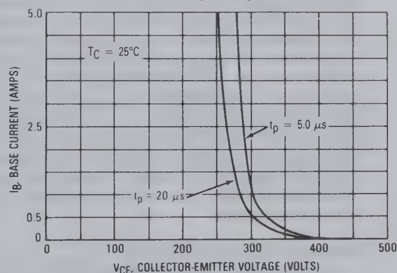


FIGURE 41 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



MJ10047

FIGURE 42 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

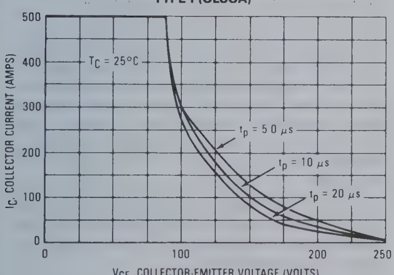
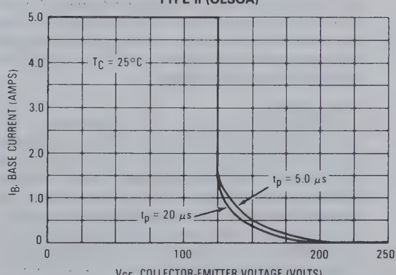


FIGURE 43 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



1.3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transitor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 32, 34, and 36 are based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on these figures may be found at any case temperature by using the appropriate curve on Figure 28.

$T_{J(pk)}$ may be calculated from the data in Figure 31. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figures 33, 35 and 37 give the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in these figures adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figures 38, 40 and 42 depict the Type I OLSOA rating for these devices. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, these figures define the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 44) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

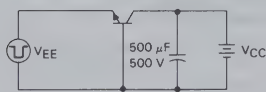
This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figures 39, 41 and 43 are measured in the circuit shown in Figure 45, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NON-REPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for these devices is 100 occurrences. Another factor is the form of turn-off bias. For these devices, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5.0$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

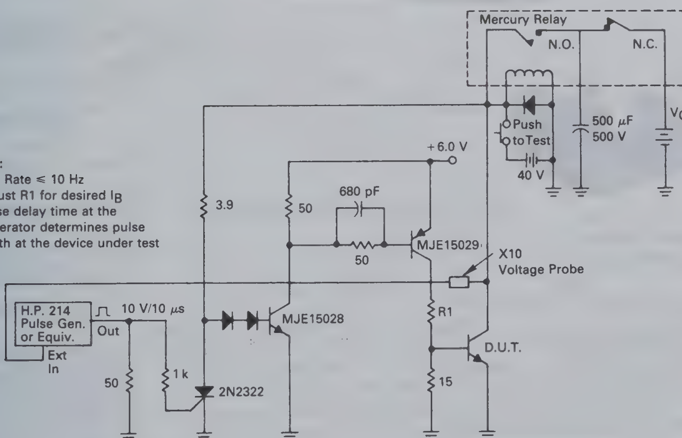
OVERLOAD SAFE OPERATING TEST CIRCUITS

FIGURE 44 — OVERLOAD SOA TEST CIRCUIT TYPE I (OLSOA)



Notes:
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

FIGURE 45 — OVERLOAD SOA TEST CIRCUIT TYPE II (OLSOA)



Notes:
- Rep Rate ≤ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test

MJ10042
MJ10045
MJ10048

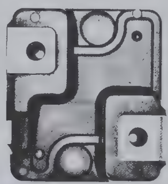
MOTOROLA

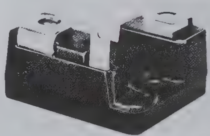
1.3

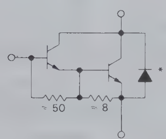
Designer's Data Sheet

25 KVA ENERGY MANAGEMENT SERIES SWITCHMODE DARLINGTON TRANSISTORS 25, 50 and 100 Ampere Operating Current

These Darlington transistors are designed for industrial service under practical operating environments found in switching high power inductive loads off 120, 230 and 460 Volt lines.





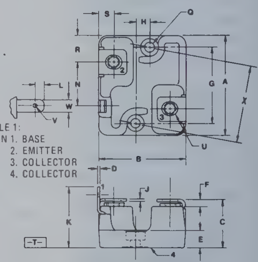


*Emitter-Collector Diode is a high power diode.

25, 50, and 100 AMPERE
NPN SILICON POWER DARLINGTON TRANSISTOR
250, 450 and 850 VOLTS
250 WATTS

Designer's Data for "Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.



STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. COLLECTOR

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
⌖ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ | B Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
4. CONTROLLING DIMENSION: INCH EXCEPT FOR METRICALLY THREADED INSERTS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.11	40.13	1.540	1.580
B	33.93	34.95	1.336	1.376
C	–	20.32	–	0.800
D	0.68	0.83	0.027	0.033
E	8.30	8.81	0.327	0.347
F	–	4.44	–	0.175
G	29.67 BSC		1.168 BSC	
H	5.08 BSC		0.200 BSC	
J	0.93	1.09	0.037	0.043
K	—	25.40	–	1.000
L	2.92	3.30	0.115	0.130
N	17.14	17.39	0.675	0.685
Q	3.73	3.88	0.147	0.153
R	10.41	10.79	0.410	0.425
S	5.84	6.35	0.230	0.250
U	M5 .8 (METRIC THRD)			
V	1.27	1.52	0.050	0.060
W	4.69	4.85	0.185	0.191
X	30.15 BSC		1.187 BSC	

CASE 353-01

MAXIMUM RATINGS

Mechanical Ratings

Rating	Value	Unit
Mounting Torque (To heat sink with 6-32 Screw) (Note 1)	8.0	in.-lb
Lead Torque (Lead to bus with 5 mm Screw) (Note 2)	20	in.-lb
Per Unit Weight	41	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.5	°C/W

Mica Insulators available as separate items.
0.003″ thick. Motorola Part Number 14CSB12387B003.

Notes:
1. A Belleville washer of 0.281″ O.D., 0.138″ I.D., 0.013″ thick and 43 pounds flat is recommended.
2. The maximum penetration of the screw should be limited to 0.50″.
3. To adapt the collector and emitter terminals to quick connect terminals, AMP 250 Series Faston tab P/N 61499-1 is suggested.
4. The mounting holes of this package are compatible with TO-204 (formerly TO-3) mounting holes.

MAXIMUM RATINGS (Continued) (T_C = 25°C unless otherwise noted.)

Rating	Symbol	MJ10042	MJ10045	MJ10048	Unit
Collector-Emitter Voltage (I_B = 0)	V_{CEO}	850	450	250	Vdc
Collector-Emitter Voltage (R_{BE} = 10 Ohms)	V_{CER}	900	500	300	Vdc
Collector-Base Voltage	V_{CB}	900	500	300	Vdc
Emitter-Base Voltage	V_{EB}		8.0		Vdc
Collector Current — Operating (T_C = 115°C) (T_C = 85°C) (T_C = 85°C)	$I_{C(op)}$	25 — —	— 50 —	— — 100*	A
Collector Current — Continuous — Peak Repetitive — Peak Nonrepetitive	I_C	37.5 75 125	75 150 250	100 300 500	A
Base Current — Continuous — Peak Nonrepetitive	I_B		25 50		A
Total Device Dissipation Derate above T_C = 25°C For 1-minute overload	P_D		250 2.0 333		Watts W/°C Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}		–55 to +150 –55 to 200		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 125 mAdc) MJ10042 MJ10045 MJ10048	$V_{CEO(sus)}$	850 450 250	— — —	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	— —	2.0 10	mA
Collector Cutoff Current (V_{CE} = Rated V_{CER}, R_{BE} = 10 Ω, T_C = 100°C)	I_{CER}	—	10	mA
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	350	mA
SAFE OPERATING AREA				
Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figures 32, 34 & 36		
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figures 33, 35 & 37		
Overload Safe Operating Area	OLSOA	See Figures 38, 39, 40, 41, 42 & 43		
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	2000	pF

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤2.0%.

* This rating is with a 50% duty cycle, and is limited by power dissipation. Higher operating currents are allowable at lower duty cycles.

1.3

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
MJ10042				
DC Current Gain	h_{FE}			
(I_C = 25 Adc, V_{CE} = 5.0 Vdc)		35	—	
(I_C = 25 Adc, V_{CE} = 10 Vdc)		40	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.0 Adc)		—	2.0	
(I_C = 37.5 Adc, I_B = 7.5 Adc)		—	5.0	
(I_C = 25 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.0 Adc)		—	3.0	
(I_C = 25 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	3.0	
MJ10045				
DC Current Gain	h_{FE}			
(I_C = 50 Adc, V_{CE} = 5.0 Vdc)		50	—	
(I_C = 50 Adc, V_{CE} = 10 Vdc)		60	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 50 Adc, I_B = 1.67 Adc)		—	2.0	
(I_C = 75 Adc, I_B = 6.0 Adc)		—	3.3	
(I_C = 50 Adc, I_B = 1.67 Adc, T_C = 100°C)		—	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 50 Adc, I_B = 1.67 Adc)		—	3.0	
(I_C = 50 Adc, I_B = 1.67 Adc, T_C = 100°C)		—	3.0	
MJ10048				
DC Current Gain	h_{FE}			
(I_C = 100 Adc, V_{CE} = 5.0 Vdc)		75	—	
(I_C = 100 Adc, V_{CE} = 10 Vdc)		90	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 100 Adc, I_B = 2.75 Adc)		—	2.0	
(I_C = 100 Adc, I_B = 2.75 Adc, T_C = 100°C)		—	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 100 Adc, I_B = 2.75 Adc)		—	3.0	
(I_C = 100 Adc, I_B = 2.75 Adc, T_C = 100°C)		—	3.0	

(1) Pulse Test: Pulse width of 300 μs, duty cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
MJ10042							
Resistive Load							
Delay Time	(V_{CC} = 300 Vdc, I_C = 25 A, I_{B1} = 2.0 A, R_{BE} = 10 Ω, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.03	0.25	μs
Rise Time			t_r	—	1.2	5.0	
Storage Time			t_s	—	35	100	
Fall Time			t_f	—	8.5	35	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 25 A, V_{CEM} = 350 V, R_{BE} = 10 Ω, I_{B1} = 2.0 A)	T_J = 100°C	t_{sv}	—	50	150	μs
Crossover Time			t_c	—	20	60	
Storage Time		T_J = 25°C	t_{sv}	—	35	100	
Crossover Time			t_c	—	10	35	
MJ10045							
Resistive Load							
Delay Time	(V_{CC} = 250 Vdc, I_C = 50 A, I_{B1} = 1.67 A, R_{BE} = 10 Ω, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.03	0.25	μs
Rise Time			t_r	—	0.9	3.0	
Storage Time			t_s	—	10	25	
Fall Time			t_f	—	3.0	10	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 50 A, V_{CEM} = 250 V, R_{BE} = 10 Ω, I_{B1} = 1.67 A)	T_J = 100°C	t_{sv}	—	15	50	μs
Crossover Time			t_c	—	4.0	15	
Storage Time		T_J = 25°C	t_{sv}	—	10	25	
Crossover Time			t_c	—	2.7	10	
MJ10048							
Resistive Load							
Delay Time	(V_{CC} = 150 Vdc, I_C = 100 A, I_{B1} = 2.75 A, R_{BE} = 10 Ω, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.035	0.25	μs
Rise Time			t_r	—	1.2	4.0	
Storage Time			t_s	—	6.3	20	
Fall Time			t_f	—	2.5	8.0	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 100 A, V_{CEM} = 150 V, R_{BE} = 10 Ω, I_{B1} = 2.75 A)	T_J = 100°C	t_{sv}	—	9.0	30	μs
Crossover Time			t_c	—	3.3	12	
Storage Time		T_J = 25°C	t_{sv}	—	6.5	20	
Crossover Time			t_c	—	2.3	8.0	
C-E DIODE CHARACTERISTICS							
Power Dissipation (I_B = 0)			P_D	—	—	125	W
Single Cycle Surge Current (60 Hz)			I_{FSM}	—	—	250	Apk
Forward Voltage (1)			V_F				Vdc
(I_F = 25 Adc)	MJ10042			—	—	1.5	
(I_F = 50 Adc)	MJ10045			—	—	1.5	
(I_F = 100 Adc)	MJ10048			—	—	2.0	
Reverse Recovery Time (d_i/d_t = 25 A/μs)			t_{rr}				μs
(I_F = 25 Adc)	MJ10042			—	4.0	12	
(I_F = 50 Adc)	MJ10045			—	3.3	10	
(I_F = 100 Adc)	MJ10048			—	2.5	8.0	
Forward Turn-On Time (Compliance Voltage = 250 V)			t_{on}				μs
(I_F = 25 Adc)	MJ10042			—	0.3	1.2	
(I_F = 50 Adc)	MJ10045			—	0.3	1.0	
(I_F = 100 Adc)	MJ10048			—	1.0	3.5	

(1) Pulse Test: Pulse width of 300 μs, duty cycle ≤2.0%.

1.3

TYPICAL ELECTRICAL CHARACTERISTICS

MJ10042

FIGURE 1 — DC CURRENT GAIN

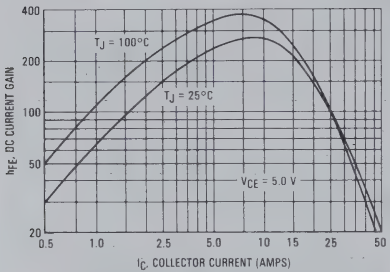
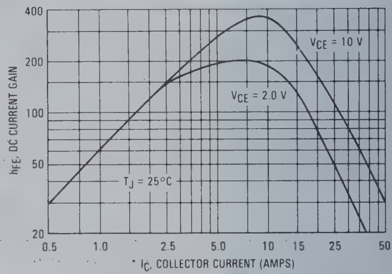


FIGURE 2 — DC CURRENT GAIN



MJ10045

FIGURE 3 — DC CURRENT GAIN

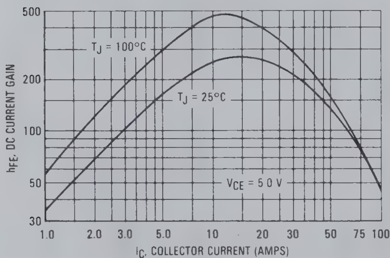
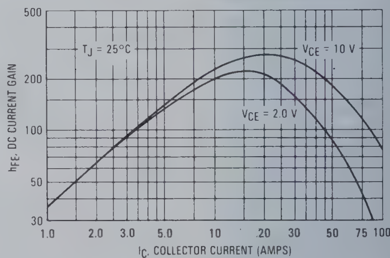


FIGURE 4 — DC CURRENT GAIN



MJ10048

FIGURE 5 — DC CURRENT GAIN

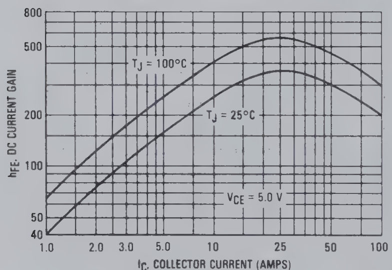
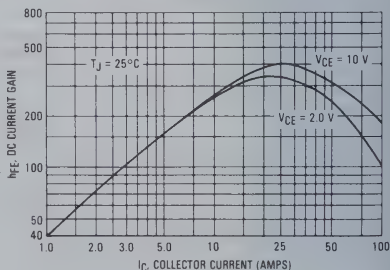


FIGURE 6 — DC CURRENT GAIN



1.3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10042

FIGURE 7 — DC CURRENT GAIN

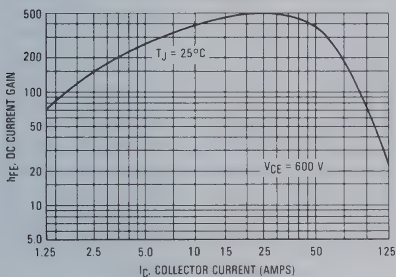


FIGURE 8 — COLLECTOR SATURATION VOLTAGE

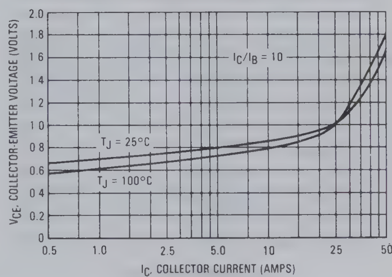


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FIGURE 9 — DC CURRENT GAIN

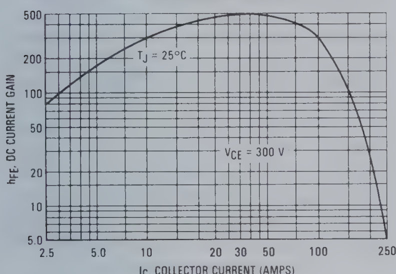

FIGURE 10 — COLLECTOR SATURATION REGION

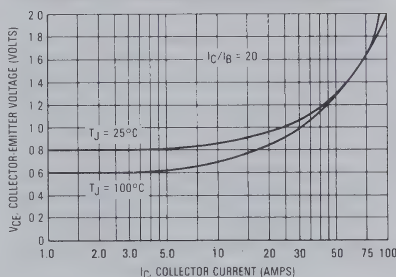

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FIGURE 11 — DC CURRENT GAIN

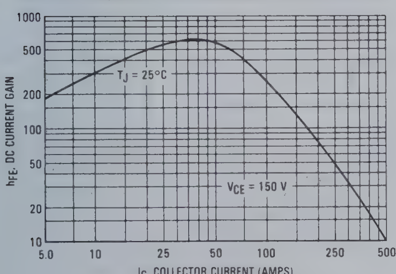
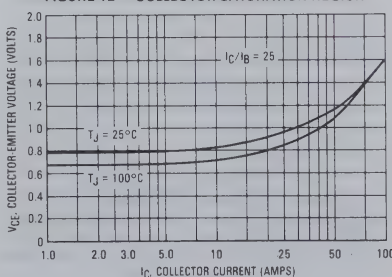


FIGURE 12 — COLLECTOR SATURATION REGION



1.3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10042

FIGURE 13 — BASE-EMITTER SATURATION VOLTAGE

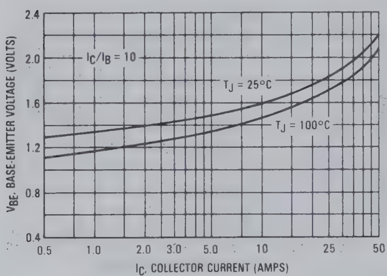


FIGURE 14 — TYPICAL PEAK REVERSE BASE CURRENT

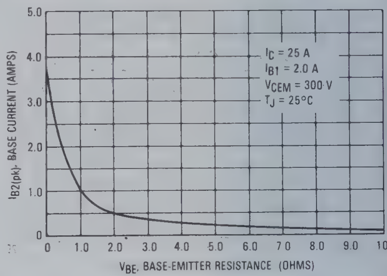


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FIGURE 15 — BASE-EMITTER SATURATION VOLTAGE

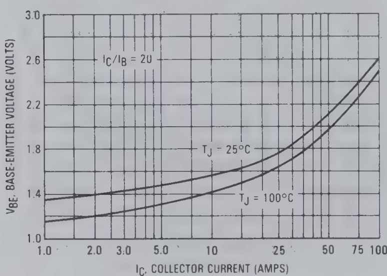

FIGURE 16 — TYPICAL PEAK REVERSE BASE CURRENT

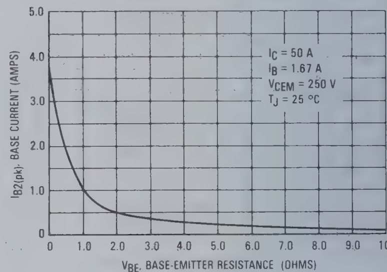

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FIGURE 17 — BASE-EMITTER SATURATION VOLTAGE

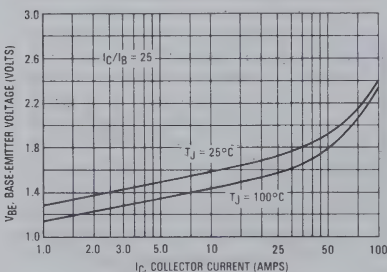
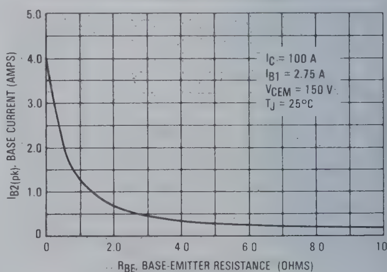


FIGURE 18 — TYPICAL PEAK REVERSE BASE CURRENT



1.3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10042

FIGURE 19 — TYPICAL INDUCTIVE SWITCHING TIMES

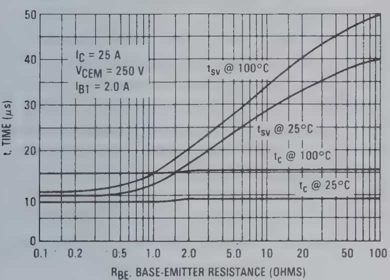
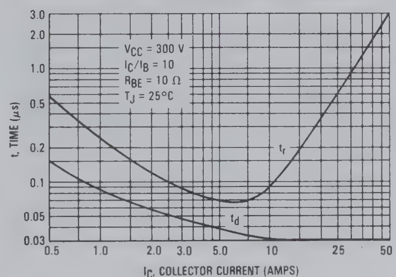


FIGURE 20 — TYPICAL TURN-ON SWITCHING TIMES



MJ10045

FIGURE 21 — TYPICAL INDUCTIVE SWITCHING TIMES

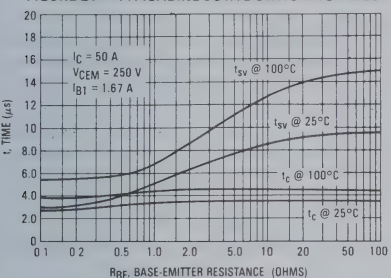


FIGURE 22 — TYPICAL TURN-ON SWITCHING TIMES

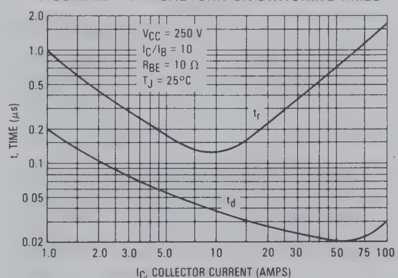


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FIGURE 23 — TYPICAL INDUCTIVE SWITCHING TIMES

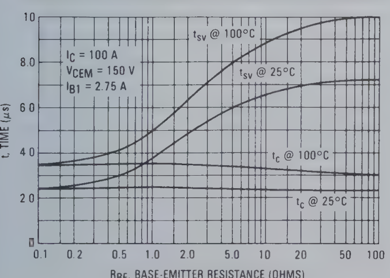
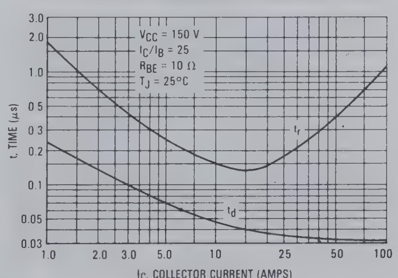


FIGURE 24 — TYPICAL TURN-ON SWITCHING TIMES



1.3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 25 — TYPICAL TURN-OFF SWITCHING TIMES MJ10042

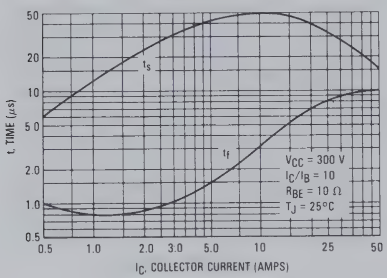


FIGURE 26 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE

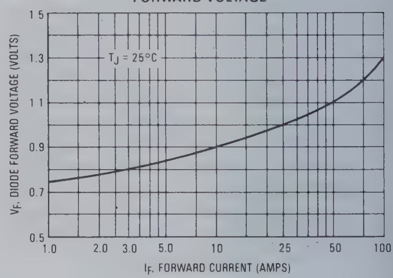


FIGURE 27 — TYPICAL TURN-OFF SWITCHING TIMES MJ10045

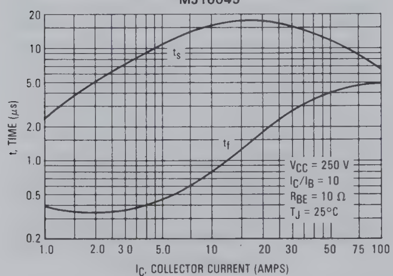


FIGURE 28 — POWER DERATING

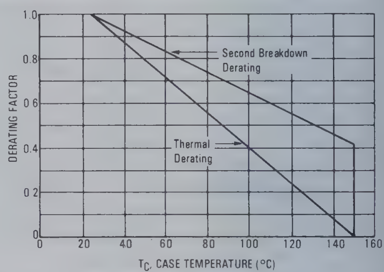


FIGURE 29 — TYPICAL TURN-OFF SWITCHING TIMES MJ10048

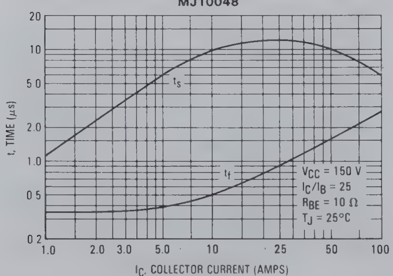
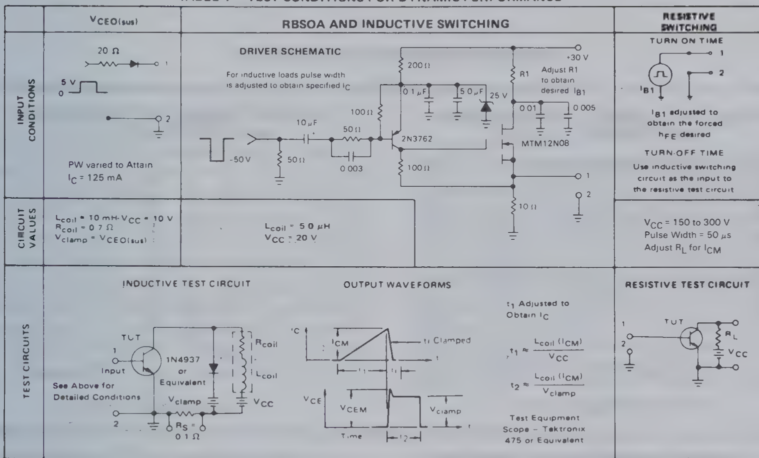


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust — V such that $V_{BE(off)}$ = 5.0 V except as required for RBSOA

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 30 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 30 — INDUCTIVE SWITCHING MEASUREMENTS

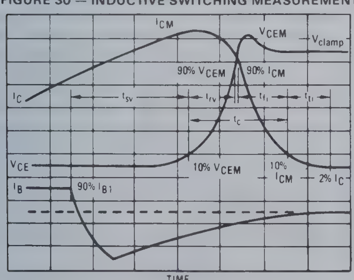
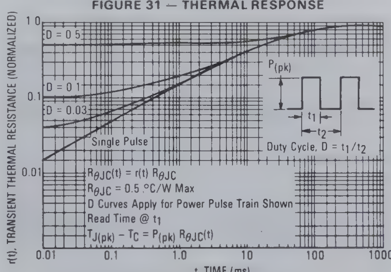


FIGURE 31 — THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

MJ10042

FIGURE 32 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

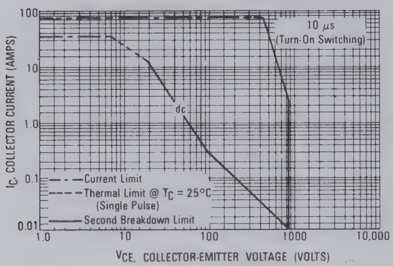


FIGURE 33 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)

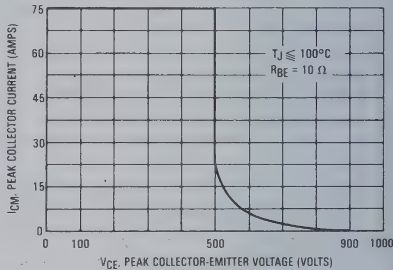


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FIGURE 34 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

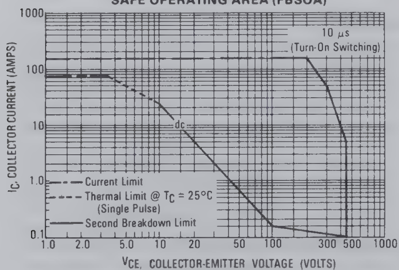

FIGURE 35 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)

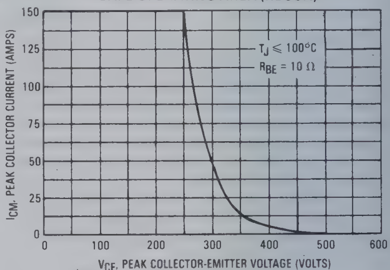

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FIGURE 36 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

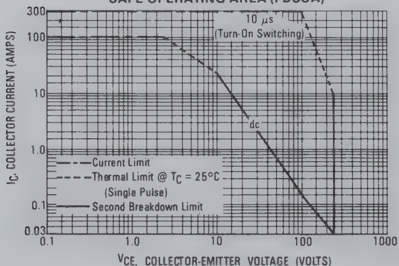
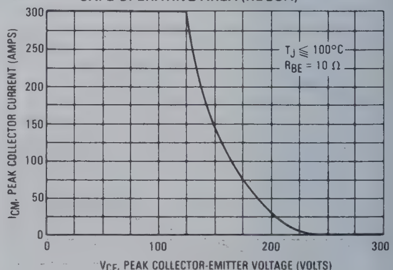


FIGURE 37 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



1.3

OVERLOAD CHARACTERISTICS

MJ10042

FIGURE 38 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

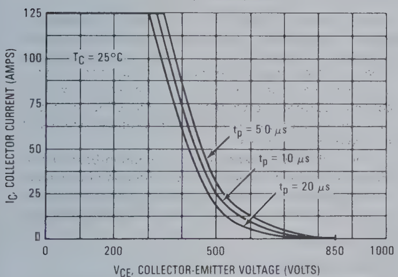
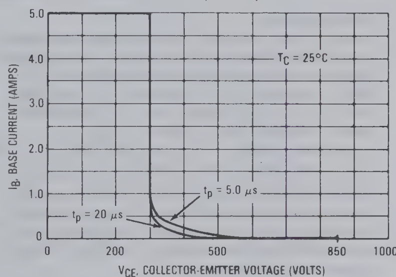


FIGURE 39 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



MJ10045

FIGURE 40 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

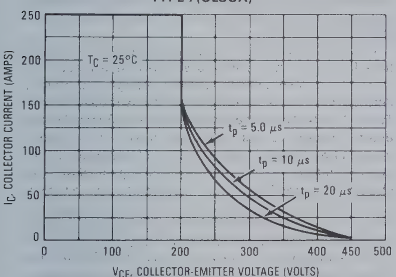
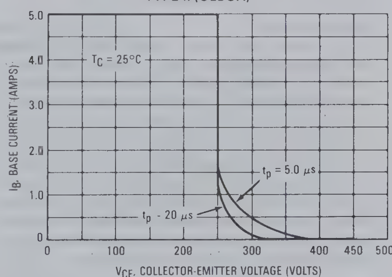


FIGURE 41 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



MJ10048

FIGURE 42 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

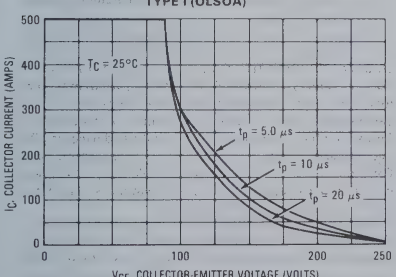
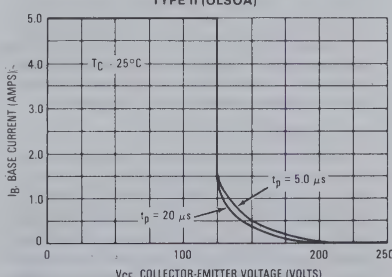


FIGURE 43 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 32, 34 and 36 are based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on these figures may be found at any case temperature by using the appropriate curve on Figure 28.

$T_{J(pk)}$ may be calculated from the data in Figure 31. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figures 33, 35 and 37 give the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in these figures adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figures 38, 40 and 42 depict the Type I OLSOA rating for these devices. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, these figures define the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 44) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figures 39, 41 and 43 are measured in the circuit shown in Figure 45, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

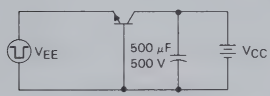
There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NON-REPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for these devices is 100 occurrences. Another factor is the form of turn-off bias. For these devices, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from I_{B2} = 0 (soft) to $V_{BE(off)}$ = 5 V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

1.3

OVERLOAD SAFE OPERATING TEST CIRCUITS

FIGURE 44 — OVERLOAD SOA TEST CIRCUIT
TYPE I (OLSOA)



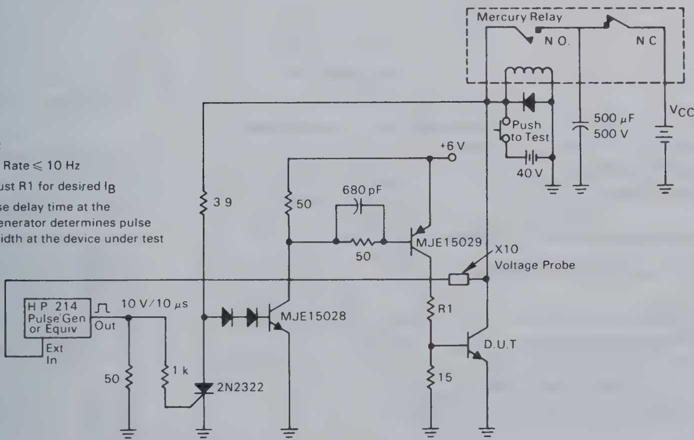
Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

FIGURE 45 — OVERLOAD SOA TEST CIRCUIT
TYPE II (OLSOA)

Notes:

- Rep Rate ⩽ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test



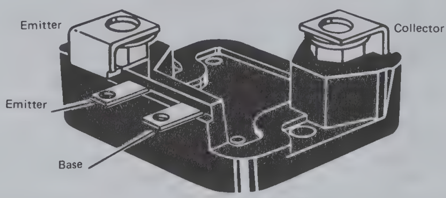
MOTOROLA

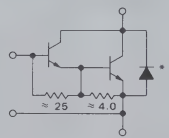
1.3

Designer's Data Sheet

50 KVA SWITCHMODE TRANSISTOR
50-Ampere Operating Current

The MJ10050 Darlington transistor is designed for industrial service under practical operating environments found in switching high power inductive loads off 460-Volt lines.





*Emitter-Collector Diode is a high power diode.

50 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
850 VOLTS
500 WATTS

Designer's Data for "Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.

MAXIMUM RATINGS

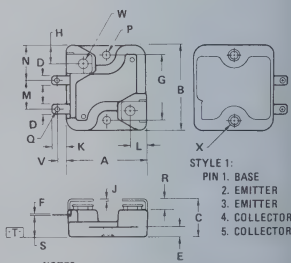
Mechanical Ratings		
Rating	**Value**	**Unit**
Mounting Torque (To heat sink with 10-32 Screw) (Note 1)	20	in.-lb
Lead Torque (Lead to bus with 1/4-20 Screw) (Note 2)	20	in.-lb
Per Unit Weight	120	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.25	°C/W

Mica Insulators available as separate items.
0.003″ thick. Motorola Part Number 14ASB12387B001.
0.006″ thick. Motorola Part Number 14ASB12387B002.

Notes:
1. A Belleville washer of 0.472″ O.D., 0.205″ I.D., 0.024″ thick and 150 pounds flat is recommended.
2. The lead torque should be limited to 20 in.-lb, unsupported to prevent rotation of the terminal in the package. The torque may be increased to 50 in.-lb if support is used to prevent rotation. The maximum penetration of the screw should be limited to 0.75″.



NOTES:
1. DIMENSION A AND B ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
⌖ ⌀ 0.36 (0.014) Ⓜ | T | A Ⓜ | B Ⓜ

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C	–	26.67	–	1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31 BSC		1.705 BSC	
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01

MAXIMUM RATINGS (Continued)

Electrical Ratings			
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	850	Vdc
Collector-Emitter Voltage (R_{BE} = 10 Ohms)	V_{CER}	900	Vdc
Collector-Base Voltage	V_{CB}	900	Vdc
Emitter-Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Operating, T_C = 125°C — Continuous, T_C = 25°C — Peak Repetitive, T_C = 25°C — Peak Nonrepetitive, T_C = 25°C	I_C	50 75 150 250	A
Base Current — Continuous — Peak Nonrepetitive	I_B	50 100	A
Total Device Dissipation @ T_C = 25°C Derate above 25°C For 1-minute overload	P_D	500 4.0 667	Watts W/°C Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}	−55 to +150 −55 to 200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 250 mAdc, I_B = 0)	$V_{CEO(sus)}$	850	—	—	Vdc
Collector Cutoff Current (V_{CE} = 900 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 900 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 — —	 — —	 2.0 10	mAdc
Collector Cutoff Current (V_{CE} = 900 Vdc, R_{BE} = 10 Ω, T_C = 100°C)	I_{CER}	—	—	10	mAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	—	650	mAdc
SAFE OPERATING AREA					
Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figure 13			
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figure 14			
Overload SOA	OLSOA	See Figures 16 and 17			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 50 Adc, V_{CE} = 5.0 Vdc) (I_C = 50 A, V_{CE} = 10 V)	h_{FE}	 35 40	 — —	 — —	
Collector-Emitter Saturation Voltage (I_C = 50 A, I_B = 4.0 A) (I_C = 75 Adc, I_B = 15 A) (I_C = 50 Adc, I_B = 4.0 A, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 2.0 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 50 Adc, I_B = 4.0 Adc) (I_C = 50 Adc, I_B = 4.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 3.0 3.0	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	4000	pF

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤2.0%.

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ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
Resistive Load						
Delay Time	(V_{CC} = 300 Vdc, I_C = 50 A, I_{B1} = 4.0 A, R_{BE} = 10 Ω, t_p = 50 μs, Duty Cycle ⩽ 2.0%)	t_d	—	0.03	0.25	μs
Rise Time		t_r	—	1.2	5.0	μs
Storage Time		t_s	—	35	100	μs
Fall Time		t_f	—	8.5	35	μs
Inductive Load, Clamped						
Storage Time	(I_{CM} = 50 A, V_{CEM} = 300 V, R_{BE} = 10 Ω, I_{B1} = 4.0 A) T_J = 100°C	t_{sv}	—	50	150	μs
Crossover Time	T_J = 100°C	t_c	—	20	60	μs
Storage Time	T_J = 25°C	t_{sv}	—	35	100	μs
Crossover Time	T_J = 25°C	t_c	—	10	35	μs
C-E DIODE CHARACTERISTICS						
Power Dissipation (I_B = 0)		P_D	—	—	250	W
Forward Voltage (1) (I_F = 50 A)		V_F	—	1.0	1.5	V
(I_F = 100 A)			—	1.2	2.0	V
Reverse Recovery Time (d_i/d_t = 25 A/μs, I_F = 50 A)		t_{rr}	—	4.0	12	μs
Forward Turn-On Time (Compliance Voltage = 50 V, I_F = 50 A)		t_{on}	—	0.3	1.2	μs
Single Cycle Surge Current (60 Hz)		I_{FSM}	—	—	500	A

(1) Pulse Test. Pulse width of 300 μs, duty cycle ⩽2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

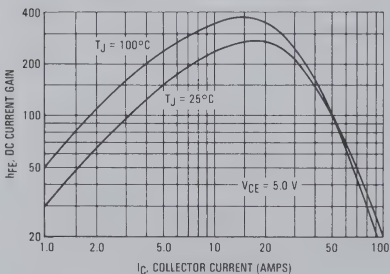


FIGURE 2 — DC CURRENT GAIN

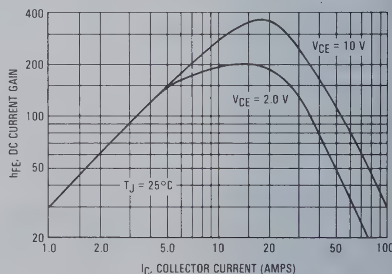


FIGURE 3 — DC CURRENT GAIN

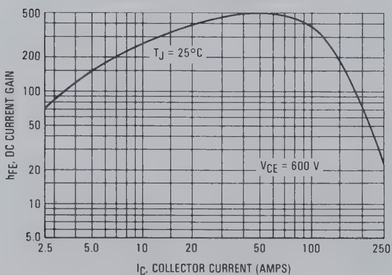
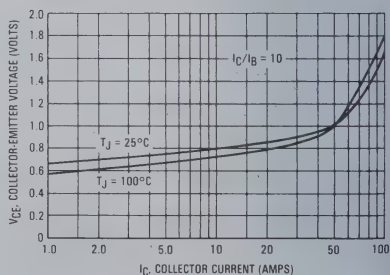


FIGURE 4 — COLLECTOR SATURATION VOLTAGE



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TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 5 — BASE-EMITTER SATURATION VOLTAGE

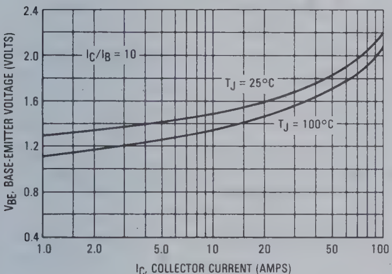
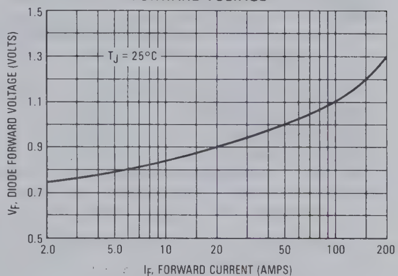


FIGURE 6 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

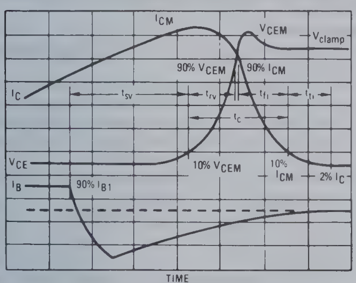


FIGURE 8 — TYPICAL INDUCTIVE SWITCHING TIMES

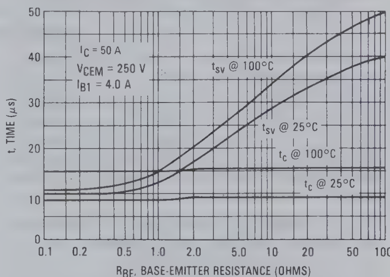


FIGURE 9 — TYPICAL TURN-ON SWITCHING TIMES

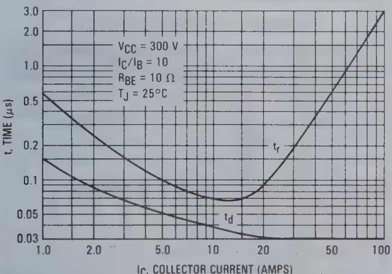
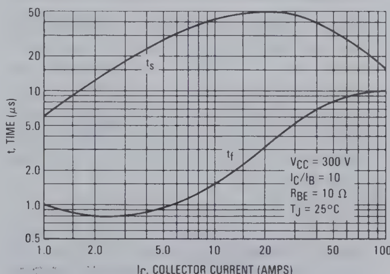
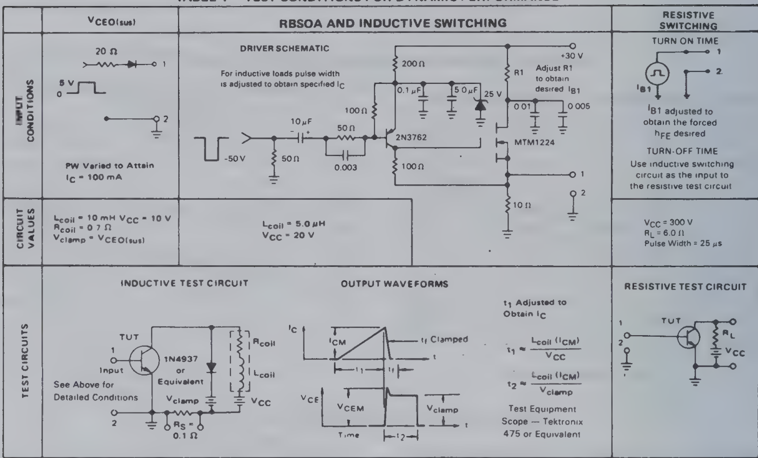


FIGURE 10 — TYPICAL TURN-OFF SWITCHING TIMES



1.3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust — V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 11 — TYPICAL PEAK REVERSE BASE CURRENT

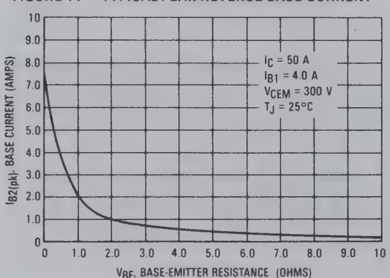
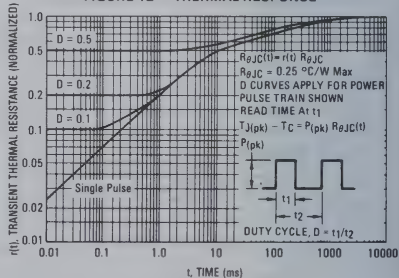


FIGURE 12 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

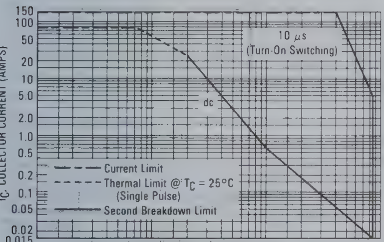


FIGURE 14 — MAXIMUM REVERSE-BIAS SAFE OPERATING AREA (RBSOA)

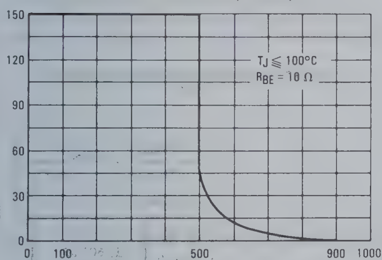
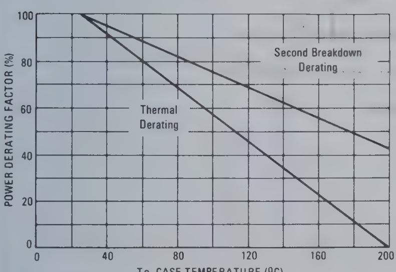


FIGURE 15 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in Figure 13 adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figure 16 depicts the Type I OLSOA rating for the MJ10050. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known,

(continued on back page)

1.3

OVERLOAD CHARACTERISTICS

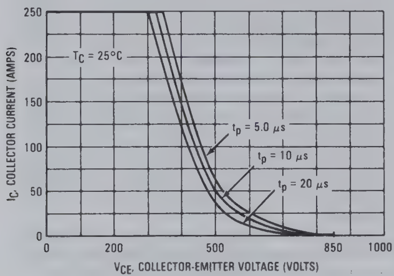


FIGURE 16 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

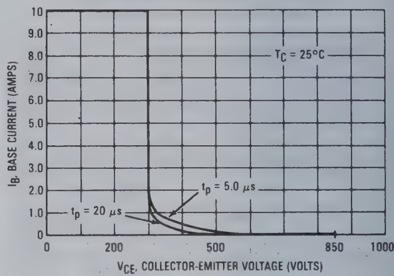


FIGURE 17 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)

FIGURE 18 — OVERLOAD SOA TEST CIRCUIT TYPE I

Notes:
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

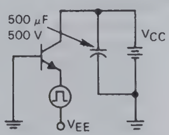
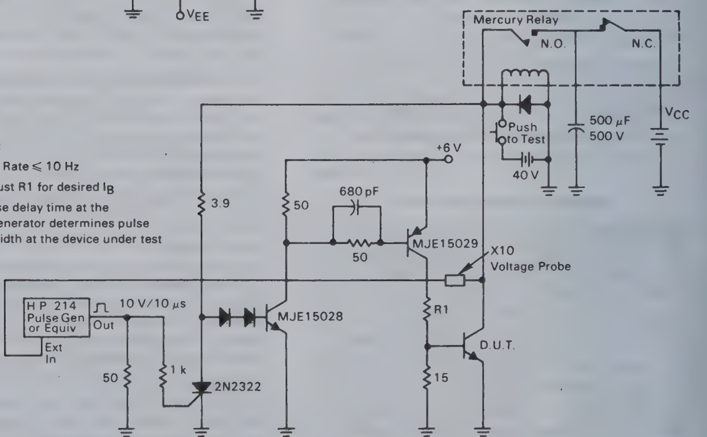


FIGURE 19 — OVERLOAD SOA TEST CIRCUIT TYPE II

Notes:
- Rep Rate ≤ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test



SAFE OPERATING AREA INFORMATION (continued)

TYPE I OLSOA (continued)

Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figure 17, is measured in the circuit shown in Figure 19, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NONREPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for the MJ10050 is 100 occurrences. Another factor is the form of turn-off bias. For the MJ10050, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

MJ10051
MJ10052

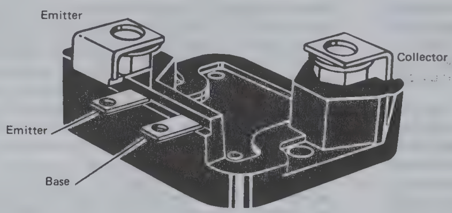
MOTOROLA

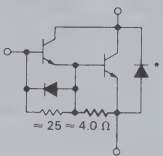
1.3

Designer's Data Sheet

50 KVA HIGH SPEED SWITCHMODE TRANSISTOR
50-Ampere Operating Current

The MJ10051 Darlington transistor is designed for industrial service under practical operating environments requiring fast switching speed for highly efficient systems operating at high frequency such as inverters, PWM controllers and other high frequency system operating from 460 V lines.





*Emitter-Collector Diode is a fast recovery, high power diode.

50 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
750 and 850 VOLTS
500 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MAXIMUM RATINGS

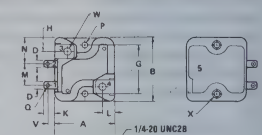
MECHANICAL RATINGS		
Rating	**Value**	**Unit**
Mounting Torque (To heat sink with 10-32 Screw) (Note 1)	20	in.-lb
Lead Torque (Lead to bus with 1/4-20 Screw) (Note 2)	20	in.-lb
Per Unit Weight	120	grams

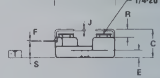
THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.25	°C/W

Mica Insulators available as separate items.
0.003″ thick. Motorola Part Number B12387B001.
0.006″ thick. Motorola Part Number B12387B002.

Notes:
1. A Belleville washer of 0.472″ O.D., 0.205″ I.D., 0.024″ thick and 150 pounds flat is recommended such as P/N AM125206 available from National Disc Spring Div., 385 Hillside Ave., Hillside N.J. 07205.
2. The lead torque should be limited to 20 in.-lb, unsupported to prevent rotation of the terminal in the package. The torque may be increased to 50 in.-lb if support is used to prevent rotation. The maximum penetration of the screw should be limited to 0.75″.





STYLE 1:
PIN 1. BASE
2. EMITTER
3. EMITTER
4. COLLECTOR
5. COLLECTOR

NOTES:
1. DIMENSION A AND B ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   ⌖ | ⌀ 0.36 (0.014) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C	–	26.67	–	1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31 BSC		1.705 BSC	
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01

MAXIMUM RATINGS (Continued)

ELECTRICAL RATINGS

Rating		Symbol	Value	Unit
Collector-Emitter Voltage	MJ10051 MJ10052	V_{CEO}	850 750	Vdc
Collector-Emitter Voltage (R_{BE} = 10 Ohms)		V_{CER}	900	Vdc
Collector-Base Voltage		V_{CB}	900	Vdc
Emitter-Base Voltage		V_{EB}	8.0	Vdc
Collector Current — Operating, T_C = 125°C — Continuous, T_C = 25°C — Peak Repetitive, T_C = 25°C — Peak Nonrepetitive, T_C = 25°C		I_C	50 75 150 250	A
Base Current — Continuous — Peak Nonrepetitive		I_B	50 100	A
Total Device Dissipation @ T_C = 25°C Derate above 25°C For 1-minute overload		P_D	500 4.0 667	Watts W/°C Watts
Operating Junction and Storage Temperature Range For 1-minute overload		T_J, T_{stg}	–55 to +150 –55 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1) (I_C = 250 mAdc, I_B = 0)	MJ10051 MJ10052	$V_{CEO(sus)}$	850 750	— —	— —	Vdc
Collector Cutoff Current (V_{CE} = 900 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 900 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	 — —	 — —	 2.0 10	mAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)		I_{EBO}	—	—	950	mAdc
SAFE OPERATING AREA						
Second Breakdown Collector Current with Base Forward-Biased		FBSOA	—			
Clamped Inductive SOA with Base Reverse-Biased		RBSOA	—			
Overload SOA		OLSOA	—			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 50 Adc, V_{CE} = 5.0 Vdc) (I_C = 50 A, V_{CE} = 10 V)		h_{FE}	 25 40	 — —	 — —	
Collector-Emitter Saturation Voltage (I_C = 50 Adc, I_B = 5.0 A) (I_C = 75 Adc, I_B = 15 A) (I_C = 50 Adc, I_B = 5.0 A, T_C = 100°C)		$V_{CE(sat)}$	 — — —	 — — —	 2.0 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 50 Adc, I_B = 5.0 Adc) (I_C = 50 Adc, I_B = 5.0 Adc, T_C = 100°C)		$V_{BE(sat)}$	 — —	 — —	 3.0 3.0	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	—	—	4000	pF

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤2.0%.

1.3

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
Resistive Load							
Delay Time	(V_{CC} = 300 Vdc, I_C = 50 A, I_{B1} = 5.0 A, $V_{BE(off)}$ = 5.0 V, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.03	0.25	μs
Rise Time			t_r	—	1.2	5.0	μs
Storage Time			t_s	—	3.3	10	μs
Fall Time			t_f	—	1.5	5.0	μs
Inductive Load, Clamped							
Storage Time	(I_{CM} = 50 A, V_{CEM} = 300 V, $V_{BE(off)}$ = 5.0 V, I_{B1} = 5.0 A)	T_J = 100°C	t_{sv}	—	5.0	15	μs
Crossover Time			t_c	—	3.0	10	μs
Storage Time		T_J = 25°C	t_{sv}	—	3.5	10	μs
Crossover Time			t_c	—	1.5	5.0	μs
C-E DIODE CHARACTERISTICS							
Power Dissipation (I_B = 0)			P_D	—	—	250	W
Forward Voltage (1) (I_F = 50 A)			V_F	—	2.7	5.0	V
Reverse Recovery Time* (di/dt = 50 A/μs, I_F = 50 A, $V_{BE(off)}$ = 5.0 V)			t_{rr}	—	0.2	1.0	μs
Forward Turn-On Time (Compliance Voltage = 50 V, I_F = 50 A)			t_{on}	—	0.1	1.0	μs
Single Cycle Surge Current (60 Hz)			I_{FSM}	—	—	500	A
Reverse Recovery Current (I_F = 50 A, di/dt = 50 A/μs)			$I_{RM(REC)}$	—	7.0	25	A

(1) Pulse Test. Pulse width ≤ 300 μs, duty cycle ≤2.0%.
*Requires negative base-emitter voltage for fast recovery performance.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

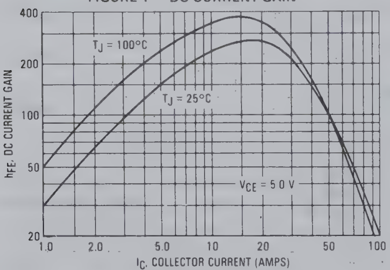


FIGURE 2 — DC CURRENT GAIN

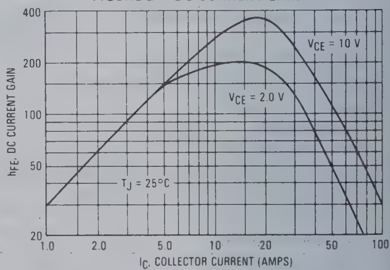


FIGURE 3 — DC CURRENT GAIN

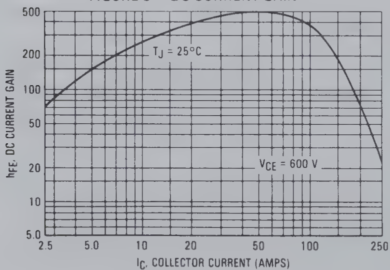
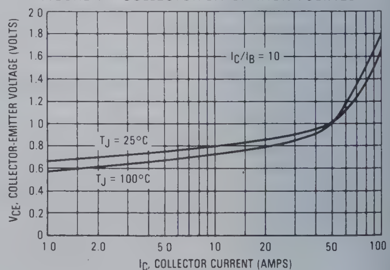


FIGURE 4 — COLLECTOR SATURATION VOLTAGE



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 5 — BASE-EMITTER SATURATION VOLTAGE

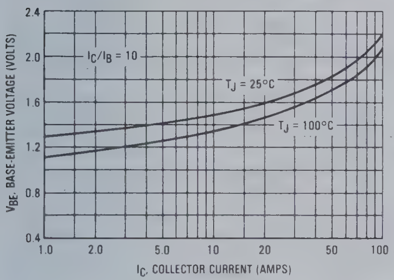
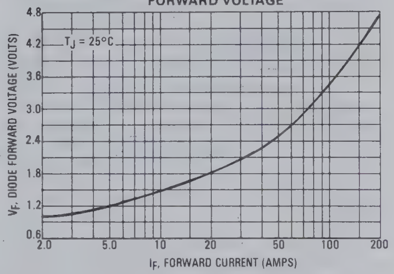


FIGURE 6 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

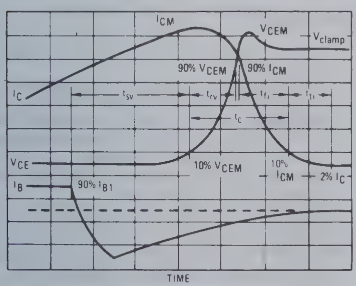


FIGURE 8 — INDUCTIVE SWITCHING TIMES

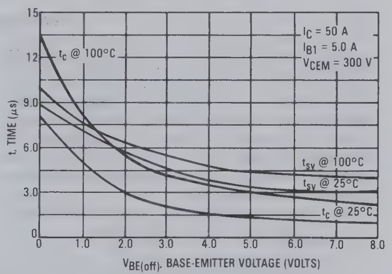


FIGURE 9 — TYPICAL TURN-ON SWITCHING TIMES

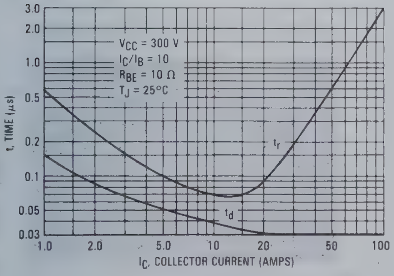
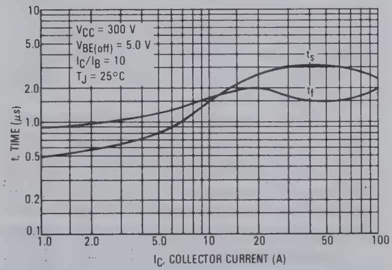
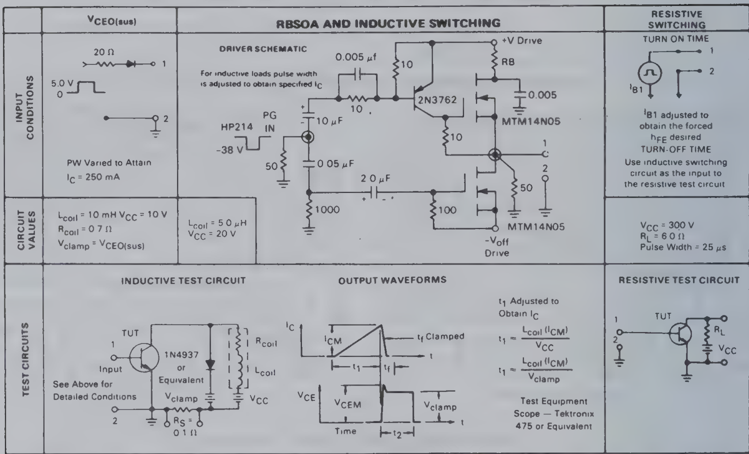


FIGURE 10 — TURN-OFF SWITCHING TIMES



1.3

TABLE 1 — RBSOA AND INDUCTIVE SWITCHING DRIVER SCHEMATIC



*Adjust − V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 11 — PEAK REVERSE BASE CURRENT

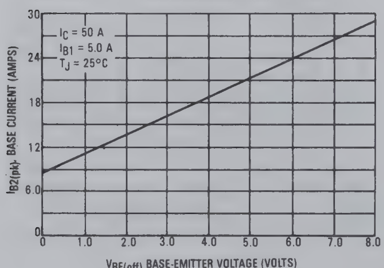
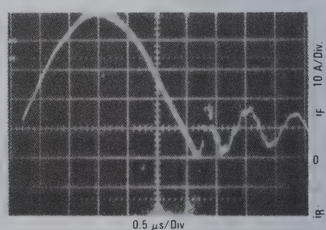


FIGURE 12 — REVERSE RECOVERY WAVEFORM



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

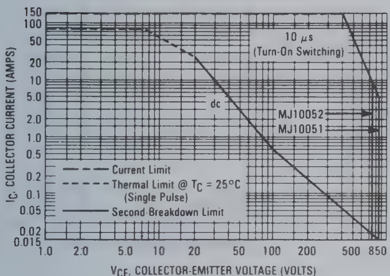


FIGURE 14 — MAXIMUM REVERSE-BIAS SAFE OPERATING AREA (RBSOA)

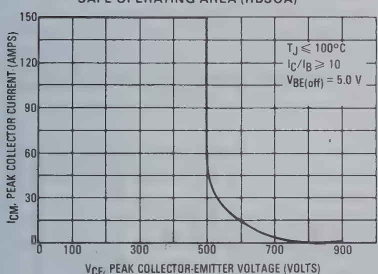
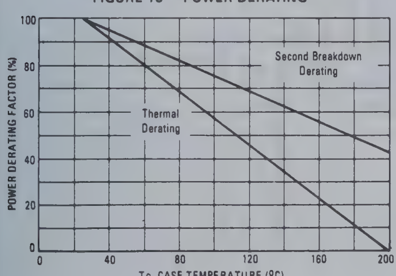


FIGURE 15 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 20. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in Figure 13 adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figure 16 depicts the Type I OLSOA rating for the devices. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault

(continued on back page)

1.3

OVERLOAD CHARACTERISTICS

FIGURE 16 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

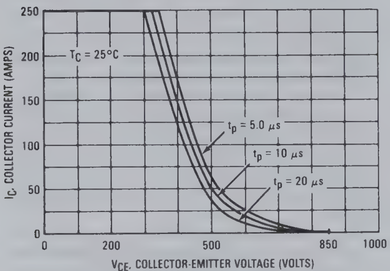


FIGURE 17 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)

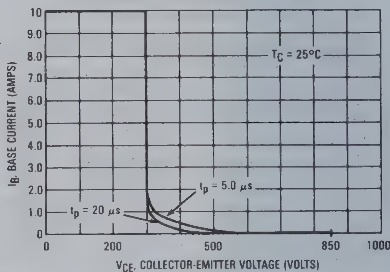


FIGURE 18 — OVERLOAD SOA TEST CIRCUIT TYPE I

Notes:
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

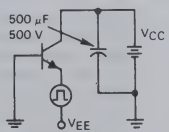
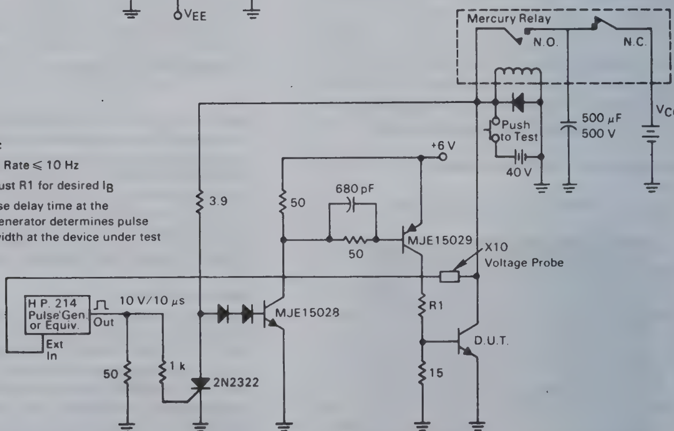


FIGURE 19 — OVERLOAD SOA TEST CIRCUIT TYPE II

Notes:
- Rep Rate ⩽ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test



SAFE OPERATING AREA INFORMATION (continued)

TYPE I OLSOA (continued)

condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

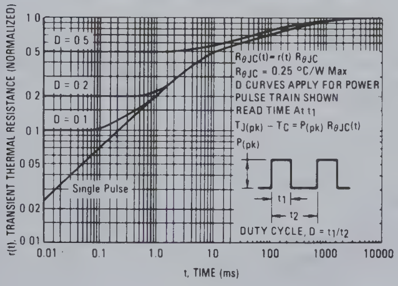
Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figure 17, is measured in the circuit shown in Figure 19, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NONREPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for the devices are 100 occurrences. Another factor is the form of turn-off bias. For the devices, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

FIGURE 20 — THERMAL RESPONSE



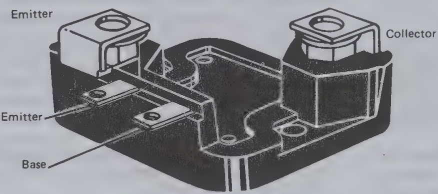
MOTOROLA

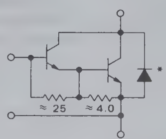
1.3

Designer's Data Sheet

50 KVA SWITCHMODE TRANSISTOR
100-Ampere Operating Current

The MJ10100 Darlington transistor is designed for industrial service under practical operating environments found in switching high power inductive loads off 230-Volt lines.



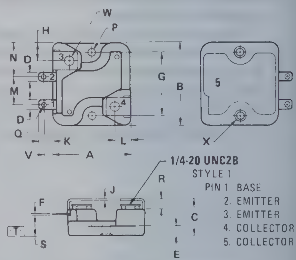


*Emitter-Collector Diode is a high power diode.

100 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
450 VOLTS
500 WATTS

Designer's Data for "Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.



NOTES:
1. DIMENSION A AND B ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
⌖ | ⌀ 0.36 (0.014) Ⓜ | T | A Ⓜ | B Ⓜ

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C	–	26.67	–	1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31 BSC		1.705 BSC	
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01
MO-040AA

MAXIMUM RATINGS

Mechanical Ratings

Rating	Value	Unit
Mounting Torque (To heat sink with 10-32 Screw) (Note 1)	20	in.-lb
Lead Torque (Lead to bus with 1/4-20 Screw) (Note 2)	20	in.-lb
Per Unit Weight	120	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.25	°C/W

Mica Insulators available as separate items.
0.003" thick. Motorola Part Number 14ASB12387B001.
0.006" thick. Motorola Part Number 14ASB12387B002.

Notes:
1. A Belleville washer of 0.472" O.D., 0.205" I.D., 0.024" thick and 150 pounds flat is recommended.
2. The lead torque should be limited to 20 in.-lb, unsupported to prevent rotation of the terminal in the package. The torque may be increased to 50 in.-lb if support is used to prevent rotation. The maximum penetration of the screw should be limited to 0.75".

MAXIMUM RATINGS (Continued)

Electrical Ratings			
Rating	**Symbol**	**Value**	**Unit**
Collector-Emitter Voltage	V_{CEO}	450	Vdc
Collector-Emitter Voltage (R_{BE} = 10 Ohms)	V_{CER}	500	Vdc
Collector-Base Voltage	V_{CB}	500	Vdc
Emitter-Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Operating, T_C = 87.5°C — Continuous, T_C = 25°C — Peak Repetitive, T_C = 25°C — Peak Nonrepetitive, T_C = 25°C	I_C	100 150 300 500	A
Base Current — Continuous — Peak Nonrepetitive	I_B	50 100	A
Total Device Dissipation @ T_C = 25°C Derate above 25°C For 1-minute overload	P_D	500 4.0 667	Watts W/°C Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}	–55 to +150 –55 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 250 mAdc, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CE} = 500 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 500 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 — —	 — —	 2.0 10	mAdc
Collector Cutoff Current (V_{CE} = 500 Vdc, R_{BE} = 10 Ω, T_C = 100°C)	I_{CER}	—	—	10	mAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	—	650	mAdc
SAFE OPERATING AREA					
Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figure 13			
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figure 14			
Overload SOA	OLSOA	See Figures 16 and 17			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 100 Adc, V_{CE} = 5.0 Vdc) (I_C = 100 A, V_{CE} = 10 V)	h_{FE}	 50 60	 — —	 — —	
Collector-Emitter Saturation Voltage (I_C = 100 Adc, I_B = 3.3 A) I_C = 150 Adc, I_B = 12 A) (I_C = 100 Adc, I_B = 3.3 A, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 2.0 3.3 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 100 Adc, I_B = 3.3 Adc) (I_C = 100 Adc, I_B = 3.3 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 3.0 3.0	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	4000	pF

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤2.0%.

1.3

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
Resistive Load							
Delay Time	(V_{CC} = 250 Vdc, I_C = 100 A, I_{B1} = 3.3 A, R_{BE} = 10 Ω, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.03	0.25	μs
Rise Time			t_r	—	0.9	3.0	μs
Storage Time			t_s	—	10	25	μs
Fall Time			t_f	—	3.0	10	μs
Inductive Load, Clamped							
Storage Time	(I_{CM} = 100 A, V_{CEM} = 250 V, R_{BE} = 10 Ω, I_{B1} = 3.3 A)	T_J = 100°C	t_{sv}	—	15	50	μs
Crossover Time			t_c	—	4.0	15	μs
Storage Time		T_J = 25°C	t_{sv}	—	10	25	μs
Crossover Time			t_c	—	2.7	10	μs
C-E DIODE CHARACTERISTICS							
Power Dissipation (I_B = 0)			P_D	—	—	250	W
Forward Voltage (1) (I_F = 100 A)			V_F	—	1.1	1.5	V
(I_F = 200 A)				—	1.4	2.0	V
Reverse Recovery Time (d_i/d_t = 25 A/μs, I_F = 100 A)			t_{rr}	—	3.3	10	μs
Forward Turn-On Time (Compliance Voltage = 250 V, I_F = 100 A)			t_{on}	—	0.3	1.0	μs
Single Cycle Surge Current (60 Hz)			I_{FSM}	—	—	500	A

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

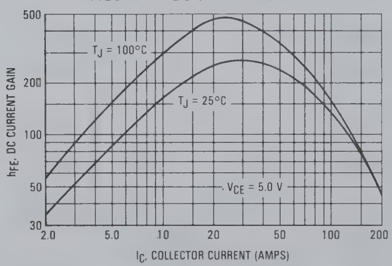


FIGURE 2 — DC CURRENT GAIN

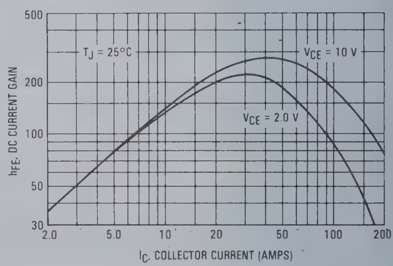


FIGURE 3 — DC CURRENT GAIN

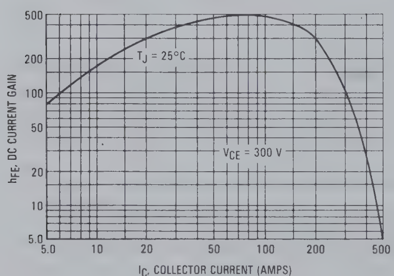
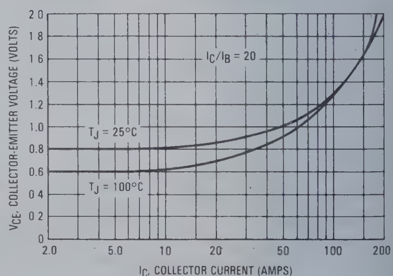


FIGURE 4 — COLLECTOR SATURATION REGION



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 5 — BASE-EMITTER SATURATION VOLTAGE

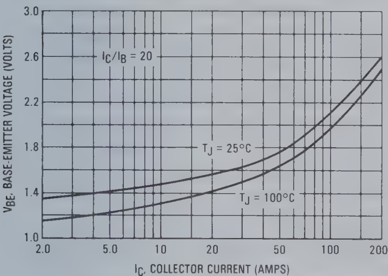
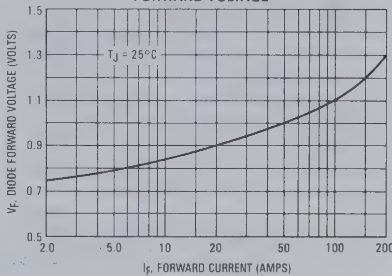


FIGURE 6 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

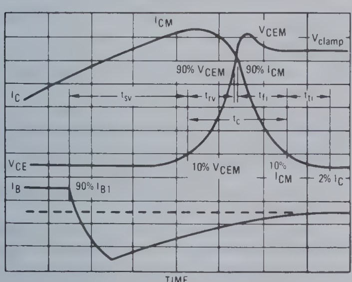


FIGURE 8 — INDUCTIVE SWITCHING TIMES

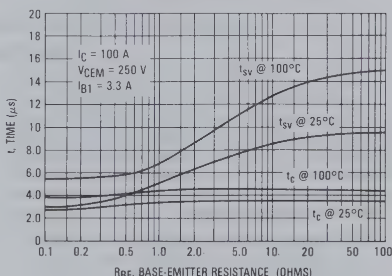


FIGURE 9 — TURN-ON SWITCHING TIMES

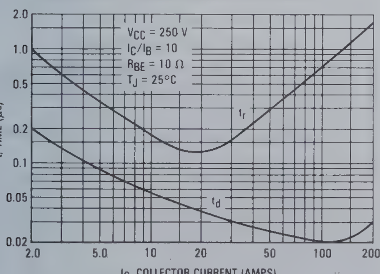
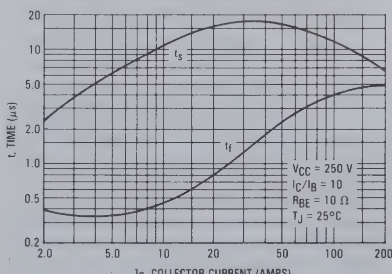
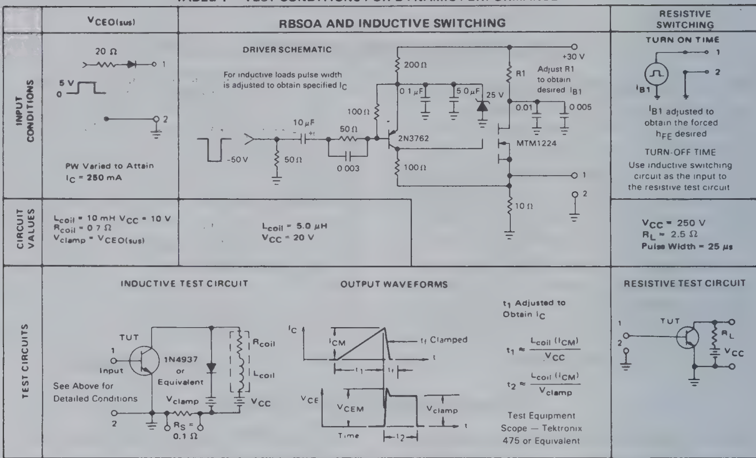


FIGURE 10 — TURN-OFF SWITCHING TIMES



1.3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust — V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 11 — PEAK REVERSE BASE CURRENT

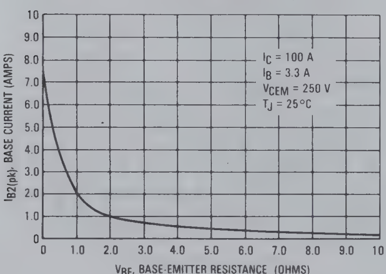
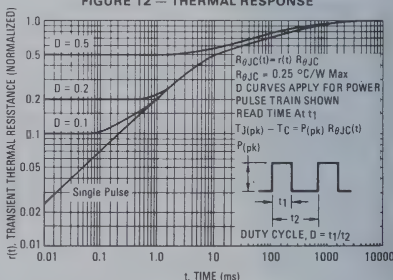


FIGURE 12 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM RATED FORWARD BIAS, SAFE OPERATING AREA (FBSOA)

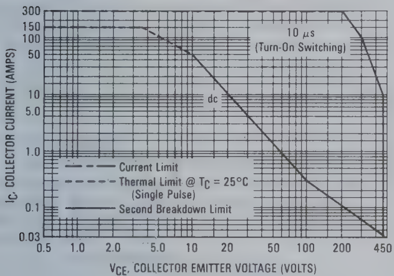


FIGURE 14 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)

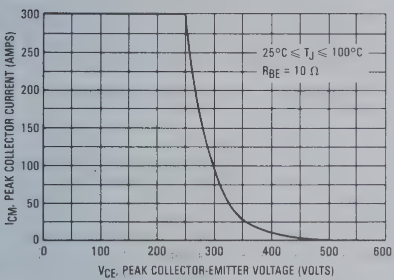
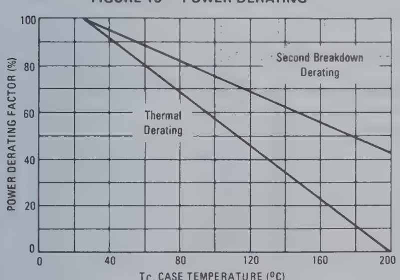


FIGURE 15 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off; in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in Figure 13 adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figure 16 depicts the Type I OLSOA rating for the MJ10100. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known,

(continued on back page)

1.3

OVERLOAD CHARACTERISTICS

FIGURE 16 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

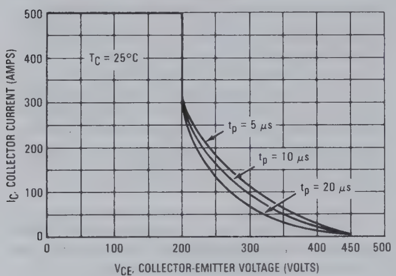


FIGURE 17 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)

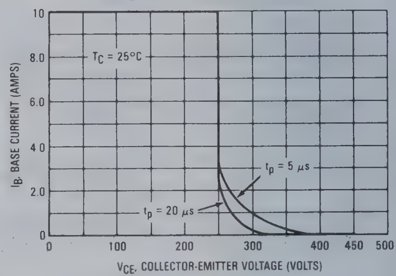


FIGURE 18 — OVERLOAD SOA TEST CIRCUIT TYPE I

Notes:
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

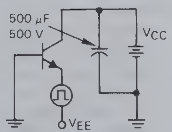
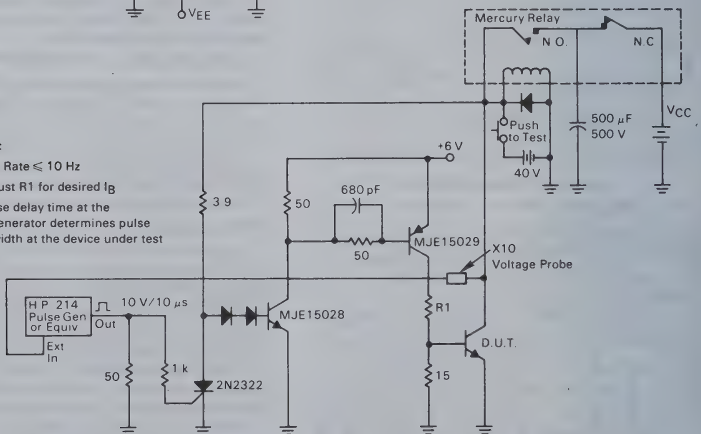


FIGURE 19 — OVERLOAD SOA TEST CIRCUIT TYPE II

Notes:
- Rep Rate ≤ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test



SAFE OPERATING AREA INFORMATION (continued)

TYPE I OLSOA (continued)

Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figure 17, is measured in the circuit shown in Figure 19, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NONREPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for the MJ10100 is 100 occurrences. Another factor is the form of turn-off bias. For the MJ10100, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

MJ10101
MJ10102

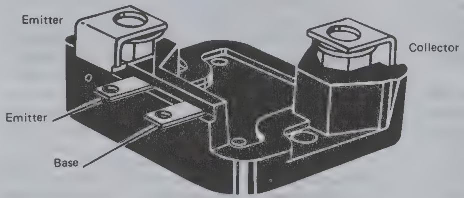
MOTOROLA

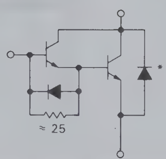
1.3

Designer's Data Sheet

50 KVA HIGH SPEED SWITCHMODE TRANSISTOR
100-Ampere Operating Current

The MJ10101 Darlington transistor is designed for industrial service under practical operating environments requiring fast switching speed for highly efficient systems operating at high frequency such as inverters, PWM controllers and other high frequency systems operating from 230 V lines.





*Emitter-Collector Diode is a fast recovery, high power diode.

100 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
350 and 450 VOLTS
500 WATTS

Designer's Data for "Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.

MAXIMUM RATINGS

Mechanical Ratings		
Rating	**Value**	**Unit**
Mounting Torque (To heat sink with 10-32 Screw) (Note 1)	20	in.-lb
Lead Torque (Lead to bus with 1/4-20 Screw) (Note 2)	20	in.-lb
Per Unit Weight	120	grams

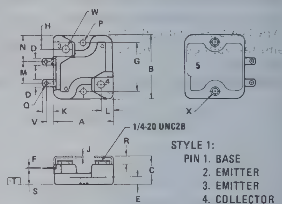
THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.25	°C/W

Mica Insulators available as separate items.
0.003" thick. Motorola Part Number B12387B001.
0.006" thick. Motorola Part Number B12387B002.

Notes:

1. A Belleville washer of 0.472" O.D., 0.205" I.D., 0.024" thick and 150 pounds flat is recommended such as P/N AM125206 available from National Disc Spring Div., 385 Hillside Ave., Hillside N.J. 07205.
2. The lead torque should be limited to 20 in.-lb, unsupported to prevent rotation of the terminal in the package. The torque may be increased to 50 in.-lb if support is used to prevent rotation. The maximum penetration of the screw should be limited to 0.75".



STYLE 1:
PIN 1. BASE
2. EMITTER
3. EMITTER
4. COLLECTOR
5. COLLECTOR

NOTES:
1. DIMENSION A AND B ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
⌖ ⌀ 0.36 (0.014) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C	–	26.67	–	1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31 BSC		1.705 BSC	
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01

MAXIMUM RATINGS (Continued)

Electrical Ratings			
Rating	**Symbol**	**Value**	**Unit**
Collector-Emitter Voltage MJ10101 MJ10102	V_{CEO}	450 350	Vdc
Collector-Emitter Voltage (R_{BE} = 10 Ohms)	V_{CER}	500	Vdc
Collector-Base Voltage	V_{CB}	500	Vdc
Emitter-Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Operating, T_C = 87.5°C — Continuous, T_C = 25°C — Peak Repetitive, T_C = 25°C — Peak Nonrepetitive, T_C = 25°C	I_C	100 150 300 500	A
Base Current — Continuous — Peak Nonrepetitive	I_B	50 100	A
Total Device Dissipation @ T_C = 25°C Derate above 25°C For 1-minute overload	P_D	500 4.0 667	Watts W/°C Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}	−55 to +150 −55 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) MJ10101 (I_C = 250 mAdc, I_B = 0) MJ10102	$V_{CEO(sus)}$	450 350	—	—	Vdc
Collector Cutoff Current (V_{CE} = 500 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 500 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 — —	 — —	 2.0 10	mAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	—	5.0	mAdc
SAFE OPERATING AREA					
Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figure 13			
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figure 14			
Overload SOA	OLSOA	See Figures 16 and 17			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 100 Adc, V_{CE} = 5.0 Vdc) (I_C = 100 A, V_{CE} = 10 V)	h_{FE}	 50 60	 — —	 — —	
Collector-Emitter Saturation Voltage (I_C = 100 Adc, I_B = 3.3 A) I_C = 150 Adc, I_B = 12 A) (I_C = 100 Adc, I_B = 3.3 A, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 2.0 3.3 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 100 Adc, I_B = 3.3 Adc) (I_C = 100 Adc, I_B = 3.3 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 3.0 3.0	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	4000	pF

(1) Pulse Test. Pulse width of 300 μs, duty cycle $\leqslant$2.0%.

1.3

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS					
Resistive Load					
Delay Time (V_{CC} = 250 Vdc, I_C = 100 A, I_{B1} = 3.3 A, $V_{BE(off)}$ = 5.0 V, t_p = 50 μs Duty Cycle ≤ 2.0%)	t_d	—	0.03	0.25	μs
Rise Time	t_r	—	0.9	3.0	μs
Storage Time	t_s	—	1.5	3.75	μs
Fall Time	t_f	—	0.4	1.25	μs
Inductive Load, Clamped					
Storage Time (I_{CM} = 100 A, $V_{BE(off)}$ = 5.0 V, V_{CEM} = 250 V I_{B1} = 3.3 A) T_J = 100°C	t_{sv}	—	2.5	7.5	μs
Crossover Time T_J = 100°C	t_c	—	0.8	3.0	μs
Storage Time T_J = 25°C	t_{sv}	—	1.5	3.75	μs
Crossover Time T_J = 25°C	t_c	—	0.5	1.5	μs
C-E DIODE CHARACTERISTICS					
Power Dissipation (I_B = 0)	P_D	—	—	250	W
Forward Voltage (1) (I_F = 100 A)	V_F	—	1.7	5.0	V
Reverse Recovery Current (I_F = 100 A, di/dt = 100 A/μs)	$I_{RM(rec)}$	—	20	50	A
Reverse Recovery Time	t_{rr}	—	0.4	1.0	μs
Forward Turn-On Time (Compliance Voltage = 250 V, I_F = 100 A)	t_{on}	—	0.1	0.5	μs
Single Cycle Surge Current (60 Hz)	I_{FSM}	—	—	500	A

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

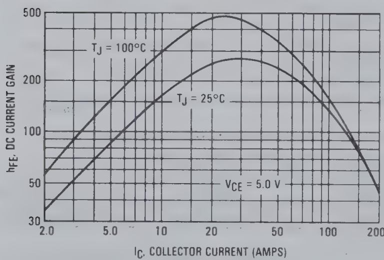


FIGURE 2 — DC CURRENT GAIN

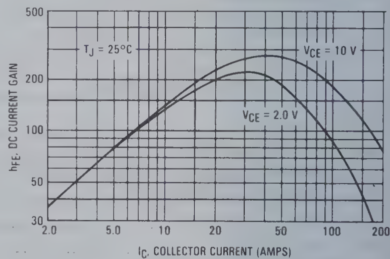


FIGURE 3 — DC CURRENT GAIN

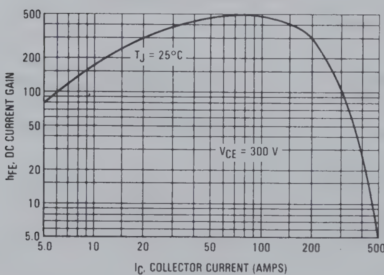
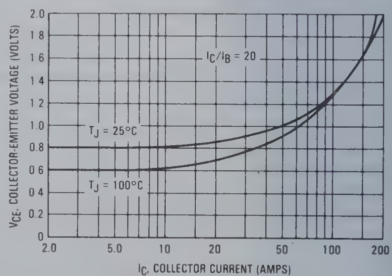


FIGURE 4 — COLLECTOR SATURATION REGION



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 5 — BASE-EMITTER SATURATION VOLTAGE

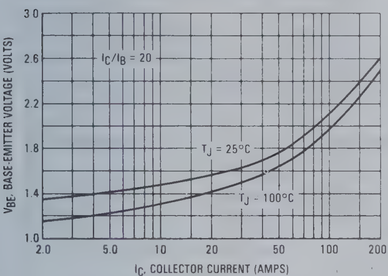
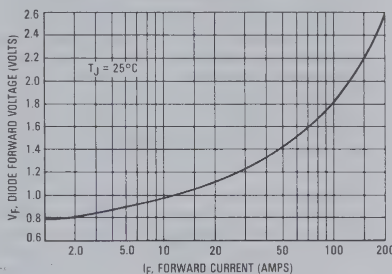


FIGURE 6 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

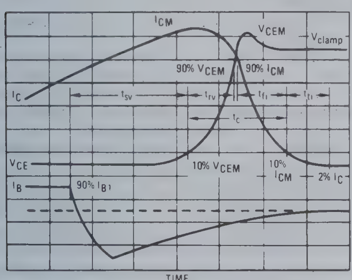


FIGURE 8 — INDUCTIVE SWITCHING TIMES

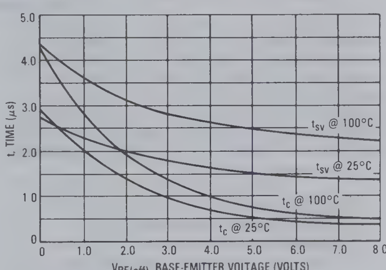


FIGURE 9 — TURN-ON SWITCHING TIMES

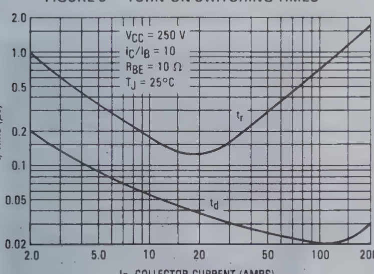


FIGURE 10 — TURN-OFF SWITCHING TIMES

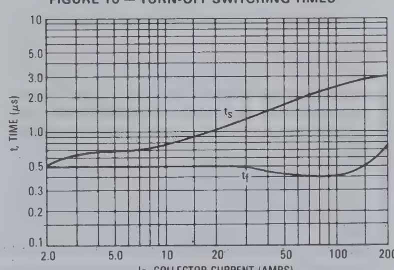
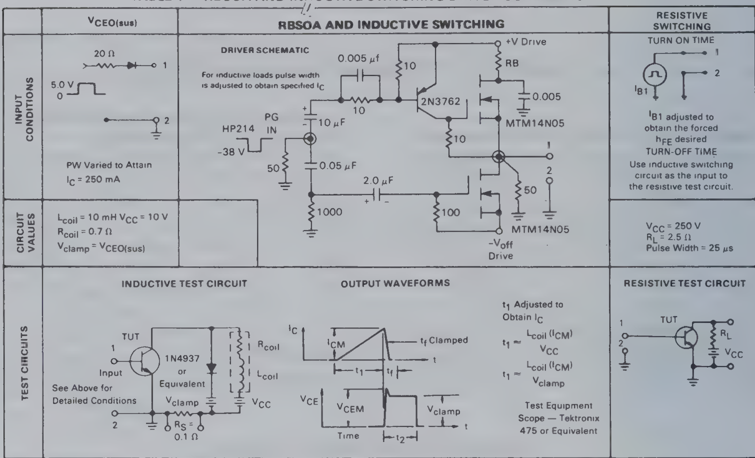


TABLE 1 — RBSOA AND INDUCTIVE SWITCHING DRIVER SCHEMATIC



*Adjust — V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{CEM}
- t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
- t_{fi} = Current Fall Time, 90—10% I_{CM}
- t_{ti} = Current Tail, 10—2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 11 — PEAK REVERSE BASE CURRENT

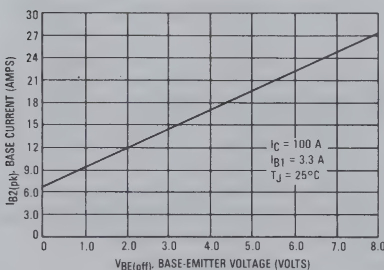
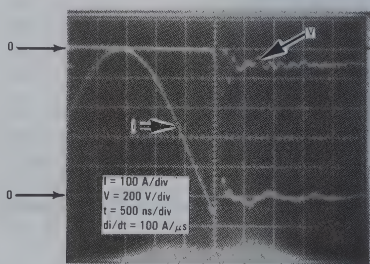


FIGURE 12 — REVERSE RECOVERY WAVEFORM



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM RATED FORWARD BIAS, SAFE OPERATING AREA

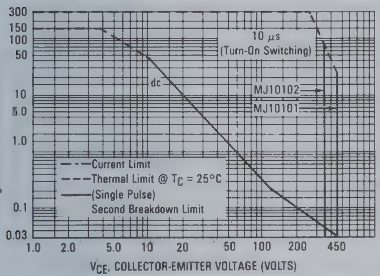


FIGURE 14 — MAXIMUM REVERSE-BIAS SAFE OPERATING AREA (RBSOA)

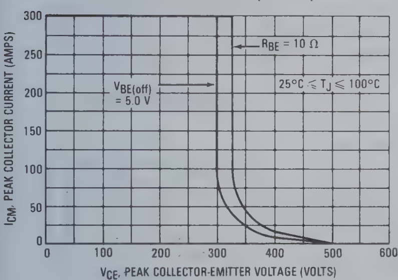
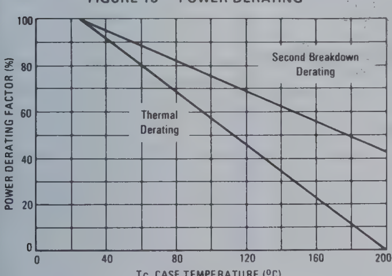


FIGURE 15 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 20. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in Figure 13 adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figure 16 depicts the Type I OLSOA rating for the MJ10101. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known,

(continued on back page)

1.3

OVERLOAD CHARACTERISTICS

FIGURE 16 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

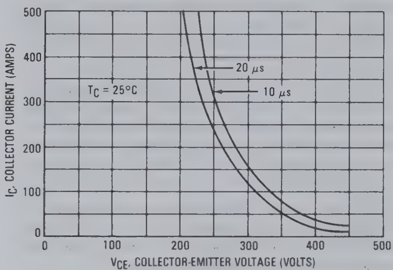


FIGURE 17 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)

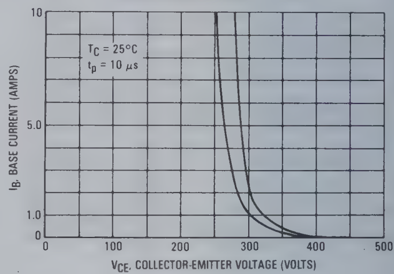


FIGURE 18 — OVERLOAD SOA TEST CIRCUIT TYPE I

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

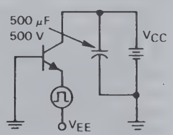
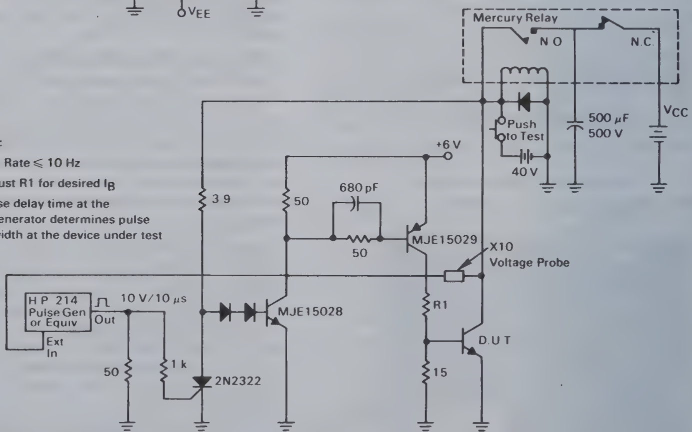


FIGURE 19 — OVERLOAD SOA TEST CIRCUIT TYPE II

Notes:

- Rep Rate ⩽ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test



SAFE OPERATING AREA INFORMATION (continued)

TYPE I OLSOA (continued)

Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

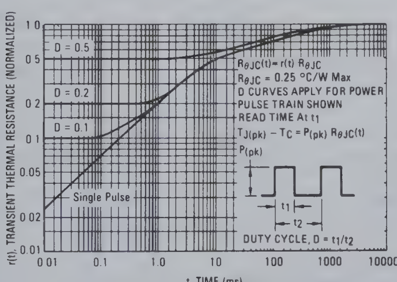
Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figure 17, is measured in the circuit shown in Figure 19, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NONREPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for the MJ10101 is 100 occurrences. Another factor is the form of turn-off bias. For the MJ10101, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} \doteq 0$ (soft) to $V_{BE(off)} = 5$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

FIGURE 20 — THERMAL RESPONSE



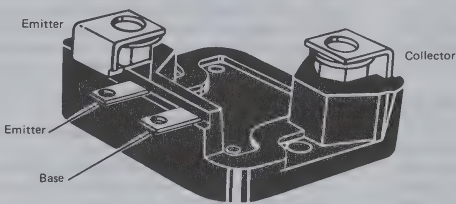
MOTOROLA

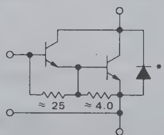
1.3

Designer's Data Sheet

50 KVA SWITCHMODE TRANSISTOR
200-Ampere Operating Current

The MJ10200 Darlington transistor is designed for industrial service under practical operating environments found in switching high power inductive loads off 120-Volt lines.



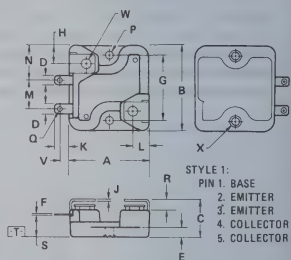


*Emitter-Collector Diode is a high power diode.

200 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
250 VOLTS
500 WATTS

Designer's Data for "Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.



STYLE 1:
PIN 1. BASE
2. EMITTER
3. EMITTER
4. COLLECTOR
5. COLLECTOR

NOTES:
1. DIMENSION A AND B ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
⌖ ⌀ 0.36 (0.014) Ⓜ | T | A Ⓜ | B Ⓜ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C	–	26.67	·	1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31 BSC		1.705 BSC	
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01

MAXIMUM RATINGS

Mechanical Ratings		
Rating	Value	Unit
Mounting Torque (To heat sink with 10-32 Screw) (Note 1)	20	in.-lb
Lead Torque (Lead to bus with 1/4-20 Screw) (Note 2)	20	in.-lb
Per Unit Weight	120	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.25	°C/W

Mica Insulators available as separate items.
0.003″ thick. Motorola Part Number 14ASB12387B001.
0.006″ thick. Motorola Part Number 14ASB12387B002.

Notes:
1. A Belleville washer of 0.472″ O.D., 0.205″ I.D., 0.024″ thick and 150 pounds flat is recommended.
2. The lead torque should be limited to 20 in.-lb, unsupported to prevent rotation of the terminal in the package. The torque may be increased to 50 in.-lb if support is used to prevent rotation. The maximum penetration of the screw should be limited to 0.75″.

MAXIMUM RATINGS (Continued)

Electrical Ratings			
Rating	**Symbol**	**Value**	**Unit**
Collector-Emitter Voltage	V_{CEO}	250	Vdc
Collector-Emitter Voltage (R_{BE} = 10 Ohms)	V_{CER}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Operating, T_C = 50°C — Continuous, T_C = 25°C — Peak Repetitive, T_C = 25°C — Peak Nonrepetitive, T_C = 25°C	I_C	200 300 600 1000	A
Base Current — Continuous — Peak Nonrepetitive	I_B	50 100	A
Total Device Dissipation @ T_C = 25°C Derate above 25°C For 1-minute overload	P_D	500 4.0 667	Watts W/°C Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}	-55 to +150 -55 to 200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 250 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current (V_{CE} = 300 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 300 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 — —	 — —	 2.0 10	mAdc
Collector Cutoff Current (V_{CE} = 300 Vdc, R_{BE} = 10 Ω, T_C = 100°C)	I_{CER}	—	—	10	mAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	—	650	mAdc
SAFE OPERATING AREA					
Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figure 13			
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figure 14			
Overload SOA	OLSOA	See Figures 16 and 17			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 200 Adc, V_{CE} = 5.0 Vdc) (I_C = 200 A, V_{CE} = 10 V)	h_{FE}	 75 90	 — —	 — —	 — —
Collector-Emitter Saturation Voltage (I_C = 200 Adc, I_B = 5.5 A) (I_C = 200 Adc, I_B = 5.5 A, T_C = 100°C)	$V_{CE(sat)}$	 — —	 — —	 2.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 200 Adc, I_B = 5.5 Adc) (I_C = 200 Adc, I_B = 5.5 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 3.5 3.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	4000	pF

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤2.0%.

1.3

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
Resistive Load							
Delay Time	(V_{CC} = 150 Vdc, I_C = 200 A, I_{B1} = 5.5 A, R_{BE} = 10 Ω, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.035	0.25	μs
Rise Time			t_r	—	1.2	4.0	μs
Storage Time			t_s	—	6.3	20	μs
Fall Time			t_f	—	2.5	8.0	μs
Inductive Load, Clamped							
Storage Time	(I_{CM} = 200 A, V_{CEM} = 150 V, R_{BE} = 10 Ω, I_{B1} = 5.5 A)	T_J = 100°C	t_{sv}	—	9.0	30	μs
Crossover Time			t_c	—	3.3	12	μs
Storage Time		T_J = 25°C	t_{sv}	—	6.5	20	μs
Crossover Time			t_c	—	2.3	8.0	μs
C-E DIODE CHARACTERISTICS							
Power Dissipation (I_B = 0)			P_D	—	—	250	W
Forward Voltage (1) (I_F = 200 A)			V_F	—	1.4	2.0	V
Reverse Recovery Time (d_i/d_t = 25 A/μs, I_F = 200 A)			t_{rr}	—	2.5	8.0	μs
Forward Turn-On Time (Compliance Voltage = 250 V, I_F = 100 A)			t_{on}	—	1.0	3.5	μs
Single Cycle Surge Current (f = 60 Hz)			I_{FSM}	—	—	500	A

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

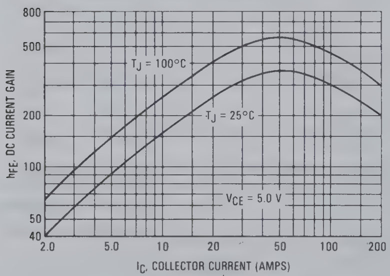


FIGURE 2 — DC CURRENT GAIN

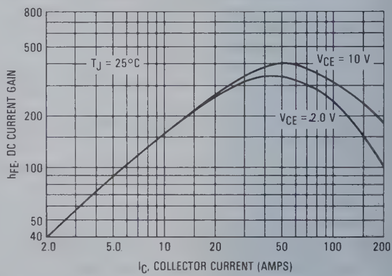


FIGURE 3 — DC CURRENT GAIN

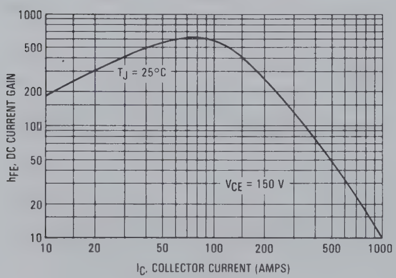
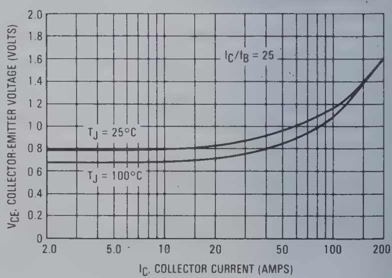


FIGURE 4 — COLLECTOR SATURATION REGION



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 5 — BASE-EMITTER SATURATION VOLTAGE

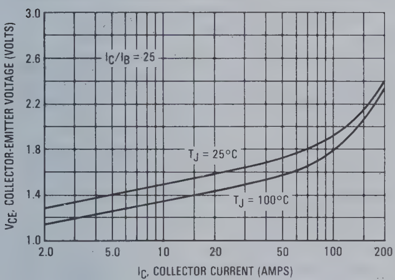
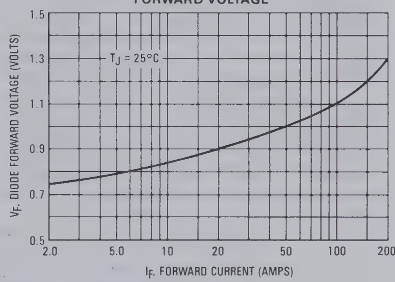


FIGURE 6 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

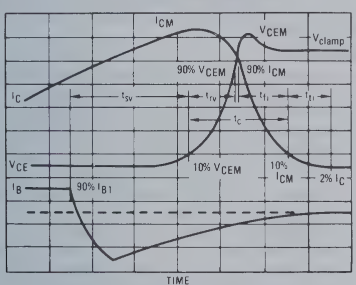


FIGURE 8 — TYPICAL INDUCTIVE SWITCHING TIMES

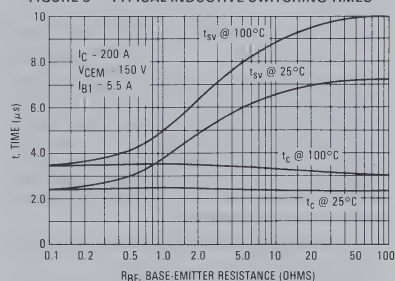


FIGURE 9 — TYPICAL TURN-ON SWITCHING TIMES

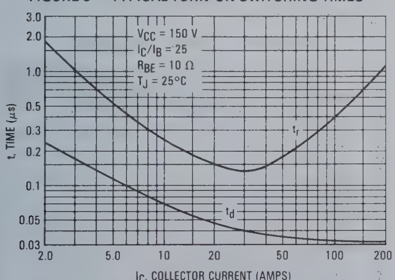
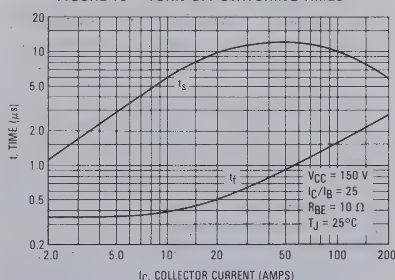
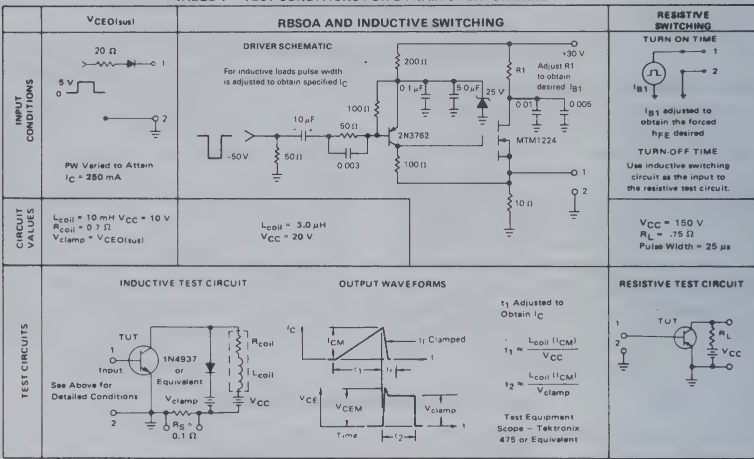


FIGURE 10 — TURN-OFF SWITCHING TIMES



1.3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust — V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

SWITCHING TIMES NOTE

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t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 11 — TYPICAL PEAK REVERSE BASE CURRENT

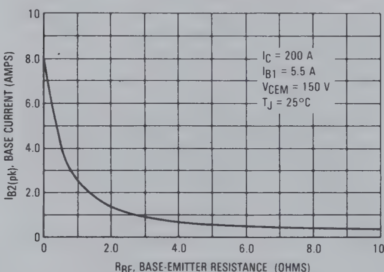
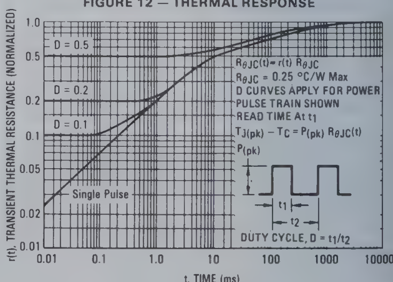


FIGURE 12 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

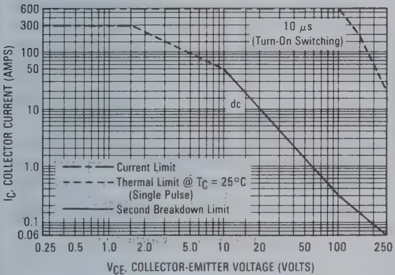


FIGURE 14 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)

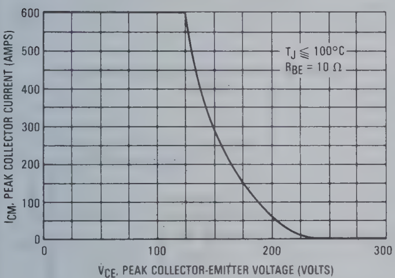
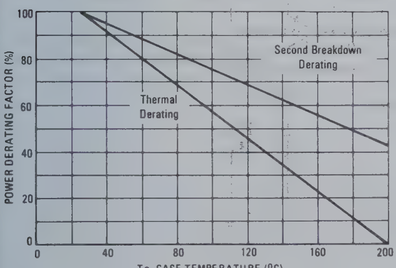


FIGURE 15 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in Figure 13 adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figure 16 depicts the Type I OLSOA rating for the MJ10200. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known,

(continued on back page)

1.3

OVERLOAD CHARACTERISTICS

FIGURE 16 — RATED OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

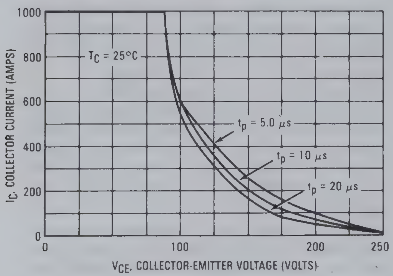


FIGURE 17 — RATED OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)

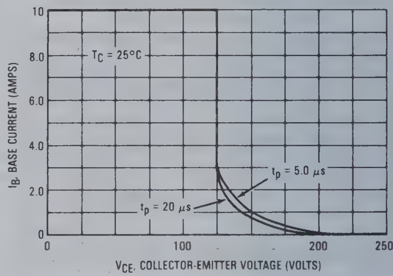


FIGURE 18 — OVERLOAD SOA TEST CIRCUIT TYPE I

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

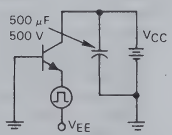
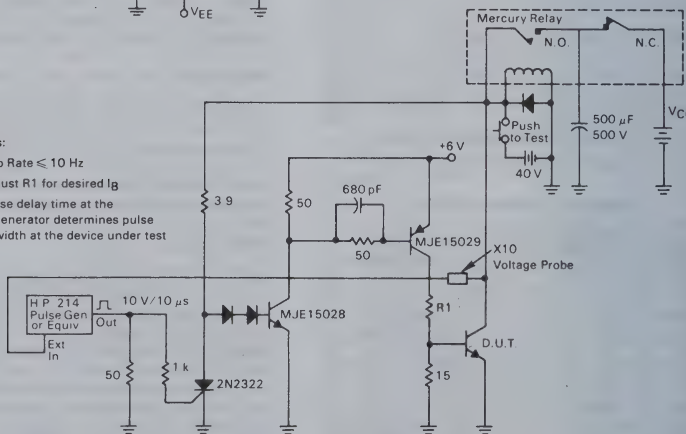


FIGURE 19 — OVERLOAD SOA TEST CIRCUIT TYPE II

Notes:

- Rep Rate ⩽ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test



SAFE OPERATING AREA INFORMATION (continued)

TYPE I OLSOA (continued)

Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figure 17, is measured in the circuit shown in Figure 19, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NONREPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for the MJ10200 is 100 occurrences. Another factor is the form of turn-off bias. For the MJ10200, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

MJ10201
MJ10202

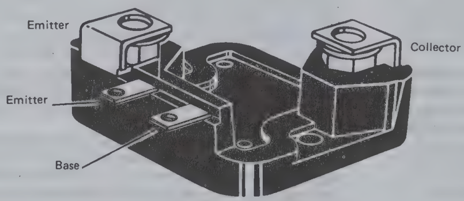
MOTOROLA

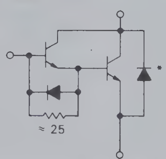
1.3

Designer's Data Sheet

50 KVA HIGH SPEED SWITCHMODE TRANSISTOR
200-Ampere Operating Current

The MJ10201 Darlington transistor is designed for industrial service under practical operating environments requiring fast switching speed for highly efficient systems operating at high frequency such as inverters, PWM controllers and other high frequency system operating from 120 V lines or batteries.



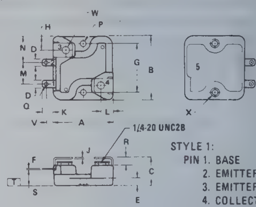


*Emitter-Collector Diode is a fast recovery, high power diode.

200 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
200 and 250 VOLTS
500 WATTS

Designer's Data for "Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.



STYLE 1:
PIN 1. BASE
2. EMITTER
3. EMITTER
4. COLLECTOR
5. COLLECTOR

NOTES:
1. DIMENSION A AND B ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
⌖ | ⌀ 0.36 (0.014) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	53.09	53.84	2.090	2.120
B	55.37	56.39	2.180	2.220
C	–	26.67	–	1.050
D	6.10	6.60	0.240	0.260
E	6.60	7.11	0.260	0.280
F	0.71	0.81	0.028	0.032
G	43.31 BSC		1.705 BSC	
H	12.57	12.82	0.495	0.505
J	1.52	1.62	0.060	0.064
K	9.50	9.75	0.374	0.384
L	10.21	10.46	0.402	0.412
M	18.92	19.18	0.745	0.755
N	23.67	23.93	0.932	0.942
P	5.08	5.21	0.200	0.205
Q	3.53	3.78	0.139	0.149
R	6.76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5.33	5.84	0.210	0.230
W	6.40	6.65	0.252	0.262
X	7.37	7.87	0.290	0.310

CASE 346-01

MAXIMUM RATINGS

Mechanical Ratings

Rating	Value	Unit
Mounting Torque (To heat sink with 10-32 Screw) (Note 1)	20	in.-lb
Lead Torque (Lead to bus with 1/4-20 Screw) (Note 2)	20	in.-lb
Per Unit Weight	120	grams

THERMAL CHARACTERISTICS

Characteristic	Value	Unit
Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.25	°C/W

Mica Insulators available as separate items.
0.003″ thick. Motorola Part Number B12387B001.
0.006″ thick. Motorola Part Number B12387B002.

Notes:
1. A Belleville washer of 0.472″ O.D., 0.205″ I.D., 0.024″ thick and 150 pounds flat is recommended such as P/N AM125206 available from National Disc Spring Div., 385 Hillside Ave., Hillside N.J. 07205.
2. The lead torque should be limited to 20 in.-lb, unsupported to prevent rotation of the terminal in the package. The torque may be increased to 50 in.-lb if support is used to prevent rotation. The maximum penetration of the screw should be limited to 0.75″.

MAXIMUM RATINGS (Continued)

Electrical Ratings			
Rating	**Symbol**	**Value**	**Unit**
Collector-Emitter Voltage MJ10201 MJ10202	V_{CEO}	250 200	Vdc
Collector-Emitter Voltage (R_{BE} = 10 Ohms)	V_{CER}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Operating, $T_C = 50°C$ — Continuous, $T_C = 25°C$ — Peak Repetitive, $T_C = 25°C$ — Peak Nonrepetitive, $T_C = 25°C$	I_C	200 300 600 1000	A
Base Current — Continuous — Peak Nonrepetitive	I_B	50 100	A
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C For 1-minute overload	P_D	500 4.0 667	Watts W/°C Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}	-55 to +150 -55 to +200	°C

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) MJ10201 (I_C = 250 mAdc, I_B = 0) MJ10202	$V_{CEO(sus)}$	250 200	—	—	Vdc
Collector Cutoff Current (V_{CE} = 500 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 500 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150°C$)	I_{CEV}	 — —	 — —	 2.0 10	mAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	—	5.0	mAdc
SAFE OPERATING AREA					
Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figure 13			
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figure 14			
Overload SOA	OLSOA	See Figures 16 and 17			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 200 Adc, V_{CE} = 5.0 Vdc) (I_C = 200 A, V_{CE} = 10 V)	h_{FE}	 75 90	 — —	 — —	
Collector-Emitter Saturation Voltage (I_C = 200 Adc, I_B = 5.5 A) (I_C = 200 Adc, I_B = 5.5 A, $T_C = 100°C$)	$V_{CE(sat)}$	 — —	 — —	 2.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 200 Adc, I_B = 5.5 Adc) (I_C = 200 Adc, I_B = 5.5 Adc, $T_C = 100°C$)	$V_{BE(sat)}$	 — —	 — —	 3.5 3.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	4000	pF

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤2.0%.

1.3

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
Resistive Load							
Delay Time	(V_{CC} = 150 Vdc, I_C = 200 A, I_{B1} = 5.5 A, t_p = 50 μs, $V_{BE(off)}$ = 5.0 V, Duty Cycle ≤ 2.0%)		t_d	—	0.035	0.25	μs
Rise Time			t_r	—	1.2	4.0	μs
Storage Time			t_s	—	1.4	4.0	μs
Fall Time			t_f	—	0.25	1.0	μs
Inductive Load, Clamped							
Storage Time	(I_{CM} = 200 A, V_{CEM} = 150 V, I_{B1} = 5.5 A, I_{B2} = 5.5 A)	T_J = 100°C	t_{sv}	—	2.8	8.0	μs
Crossover Time			t_c	—	1.4	4.0	μs
Storage Time		T_J = 25°C	t_{sv}	—	2.2	6.5	μs
Crossover Time			t_c	—	1.0	3.0	μs
C-E DIODE CHARACTERISTICS							
Power Dissipation (I_B = 0)			P_D	—	—	250	W
Forward Voltage (1) (I_F = 200 A)			V_F	—	2.5	5.0	V
Reverse Recovery Time (d_i/d_t = 25 A/μs, I_F = 200 A)			t_{rr}	—	0.4	1.0	μs
Forward Turn-On Time (Compliance Voltage = 200 V, I_F = 100 A)			t_{on}	—	0.4	1.0	μs
Single Cycle Surge Current (f = 60 Hz)			I_{FSM}	—	—	500	A
Reverse Recovery Current (I_F = 200 A, di/dt = 200 A/μs)			$I_{RM(REC)}$	—	50	100	A

(1) Pulse Test. Pulse width ≤ 300 μs, duty cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

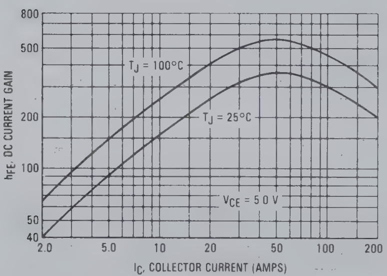


FIGURE 2 — DC CURRENT GAIN

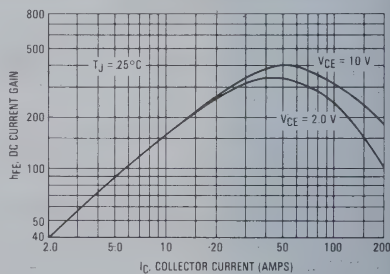


FIGURE 3 — DC CURRENT GAIN

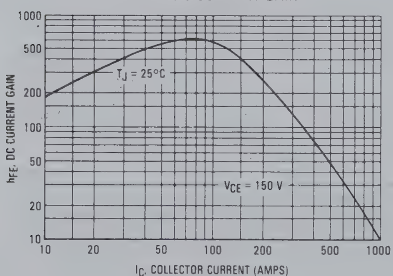
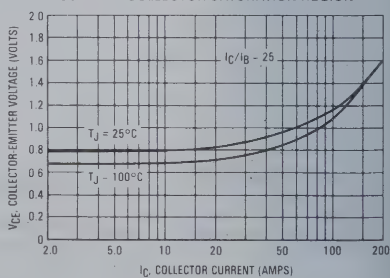


FIGURE 4 — COLLECTOR SATURATION REGION



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 5 — BASE-EMITTER SATURATION VOLTAGE

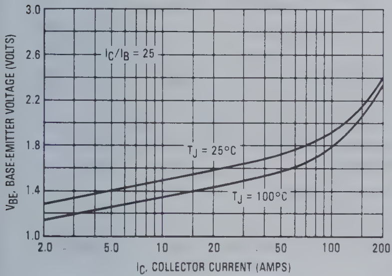
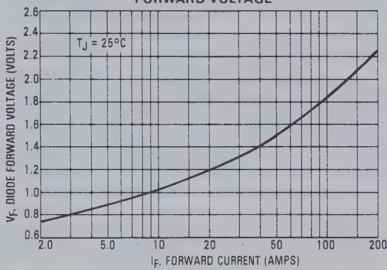


FIGURE 6 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE



TYPICAL SWITCHING CHARACTERISTICS

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

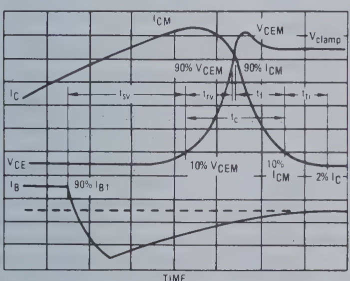


FIGURE 8 — INDUCTIVE SWITCHING TIMES

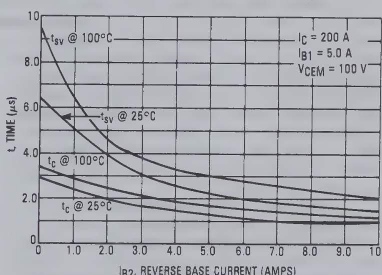


FIGURE 9 — TYPICAL TURN-ON SWITCHING TIMES

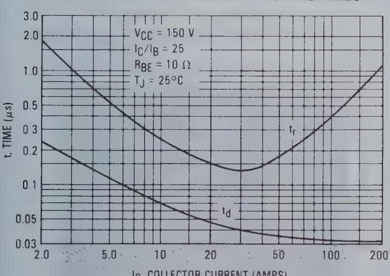
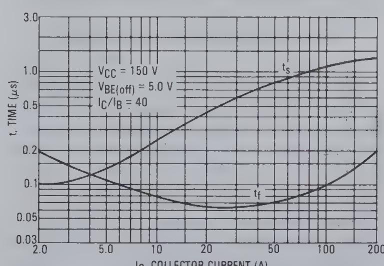
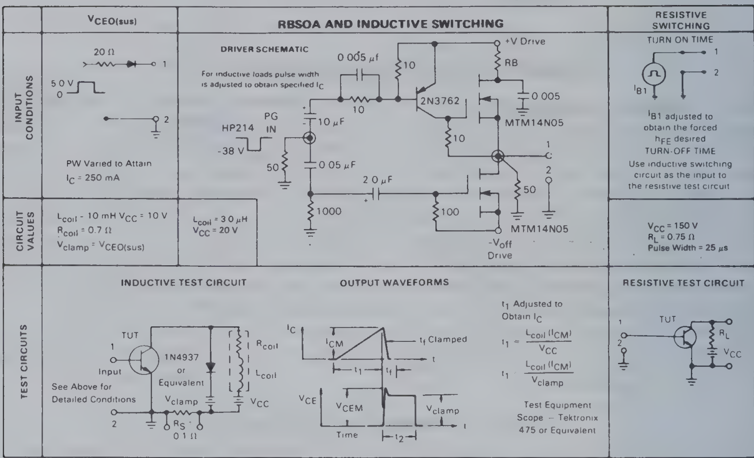


FIGURE 10 — TURN-OFF SWITCHING TIMES



1.3

TABLE 1 — RBSOA AND INDUCTIVE SWITCHING DRIVER SCHEMATIC



*Adjust — V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 11 — PEAK REVERSE BASE CURRENT

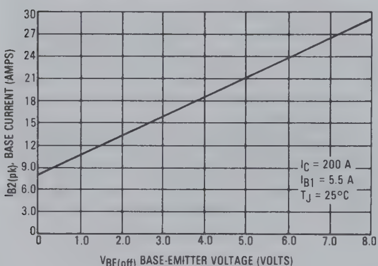
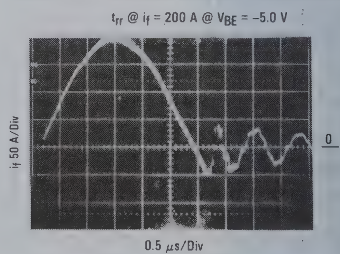


FIGURE 12 — REVERSE RECOVERY WAVEFORM



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

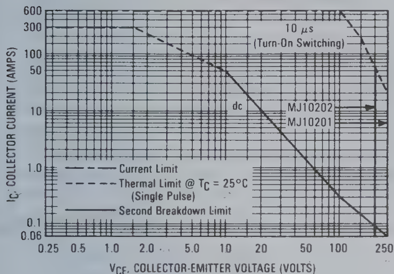


FIGURE 14 — MAXIMUM RATED REVERSE BIAS SAFE OPEATING AREA (RBSOA)

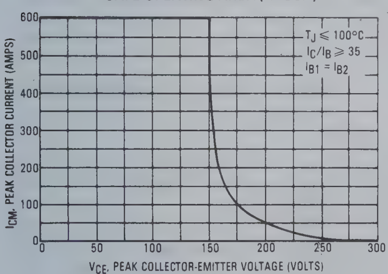
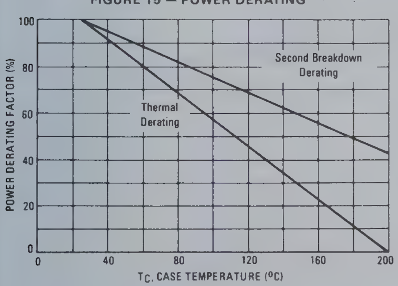


FIGURE 15 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 20. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in Figure 13 adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figure 16 depicts the Type I OLSOA rating for the devices. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known,

(continued on back page)

1.3

OVERLOAD CHARACTERISTICS

FIGURE 16 — RATED OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

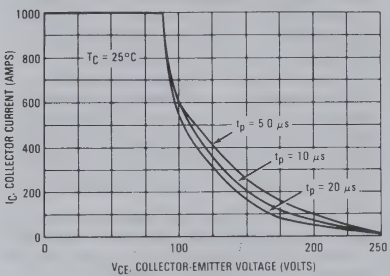


FIGURE 17 — RATED OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)

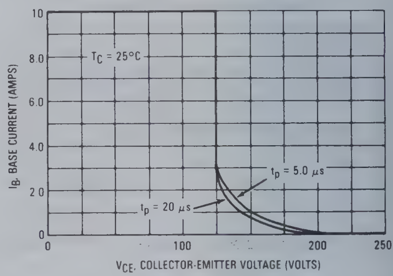


FIGURE 18 — OVERLOAD SOA TEST CIRCUIT TYPE I

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

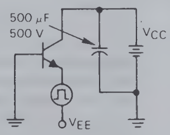
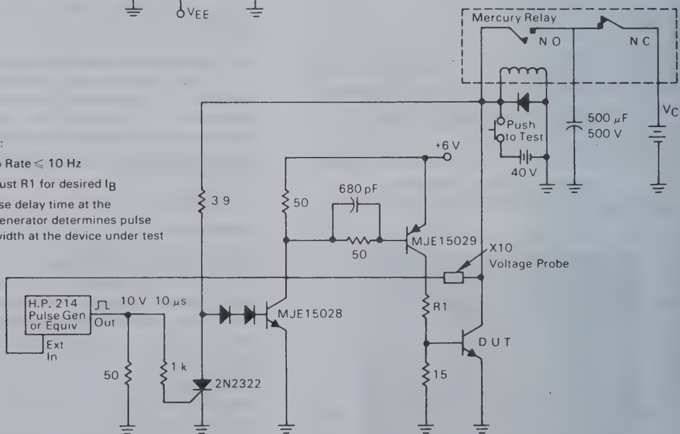


FIGURE 19 — OVERLOAD SOA TEST CIRCUIT TYPE II

Notes:

- Rep Rate ≤ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test



SAFE OPERATING AREA INFORMATION (continued)

TYPE I OLSOA (continued)

Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

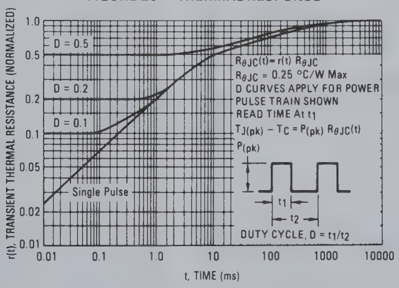
Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figure 17, is measured in the circuit shown in Figure 19, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NONREPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for the devices are 100 occurrences. Another factor is the form of turn-off bias. For the devices, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

FIGURE 20 — THERMAL RESPONSE



PNP

MJ11011, MJ11013, MJ11015

NPN

MJ11012, MJ11014, MJ11016

1.3

MOTOROLA

HIGH-CURRENT COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – h_{FE} = 1000 (Min) @ I_C = 20 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor
- Junction Temperature to +200°C

30 AMPERE

DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

60-120 VOLTS
200 WATTS

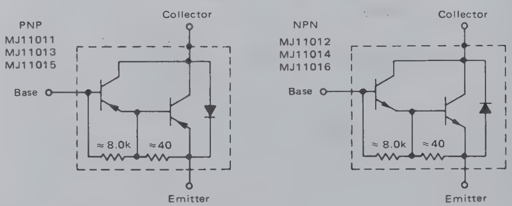
MAXIMUM RATINGS

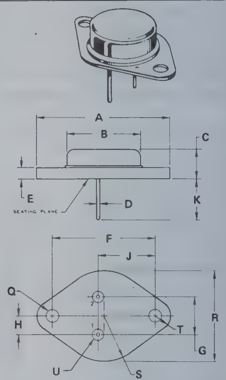
Rating	Symbol	MJ11011 MJ11012	MJ11013 MJ11014	MJ11015 MJ11016	Unit
Collector-Emitter Voltage	V_{CEO}	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector Current	I_C	30			Adc
Base Current	I_B	1			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C @ T_C = 100°C	P_D	200 1.15			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.87	°C/W
Maximum Lead Temperature for Soldering Purposes for ⩽ 10 Seconds.	T_L	275	°C

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE I–04

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1)		BV_{CEO}			Vdc
(I_C = 100 mAdc, I_B = 0)	MJ11011,MJ11012		60	–	
	MJ11013,MJ11014		90	–	
	MJ11015,MJ11016		120	–	
Collector Emitter Leakage Current		I_{CER}			mAdc
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm)	MJ11011,MJ11012		–	1	
(V_{CE} = 90 Vdc, R_{BE} = 1 k ohm)	MJ11013,MJ11014		–	1	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm)	MJ11015,MJ11016		–	1	
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11011,MJ11012		–	5	
(V_{CE} = 90 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11013,MJ11014		–	5	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11015,MJ11016		–	5	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	–	5	mAdc
Collector-Emitter Leakage Current (V_{CE} = 50 Vdc, I_B = 0)		I_{CEO}	–	1	mAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 20 Adc, V_{CE} = 5 Vdc)			1000	–	
(I_C = 30 Adc, V_{CE} = 5 Vdc)			200	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 200 mAdc)			–	3	
(I_C = 30 Adc, I_B = 300 mAdc)			–	4	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
I_C = 20 Adc, I_B = 200 mAdc)			–	3.5	
I_C = 30 Adc, I_B = 300 mAdc)			–	5	
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3 Vdc, f = 1 MHz)		$\|h_{fe}\|$	4	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 2 – DC CURRENT GAIN (1)

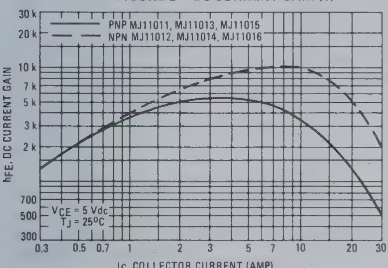


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

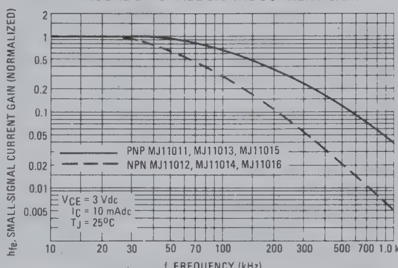


FIGURE 4 – "ON" VOLTAGES (1)

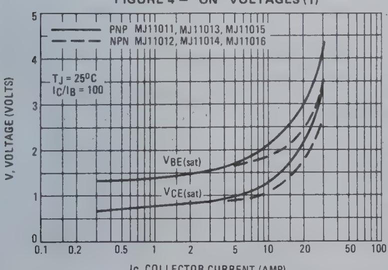
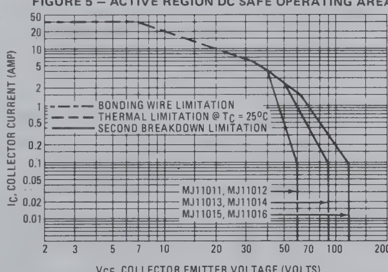


FIGURE 5 – ACTIVE REGION DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

PNP NPN
MJ11017 MJ11018
MJ11019 MJ11020
MJ11021 MJ11022

MOTOROLA

1.3

COMPLEMENTARY DARLINGTON SILICON POWER TRANSISTORS

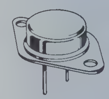
. . . designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High dc Current Gain @ 10 Adc — h_{FE} = 400 Min (All Types)
- Collector-Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 150 Vdc (Min) — MJ11018, 17
  = 200 Vdc (Min) — MJ11020, 19
  = 250 Vdc (Min) — MJ11022, 21
- Low Collector-Emitter Saturation
  $V_{CE(sat)}$ = 1.0 V (Typ) @ I_C = 5.0 A
  = 1.8 V (Typ) @ I_C = 10 A
- Monolithic Construction
- 100% SOA Tested @ V_{CE} = 44 V, I_C = 4.0 A, t = 250 ms.

15 AMPERE

DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

150, 200, 250 VOLTS
175 WATTS



MAXIMUM RATINGS

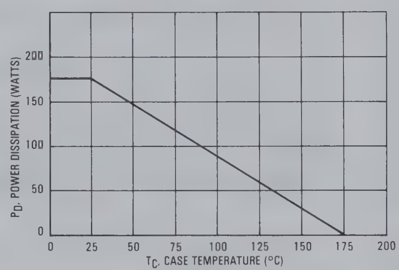
Rating	Symbol	MJ11018 MJ11017	MJ11020 MJ11019	MJ11022 MJ11021	Unit
Collector-Emitter Voltage	V_{CEO}	150	200	250	Vdc
Collector-Base Voltage	V_{CB}	150	200	250	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous Peak	I_C		15 30		Adc
Base Current	I_B		0.5		Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D		175 1.16		Watts W/°C
Operating and Storage Junction Temperature Range	T_J T_{stg}		−65 to +175 −65 to +200		°C °C

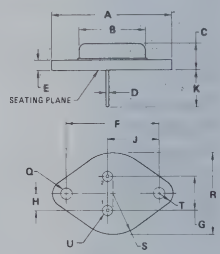
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.86	°C/W

(1) Pulse Test: Pulse Width 5.0 ms, Duty Cycle ≤ 10%

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1–04

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

ELECTRICAL CHARACTERISTICS (T_C = 25°C Unless Otherwise Noted)

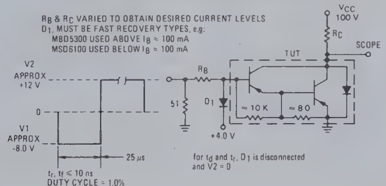
Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1)	$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0) MJ11017, MJ11018		150	—	
MJ11019, MJ11020		200	—	
MJ11021, MJ11022		250	—	
Collector Cutoff Current	I_{CEO}			mAdc
(V_{CE} = 75, I_B = 0) MJ11017, MJ11018		—	1.0	
(V_{CE} = 100, I_B = 0) MJ11019, MJ11020		—	1.0	
(V_{CE} = 125, I_B = 0) MJ11021, MJ11022		—	1.0	
Collector Cutoff Current	I_{CEV}			mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)		—	0.5	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_J = 150°C)		—	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			—
(I_C = 10 Adc, V_{CE} = 5.0 Vdc)		400	15,000	
(I_C = 15 Adc, V_{CE} = 5.0 Vdc)		100	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 100 mA)		—	2.0	
(I_C = 15 Adc, I_B = 150 mA)		—	3.4	
Base-Emitter On Voltage I_C = 10 A, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
Base-Emitter Saturation Voltage (I_C = 15 Adc, I_B = 150 mA)	$V_{BE(sat)}$	—	3.8	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common Emitter Small Signal Short Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$[h_{fe}]$	3.0	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}			pF
MJ11018, MJ11020, MJ11022		—	400	
MJ11017, MJ11019, MJ11021		—	600	
Small-Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz	h_{fe}	100	—	—

SWITCHING CHARACTERISTICS

Characteristics		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	(V_{CC} = 100 V, I_C = 10 A, I_B = 100 mA $V_{BE(off)}$ = 5.0 V) (See Figure 2.)	t_d	150	75	ns
Rise Time		t_r	1.2	0.5	μs
Storage Time		t_s	4.4	2.7	μs
Fall Time		t_f	10.0	2.5	μs

(1)Pulsed Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 — THERMAL RESPONSE

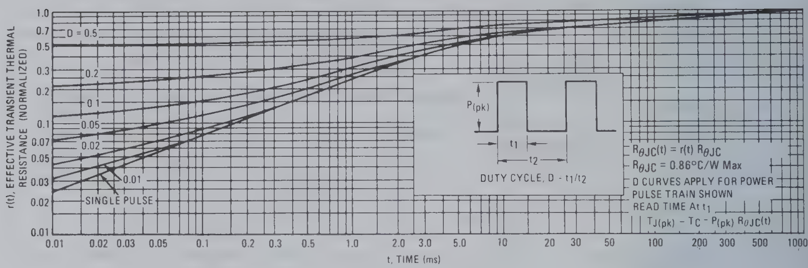


FIGURE 4 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (FBSOA)

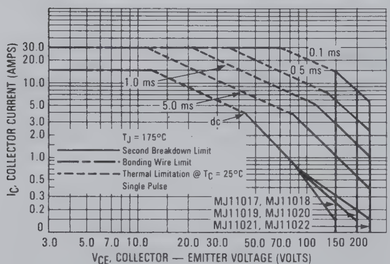
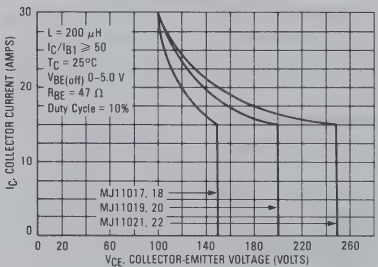


FIGURE 5 — MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 175°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 175°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives RBSOA characteristics.

FIGURE 6 — DC CURRENT GAIN

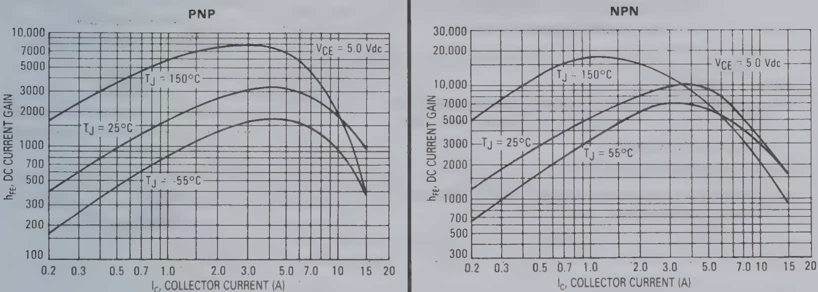


FIGURE 7 — COLLECTOR SATURATION REGION

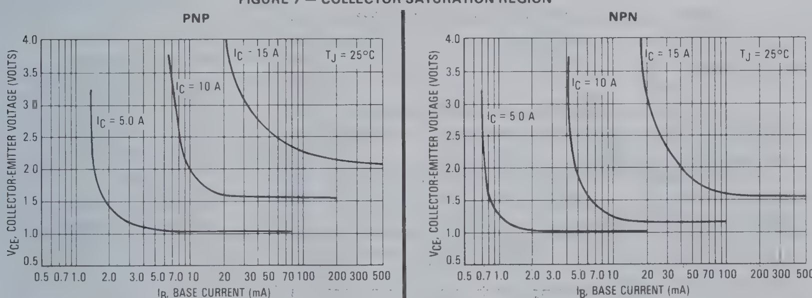
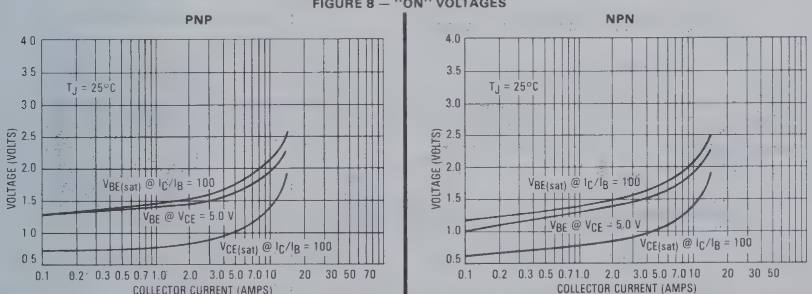


FIGURE 8 — "ON" VOLTAGES



NPN PNP

MJ11028 MJ11029
MJ11030 MJ11031
MJ11032 MJ11033

MOTOROLA

1.3

HIGH-CURRENT COMPLEMENTARY SILICON TRANSISTORS

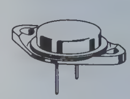
. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 1000 (Min) @ I_C = 25 Adc
  h_{FE} = 400 (Min) @ I_C = 50 Adc
- Curves to 100 A (Pulsed)
- Diode Protection to Rated I_C
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor
- Junction Temperature to +200°C

50 AMPERE

COMPLEMENTARY SILICON DARLINGTON POWER TRANSISTOR

60–120 VOLTS
300 WATTS

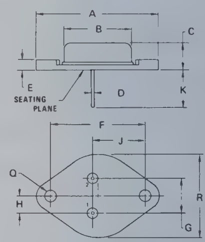


MAXIMUM RATINGS

Rating	Symbol	MJ11028 MJ11029	MJ11030 MJ11031	MJ11032 MJ11033	Unit
Collector-Emitter Voltage	V_{CEO}	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector Current—Continuous Peak	I_C I_{CM}	50 100			Adc
Base Current—Continuous	I_B	2			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C @ T_C = 100°C	P_D	300 1.71			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Maximum Lead Temperature for Soldering Purposes for ≤ 10 seconds	T_L	275	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.584	°C

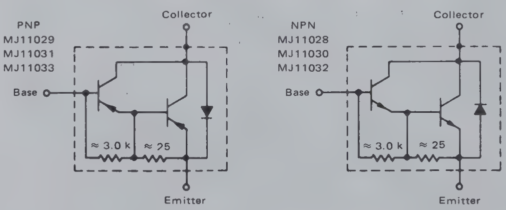


STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
(TO-3 Except Pin Diameter)

FIGURE 1 — DARLINGTON CIRCUIT SCHEMATIC

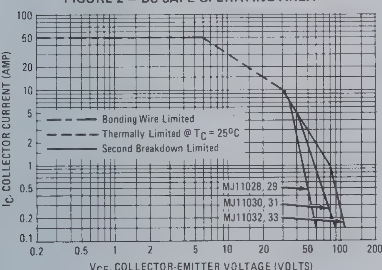


ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1)	BV_{CEO}			Vdc
(I_C = 100 mAdc, I_B = 0) MJ11028 MJ11029		60	–	
MJ11030 MJ11031		90	–	
MJ11032 MJ11033		120	–	
Collector-Emitter Leakage Current	I_{CER}			mAdc
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm) MJ11028 MJ11029		–	2	
(V_{CE} = 90 Vdc, R_{BE} = 1 k ohm) MJ11030 MJ11031		–	2	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm) MJ11032 MJ11033		–	2	
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm, T_C = 150°C) MJ11028 MJ11029		–	10	
(V_{CE} = 90 Vdc, R_{BE} = 1 k ohm, T_C = 150°C) MJ11030 MJ11031		–	10	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm, T_C = 150°C) MJ11032 MJ11033		–	10	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	–	5	mAdc
Collector-Emitter Leakage Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	–	2	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
(I_C = 25 Adc, V_{CE} = 5 Vdc)		1 k	18 k	
(I_C = 50 Adc, V_{CE} = 5 Vdc)		400	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 250 mAdc)		–	2.5	
(I_C = 50 Adc, I_B = 500 mAdc)		–	3.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 200 mAdc)		–	3.0	
(I_C = 50 Adc, I_B = 300 mAdc)		–	4.5	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 3 – DC CURRENT GAIN

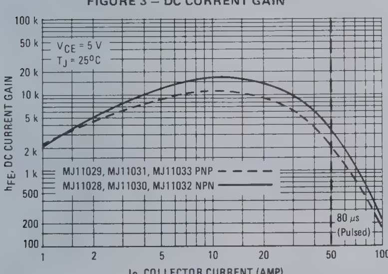
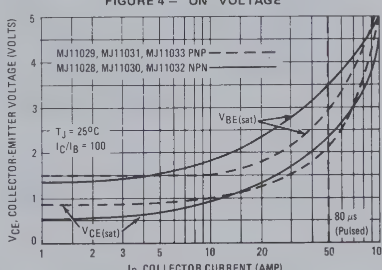


FIGURE 4 – "ON" VOLTAGE



MOTOROLA

1.3

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage —
  V_{CEX} = 1500 Volts
- Glassivated Base-Collector Junction
- Forward Bias Safe Operating Area @ 50 μs = 15 A, 300 V
- Switching Times with Inductive Loads —
  t_f = 0.65 μs (Typ) @ I_C = 2.0 A

2.5 AMPERE
NPN SILICON
POWER TRANSISTOR

1500 VOLTS
75 WATTS

Designer's Data for "Worst Case" Conditions

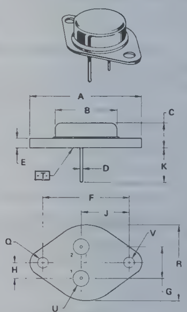
The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous	I_C	2.5	Adc
Base Current — Continuous	I_B	2.0	Adc
Emitter Current — Continuous	I_E	4.5	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	75 30 0.6	Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C



NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   | ⌖ | ⌀0.13 (0.005) Ⓜ | T | V Ⓜ |
   FOR LEADS.
   | ⌖ | ⌀0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37	–	1.550
B		21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

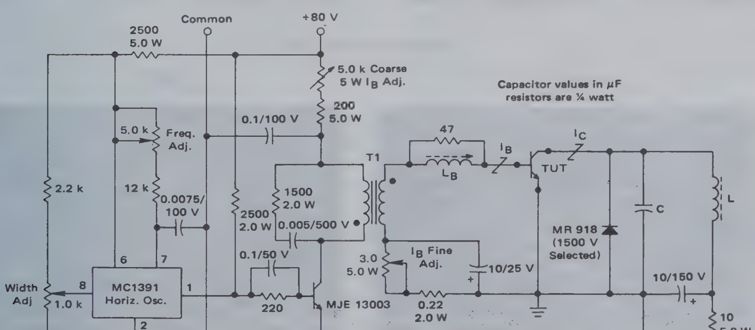
CASE 1-05

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.8 Adc)	$V_{CE(sat)}$	–	–	5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.8 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base-Forward Biased	$I_{S/B}$		See Figure 14		–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	50	–	pF
Current Gain — Bandwidth Product (1) (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	–	4.0	–	MHz
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 2.0 Adc, I_{B1} = 1.0 Adc, L_B = 12 μH, See Figure 1)	t_f	–	0.65	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 1 — TEST CIRCUIT



I_C	L	C
0.75 A	4.25 mH	.003 μF
1.5	2.18 mH	.006 μF
2.0	1.6 mH	.008 μF

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance — 39 mH. Secondary Inductance — 22 mH, Leakage Inductance with primary shorted — 2.0 μH, Primary 260 turns #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst case component variations and maximum high voltage loading must also be taken into account.

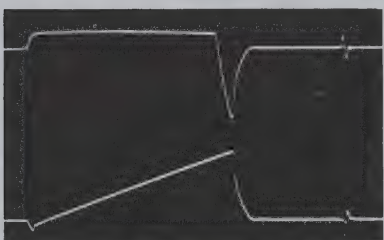
If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1}\ h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1}\ h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation $I_{B1}\ h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

TEST CIRCUIT WAVEFORMS

FIGURE 2

I_B

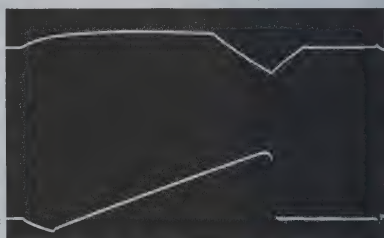


I_C

(time)

FIGURE 3

I_B



I_C

(time)

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 — OPTIMIZING DRIVE @ I_C = 0.75 A

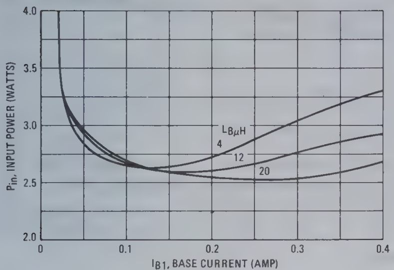


FIGURE 5 — OPTIMIZING DRIVE @ I_C = 1.5 A

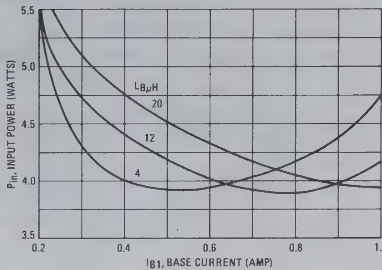


FIGURE 6 — OPTIMIZING DRIVE @ I_C = 2.0 A

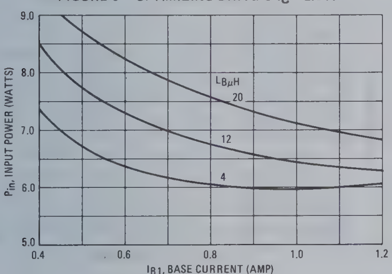


FIGURE 7 — SWITCHING BEHAVIOR versus TEMPERATURE

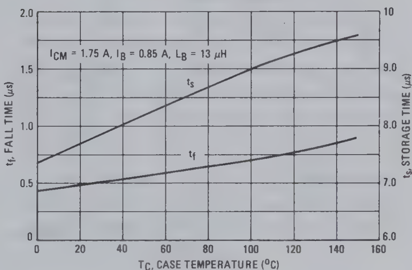


FIGURE 8 — OPTIMUM DRIVE CONDITIONS

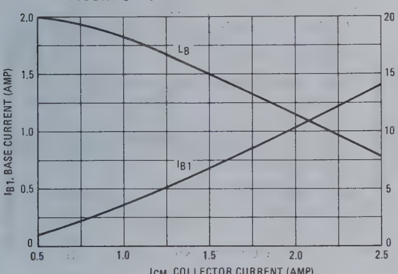


FIGURE 9 — SWITCHING BEHAVIOR versus I_{CM}

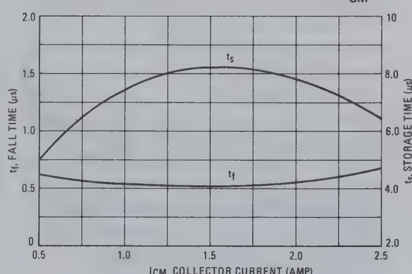


FIGURE 10 — THERMAL RESPONSE

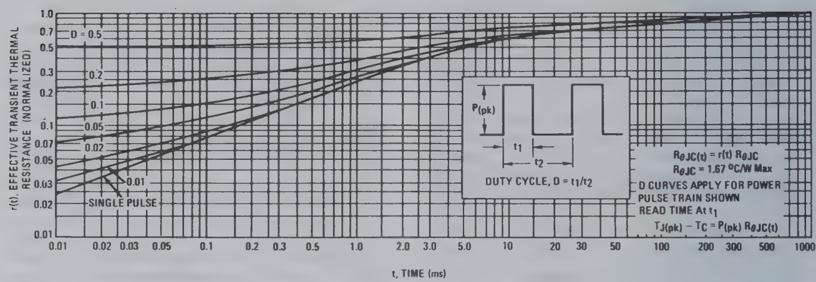


FIGURE 11 — COLLECTOR SATURATION REGION

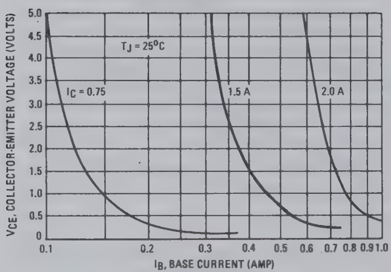


FIGURE 12 — DC CURRENT GAIN

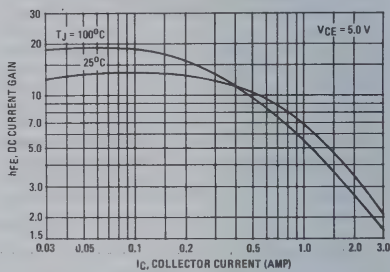


FIGURE 13 — "ON" VOLTAGES

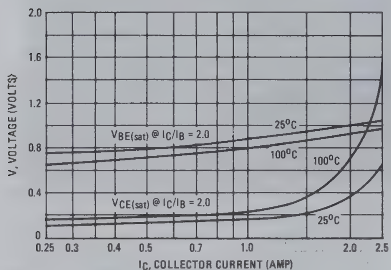
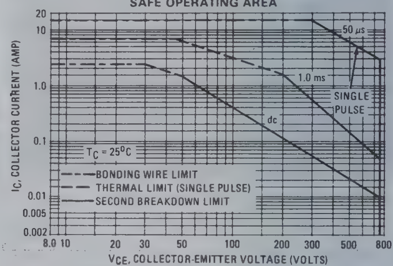


FIGURE 14-MAXIMUM FORWARD BIAS SAFE OPERATING AREA



NOTE:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 μs SB curve is beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

MOTOROLA

HORIZONTAL DEFLECTION TRANSISTOR

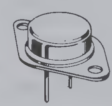
. . . specifically designed for use in CRT deflection circuits.

- Collector-Emitter Voltage — V_{CEX} = 1500 Volts
- Glassivated Base-Collector Junction
- Forward Bias Safe Operating Area @ 50 μs = 20 A, 300 V
- Switching Times with Inductive Loads —
  t_f = 0.5 μs (Typ) @ I_C = 3.0 A

4 AMPERE

NPN SILICON POWER TRANSISTOR

1500 VOLTS
100 WATTS

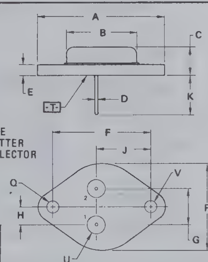


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector-Current – Continuous	I_C	4.0	Adc
Base Current — Continuous	I_B	3.0	Adc
Emitter Current — Continuous	I_E	7.0	Adc
Total Power Dissipation @ $T_C = 25^oC$ $T_C = 100^oC$ Derate above 25^oC	P_D	100 40 0.8	Watts Watts W/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^oC/W$
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	275	^oC



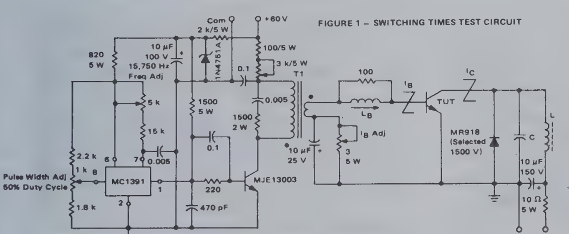
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
| ⌖ | ∅0.13 (0.005) Ⓜ | T | V Ⓜ |
FOR LEADS:
| ⌖ | ∅0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

FIGURE 1 — TEST CIRCUIT



I_C A	L mH	C μF
3.0	1.00	0.012

DRIVER TRANSFORMER (T1)
Motorola part number 25D68782A-05-1/4″ laminate "E" iron core. Primary Inductance — 39 mH, Secondary Inductance — 0.22 mH, Leakage Inductance with primary shorted — 2.0 μH. Primary 260 turns, #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 1.2 Adc)	$V_{CE(sat)}$	–	–	5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 1.2 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 5			–
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	–	4	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	90	–	pF
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 3.0 Adc, I_{B1} = 1.2 Adc, L_B = 8.0 μH, See Figure 1)	t_f	–	0.5	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 2 – DC CURRENT GAIN

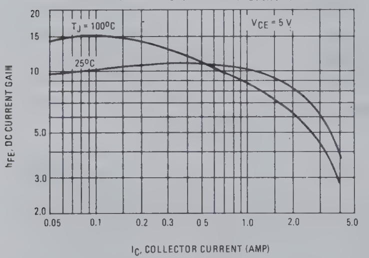


FIGURE 3 – COLLECTOR SATURATION REGION

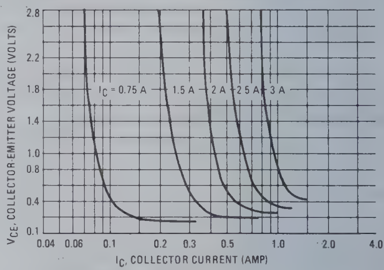


FIGURE 4 – "ON" VOLTAGES

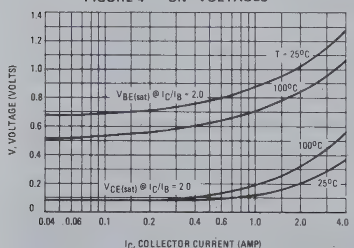
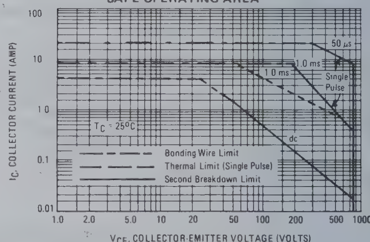


FIGURE 5 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA



NOTE:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 μs and 1 ms curves are beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

MOTOROLA

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage — V_{CEX} = 1500 Vdc
- Glassivated Base-Collector Junction
- Safe Operating Area @ 50 μs = 20 A, 400 V
- Switching Times with Inductive Loads — t_f = 0.4 μs (Typ) @ I_C = 4.5 A

5.0 AMPERE

NPN SILICON POWER TRANSISTORS

1500 VOLTS
100 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJ12004 MJH12004	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	5.0	Adc
Base Current — Continuous	I_B	4.0	Adc
Emitter Current — Continuous	I_E	9.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	100 40 0.8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

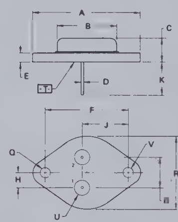
THERMAL CHARACTERISTICS

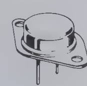
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

MJ12004





PIN 1 BASE
2 EMITTER
CASE COLLECTOR

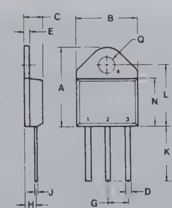
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	-	39.37	-	1.550
B		21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R		26.67		1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

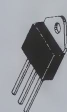
NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. T IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
   ⌖ | ⌀ 13 (0.005) Ⓜ | T | V Ⓜ

   FOR LEADS
   ⌖ | ⌀ 13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

CASE 1-05
TO-204AA
(Formerly TO-3)

MJH12004





1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

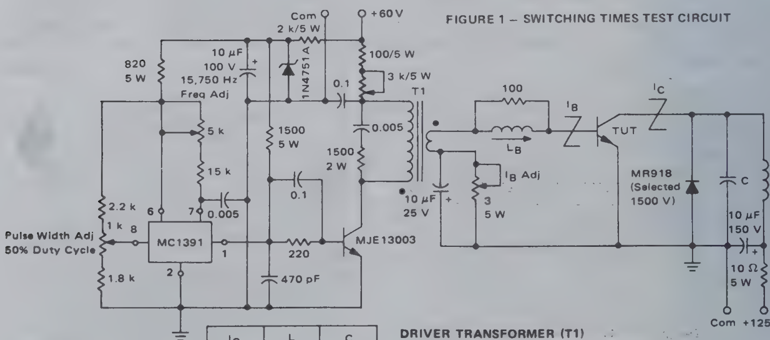
1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^o$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 1.8 Adc) (I_C = 3.5 Adc, I_B = 1.5 Adc)	$V_{CE(sat)}$	– –	– –	5.0 5.0	Vdc
Base Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 1.8 Adc) (I_C = 3.5 Adc, I_B = 1.5 Adc)	$V_{BE(sat)}$	– –	– –	1.5 1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14			
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1 MHz)	f_T	–	4	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	125	–	pF
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 4.5 Adc, I_{B1} = 1.8 Adc, L_B = 8.0 μH, See Figure 1) $T_C = 25^oC$ $T_C = 100^oC$	t_f	– –	0.4 0.6	1.0 –	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



I_C A	L mH	C μF
3.5	0.87	0.013
4.5	0.67	0.017

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance — 39 mH, Secondary Inductance — 0.22 mH, Leakage Inductance with primary shorted — 2.0 μH. Primary 260 turns, #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

BASE DRIVE: The Key to Performance

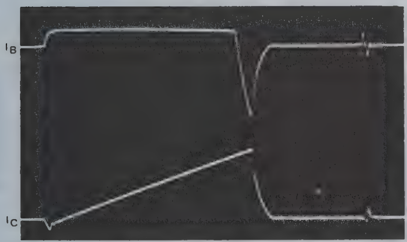
By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1}\ h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1}\ h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor *initiation* of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation $I_{B1}\ h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

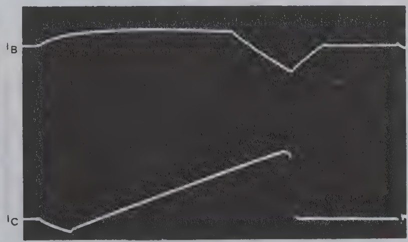
TEST CIRCUIT WAVEFORMS

FIGURE 2



(time)

FIGURE 3



(time)

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 — OPTIMIZING DRIVE @ 3.5 A

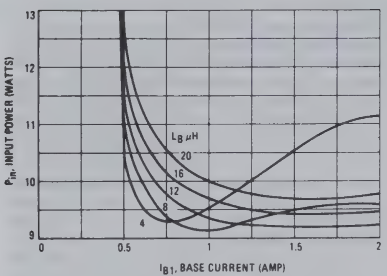


FIGURE 5 — OPTIMIZING DRIVE @ 4.5 A

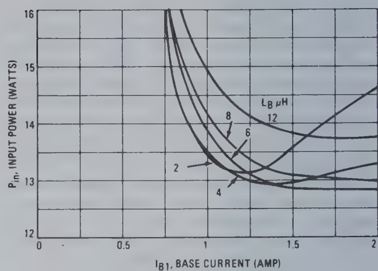


FIGURE 6 — SWITCHING BEHAVIOR versus TEMPERATURE

I_{CM} = 3.5 A, I_B = 1.5 A, L_B = 14 μH

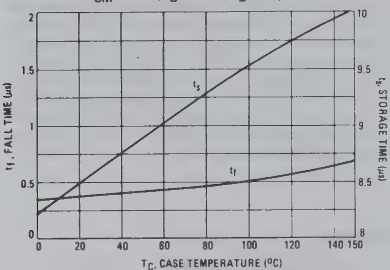


FIGURE 7 — SWITCHING BEHAVIOR versus TEMPERATURE

I_{CM} = 4.5 A, I_B = 1.75 A, L_B = 8 μH

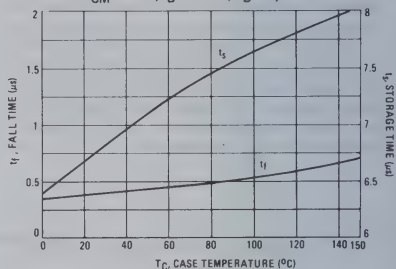


FIGURE 8 — OPTIMUM DRIVE CONDITIONS

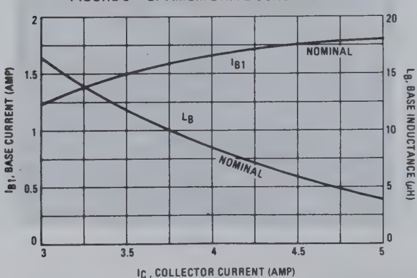
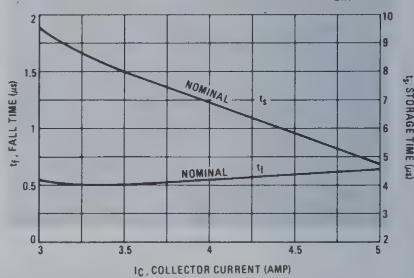


FIGURE 9 — SWITCHING BEHAVIOR versus I_{CM}



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 10 — DC CURRENT GAIN

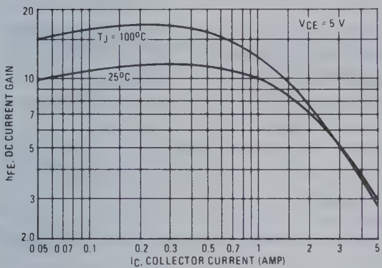
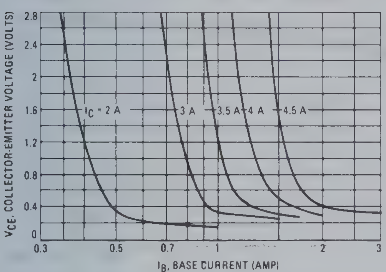
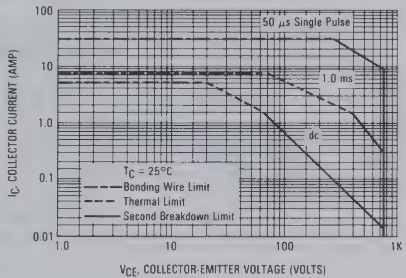


FIGURE 12 — COLLECTOR SATURATION REGION



SAFE OPERATING AREA INFORMATION

FIGURE 11 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

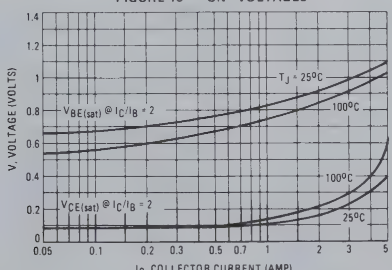


NOTE:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 μs SB curve is beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

FIGURE 13 – "ON" VOLTAGES



1.3

THERMAL RESPONSE

FIGURE 14 — MJ12004

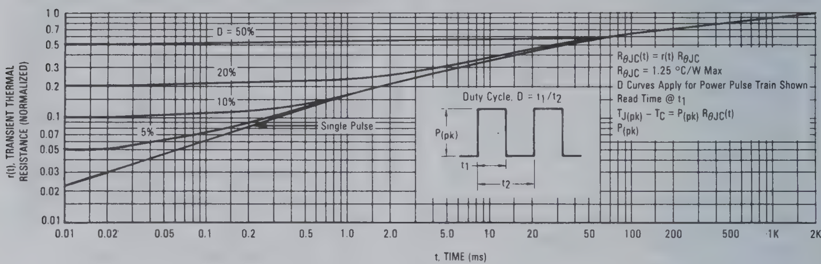
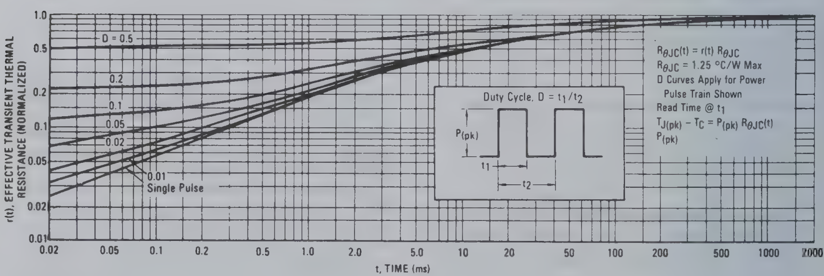


FIGURE 15 — MJH12004



MJ12005

MOTOROLA

1.3

HORIZONTAL DEFLECTION TRANSISTOR

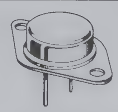
. . . specifically designed for use in deflection circuits.

- V_{CEX} = 1500 V
- Glassivated Base-Collector Junction
- Safe Operating Area @ 50 μs = 20 A, 400 V

8 AMPERE

NPN SILICON POWER TRANSISTOR

1500 VOLTS
100 WATTS

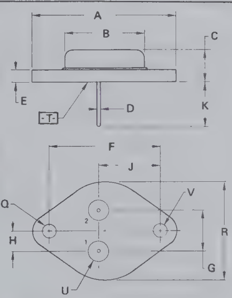


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
Base Current — Continuous	I_B	4.0	Adc
Emitter Current — Continuous	I_E	12	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	100 0.8	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to + 150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	^oC



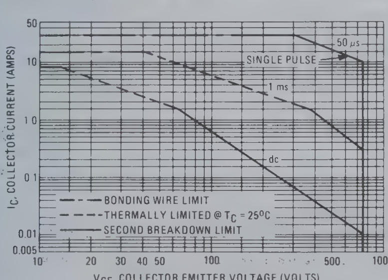
NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ϕ.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ϕ.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

FIGURE 1 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (V_C = 50 mAdc, I_B = 0)	$V_{CEO sus)}$	750	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	–	–	0.25	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	–	–	5.0	Vdc
Base Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	–	–	See Figure 1	
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 5.0 Adc, I_{B1} = 1.0 Adc, L_B = 8.0 μH)	t_f	–	0.4	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 2 – DC CURRENT GAIN

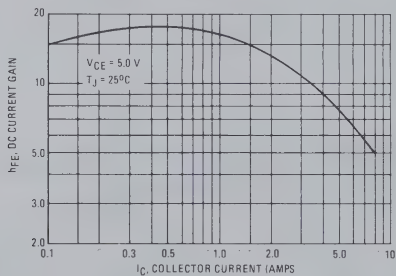
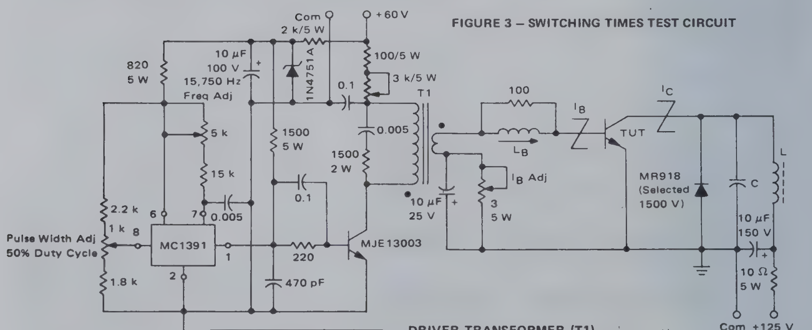


FIGURE 3 – SWITCHING TIMES TEST CIRCUIT



I_C A	L mH	C μF
5.0	0.575	0.018

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance – 39 mH, Secondary Inductance – 0.22 mH, Leakage Inductance with primary shorted – 2.0 μH. Primary 260 turns, #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

MOTOROLA

HORIZONTAL DEFLECTION TRANSISTOR

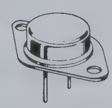
. . . specifically designed for use in CRT deflection circuits.

- Collector-Emitter Voltage — V_{CEX} = 950 Volts
- Glassivated Base-Collector Junction
- Forward Bias Safe Operating Area @ 50 μs = 30 A, 300 V
- Switching Times with Inductive Loads — t_f = 0.5 μs (Typ) @ I_C = 5.0 A

10 AMPERE

NPN SILICON POWER TRANSISTOR

950 VOLTS
100 WATTS

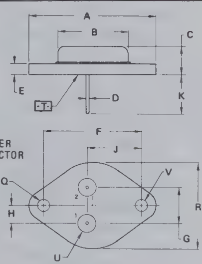


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	V_{CEX}	950	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector-Current — Continuous	I_C	10	Adc
Base Current — Continuous	I_B	5.0	Adc
Emitter Current — Continuous	I_E	15	Adc
Total Power Dissipation @ T_C = 25°C T_C = 100°C Derate above 25°C	P_D	100 40 0.8	Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C



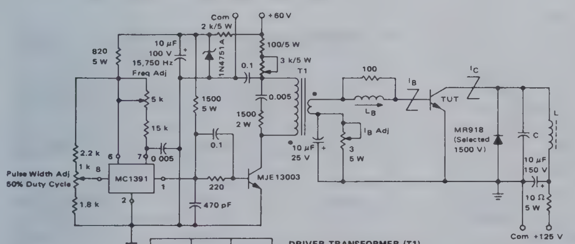
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	-	39.37		1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

FIGURE 1 — TEST CIRCUIT



I_C A	L mH	C μF
5 0	0 57	0 039

DRIVER TRANSFORMER (T1)
Motorola part number 25D68782A-05-1/4″ laminate "E" iron core. Primary Inductance — 39 mH, Secondary Inductance — 0.22 mH, Leakage Inductance with primary shorted — 2.0 μH. Primary 260 turns, #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	400	–	–	Vdc
Collector Cutoff Current (V_{CE} = 950 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.2 Adc)	$V_{CE(sat)}$	–	–	5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.2 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 5			–
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	–	6.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	150	–	pF
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 5.0 Adc, I_{B1} = 1.2 Adc, L_B = 8.0 μH, See Figure 1)	t_f	–	0.5	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 2 – DC CURRENT GAIN

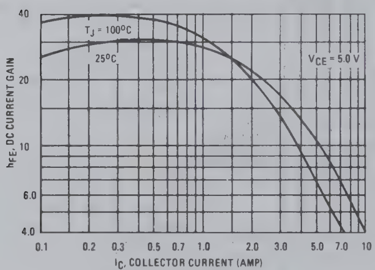


FIGURE 3 – COLLECTOR SATURATION REGION

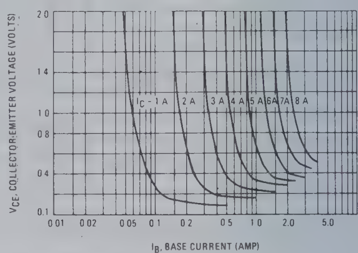


FIGURE 4 – "ON" VOLTAGES

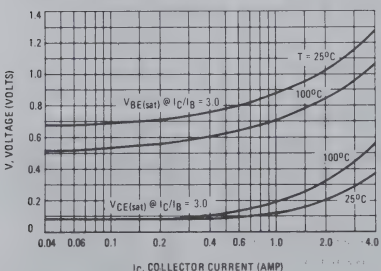
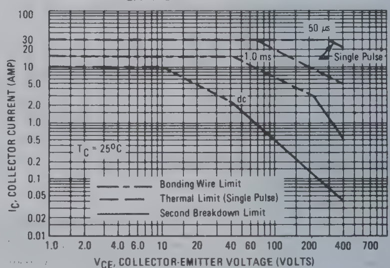


FIGURE 5 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA



NOTE.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 μs and 1 ms curves are beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

MJ12020
MJ12021
MJ12022

MOTOROLA

1.3

Designer's Data Sheet

HIGH PERFORMANCE NPN DEFLECTION TRANSISTORS

These transistors are designed for high resolution video systems, such as, high density graphic displays, data terminals, video scanners . . . wherever high frequency deflection is required.

- Fast Turn-Off Times
- Maximum Storage and Fall Times Specified at 100°C
- Operating Junction Temperature Range –65°C to +200°C
- High f_T of 15 MHz

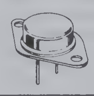
5.0, 8.0 and 15 AMPERE

NPN SILICON DEFLECTION POWER TRANSISTORS

850 VOLTS
125, 150 and 175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



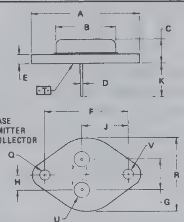
MAXIMUM RATINGS

Rating	Symbol	MJ12020	MJ12021	MJ12022	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450			Vdc
Collector-Emitter Voltage	V_{CEV}	850			Vdc
Emitter Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 10	8.0 16	15 20	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4.0 8.0	6.0 12	10 15	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	 125 71.5 0.714	 150 85.5 0.86	 175 100 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200			°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJ12020	MJ12021	MJ12022	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	1.17	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275			°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	∅.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	∅.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA (TO-3)

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)		$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	 — —	 — —	 0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figures 19, 21 or 23			
Turn-Off SOA with Base Reverse Biased		RBSOA	See Figures 20, 22 or 24			
ON CHARACTERISTICS (1)						
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)	 MJ12020 MJ12021 MJ12022	$V_{CE(sat)}$	 — — —	 — — —	 1.2 1.2 1.2	Vdc
Base Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)	 MJ12020 MJ12021 MJ12022	$V_{BE(sat)}$	 — — —	 — — —	 1.5 1.5 1.5	Vdc
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)	 MJ12020 MJ12021 MJ12022	h_{FE}	 5.0 5.0 5.0	 — — —	 — — —	—
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth Product (I_C = 0.3 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz) (I_C = 1.3 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	 MJ12020 MJ12021 MJ12022	f_T	 15 15 15	 — — —	 — — —	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 kHz)	 MJ12020 MJ12021 MJ12022	C_{ob}	 — — —	 — — —	 200 350 400	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
MJ12020							
Inductive Switching, Clamped Drive							
Storage Time	(I_C = 3.0 Adc, I_B = 0.6 Adc, V_{CC} = 40 Vdc, $V_{BE(off)}$ = 4.0 Vdc, Pulse Width = 8.0 μs, Duty Cycle ⩽ 2%) See Table 1	T_J = 25°C	t_s	—	440	1200	ns
Fall Time			t_f	—	130	300	
Storage Time		T_J = 100°C	t_s	—	550	1500	
Fall Time			t_f	—	200	500	
Inductive Switching, Series Base Inductance							
Fall Time (I_C = 3.0 Adc, I_B = 0.6 Adc, L_B = 24 μH) See Table 2			t_f	—	175	—	ns
MJ12021							
Inductive Switching, Clamped Drive							
Storage Time	(I_C = 5.0 Adc, I_B = 1.0 Adc, V_{CC} = 60 Vdc, $V_{BE(off)}$ = 4.0 Vdc, Pulse Width = 8.0 μs, Duty Cycle ⩽ 2%) See Table 1	T_J = 25°C	t_s	—	550	1200	ns
Fall Time			t_f	—	100	300	
Storage Time		T_J = 100°C	t_s	—	750	1600	
Fall Time			t_f	—	180	500	
Inductive Switching, Series Base Inductance							
Fall Time (I_C = 5.0 Adc, I_B = 1.0 Adc, L_B = 24 μH) See Table 2			t_f	—	300	—	ns
MJ12022							
Inductive Switching, Clamped Drive							
Storage Time	(I_C = 10 Adc, I_B = 2.0 Adc, V_{CC} = 120 Vdc, $V_{BE(off)}$ = 4.0 Vdc, Pulse Width = 8.0 μs, Duty Cycle ⩽ 2%) See Table 1	T_J = 25°C	t_s	—	820	1800	ns
Fall Time			t_f	—	100	300	
Storage Time		T_J = 100°C	t_s	—	1100	2500	
Fall Time			t_f	—	130	400	
Inductive Switching, Series Base Inductance							
Fall Time (I_C = 10 Adc, I_B = 2.0 Adc, L_B = 24 μH) See Table 2			t_f	—	350	—	ns

1.3

TYPICAL ELECTRICAL CHARACTERISTICS

MJ12020

FIGURE 1 — DC CURRENT GAIN

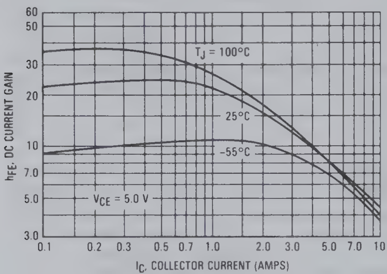
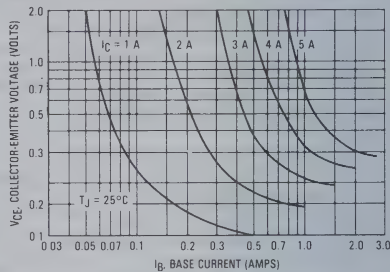


FIGURE 2 — COLLECTOR SATURATION REGION



MJ12021

FIGURE 3 — DC CURRENT GAIN

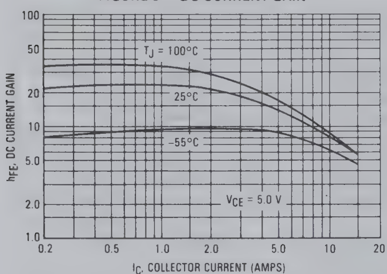
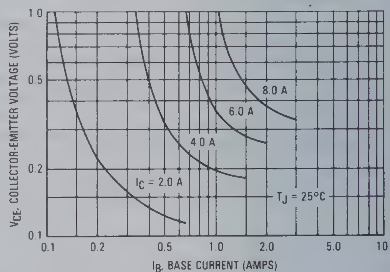


FIGURE 4 — COLLECTOR SATURATION REGION



MJ12022

FIGURE 5 — DC CURRENT GAIN

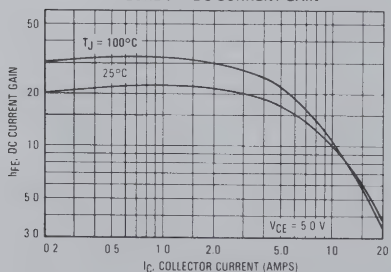
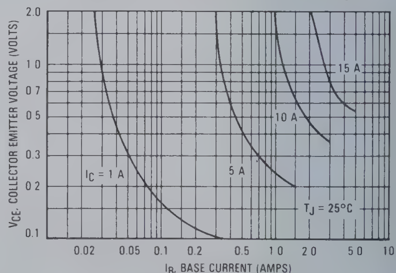


FIGURE 6 — COLLECTOR SATURATION REGION



TYPICAL ELECTRICAL CHARACTERISTICS

MJ12020

FIGURE 7 — COLLECTOR-EMITTER SATURATION VOLTAGE

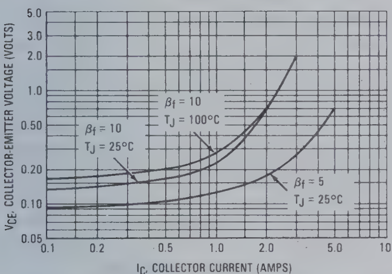
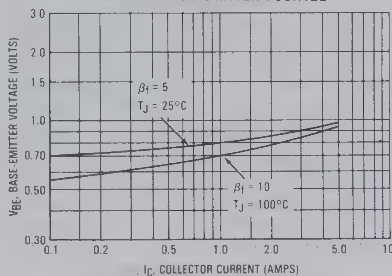


FIGURE 8 — BASE-EMITTER VOLTAGE



MJ12021

FIGURE 9 — COLLECTOR-EMITTER SATURATION VOLTAGE

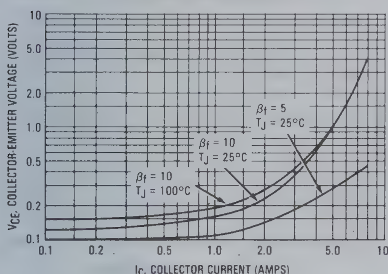
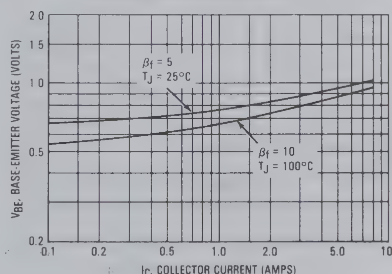


FIGURE 10 — BASE-EMITTER VOLTAGE



MJ12022

FIGURE 11 — COLLECTOR-EMITTER SATURATION VOLTAGE

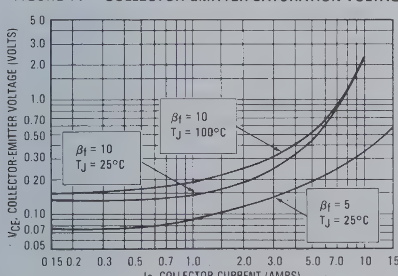
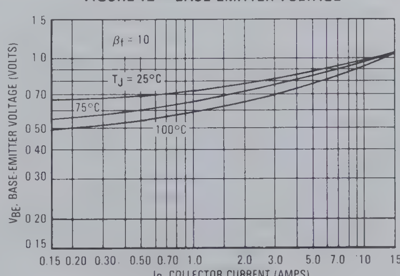


FIGURE 12 — BASE-EMITTER VOLTAGE



1.3

TYPICAL DYNAMIC CHARACTERISTICS

MJ12020

FIGURE 13 — STORAGE TIME

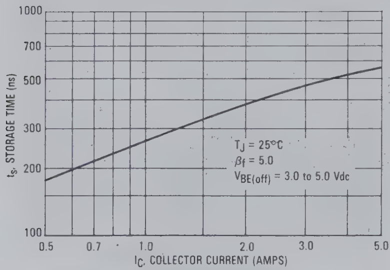
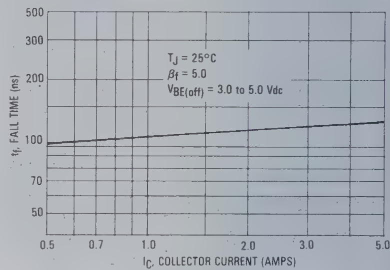


FIGURE 14 — FALL TIME



MJ12021

FIGURE 15 — STORAGE TIME

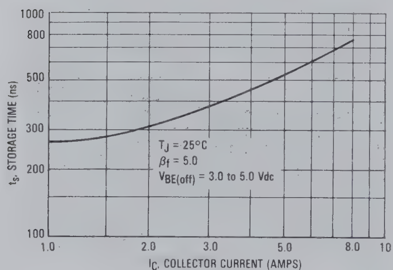
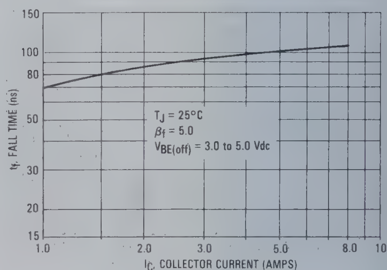


FIGURE 16 — FALL TIME



MJ12022

FIGURE 17 — STORAGE TIME

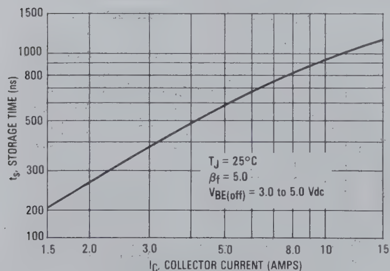
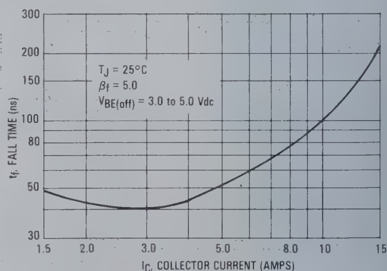


FIGURE 18 — FALL TIME



SAFE OPERATING AREA INFORMATION

MJ12020

FIGURE 19 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

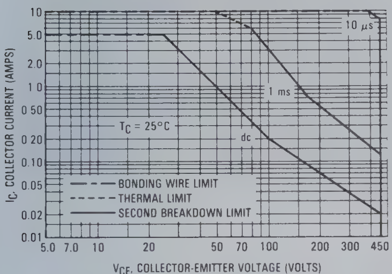
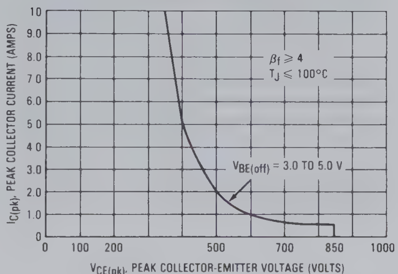


FIGURE 20 — MAXIMUM RATED TURN-OFF SAFE OPERATING AREA



MJ12021

FIGURE 21 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

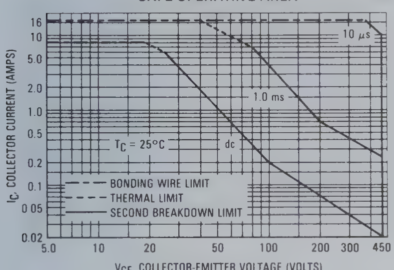
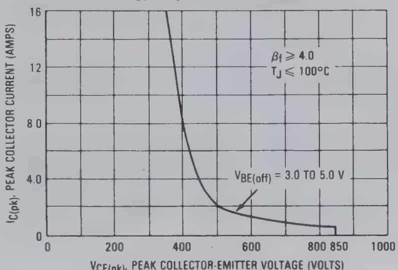


FIGURE 22 — MAXIMUM RATED TURN-OFF SAFE OPERATING AREA



MJ12022

FIGURE 23 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

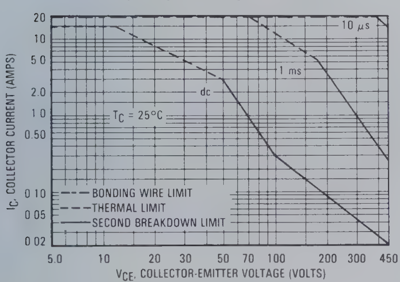
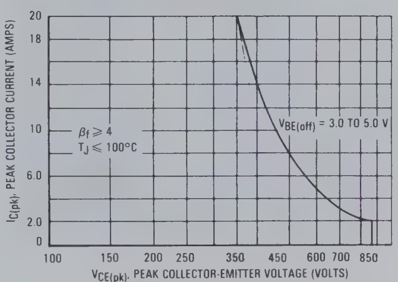


FIGURE 24 — MAXIMUM RATED TURN-OFF SAFE OPERATING AREA



1.3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 19, 21 and 23 are based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 19, 21 and 23 may be found at any case temperature by using the appropriate curve on Figure 28.

$T_{J(pk)}$ may be calculated from the data in Figures 29, 30 or 31. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TURN-OFF

In deflection circuits, high voltage and high current normally do not occur simultaneously during turn-off with the base-emitter reverse biased. The safe level of operating these devices is specified as the Turn-Off Safe Operating Area, and represents the area the lead line may traverse during reverse biased turn off. For reliable operation, all abnormal operating conditions should be checked for operation within this area.

FIGURE 25 — CAPACITANCE VARIATION
MJ12020

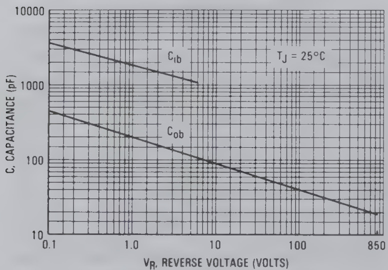


FIGURE 26 — CAPACITANCE VARIATION
MJ12021

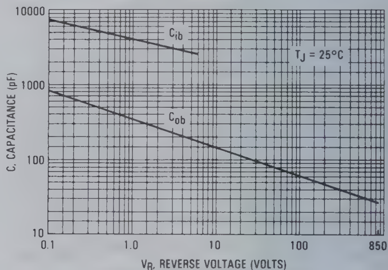


FIGURE 27 — CAPACITANCE VARIATION
MJ12022

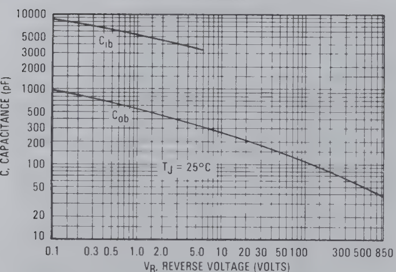
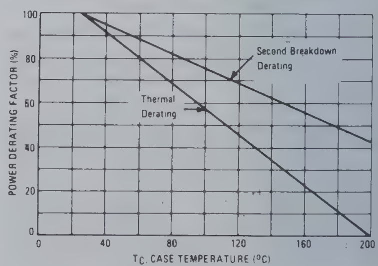


FIGURE 28 — POWER DERATING



THERMAL RESPONSE

FIGURE 29 — MJ12020

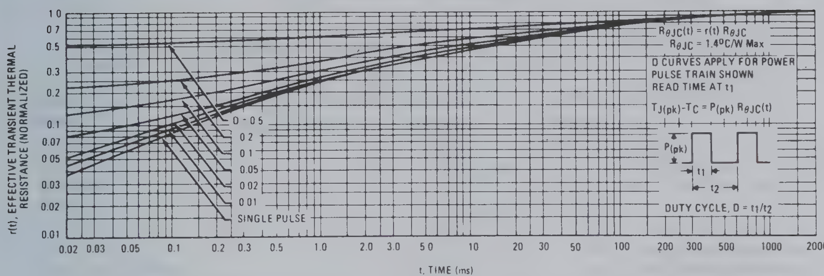


FIGURE 30 — MJ12021

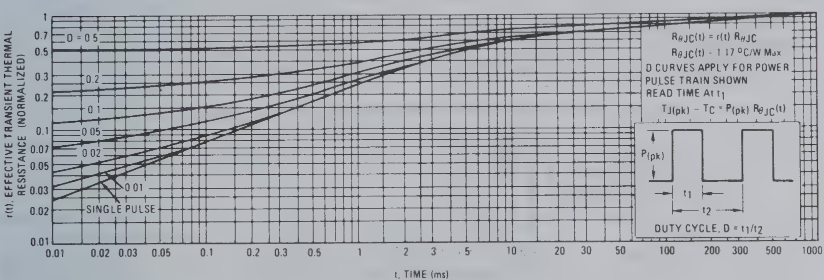
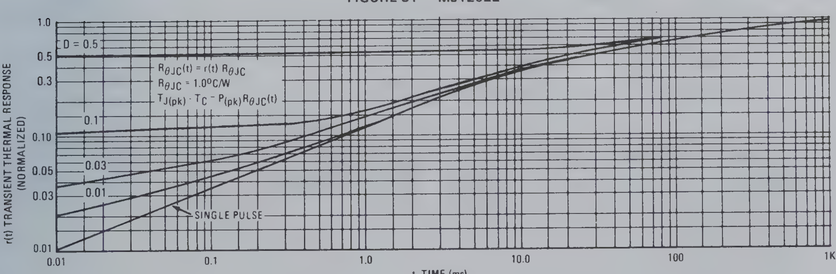
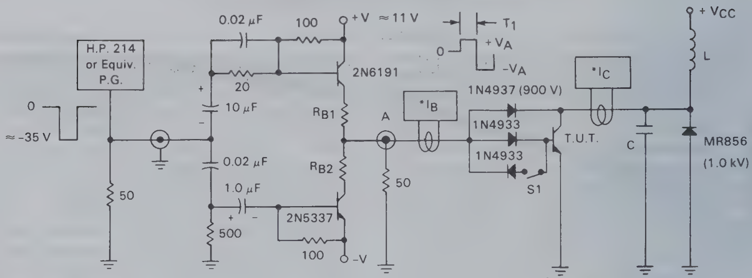


FIGURE 31 — MJ12022



1.3

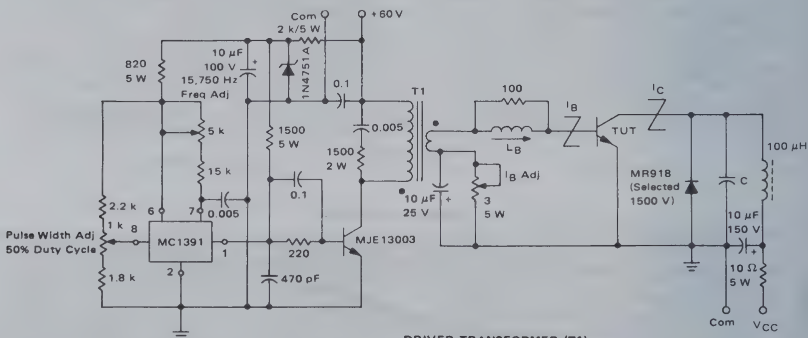
TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



T_1 adjusted to obtain $I_{C(pk)}$
$-V_A$ adjusted to obtain $V_{BE(off)}$

$V_{(BR)CEO}$	Inductive Switching, Clamped Drive			Turn-Off SOA		
L = 10 mH	MJ12020	MJ12021	MJ12022	MJ12020	MJ12021	MJ12022
$R_{B2} = \infty$ V_{CC} = 20 Vdc S1 — Open	C = 0.003 μF V_{CC} = 40 Vdc	C = 0.020 μF V_{CC} = 60 Vdc	C = 0.036 μF V_{CC} = 120 Vdc	C = 0.003 μF V_{CC} = 20 Vdc	C = 0.020 μF V_{CC} = 35 Vdc	C = 0.037 μF V_{CC} = 55 Vdc
*Tektronix P-6042 or Equivalent	L = 100 μH, S1 — Closed R_{B2} = 0, R_{B1} selected for required I_{B1} Scope — Tektronix 7403 or Equivalent			L = 100 μH R_{B2} = 0, R_{B1} selected for required I_{B1} S1 — Closed		

TABLE 2 — TEST CIRCUIT FOR INDUCTIVE SWITCHING WITH BASE INDUCTANCE



Device	V_{CC} (Volts)	$I_{C(pk)}$ (Amp)	C (μF)
MJ12020	20	3.0	0.003
MJ12021	35	5.0	0.;020
MJ12022	55	10	0.036

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance — 39 mH, Secondary Inductance — 0.22 mH, Leakage Inductance with primary shorted — 2.0 μH. Primary 260 turns, #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

MOTOROLA

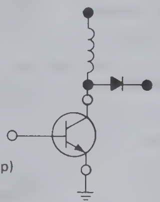
MJ13014
MJ13015

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ13014 and MJ13015 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn - Off Times:
- 60 ns Inductive Fall Time @ 25°C (Typ)
- 120 ns Inductive Crossover Time @ 25°C (Typ)
- 800 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

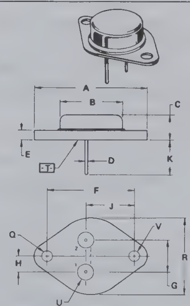
10 AMPERE

NPN SILICON POWER TRANSISTORS

350 AND 400 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	⌀.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS

⌖	⌀.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B		21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

MAXIMUM RATINGS

Rating	Symbol	MJ13014	MJ13015	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	550	600	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 20		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	5.0 10		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	150 85.5 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ⩽ 10%.

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJ13014	$V_{CEO(sus)}$	350	–	–	Vdc
	MJ13015		400	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	–	0.5	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 5 Vdc)		h_{FE}	12	–	40	–
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	–	–	1.4	Vdc
(I_C = 10 Adc, I_B = 2.0 Adc)			–	–	5.0	
(I_C = 5 Adc, I_B = 1.0 Adc, T_C = 100°C)			–	–	2.4	
Base-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	–	1.5	Vdc
(I_C = 5 Adc, I_B = 1.0 Adc, T_C = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	50	–	350	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = 1.0 A,	t_d	–	0.01	0.1	μs
Rise Time	t_p = 25 μs, Duty Cycle ≲ 2%)	t_r	–	0.085	0.5	μs
Storage Time	(V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = 1.0 A,	t_s	–	0.8	2.0	μs
Fall Time	$V_{BE(off)}$ = 5.0 Vdc, t_p = 25 μs, Duty Cycle ≲ 2%)	t_f	–	0.095	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 5 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 1.0 A,	t_{sv}	–	1.5	3.5	μs
Crossover Time	$V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.25	1.0	μs
Fall Time		t_{fi}	–	0.12	–	μs
Storage Time	(I_C = 5 A (pk), V_{clamp} = 250 Vdc, I_{B1} = 1.0 A,	t_{sv}	–	0.8	–	μs
Crossover Time	$V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_c	–	0.12	–	μs
Fall Time		t_{fi}	–	0.06	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

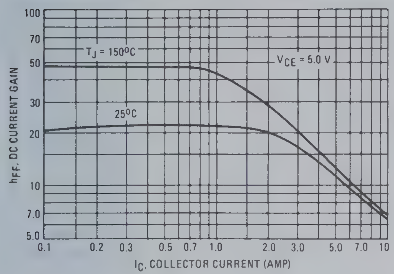


FIGURE 2 — COLLECTOR SATURATION REGION

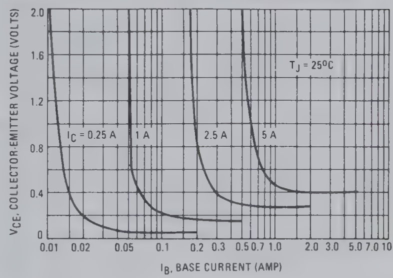


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

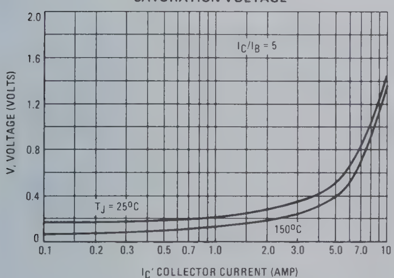


FIGURE 4 — BASE-EMITTER VOLTAGE

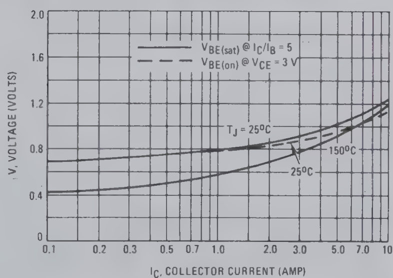


FIGURE 5 — COLLECTOR CUTOFF REGION

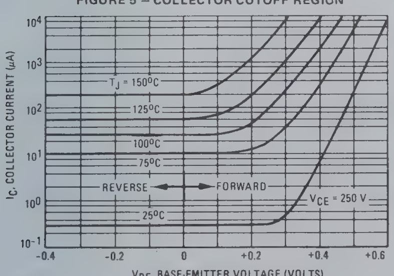
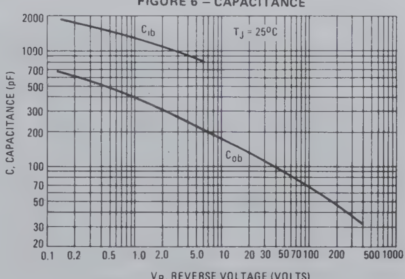
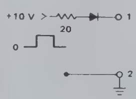


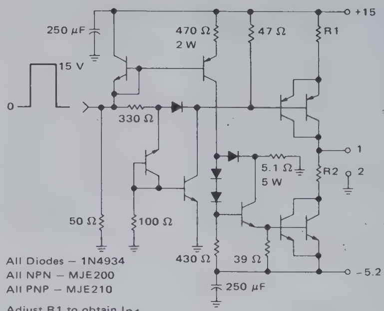
FIGURE 6 — CAPACITANCE



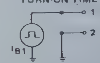
1.3

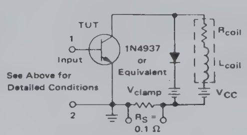
TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

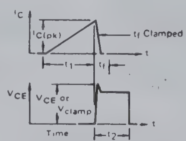
<table>
<tr><th></th><th>$V_{CEO(sus)}$</th><th>RBSOA AND INDUCTIVE SWITCHING</th><th>RESISTIVE SWITCHING</th></tr>
<tr><td>INPUT CONDITIONS</td><td>

PW Varied to Attain I_C = 100 mA</td><td>

All Diodes – 1N4934
All NPN – MJE200
All PNP – MJE210

Adjust R1 to obtain I_{B1}
For switching and RB_{SOA}, R2 = 0
For $BV_{CEO(sus)}$, R2 = ∞</td><td>TURN-ON TIME


I_{B1} adjusted to obtain the forced h_{FE} desired
TURN OFF TIME
Use inductive switching driver as the input to the resistive test circuit.</td></tr>
<tr><td>CIRCUIT VALUES</td><td>L_{coil} = 80 mH V_{CC} = 10 V
R_{coil} = 0.7 Ω</td><td>L_{coil} = 180 μH
R_{coil} = 0.05 Ω
V_{CC} = 20 V
V_{clamp} = 250 V
R_B adjusted to attain desired I_{B1}</td><td>V_{CC} = 250 V
R_L = 50 Ω
Pulse Width = 10 μs</td></tr>
<tr><td>TEST CIRCUITS</td><td colspan="2">INDUCTIVE TEST CIRCUIT


OUTPUT WAVEFORMS


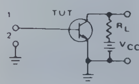
t_1 Adjusted to Obtain I_C
$t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$
$t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$
Test Equipment
Scope – Tektronix 475 or Equivalent</td><td>RESISTIVE TEST CIRCUIT

</td></tr>
</table>

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

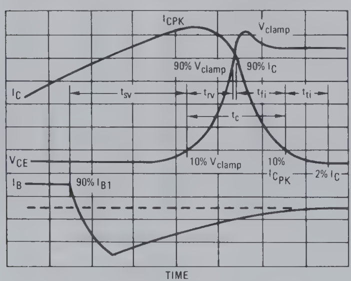
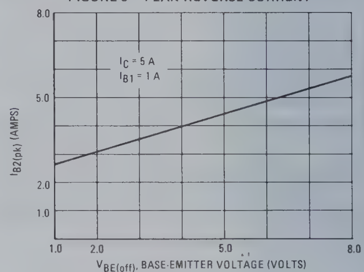


FIGURE 8 – PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

FIGURE 9 — TURN-ON SWITCHING TIMES

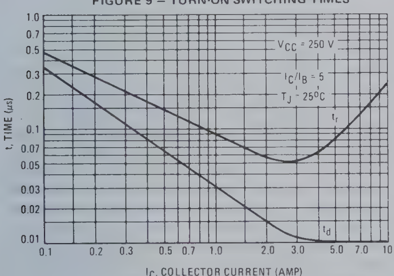


FIGURE 10 — TURN-OFF TIME

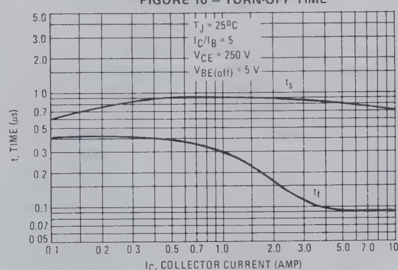
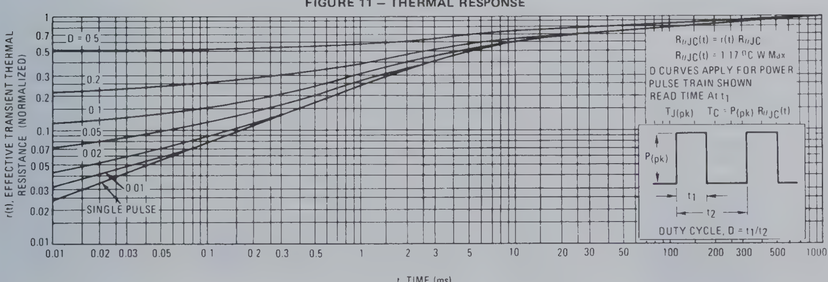


FIGURE 11 — THERMAL RESPONSE



1.3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

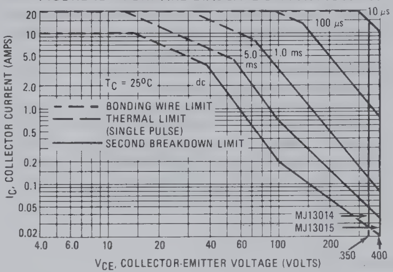
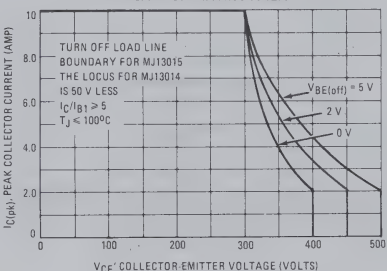


FIGURE 13 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

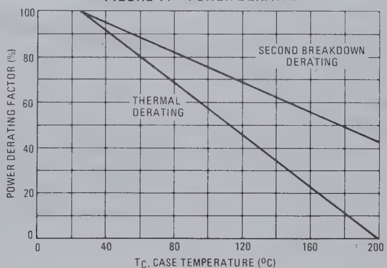
The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 14 — POWER DERATING



MJ13070
MJ13071

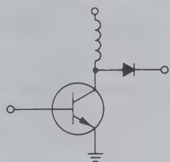
MOTOROLA

1.3

Designer's Data Sheet

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The MJ13070 and MJ13071 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:



- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 100 ns Inductive Fall Time @ 25°C (Typ)
- 150 ns Inductive Crossover Time @ 25°C (Typ)
- 400 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range −65 to +200°C

100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

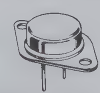
5 AMPERE

NPN SILICON POWER TRANSISTORS

400 AND 450 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



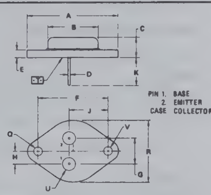
MAXIMUM RATINGS

Rating	Symbol	MJ13070	MJ13071	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	750	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 8.0		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.0 4.0		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	125 71.5 0.714		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. $\boxed{T}$ IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

⌖	∅0.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS

⌖	∅0.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37		1.550
B	–	21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3 TYPE

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ13070	$V_{CEO(sus)}$	400	—	—	Vdc
MJ13071		450	—	—	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.5	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 12		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)	$V_{CE(sat)}$	—	—	1.0	Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)		—	—	3.0	
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		—	—	2.0	
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	250	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 250 Adc, I_C = 3.0 Adc, I_{B1} = 0.4 Adc, t_p = 30 μs, Duty Cycle ≤2%, $V_{BE(off)}$ = 5.0 Vdc)	t_d	—	0.03	0.05	μs
Rise Time	t_r	—	0.10	0.40	
Storage Time	t_s	—	0.40	1.50	
Fall Time	t_f	—	0.175	0.50	
Inductive Load, Clamped (Table 1)					
Storage Time ($I_{C(pk)}$ = 3.0 A, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V) (T_J = 100°C)	t_{sv}	—	0.70	2.0	μs
Crossover Time (T_J = 100°C)	t_c	—	0.28	0.50	
Fall Time (T_J = 100°C)	t_{fi}	—	0.15	0.30	
Storage Time (T_J = 25°C)	t_{sv}	—	0.40	—	
Crossover Time (T_J = 25°C)	t_c	—	0.15	—	
Fall Time (T_J = 25°C)	t_{fi}	—	0.10	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤2%

$\beta_f \; \frac{I_C}{I_B}$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

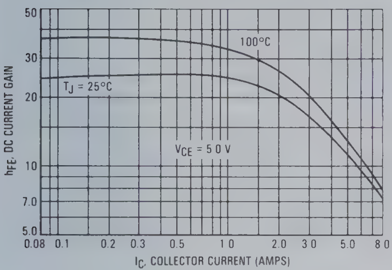


FIGURE 2 — COLLECTOR SATURATION REGION

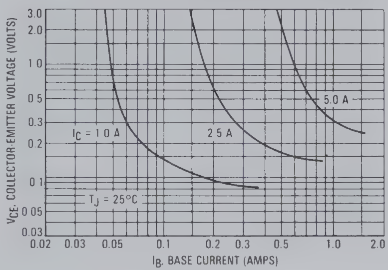


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

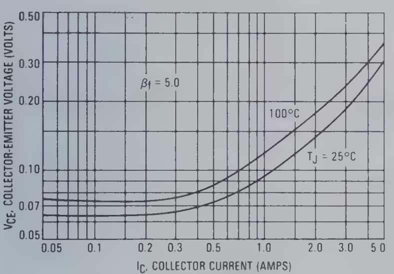


FIGURE 4 — BASE-EMITTER VOLTAGE

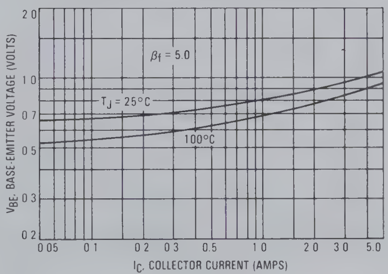


FIGURE 5 — COLLECTOR CUTOFF REGION

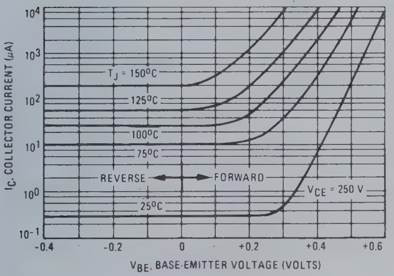
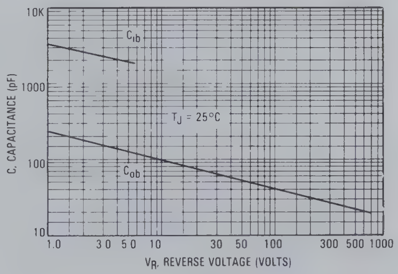


FIGURE 6 — CAPACITANCE



1.3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

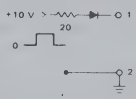
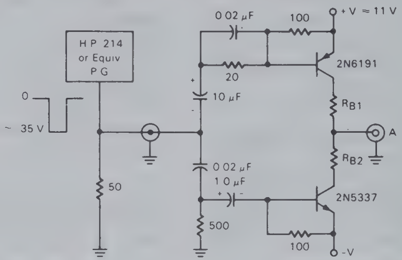
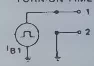
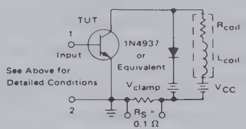
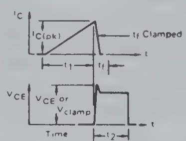
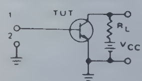
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} 180 µH R_{coil} 0.05 Ω V_{CC} 20 V V_{clamp} 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L 83 Ω Pulse Width = 10 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

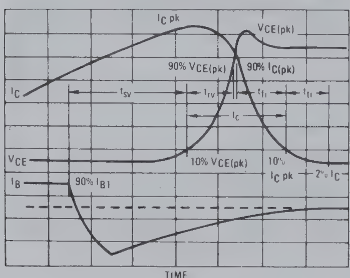
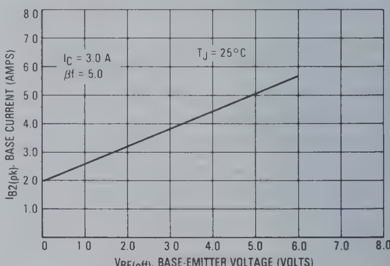


FIGURE 8 — PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

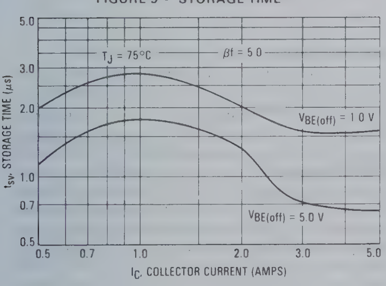


FIGURE 10 — CROSSOVER AND FALL TIMES

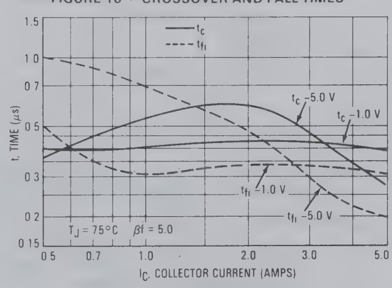
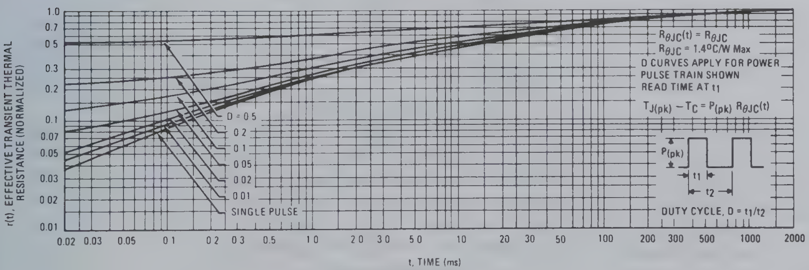


FIGURE 11 — THERMAL RESPONSE



1.3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

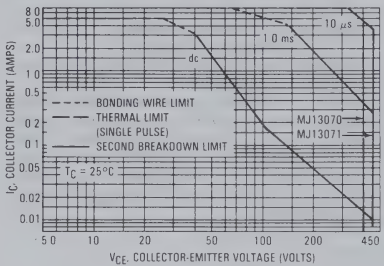
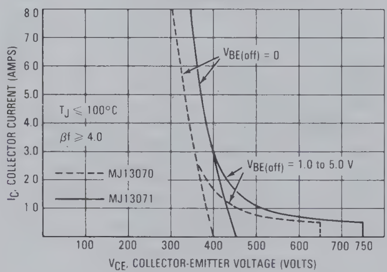


FIGURE 13 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

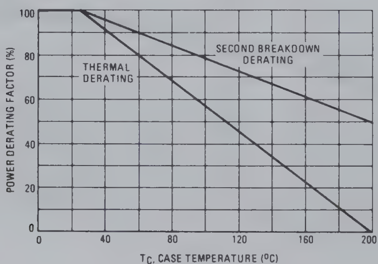
The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 14 — POWER DERATING



MJ13080
MJ13081

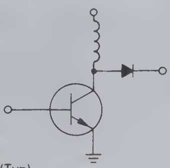
MOTOROLA

1.3

Designer's Data Sheet

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The MJ13080 and MJ13081 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:



- Switching Regulators
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Fast Turn-Off Times
- 100 ns Inductive Fall Time @ 25°C (Typ)
- 150 ns Inductive Crossover Time @ 25°C (Typ)
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100°C Performance Specified for:
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- Saturation Voltages
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400 AND 450 VOLTS
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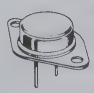

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Rating	Symbol	MJ13080	MJ13081	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	750	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8.0 12		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	3.0 6.0		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	150 85.5 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

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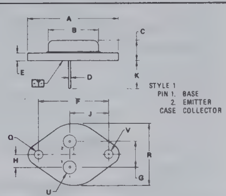

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2. T IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
   ⌖ | ⌀ 13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS
   ⌖ | ⌀ 13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

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D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
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H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
[illegible]	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3 TYPE

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ13080	$V_{CEO(sus)}$	400	—	—	Vdc
MJ13081		450	—	—	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.5	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	—	—	1.0	Vdc
(I_C = 8.0 Adc, I_B = 1.6 Adc)		—	—	3.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		—	—	2.0	
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	300	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 250 Vdc, I_C = 5.0 Adc, I_{B1} = 0.7 Adc, t_p = 30 μs, Duty Cycle ≤2%, $V_{BE(off)}$ = 5.0 Vdc)	t_d	—	0.025	0.05	μs
Rise Time	t_r	—	0.10	0.50	
Storage Time	t_s	—	0.50	1.50	
Fall Time	t_f	—	0.15	0.50	
Inductive Load, Clamped (Table 1)					
Storage Time ($I_{C(pk)}$ = 5.0 A, I_{B1} = 0.7 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V) (T_J = 100°C)	t_{sv}	—	0.75	2.20	μs
Crossover Time (T_J = 100°C)	t_c	—	0.22	0.40	
Fall Time (T_J = 100°C)	t_{fi}	—	0.175	0.35	
Storage Time (T_J = 25°C)	t_{sv}	—	0.40	—	
Crossover Time (T_J = 25°C)	t_c	—	0.15	—	
Fall Time (T_J = 25°C)	t_{fi}	—	0.10	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$\beta_f = \frac{I_C}{I_B}$

1.3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

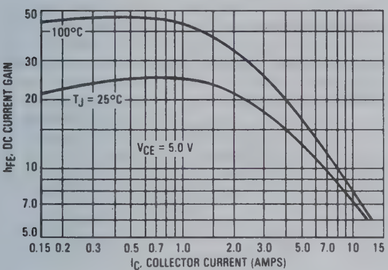


FIGURE 2 — COLLECTOR SATURATION REGION

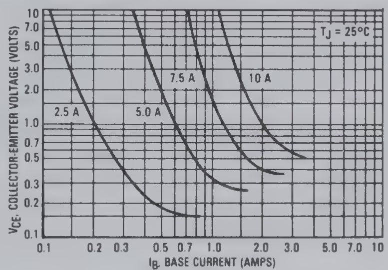


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

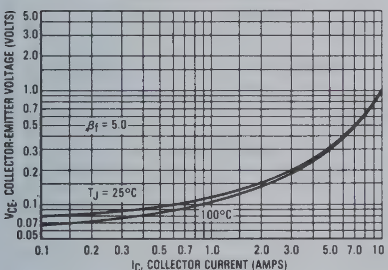


FIGURE 4 — BASE-EMITTER VOLTAGE

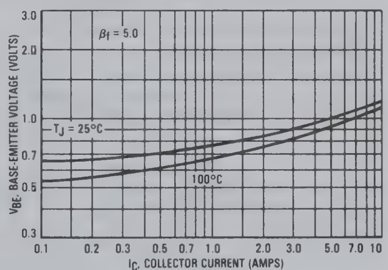


FIGURE 5 — COLLECTOR CUTOFF REGION

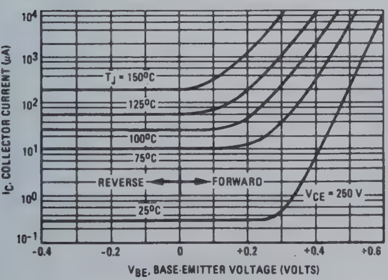
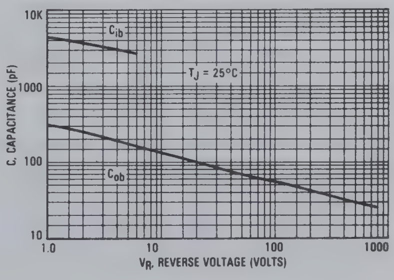
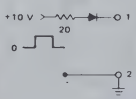


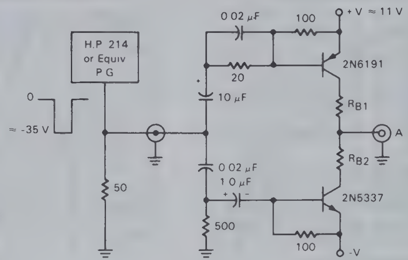
FIGURE 6 — CAPACITANCE

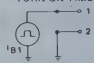


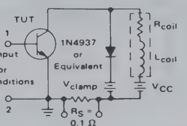
1.3

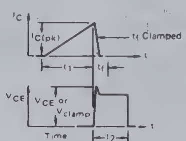
TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

<table>
<tr><th></th><th>$V_{CEO(sus)}$</th><th>RBSOA AND INDUCTIVE SWITCHING</th><th>RESISTIVE SWITCHING</th></tr>
<tr><td>INPUT CONDITIONS</td>
<td>

PW Varied to Attain I_C = 100 mA</td>
<td>

Adjust R1 to obtain I_{B1}
For switching and RB_{SOA}, R2 = 0
For $BV_{CEO(sus)}$, R2 = ∞</td>
<td>TURN ON TIME


I_{B1} adjusted to obtain the forced h_{FE} desired
TURN OFF TIME
Use inductive switching driver as the input to the resistive test circuit.</td></tr>
<tr><td>CIRCUIT VALUES</td>
<td>L_{coil} = 80 mH V_{CC} = 10 V
R_{coil} = 0.7 Ω</td>
<td>L_{coil} = 180 μH
R_{coil} = 0.05 Ω
V_{CC} = 20 V
V_{clamp} = 250 V
R_B adjusted to attain desired I_{B1}</td>
<td>V_{CC} = 250 V
R_L = 50 Ω
Pulse Width = 30 μs</td></tr>
<tr><td>TEST CIRCUITS</td>
<td>INDUCTIVE TEST CIRCUIT


See Above for Detailed Conditions</td>
<td>OUTPUT WAVEFORMS


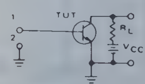
t_1 Adjusted to Obtain I_C
$t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$
$t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$
Test Equipment
Scope — Tektronix
475 or Equivalent</td>
<td>RESISTIVE TEST CIRCUIT

</td></tr>
</table>

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

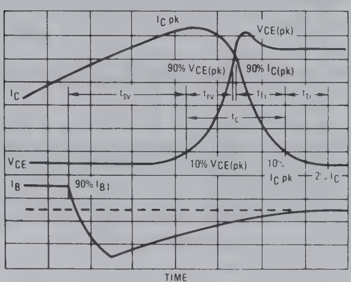
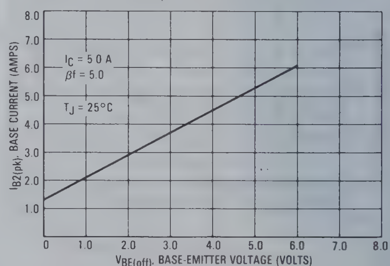


FIGURE 8 — PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

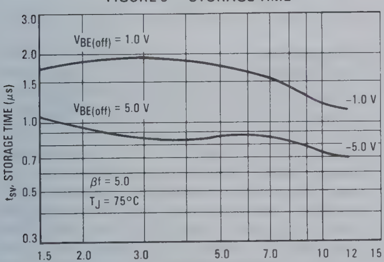


FIGURE 10 — CROSSOVER AND FALL TIMES

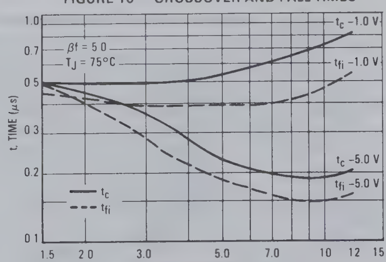
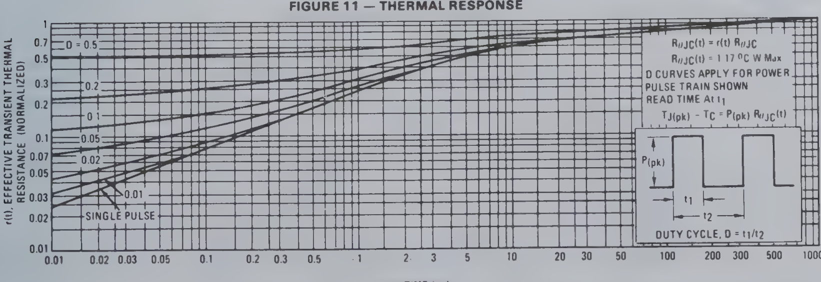


FIGURE 11 — THERMAL RESPONSE



1.3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

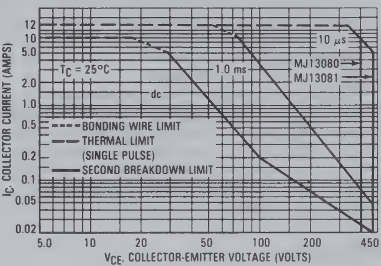
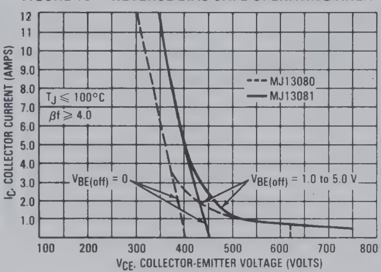


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

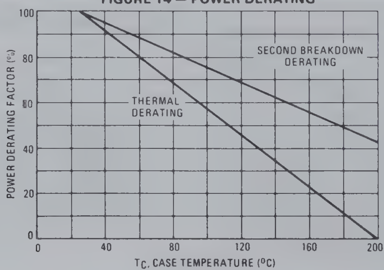
The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 14 — POWER DERATING



MJ13090
MJ13091
MJH13090
MJH13091

MOTOROLA

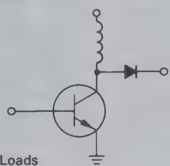
1.3

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads — 150 ns Inductive Fall Time (Typ)
- Saturation Voltages
- Leakage Currents

15 AMPERE

NPN SILICON POWER TRANSISTORS

400 AND 450 VOLTS
125 and 175 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJ13090	MJ13091	MJH13090	MJH13091	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	750	650	750	Vdc
Emitter-Base Voltage	V_{EB}	6.0				Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20				Adc
Base Current — Continous — Peak (1)	I_B I_{BM}	5.0 10				Adc
Total Device Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	175 100 1.0		125 50 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200		-55 to 150		°C

THERMAL CHARACTERISTICS

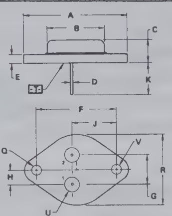
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds.	T_L	275	°C

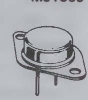
(1) Pulse Test: Pulse Width $\leq$ 5.0 μs, Duty Cycle $\geq$10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MJ13090
MJ13091





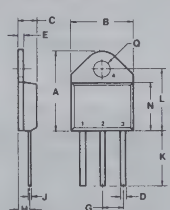
STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

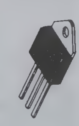
NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(Formerly TO-3)

MJH13090
MJH13091





1 BASE
2 COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.168

CASE 340-01
TO-218AC

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1)	$V_{CEO(sus)}$				Vdc
(I_C = 100 mA, I_B = 0) MJ13090, MJH13090		400	—	—	
MJ13091, MJH13091		450	—	—	
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.5	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figures 12 and 13			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 14			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc	h_{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2.0 Adc)		—	—	1.0	
(I_C = 15 Adc, I_B = 3.0 Adc)		—	—	3.0	
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	—	2.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2.0 Adc)		—	—	1.5	
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	350	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1) — (V_{CC} = 250 Vdc, I_C = 10 Adc, I_{B1} = 1.25 Adc, t_p = 30 µs, Duty Cycle ≤2%, $V_{BE(off)}$ = 5.0 Vdc)					
Delay Time	t_d	—	0.03	0.05	µs
Rise Time	t_r	—	0.13	0.50	
Storage Time	t_s	—	0.55	2.50	
Fall Time	t_f	—	0.10	0.50	
Inductive Load, Clamped (Table 1) — ($I_{C(pk)}$ = 10 A, I_{B1} = 1.25 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V)					
Storage Time (T_J = 100°C)	t_{sv}	—	0.80	3.00	µs
Crossover Time (T_J = 100°C)	t_c	—	0.175	0.40	
Fall Time (T_J = 100°C)	t_{fi}	—	0.15	0.30	
Storage Time (T_J = 25°C)	t_{sv}	—	0.50	—	
Crossover Time (T_J = 25°C)	t_c	—	0.15	—	
Fall Time (T_J = 25°C)	t_{fi}	—	0.10	—	

(1) Pulse Test: PW = 300 µs, Duty Cycle ≤ 2%.

$^*\beta_f = \frac{I_C}{I_B}$

1.3

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

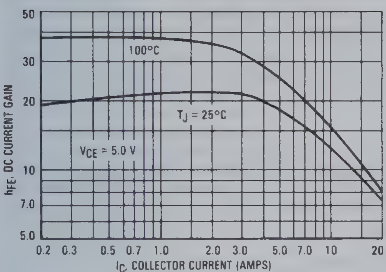


FIGURE 2 — COLLECTOR SATURATION REGION

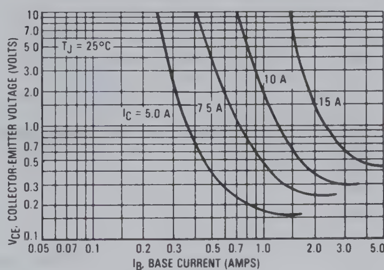


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

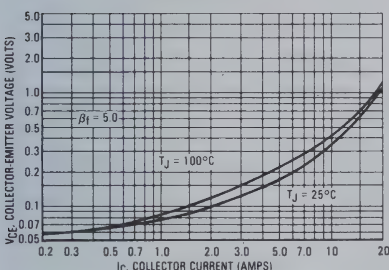


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

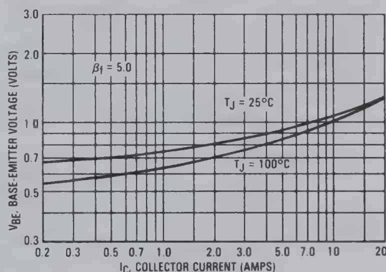


FIGURE 5 — COLLECTOR CUTOFF REGION

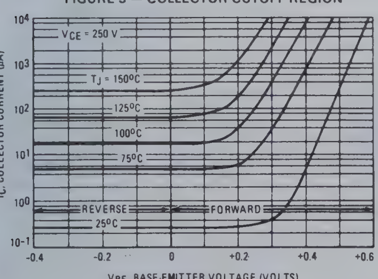
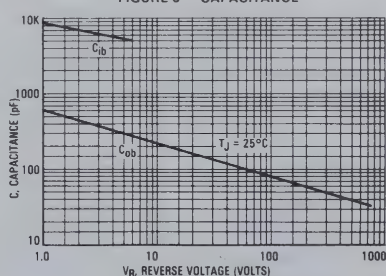


FIGURE 6 — CAPACITANCE



1.3

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

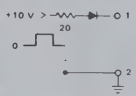
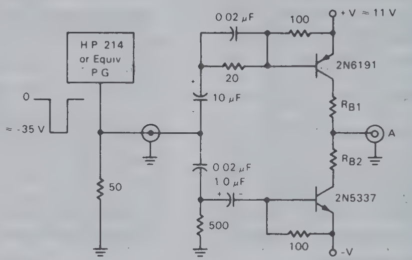
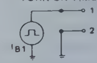
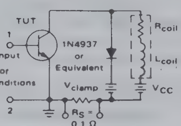
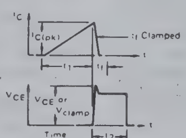
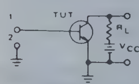
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Connect Point A to base of TUT Adjust –V to obtain desired $V_{BE(off)}$ at Point A Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$ R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_{B1} adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 30 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT See Above for Detailed Conditions 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

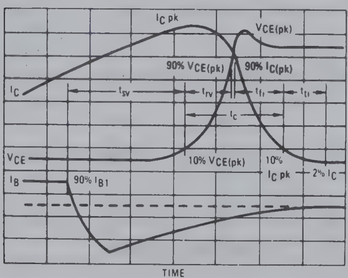
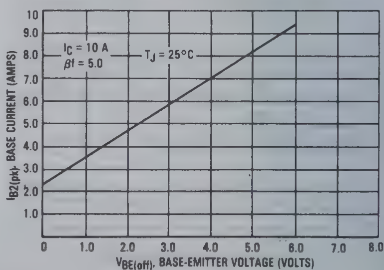


FIGURE 8 — PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{clamp}
t_{rv} = Voltage Rise Time, 10—90% V_{clamp}
t_{fi} = Current Fall Time, 90—10% I_C
t_{ti} = Current Tail, 10—2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

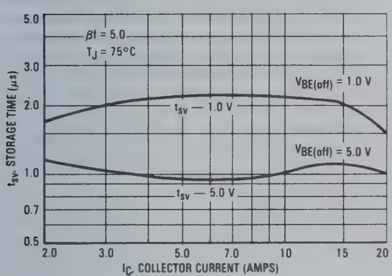


FIGURE 10 — CROSSOVER AND FALL TIMES

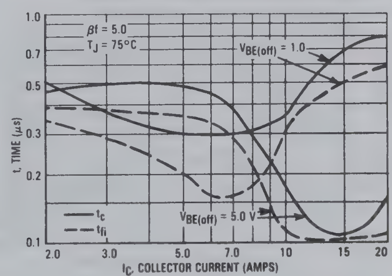
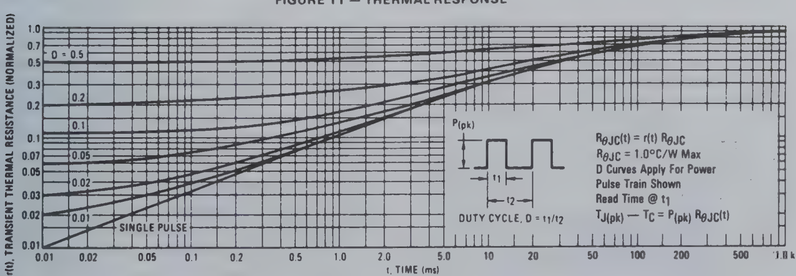


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA MJ13090 and MJ13091

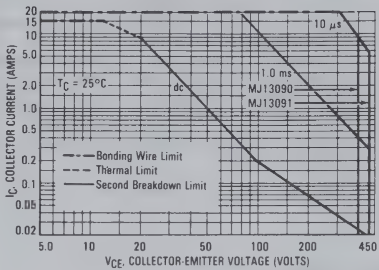
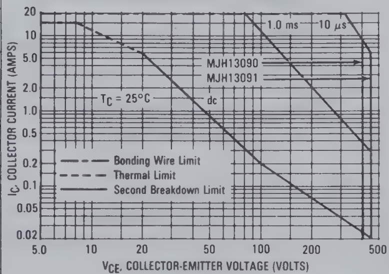


FIGURE 13 — FORWARD BIAS SAFE OPERATING AREA MJH13090 and MJH13091



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 12 and 13 are based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 12 and 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives RBSOA characteristics.

FIGURE 14 — REVERSE BIAS SAFE OPERATING AREA

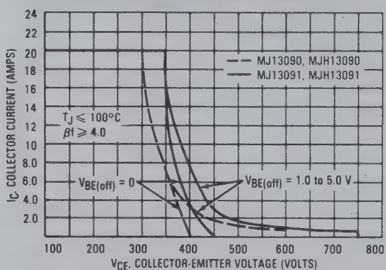
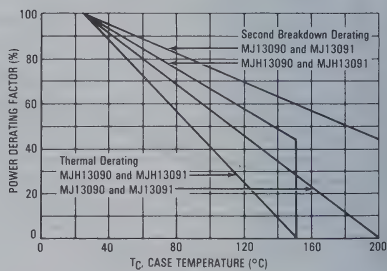


FIGURE 15 — POWER DERATING

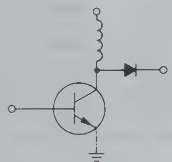


MOTOROLA

Designer's Data Sheet

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The MJ13100 and MJ13101 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:



- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 30 ns Inductive Fall Time @ 25°C (Typ)
- 50 ns Inductive Crossover Time @ 25°C (Typ)
- 900 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range –65 to +200°C

100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

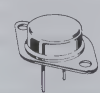
20 AMPERE

NPN SILICON POWER TRANSISTORS

400 AND 450 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



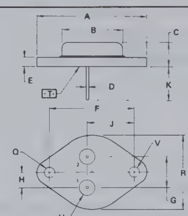
MAXIMUM RATINGS

Rating	Symbol	MJ13100	MJ13101	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	750	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ⩽ 10%.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

⌖	Ø.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS

⌖	Ø.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14 5, 1973

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3 TYPE

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ13100	$V_{CEO(sus)}$	400	—	—	Vdc
MJ13101		450	—	—	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.5	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 12		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 15 Adc, V_{CE} = 3.0 Vdc	h_{FE}	8.0	—	40	—
Collector-Emitter Saturation Voltage (I_C = 15 Adc, I_B = 3.0 Adc)	$V_{CE(sat)}$	—	—	1.0	Vdc
(I_C = 20 Adc, I_B = 4.0 Adc)		—	—	3.0	
(I_C = 15 Adc, I_B = 3.0 Adc, T_C = 100°C)		—	—	2.0	
Base-Emitter Saturation Voltage (I_C = 15 Adc, I_B = 3.0 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 15 Adc, I_B = 3.0 Adc, T_C = 100°C)		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	450	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 250 Vdc, I_C = 15 Adc, I_{B1} = 2.0 Adc, t_p = 30 μs, Duty Cycle ≤2%, $V_{BE(off)}$ = 5.0 Vdc)	t_d	—	0.02	0.05	μs
Rise Time	t_r	—	0.13	0.50	
Storage Time	t_s	—	0.90	3.5	
Fall Time	t_f	—	0.10	0.50	
Inductive Load, Clamped (Table 1) ($I_{C(pk)}$ = 15 A, I_{B1} = 2.0 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V)					
Storage Time (T_J = 100°C)	t_{sv}	—	1.25	4.0	μs
Crossover Time (T_J = 100°C)	t_c	—	0.15	0.50	
Fall Time (T_J = 100°C)	t_{fi}	—	0.13	0.40	
Storage Time (T_J = 25°C)	t_{sv}	—	0.90	—	
Crossover Time (T_J = 25°C)	t_c	—	0.05	—	
Fall Time (T_J = 25°C)	t_{fi}	—	0.03	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$^{*}\beta_f = \frac{I_C}{I_B}$

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

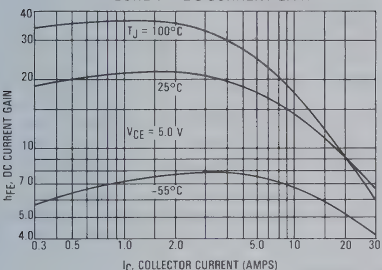


FIGURE 2 — COLLECTOR SATURATION REGION

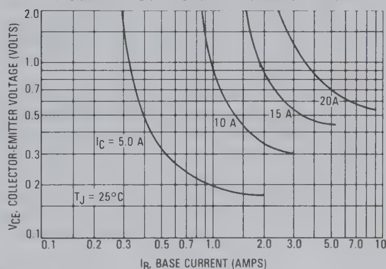


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

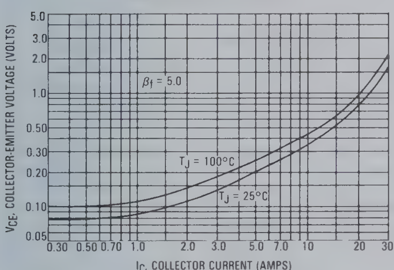


FIGURE 4 — BASE-EMITTER VOLTAGE

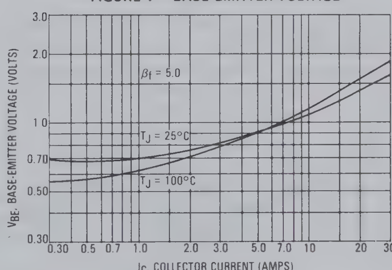


FIGURE 5 — COLLECTOR CUTOFF REGION

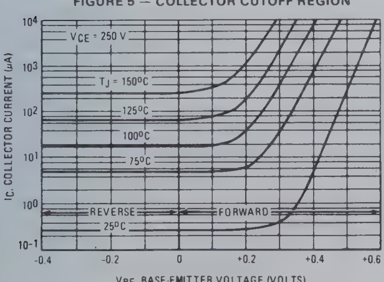
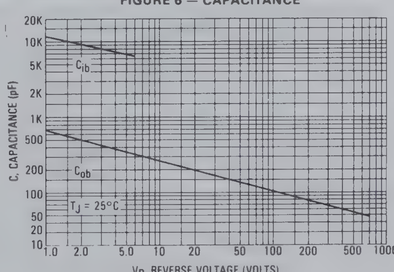


FIGURE 6 — CAPACITANCE



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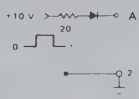
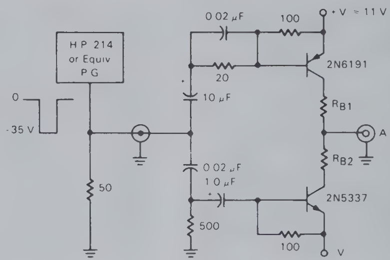
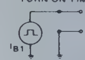
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit
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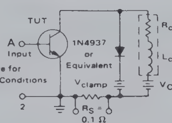
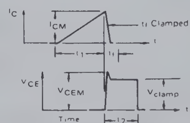
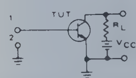
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

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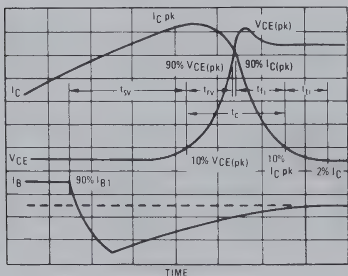

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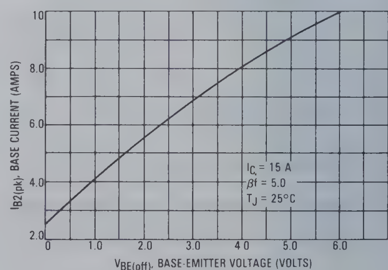

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In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

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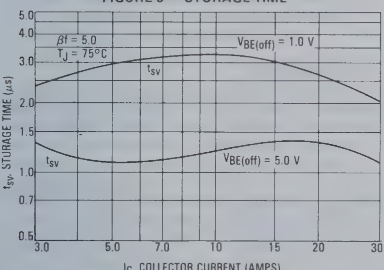
INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME



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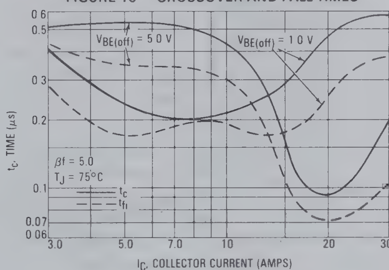
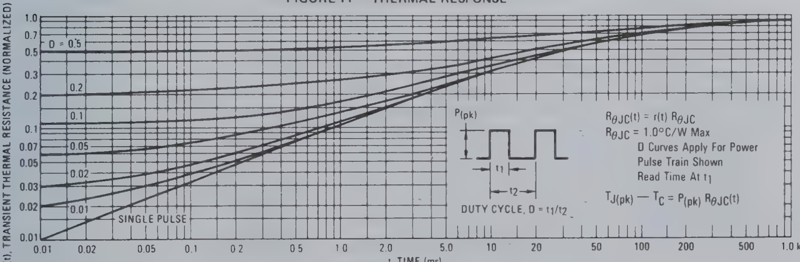


FIGURE 11 — THERMAL RESPONSE



1.3

The Safe Operating Area figures shown in figure 12 and 13 are specified for these devices under the test conditions shown

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

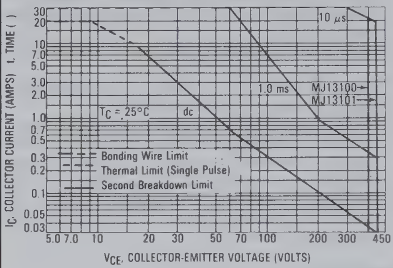
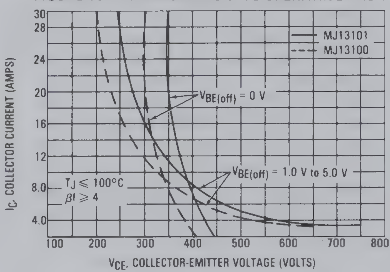


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

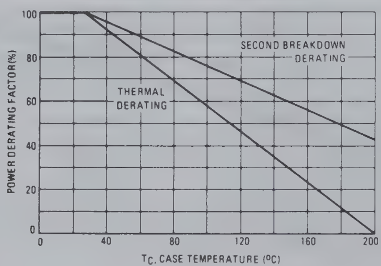
The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

FIGURE 14 — POWER DERATING



MJ13330
MJ13331

MOTOROLA

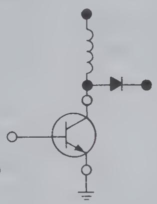
1.3

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ13330 and MJ13331 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Time
- 75 ns Inductive Fall Time–25°C (Typ)
- 150 ns Inductive Crossover Time–25°C (Typ)
- 900 ns Inductive Storage Time–25°C (Typ)

Operating Temperature Range −65 to +200°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

20 AMPERE

NPN SILICON POWER TRANSISTORS

200 and 250 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

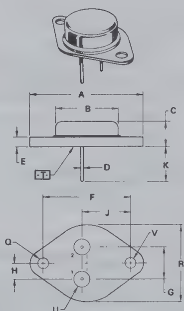
MAXIMUM RATINGS

Rating	Symbol	MJ13330	MJ13331	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	200	250	Vdc
Collector-Emitter Voltage	V_{CEV}	400	450	Vdc
Emitter Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 20		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES.
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

   | ⌖ | ⌀.13 (0.005) Ⓜ | T | V Ⓜ |

   FOR LEADS

   | ⌖ | ⌀.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

Similar device types with higher V_{CEO} ratings are: MJ13332 (350 V) thru MJ13335 (500 V).

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100$ mA, $I_B = 0$) MJ13330		$V_{CEO(sus)}$	200	–	–	Vdc
MJ13331			250	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc)		I_{CEV}	–	–	0.25	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc, $T_C = 150^oC$)			–	–	5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $R_{BE} = 50\ \Omega$, $T_C = 100^oC$)		I_{CER}	–	–	5	mAdc
Emitter Cutoff Current ($V_{EB} = 6$ Vdc, $I_C = 0$)		I_{EBO}	–	–	0.5	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with base reverse biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain ($I_C = 5$ Adc, $V_{CE} = 5$ Vdc)		h_{FE}	15	–	75	–
($I_C = 10$ Adc, $V_{CE} = 5$ Vdc)			8.0	–	40	
Collector-Emitter Saturation Voltage ($I_C = 10$ Adc, $I_B = 1.5$ Adc)		$V_{CE(sat)}$	–	–	1.5	Vdc
($I_C = 20$ Adc, $I_B = 5$ Adc)			–	–	3.5	
($I_C = 10$ Adc, $I_B = 1.8$ Adc, $T_C = 100^oC$)			–	–	2.5	
Base-Emitter Saturation Voltage ($I_C = 10$ Adc, $I_B = 1.5$ Adc)		$V_{BE(sat)}$	–	–	1.8	Vdc
($I_C = 10$ Adc, $I_B = 1.8$ Adc, $T_C = 100^oC$)			–	–	1.8	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product ($I_C = 300$ mAdc, $V_{CE} = 10$ Vdc, $f_{test} = 1$ MHz)		f_T	5	–	40	MHz
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f_{test} = 100$ kHz)		C_{ob}	100	–	400	pF
SWITCHING CHARACTERSITICS						
Resistive Load (Table 1)						
Delay Time	($V_{CC} = 175$ Vdc, $I_C = 10$ A, $I_{B1} = 1.5$ Adc, $V_{BE(off)} = 5$ Vdc, $t_p = 50\ \mu s$, Duty Cycle $\leqslant 2\%$)	t_d	–	0.08	0.20	μs
Rise Time		t_r	–	0.55	1.0	μs
Storage Time		t_s	–	0.70	3.5	μs
Fall Time		t_f	–	0.11	0.7	μs
Inductive Load, Clamped (Table 1)						
Storage Time	($I_C = 10$ A(pk), $V_{clamp} = 200$ Vdc, $I_{B1} = 1.8$ Adc, $V_{BE(off)} = 5$ Vdc, $T_C = 100^oC$)	t_{sv}	–	1.35	4.5	μs
Crossover Time		t_c	–	0.45	1.8	μs
Storage Time	($I_C = 10$ A(pk), $V_{clamp} = 200$ Vdc, $I_{B1} = 1.5$ Adc, $V_{BE(off)} = 5$ Vdc, $T_C = 25^oC$)	t_{sv}	–	0.90	-	μs
Crossover Time		t_c	–	0.15	–	μs
Fall Time		t_{fi}	–	0.075	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle $\leqslant 2\%$.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

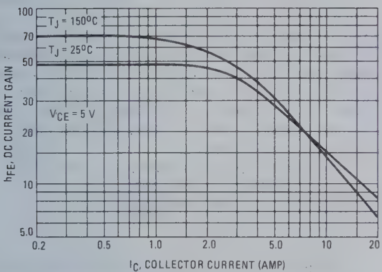


FIGURE 2 – COLLECTOR SATURATION REGION

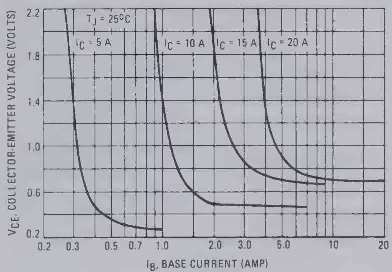


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

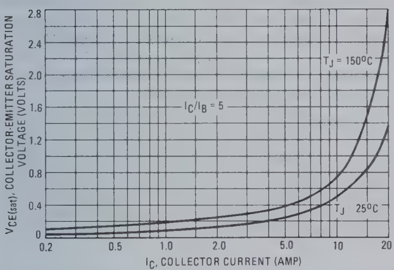


FIGURE 4 – BASE-EMITTER VOLTAGE

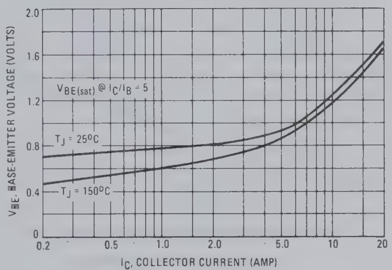


FIGURE 5 – COLLECTOR CUTOFF REGION

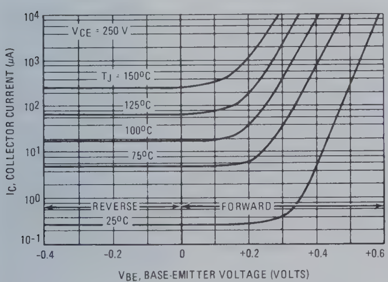
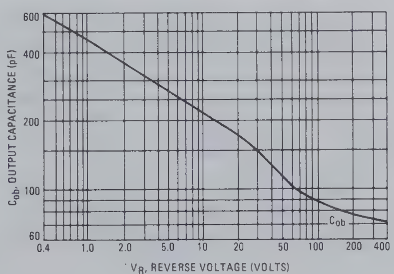


FIGURE 6 – OUTPUT CAPACITANCE



1.3

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

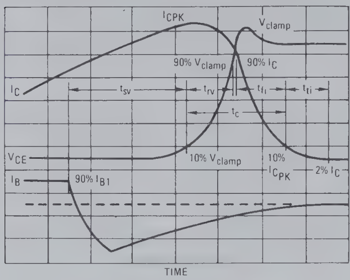
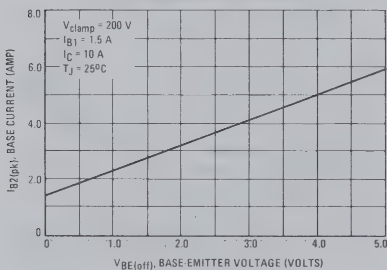


FIGURE 8 — REVERSE BASE CURRENT versus BASE EMITTER VOLTAGE



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

FIGURE 9 — TURN-ON TIME

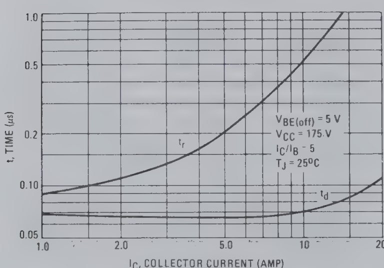


FIGURE 10 — TURN-OFF TIME

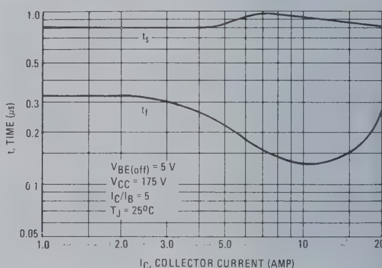


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

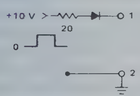
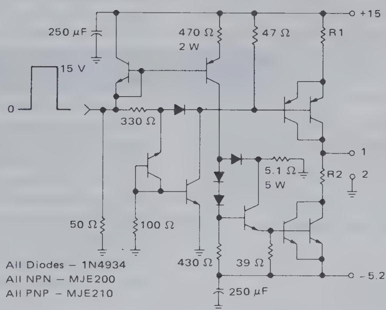
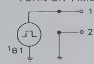
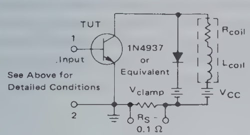
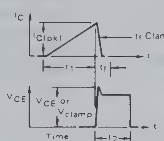
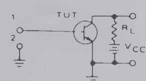
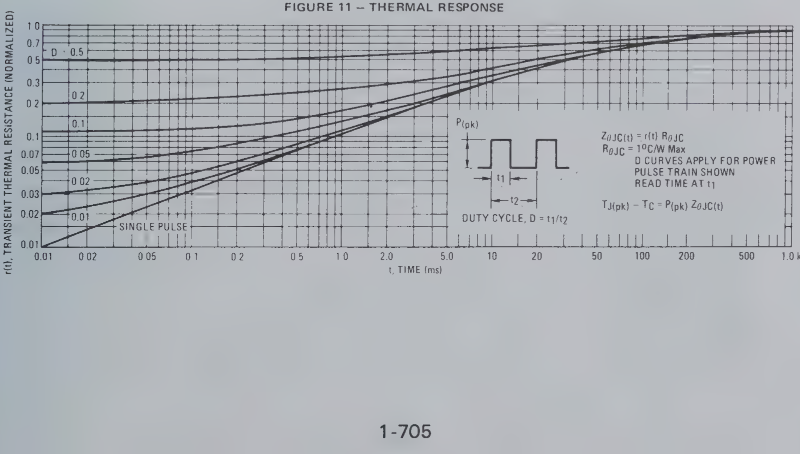
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 200 V	V_{CC} = 175 V R_L = 17.5 Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 11 – THERMAL RESPONSE



1.3

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

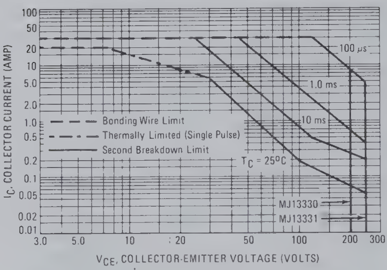
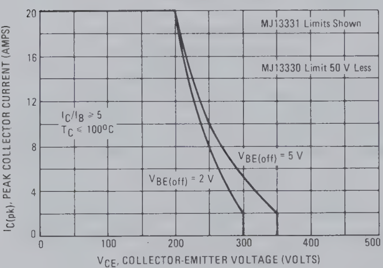


FIGURE 13 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

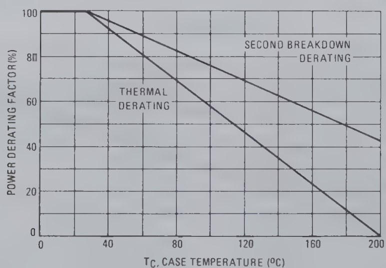
The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 — POWER DERATING



MOTOROLA

MJ13332 MJ13334
MJ13333 MJ13335

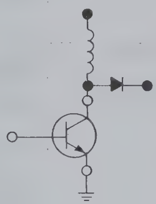
1.3

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ13332 through MJ13335 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
  200 ns Inductive Fall Time—25°C (Typ)
  1.8 μs Inductive Storage Time—25°C (Typ)

Operating Temperature Range −65 to +200°C

100°C Performance Specified for:
  Reversed Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents

20 AMPERE

NPN SILICON POWER TRANSISTORS

350–500 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

MAXIMUM RATINGS

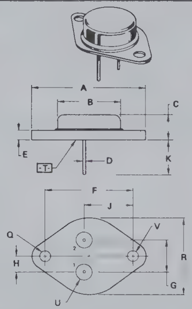
Rating	Symbol	MJ13332	MJ13333	MJ13334	MJ13335	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	450	500	Vdc
Collector-Emitter Voltage	V_{CEV}	650	700	750	800	Vdc
Emitter Base Voltage	V_{EB}	6.0				Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	20 30				Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	10 15				Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	175 100 1.0				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ⩽ 10%.

Similar device types available with lower V_{CEO} ratings, see the MJ13330 (200 V) and MJ13331 (250 V).



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
   ⌖ | Ø.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | Ø.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B		21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ13335	$V_{CEO(sus)}$	500	–	–	Vdc
MJ13334		450	–	–	
MJ13333		400	–	–	
MJ13332		350	–	–	
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150^oC$)		–	–	5.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, $T_C = 100^oC$)	I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	60	–
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2.0 Adc)		–	–	1.8	
(I_C = 20 Adc, I_B = 6.7 Adc)		–	–	5.0	
(I_C = 10 Adc, I_B = 2.0 Adc, $T_C = 100^oC$)		–	–	2.4	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2.0 Adc)		–	–	1.8	
(I_C = 10 Adc, I_B = 2.0 Adc, $T_C = 100^oC$)		–	–	1.8	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	125	–	500	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 10 μs, Duty Cycle ⩽ 2.0%)	t_d	–	0.02	0.1	μs
Rise Time	t_r	–	0.3	0.7	μs
Storage Time	t_s	–	1.6	4.0	μs
Fall Time	t_f	–	0.3	0.7	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, $T_C = 100^oC$)	t_{sv}	–	2.5	5.0	μs
Crossover Time	t_c	–	0.8	2.0	μs
Storage Time (I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, $T_C = 25^oC$)	t_{sv}	–	1.8	–	μs
Crossover Time	t_c	–	0.4	–	μs
Fall Time	t_{fi}	–	0.2	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ⩽ 2%.

1.3

FIGURE 1 — DC CURRENT GAIN

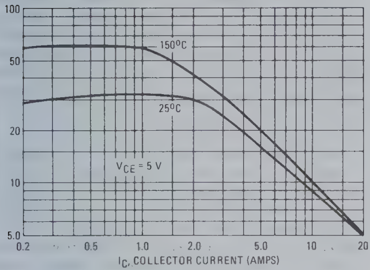


FIGURE 2 — COLLECTOR SATURATION REGION

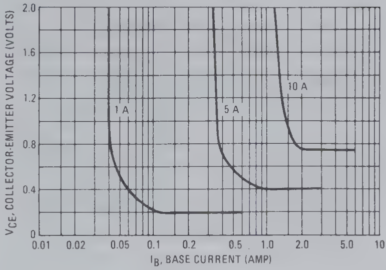


FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION

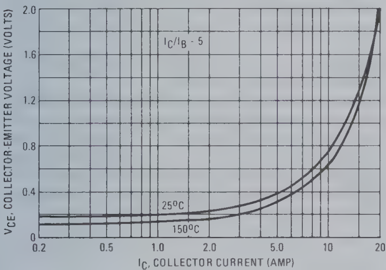


FIGURE 4 — BASE-EMITTER VOLTAGE

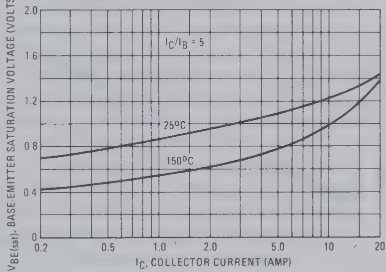


FIGURE 5 — COLLECTOR CUTOFF REGION

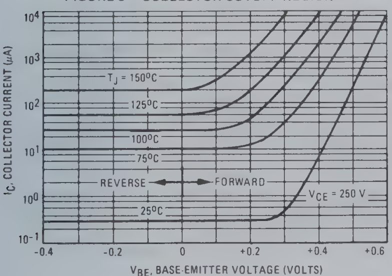


FIGURE 6 — CAPACITANCE

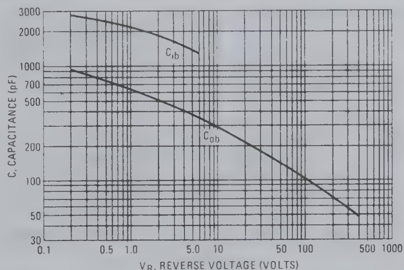


FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

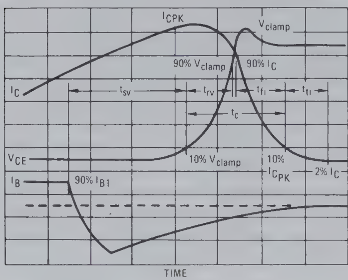
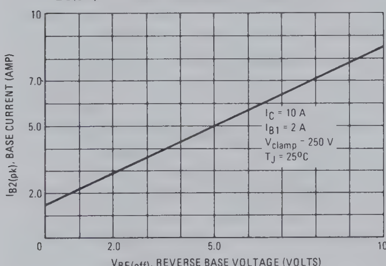


FIGURE 8 — REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 — TURN-ON SWITCHING TIMES

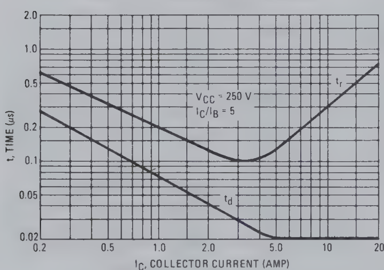
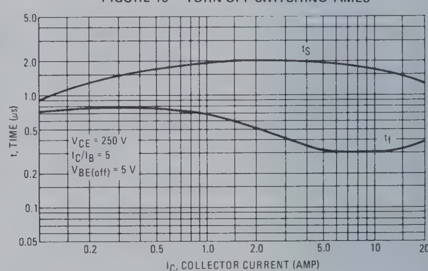


FIGURE 10 — TURN-OFF SWITCHING TIMES



1.3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

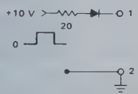
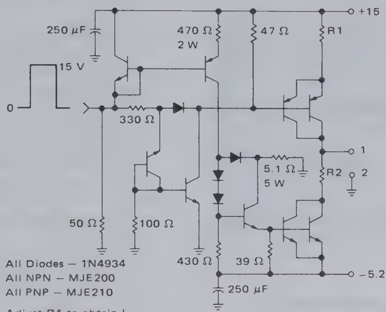
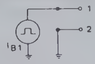
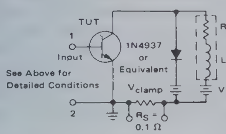
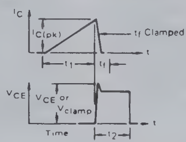
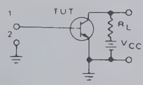
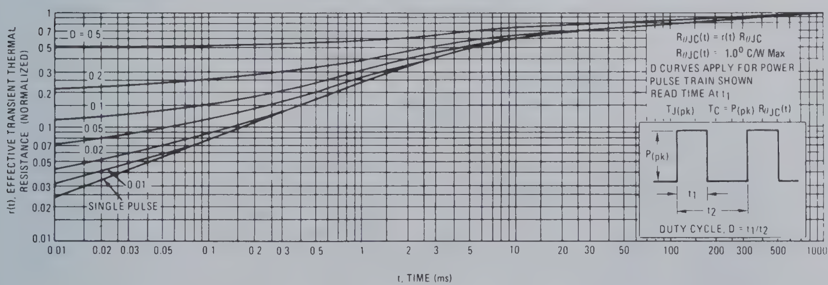
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes — 1N4934 All NPN — MJE200 All PNP — MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 11 — THERMAL RESPONSE



1.3

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

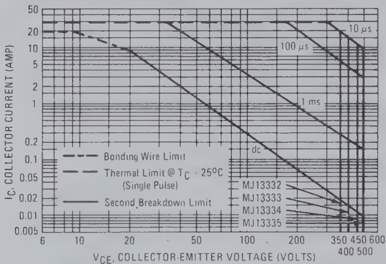
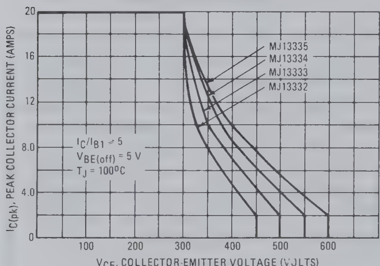


FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

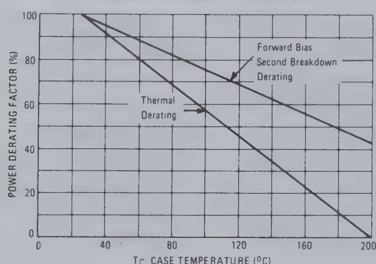
The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 — POWER DERATING



NPN PNP

MJ14000 MJ14001
MJ14002 MJ14003

MOTOROLA

1.3

HIGH-CURRENT COMPLEMENTARY SILICON POWER TRANSISTORS

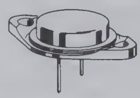
. . . designed for use in high-power amplifier and switching circuit applications.

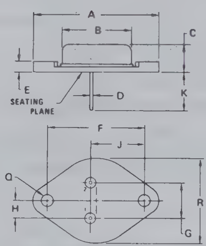
- High Current Capability — I_C Continuous = 60 Amperes
- DC Current Gain — h_{FE} = 15-100 @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C = 50 Adc

60 AMPERES

COMPLEMENTARY SILICON POWER TRANSITORS

60-80 VOLTS
300 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-204AE

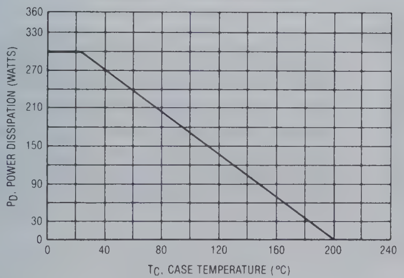
MAXIMUM RATINGS

Rating	Symbol	MJ14000 MJ14001	MJ14002 MJ14003	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CBO}	60	80	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector Current — Continuous	I_C	60		Adc
Base Current — Continuous	I_B	15		Adc
Emitter Current — Continuous	I_E	75		
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.7		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.584	°C/W

FIGURE 1 — POWER DERATING



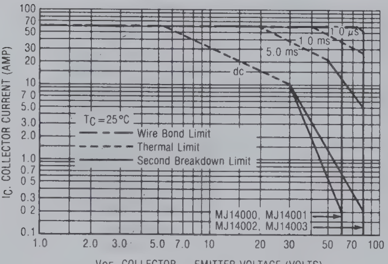
1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	MJ14000, MJ14001		60	–	
	MJ14002, MJ14003		80	–	
Collector Cutoff Current		I_{CEO}			mA
(V_{CE} = 30 Vdc, I_B = 0)	MJ14000, MJ14001		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	MJ14402, MJ14003		–	1.0	
Collector Cutoff Current		I_{CEX}			mA
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 V)	MJ14000, MJ14001		–	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 V)	MJ14002, MJ14003		–	1.0	
Collector Cutoff Current		I_{CBO}			mA
(V_{CB} = 60 Vdc, I_E = 0)	MJ14000, MJ14001		–	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	MJ14002, MJ14003		–	1.0	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	–	1.0	mA
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 25 Adc, V_{CE} = 3.0 V)			30	–	
(I_C = 50 Adc, V_{CE} = 3.0 V)			15	100	
(I_C = 60 Adc, V_{CE} = 3.0 V)			5	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			–	1	
(I_C = 50 Adc, I_B = 5.0 Adc)			–	2.5	
(I_C = 60 Adc, I_B = 12 Adc)			–	3	
Base-Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			–	2	
(I_C = 50 Adc, I_B = 5.0 Adc)			–	3	
(I_C = 60 Adc, I_B = 12 Adc)			–	4	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	2000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA



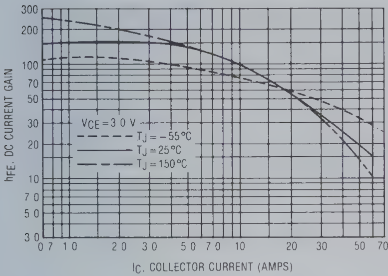
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

TYPICAL ELECTRICAL CHARACTERISTICS

NPN
MJ14000, MJ14002

FIGURE 3 — DC CURRENT GAIN



PNP
MJ14001, MJ14003

FIGURE 4 — DC CURRENT GAIN

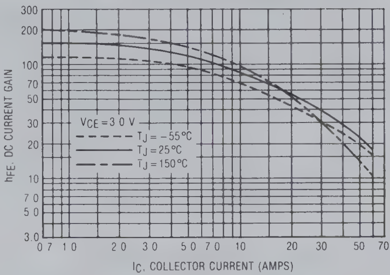


FIGURE 5 — COLLECTOR SATURATION REGION

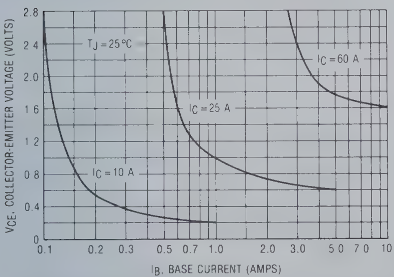


FIGURE 6 — COLLECTOR SATURATION REGION

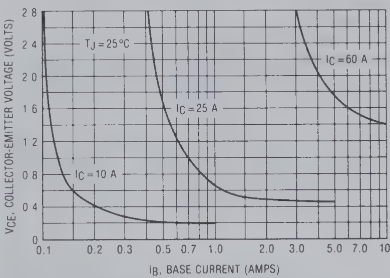


FIGURE 7 — "ON" VOLTAGES

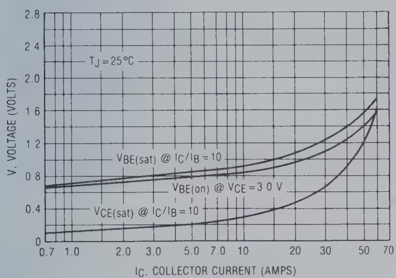


FIGURE 8 — "ON" VOLTAGES

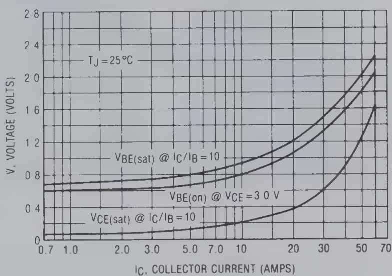


FIGURE 9 — TURN-ON SWITCHING TIMES

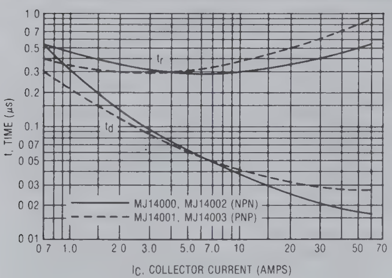


FIGURE 10 – TURN-OFF SWITCHING TIMES

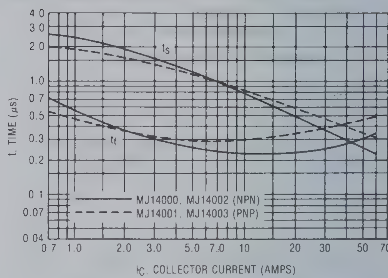


FIGURE 11 — CAPACITANCE VARIATION

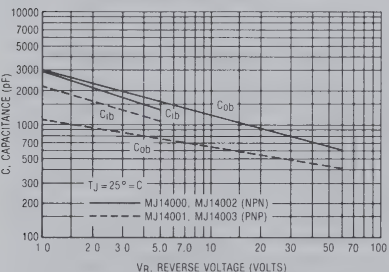
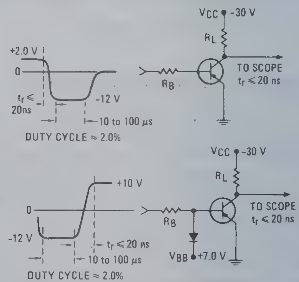
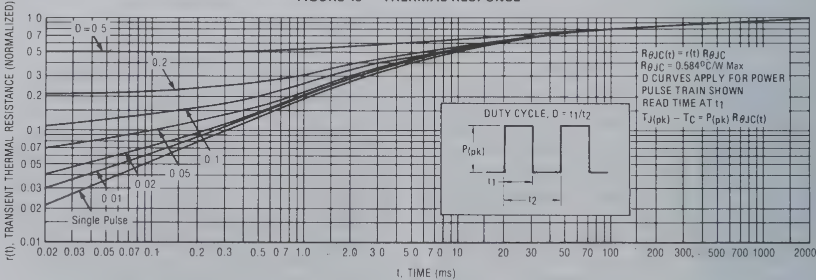


FIGURE 12 — SWITCHING TEST CIRCUIT



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

FIGURE 13 — THERMAL RESPONSE



MOTOROLA

NPN MJ15001 PNP MJ15002

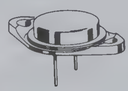
1.3

COMPLEMENTARY SILICON POWER TRANSISTORS

The MJ15001 and MJ15002 are EPIBASE power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —
  200 W @ 40 V
  50 W @ 100 V
- For Low Distortion Complementary Designs
- High DC Current Gain —
  h_{FE} = 25 (Min) @ I_C = 4 Adc

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
140 VOLTS
200 WATTS

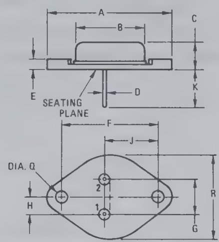


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	140	Vdc
Collector-Base Voltage	V_{CBO}	140	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current — Continuous	I_B	5	Adc
Emitter Current — Continuous	I_E	20	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	200 1.14	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for ≤10s.	T_L	265	^oC



PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

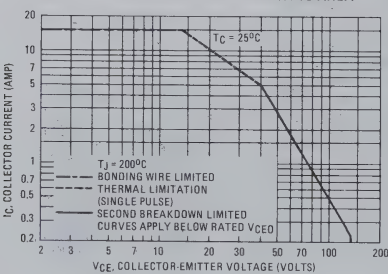
1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
Collector Cutoff Current	I_{CEX}	–		
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc)			100	μAdc
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			2	mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	–	250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$			Adc
(V_{CE} = 40 Vdc, t = 1 s (non-repetitive))		5	–	
(V_{CE} = 100 Vdc, t = 1 s (non-repetitive)		0.5	–	
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	–
Collector-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	–	1	Vdc
Base-Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	–	2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	1000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

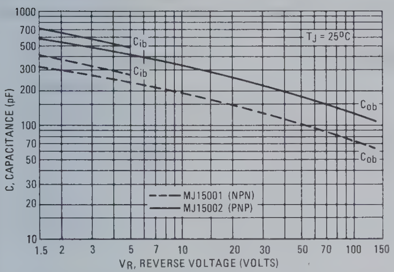


FIGURE 3 – CURRENT-GAIN – BANDWIDTH PRODUCT

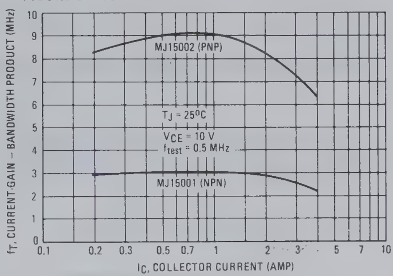
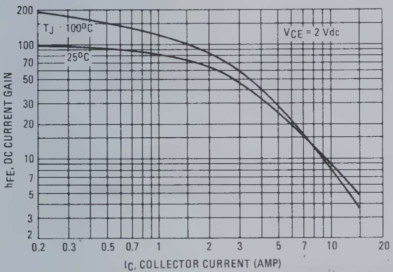


FIGURE 4 – DC CURRENT GAIN

MJ15001



MJ15002

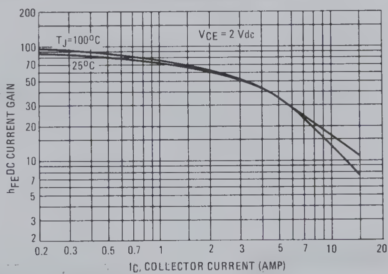
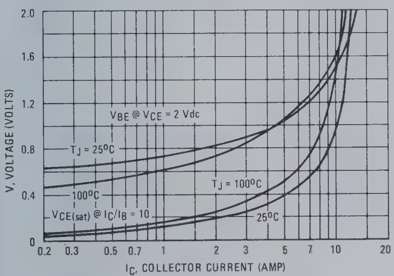
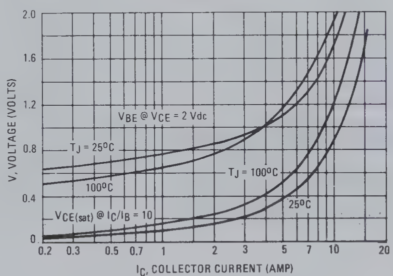


FIGURE 5 – "ON" VOLTAGE

MJ15001



MJ15002



MJ15003 NPN
MJ15004 PNP

MOTOROLA

1.3

COMPLEMENTARY SILICON POWER TRANSISTORS

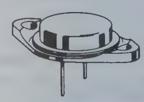
The MJ15003 and MJ15004 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) — 250 W @ 50 V
- For Low Distortion Complementary Designs
- High DC Current Gain — h_{FE} = 25 (Min) @ I_C = 5 Adc

20 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

140 VOLTS
250 WATTS

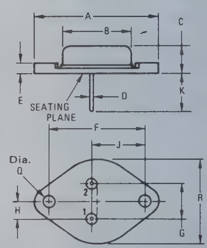


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	140	Vdc
Collector-Base Voltage	V_{CBO}	140	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current — Continuous	I_C	20	Adc
Base Current — Continuous	I_B	5	Adc
Emitter Current — Continuous	I_E	25	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	250 1.43	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/16″ from Case for ≤10s.	T_L	265	^oC



PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

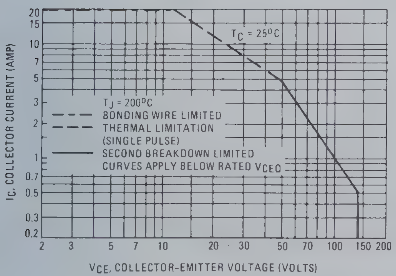
1.3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}		100 2	μAdc mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}		250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}		100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non-repetitive)) (V_{CE} = 100 Vdc, t = 1 s (non-repetitive))	$I_{S/b}$	5 1	– –	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 5 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)	$V_{CE(sat)}$		1	Vdc
Base-Emitter On Voltage (I_C = 5 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	–	2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	1000	pF

(1) Pulse Test: Pulse Width 300 μs, Duty Cycle = 2%.

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

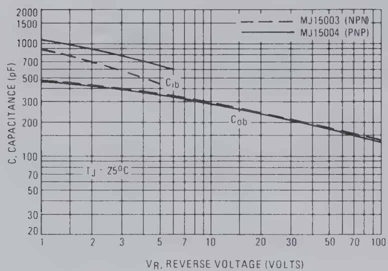


FIGURE 3 – CURRENT GAIN – BANDWIDTH PRODUCT

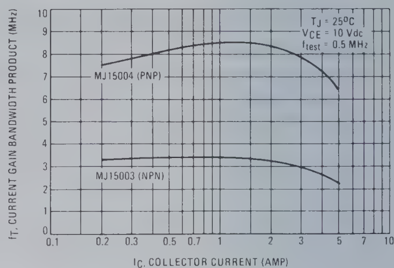
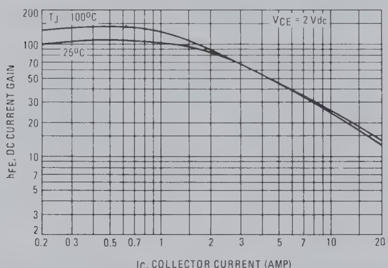


FIGURE 4 – DC CURRENT GAIN

MJ15003



MJ15004

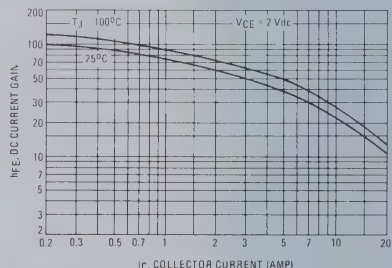
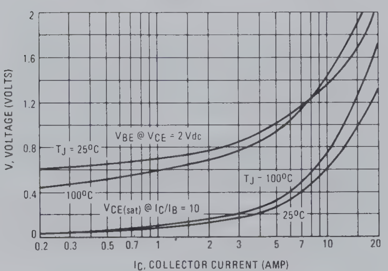
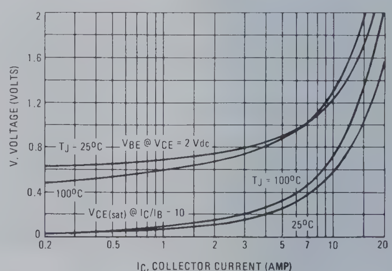


FIGURE 5 – "ON" VOLTAGE

MJ15003



MJ15004



NPN MJ15011 PNP MJ15012

MOTOROLA

1.3

Advance Information

COMPLEMENTARY SILICON POWER TRANSISTORS

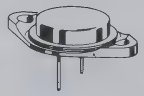
The MJ15011 and MJ15012 are PowerBase power transistors designed for high-power audio, disk head positioners, and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc-to-dc converters or inverters.

- High Safe Operating Area (100% Tested)
  1.2 A @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{FE} = 20 (Min) @ 2 A, 2 V
  $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 4 A, I_B = 0.4 A
- For Low Distortion Complementary Designs

10 AMPERE

COMPLEMENTARY POWER TRANSISTORS

250 VOLTS
200 WATTS



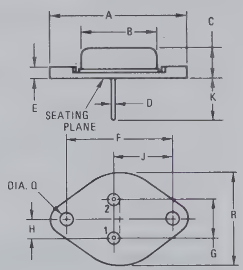
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector-Emitter Voltage	V_{CEX}	250	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 15	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 5	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes	T_L	265	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

This is advance information and specifications are subject to change without notice.

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 100 mA)	$V_{CEO(sus)}$	250	–	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc)	I_{CEO}	–	1	mAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	500	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc)	I_{EBO}	–	500	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
(I_C = 2 Adc, V_{CE} = 2 Vdc)		20	100	
(I_C = 4 Adc, V_{CE} = 2 Vdc)		5	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 2 Adc, I_B = 0.2 Adc)		–	0.8	
(I_C = 4 Adc, I_B = 0.4 Adc)		–	2.5	
Base-Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	–	2	Vdc
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, f = 1 MHz)	C_{ob}	–	750	pF
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$			Adc
(V_{CE} = 40 Vdc, t = 0.5 s)		5		
(V_{CE} = 100 Vdc, t = 0.5 s)		1.4	–	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – DC CURRENT GAIN

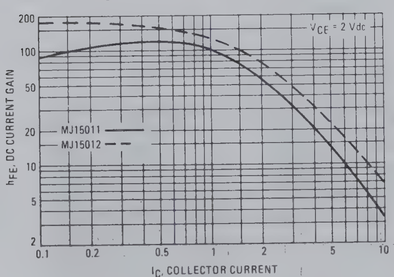
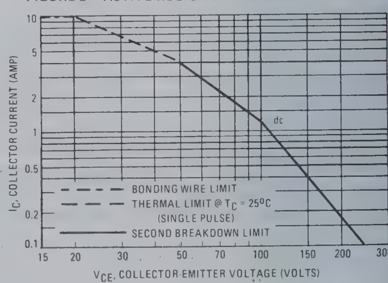


FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



MOTOROLA

NPN MJ15022 MJ15024

1.3

SILICON POWER TRANSISTORS

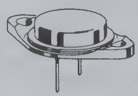
The MJ15022 and MJ15024 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

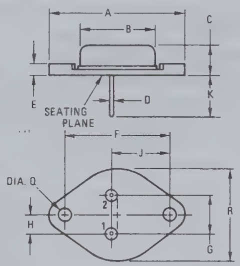
- High Safe Operating Area (100% Tested) — 2 A @ 80 V
- High DC Current Gain — h_{FE} = 15 (Min) @ I_C = 8 Adc

16 AMPERE

SILICON POWER TRANSISTORS

200 and 250 VOLTS
250 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.

CASE 1-04
(TO-204AA)

MAXIMUM RATINGS

Rating	Symbol	MJ15022	MJ15024	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Base Voltage	V_{CBO}	350	400	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector-Emitter Voltage	V_{CEX}	400		Vdc
Collector Current — Continuous Peak (1)	I_C	16 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	250 1.43		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	$^oC/W$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

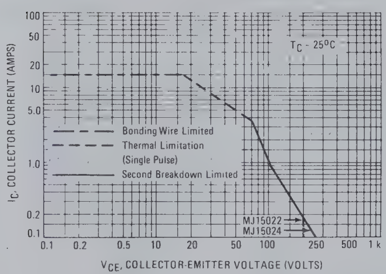
1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			
(I_C = 100 mAdc, I_B = 0)	MJ15022		200	–	
	MJ15024		250	–	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15022		–	250	μAdc
(V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15024		–	250	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 150 Vdc, I_B = 0)	MJ15022		–	500	
(V_{CE} = 200 Vdc, I_B = 0)	MJ15024		–	500	
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_B = 0)	Both	I_{EBO}	–	500	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$			Adc
(V_{CE} = 50 Vdc, t = 0.5 s (non-repetitive))			5	–	
(V_{CE} = 80 Vdc, t = 0.5 s (non-repetitive))			2	–	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 8 Adc, V_{CE} = 4 Vdc)			15	60	
(I_C = 16 Adc, V_{CE} = 4 Vdc)			5	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)			–	1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)				4.0	
Base-Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	–	2.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	–	500	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ⩽ 2%.

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

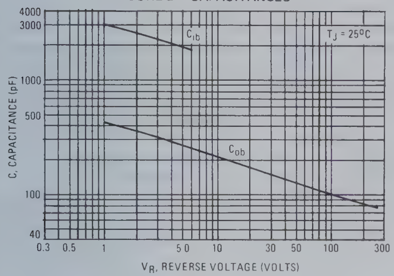


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

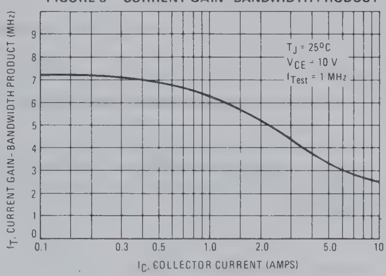


FIGURE 4 – DC CURRENT GAIN

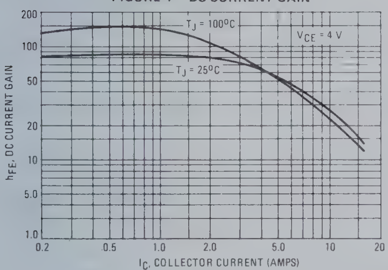


FIGURE 5 – "ON" VOLTAGE

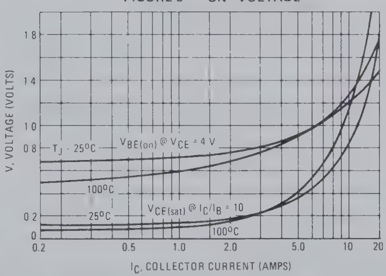
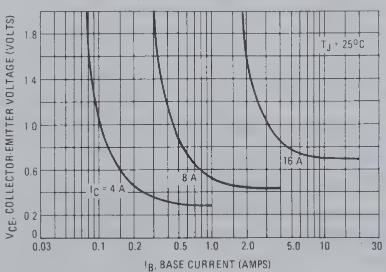


FIGURE 6 – COLLECTOR SATURATION REGION



PNP

MJ15023
MJ15025

MOTOROLA

1.3

SILICON POWER TRANSISTORS

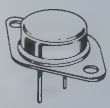
The MJ15023 and MJ15025 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

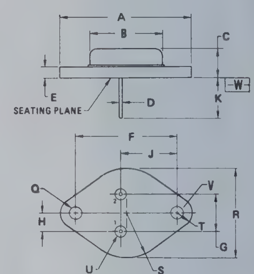
- High Safe Operating Area (100% Tested) — 2 A @ 80 V
- High DC Current Gain — h_{FE} = 15 (Min) @ I_C = 8 Adc

16 AMPERE

SILICON POWER TRANSISTORS

200 and 250 VOLTS
250 WATTS





STYLE 1
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

NOTE.
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

CASE 1-04
(TO-204AA)

MAXIMUM RATINGS

Rating	Symbol	MJ15023	MJ15025	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Base Voltage	V_{CBO}	350	400	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector-Emitter Voltage	V_{CEX}	400		Vdc
Collector Current — Continuous Peak (1)	I_C	16 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Power Dissipation @ $T_C = 25^{\circ}C$ Derate above $25^{\circ}C$	P_D	250 1.43		Watts $W/^{\circ}C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^{\circ}C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	$^{\circ}C/W$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

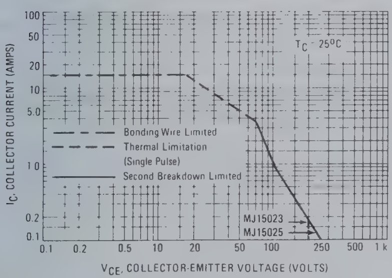
1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			
(I_C = 100 mAdc, I_B = 0)	MJ15023		200	–	
	MJ15025		250	–	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15023		-	250	μAdc
(V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15025		–	250	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 150 Vdc, I_B = 0)	MJ15023		–	500	
(V_{CE} = 200 Vdc, I_B = 0)	MJ15025		–	500	
Emitter Cutoff Current		I_{EBO}		500	μAdc
(V_{CE} = 5 Vdc, I_B = 0)	Both				
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$			Adc
(V_{CE} = 50 Vdc, t = 0.5 s (non-repetitive))			5	-	
(V_{CE} = 80 Vdc, t = 0.5 s (non-repetitive))			2	–	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 8 Adc, V_{CE} = 4 Vdc)			15	60	
(I_C = 16 Adc, V_{CE} = 4 Vdc)			5	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)				1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)				4.0	
Base-Emitter On Voltage		$V_{BE(on)}$	–	2.2	Vdc
(I_C = 8 Adc, V_{CE} = 4 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	4	–	MHz
(I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)					
Output Capacitance		C_{ob}	–	600	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

1.3

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

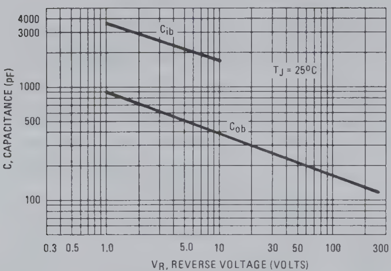


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

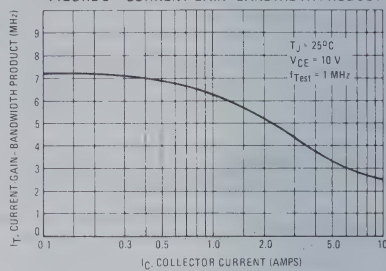


FIGURE 4 – DC CURRENT GAIN

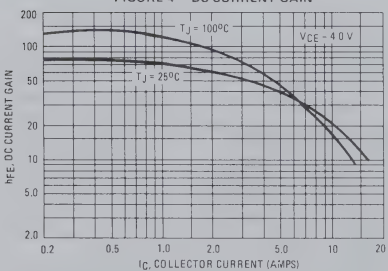
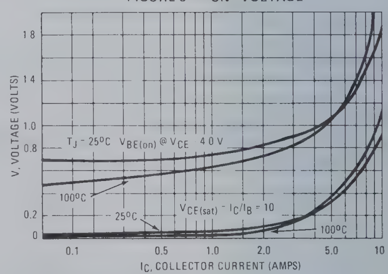


FIGURE 5 – "ON" VOLTAGE



MOTOROLA

MJ15026 NPN
MJ15027 PNP

SILICON POWER TRANSISTORS

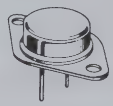
The MJ15026 and MJ15027 are PowerBase transistors designed for high power audio, disk head positioners and other linear applications.

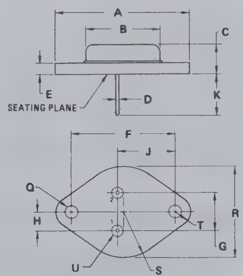
- High Gain, Complimentary Silicon Power Transistors for Audio and Other Power Amplifiers
- High Safe Operating Area (100% Tested)
  50 V — 5.0 A
  80 V — 2.0 A
- Excellent Frequency Response
  f_T = 24 MHz (Typ)

16 AMPERE

SILICON POWER TRANSISTORS

200 VOLTS
NPN and PNP





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	200	Vdc
Collector-Base Voltage	V_{CBO}	200	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak (1)	I_C	16 32	Adc
Base Current — Continuous	I_B	70	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

(1) Pulse Test: Pulse Width =5.0 ms, Duty Cycle ≤ 10%.

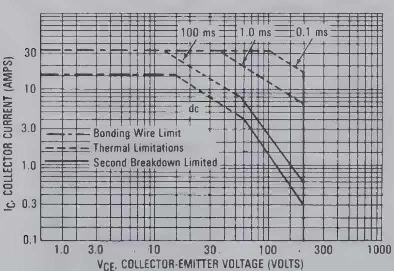
1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 20 mA, I_B = 0)	$V_{CEO(sus)}$	200	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	1.0	mA
Collector Cutoff Current (V_{CE} = 120 Vdc, I_B = 0)	I_{CEO}	—	1.0	mA
Emitter Cutoff Current (V_{CE} = 5.0 V, I_B = 0)	I_{EBO}	—	1.0	mA
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward-Biased	$I_{S/b}$			Adc
(V_{CE} = 50 Vdc, t = 0.5 s (non-repetitive))	—	5.0		
(V_{CE} = 80 Vdc, t = 0.5 s (non-repetitive))	—	2.0		
***ON CHARACTERISTICS**				
DC Current Gain	h_{FE}			—
(I_C = 5.0 Adc, V_{CE} = 5.0 V)		25	150	
(I_C = 16 Adc, V_{CE} = 5.0 V)		6.0	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)		—	1.0	
I_C = 16 Adc, I_B = 4.0 Adc)		—	3.0	
Base-Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(sat)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	15	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)	C_{ob}	—	750	pF

(1) **Pulse Test: Pulse Width** = 300 μs, Duty Cycle ≤ 2%

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL ELECTRICAL CHARACTERISTICS

MJ15026 NPN

FIGURE 2 — DC CURRENT GAIN

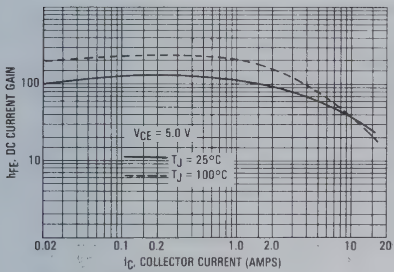


FIGURE 4 — COLLECTOR SATURATION REGION

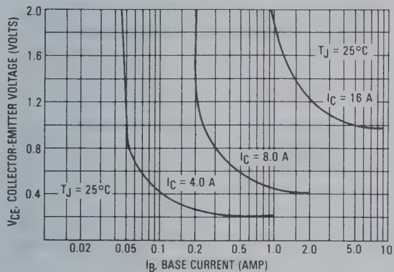
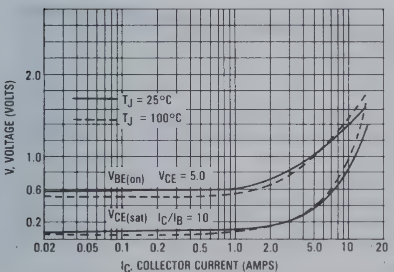


FIGURE 6 — "ON" VOLTAGE



MJ15027 PNP

FIGURE 3 — DC CURRENT GAIN

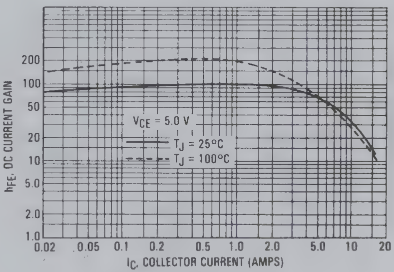


FIGURE 5 — COLLECTOR SATURATION REGION

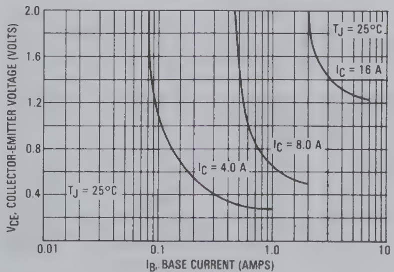
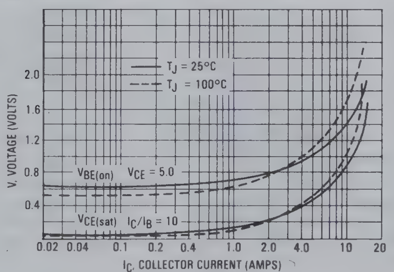


FIGURE 7 — "ON" VOLTAGE

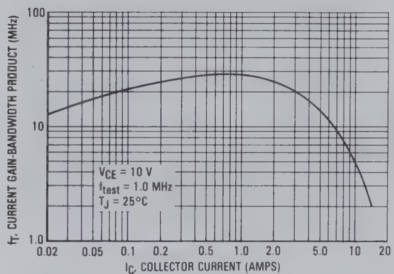


1.3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ15026 NPN

FIGURE 8 — CURRENT GAIN-BANDWIDTH PRODUCT



MJ15027 PNP

FIGURE 9 — CURRENT GAIN-BANDWIDTH PRODUCT

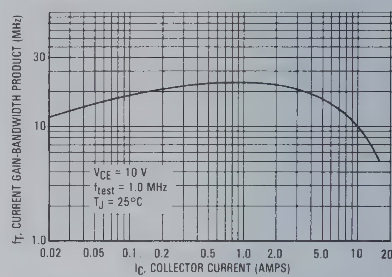


FIGURE 10 — CAPACITANCE VARIATION

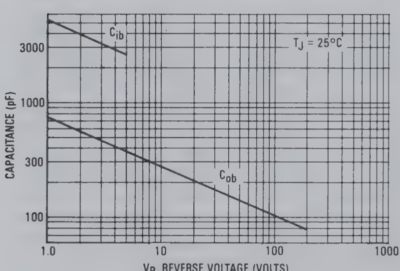


FIGURE 11 — CAPACITANCE VARIATION

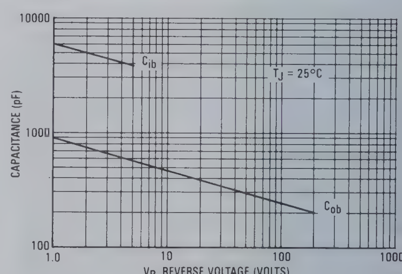
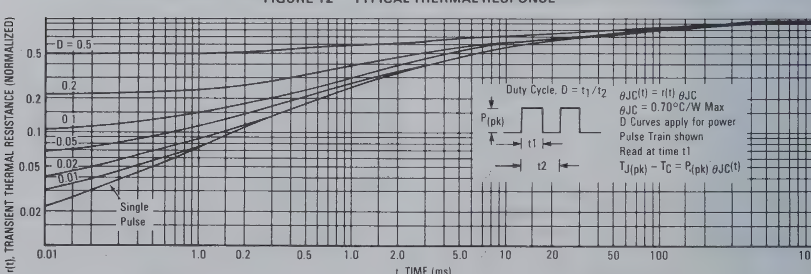


FIGURE 12 — TYPICAL THERMAL RESPONSE



MJ16002
MJ16004

MOTOROLA

1.3

Designers Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16004 is a selected high-gain version of the MJ16002 for applications where drive current is limited.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  50 ns Inductive Fall Time — 75°C (Typ)
  70 ns Inductive Crossover Time — 75°C (Typ)
  500 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range −65 to +200°C
- 100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents

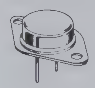
5 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



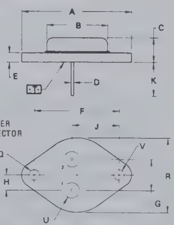
MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 10	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4.0 8.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	125 71.5 0.714	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ⩽ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

⌖	⌀0.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS.

⌖	⌀0.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21 08	–	0 830
C	6.35	7 62	0 250	0 300
D	0.97	1 09	0 038	0 043
E	1 40	1 78	0 055	0.070
F	30.15 BSC		1 187 BSC	
G	10.92 BSC		0.430 BSC	
H	5 46 BSC		0 215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0 480
Q	3.81	4.19	0 150	0 165
R		26.67	–	1.050
U	4.83	5 33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3 TYPE

1.3

MJ16002

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)							
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 16			
ON CHARACTERISTICS (1)							
Collector-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 0.2 Adc) (I_C = 3.0 Adc, I_B = 0.4 Adc) (I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)			$V_{CE(sat)}$	— — —	— — —	1.0 2.5 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.4 Adc) (I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)			$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc			h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	—	—	200	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ⩽2.0%)	(I_{B2} = 0.8 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100	ns
Rise Time			t_r	—	100	300	
Storage Time			t_s	—	1000	3000	
Fall Time			t_f	—	60	300	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	400	—	
Fall Time			t_f	—	130	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	500	1600	ns
Fall Time			t_{fi}	—	100	200	
Crossover Time			t_c	—	120	250	
Storage Time		(T_J = 150°C)	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ⩽2%.

$^{*}\beta_f = \frac{I_C}{I_{B1}}$

1.3

MJ16004

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)							
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 16			
ON CHARACTERISTICS (1)							
Collector-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 0.15 Adc) (I_C = 3.0 Adc, I_B = 0.3 Adc) (I_C = 3.0 Adc, I_B = 0.3 Adc, T_C = 100°C)			$V_{CE(sat)}$	— — —	— — —	1.0 2.5 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc) (I_C = 3.0 Adc, I_B = 0.3 Adc, T_C = 100°C)			$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc			h_{FE}	7.0	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	—	—	200	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.3 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 0.6 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100	ns
Rise Time			t_r	—	130	300	
Storage Time			t_s	—	800	2700	
Fall Time			t_f	—	80	350	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	250	—	
Fall Time			t_f	—	60	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.3 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	400	1300	ns
Fall Time			t_{fi}	—	80	150	
Crossover Time			t_c	—	90	200	
Storage Time		(T_J = 150°C)	t_{sv}	—	450	—	
Fall Time			t_{fi}	—	100	—	
Crossover Time			t_c	—	110	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$^*\beta_f = \frac{I_C}{I_{B1}}$

1.3

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

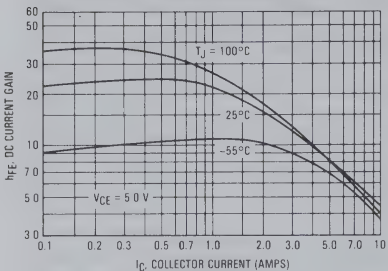


FIGURE 2 — COLLECTOR SATURATION REGION

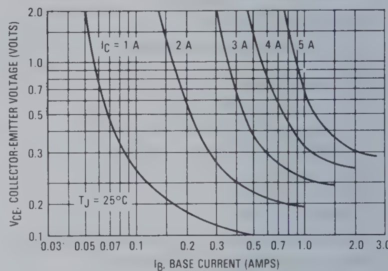


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

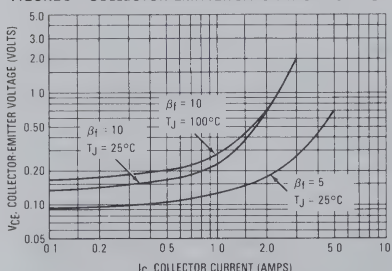


FIGURE 4 — BASE-EMITTER VOLTAGE

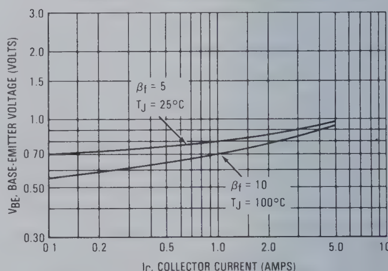


FIGURE 5 — COLLECTOR CUTOFF REGION

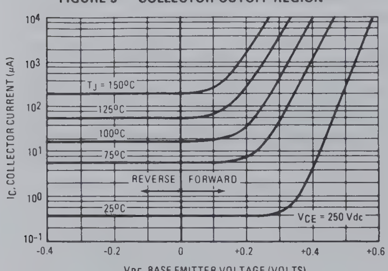
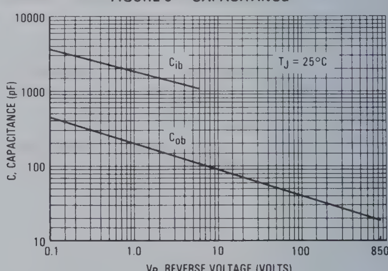


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

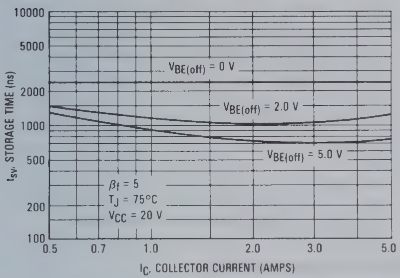


FIGURE 8 — STORAGE TIME

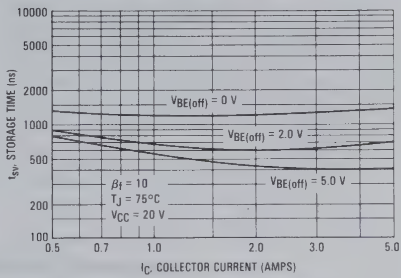


FIGURE 9 — COLLECTOR CURRENT FALL TIME

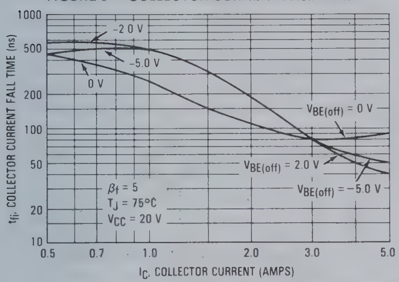


FIGURE 10 — COLLECTOR CURRENT FALL TIME

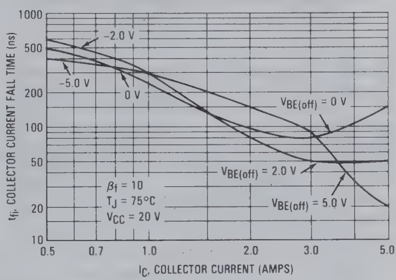


FIGURE 11 — CROSSOVER TIME

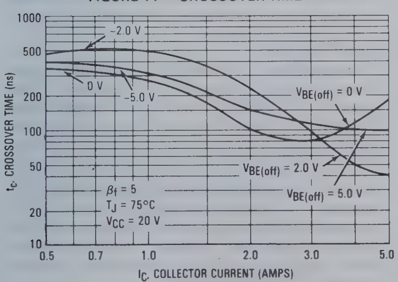
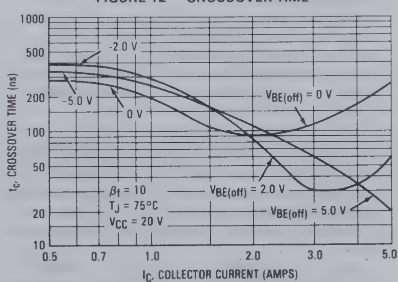


FIGURE 12 — CROSSOVER TIME



1.3

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

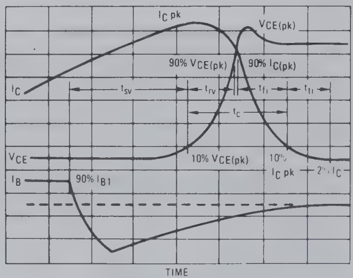
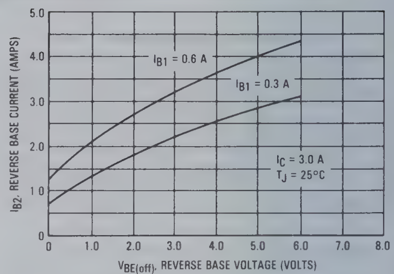


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

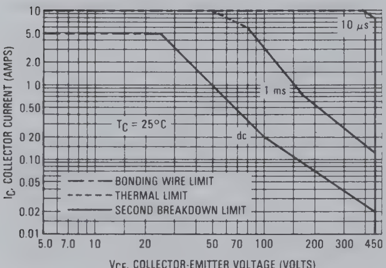
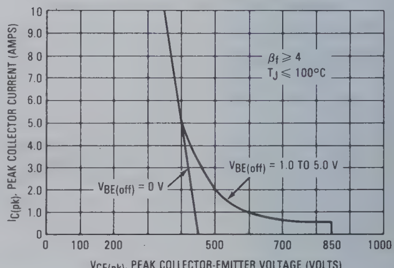


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

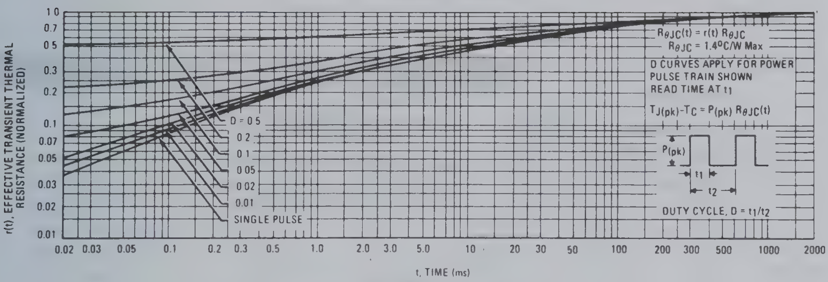


FIGURE 18 — POWER DERATING

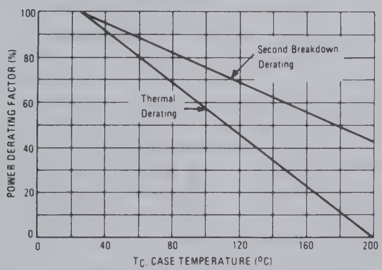
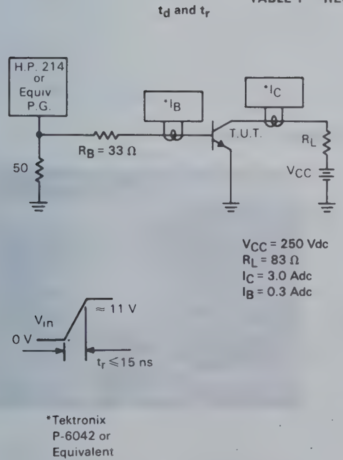
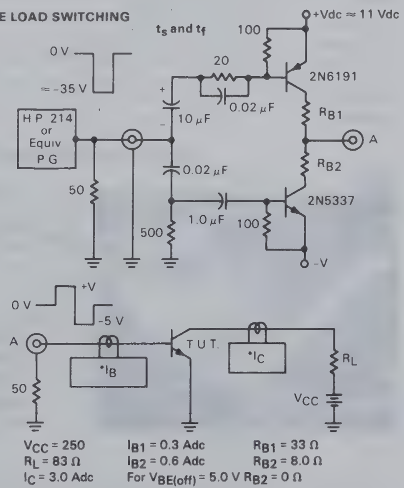


TABLE 1 — RESISTIVE LOAD SWITCHING

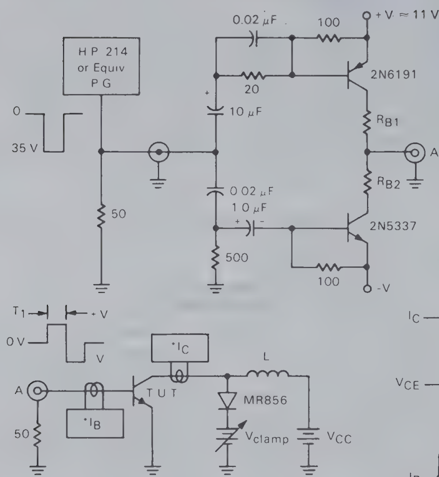


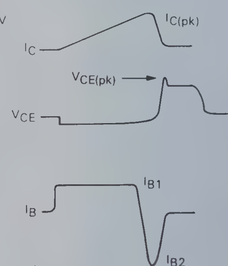


*Note: Adjust $-V$ to obtain desired $V_{BE(off)}$ at Point A.

1.3

TABLE 2 — INDUCTIVE LOAD SWITCHING





$T_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

BV_{CEO}
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

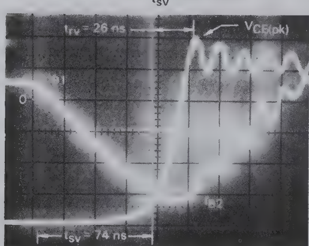
*Tektronix
P-6042 or
Equivalent

Scope - Tektronix
7403 or
Equivalent

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

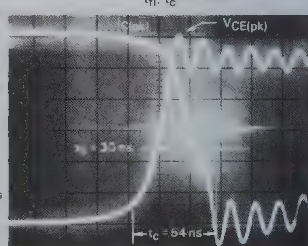
TYPICAL INDUCTIVE SWITCHING WAVEFORMS

t_{sv}



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.3 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 300 Volts
T_C = 25°C
Time Base =
20 ns/cm

t_{fi}, t_c



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.3 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 300 Volts
T_C = 25°C
Time Base =
20 ns/cm

MJ16002A
MJH16002A

MOTOROLA

1.3

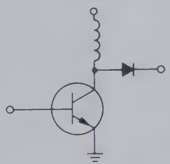
Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Features:

- Fast Turn-Off Times
  - 100 ns Inductive Fall Time — 100°C (Typ)
  - 120 ns Inductive Crossover Time — 100°C (Typ)
  - 500 ns Inductive Storage Time — 100°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

5.0 AMPERE

NPN SILICON POWER TRANSISTORS

1000 VOLTS
125 WATTS

MAXIMUM RATINGS

Rating	Symbol	Max		Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	500		Vdc
Collector-Emitter Voltage	V_{CEV}	1000		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5 0 10		Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	4 0 8 0		Adc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C
		MJ16002A	MJH16002A	
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	125 71.5 0.714	100 40 0 833	Watts W/°C

THERMAL CHARACTERISTICS

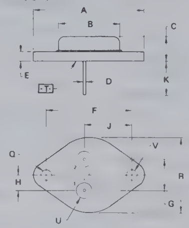
Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1 4	1 25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	275	°C

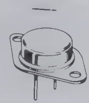
(1) Pulse Test Pulse Width = 5 ms, Duty Cycle ≤ 10%

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design

MJ16002A





STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

NOTES
1 DIMENSIONS Q AND V ARE DATUMS
2 [T] IS SEATING PLANE AND DATUM
3 POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

⌖	⌀ 13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS

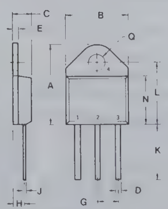
⌖	⌀ 13 (0 005) Ⓜ T	V Ⓜ	Q Ⓜ

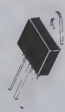
4 DIMENSIONS AND TOLERANCES PER ANSI Y14 5 1973

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37	–	1 550
B		21.08	–	0.830
C	6 35	7.62	0.250	0.300
D	0 97	1.09	0.038	0 043
E	1 40	1.78	0.055	0 070
F	30 15 BSC		1.187 BSC	
G	10 92 BSC		0.430 BSC	
H	5 46 BSC		0.215 BSC	
J	16 89 BSC		0.665 BSC	
K	11 18	12.19	0.440	0 480
Q	3 81	4.19	0.151	0 165
R		26.67	–	1.050
U	4 83	5.33	0.190	0.210
V	3 81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(Formerly TO-3)

MJH16002A





STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20 32	21 08	0 800	0 830
B	15 49	15 90	0 610	0 626
C	4 19	5 08	0 165	0 200
D	1 02	1 65	0 040	0 065
E	1 35	1 65	0 053	0 065
G	5 21	5 72	0 205	0 225
H	2 41	3 20	0 095	0 126
J	0 38	0 64	0 015	0 025
K	12 70	15 49	0 500	0 610
L	15 88	16 51	0 625	0 650
N	12 19	12 70	0 480	0 500
Q	4 04	4 22	0 159	0 166

CASE 340-01
TO-218AC
PLASTIC PACKAGE

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 0.2 Adc) (I_C = 3.0 Adc, I_B = 0.4 Adc) (I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	— — —	1.0 2.5 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.4 Adc) (I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc	h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	200	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 0.8 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100	ns
Rise Time			t_r	—	100	300	
Storage Time			t_s	—	1000	3000	
Fall Time			t_f	—	60	300	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	400	—	
Fall Time			t_f	—	130	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	500	1600	ns
Fall Time			t_{fi}	—	100	200	
Crossover Time			t_c	—	120	250	
Storage Time		(T_J = 150°C)	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

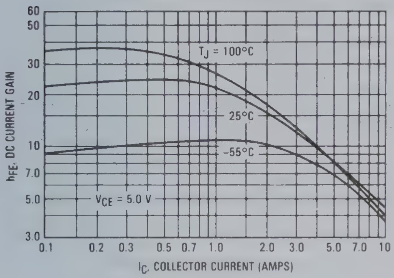


FIGURE 2 — COLLECTOR SATURATION REGION

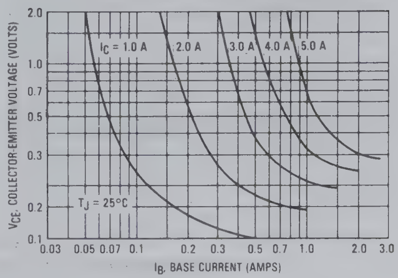


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

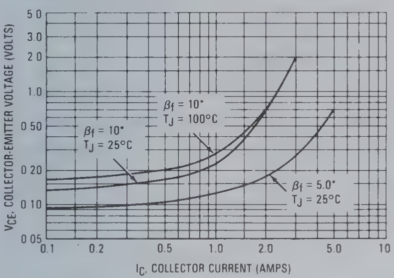


FIGURE 4 — BASE-EMITTER VOLTAGE

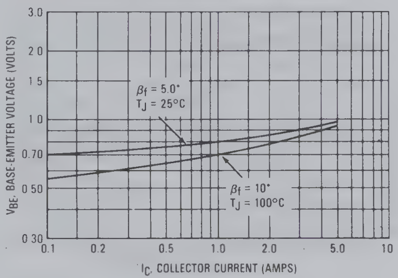


FIGURE 5 — COLLECTOR CUTOFF REGION

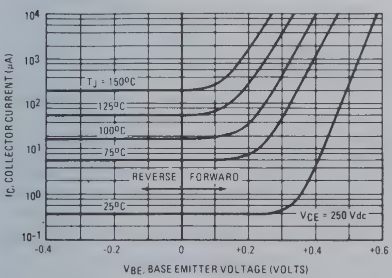
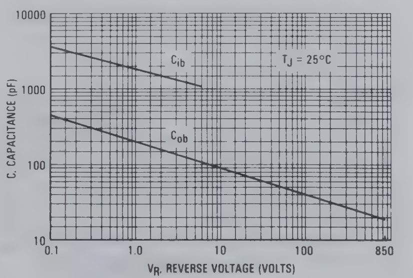


FIGURE 6 — CAPACITANCE



$*\beta_f = \frac{I_C}{I_{B1}}$

1.3

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

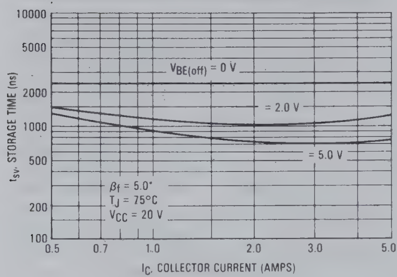


FIGURE 8 — STORAGE TIME

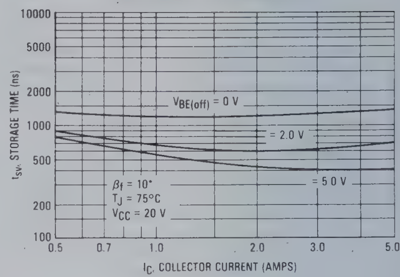


FIGURE 9 — COLLECTOR CURRENT FALL TIME

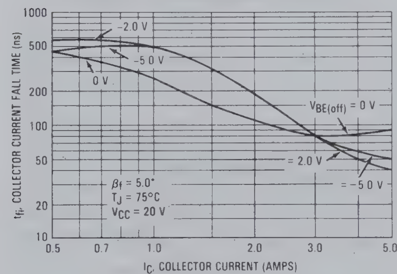


FIGURE 10 — COLLECTOR CURRENT FALL TIME

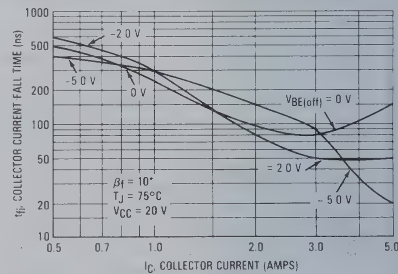


FIGURE 11 — CROSSOVER TIME

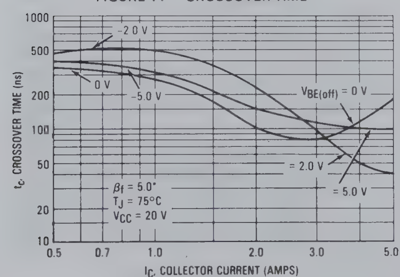
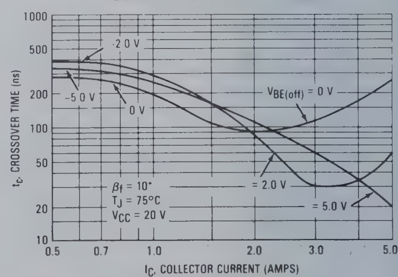


FIGURE 12 — CROSSOVER TIME



$^*\beta_f = \frac{I_C}{I_{B1}}$

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

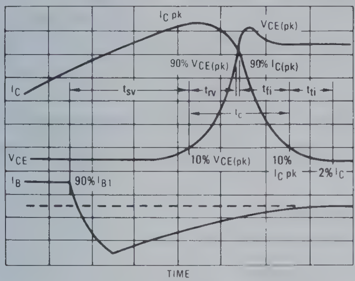
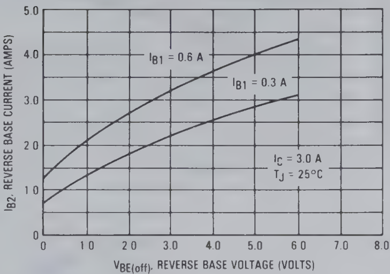


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

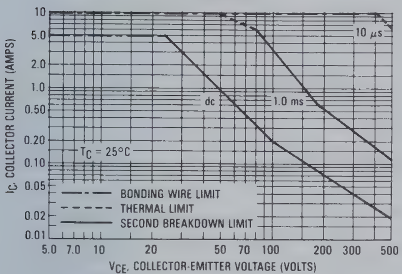
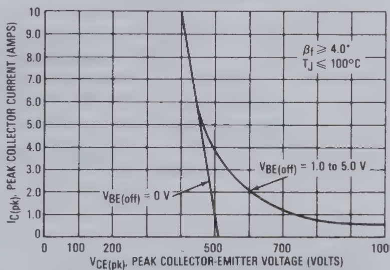


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



$*\beta_f = \frac{I_C}{I_{B1}}$

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

1.3

FIGURE 17 — THERMAL RESPONSE

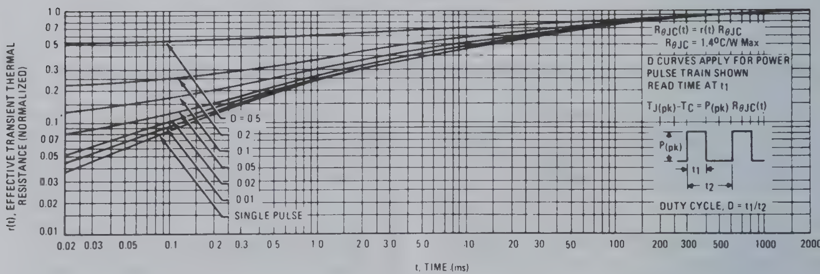


FIGURE 18 — POWER DERATING

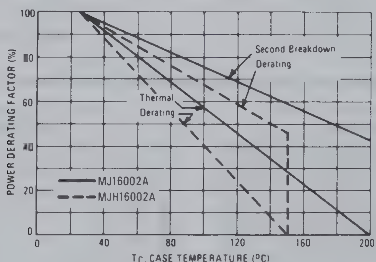
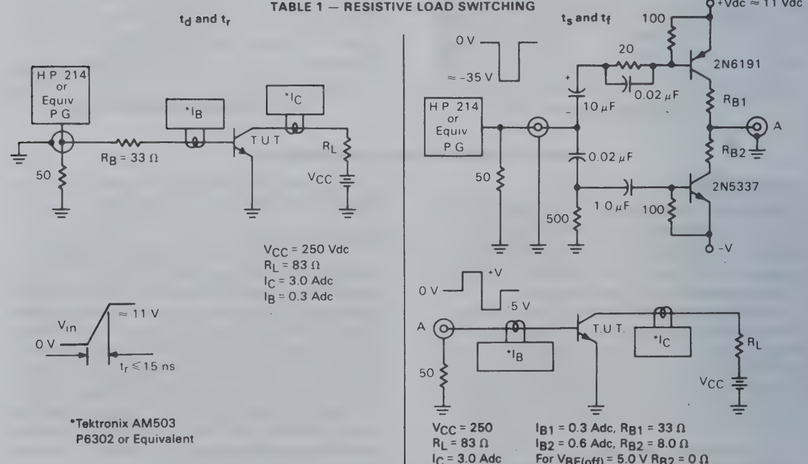
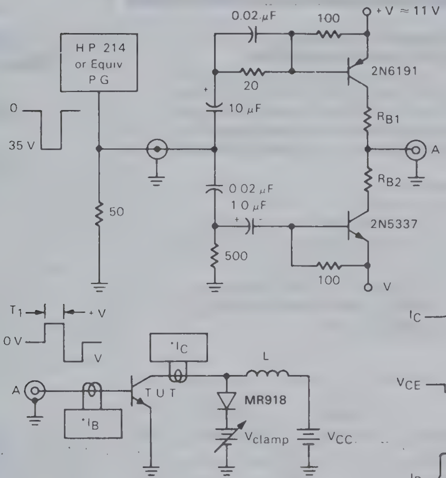


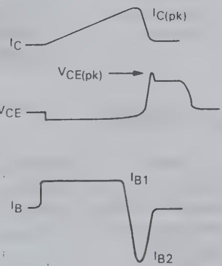
TABLE 1 — RESISTIVE LOAD SWITCHING



Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING





$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$BV_{CEO(sus)}$
$L = 10$ mH
$R_{B2} = \infty$
$V_{CC} = 20$ Volts
$I_{C(pk)} = 100$ mA

*Tektronix AM503
P6302 or Equivalent

Inductive Switching
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

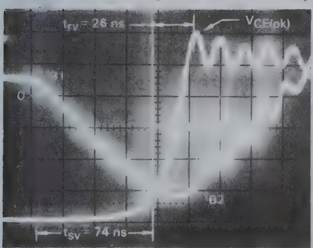
Scope — Tektronix
7403 or Equivalent

RBSOA
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

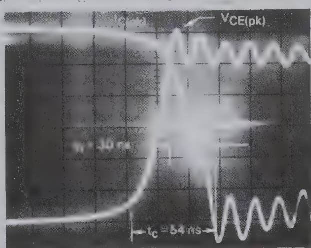
TYPICAL INDUCTIVE SWITCHING WAVEFORMS

t_{sv}



$I_{C(pk)} = 3.0$ Amps
$I_{B1} = 0.3$ Amp
$V_{BE(off)} = 5.0$ Volts
$V_{CE(pk)} = 300$ Volts
$T_C = 25°C$
Time Base =
20 ns/cm

t_{fi}, t_c



$I_{C(pk)} = 3.0$ Amps
$I_{B1} = 0.3$ Amp
$V_{BE(off)} = 5.0$ Volts
$V_{CE(pk)} = 300$ Volts
$T_C = 25°C$
Time Base =
20 ns/cm

MJ16006
MJ16008
MJH16006
MJH16008

MOTOROLA

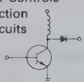
1.3

Designers Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16008 and MJH16008 are selected high gain versions of the MJ16006 and MJH16006 for applications where drive current is limited.

Typical Applications:
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits



Features:
- Fast Turn-Off Times
  - 70 ns Inductive Fall Time – 100°C (Typ)
  - 100 ns Inductive Crossover Time – 100°C (Typ)
  - 500 ns Inductive Storage Time – 100°C (Typ)
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Load
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

8.0 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
125 AND 150 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJ16006 MJ16008	MJH16006 MJH16008	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450		Vdc
Collector-Emitter Voltage	V_{CEV}	850		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8.0 16		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6.0 12		Adc
Total Device Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	 150 85.5 0.86	 125 50 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	–55 to 150	°C

THERMAL CHARACTERISTICS

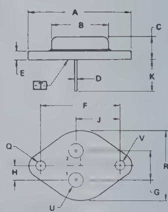
Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	1.0	°C/W
Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds.	T_L	275		°C

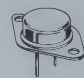
(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit Curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MJ16006
MJ16008





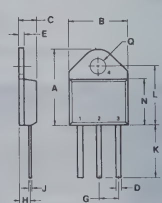
STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   | ⌖ | ϕ0.13 (0.005) Ⓜ | T | V Ⓜ |
   FOR LEADS.
   | ⌖ | ϕ0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B		21.08	–	0.830
C	6 35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1 187 BSC	
G	10 92 BSC		0 430 BSC	
H	5 46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0 440	0.480
Q	3 81	4.19	0.151	0.165
R	-	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(Formerly TO-3)

MJH16006
MJH16008



1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20 32	21 08	0 800	0 830
B	15 49	15 90	0 610	0 626
C	4 19	5 08	0 165	0 200
D	1 02	1 65	0 040	0 065
E	1 35	1 65	0 053	0 065
G	5 21	5 72	0 205	0 225
H	2 41	3 20	0.095	0.126
J	0 38	0 64	0 015	0 025
K	12 70	15 49	0 500	0 610
L	15 88	16 51	0 625	0 650
N	12.19	12 70	0 480	0 500
Q	4 04	4 22	0 159	0 166

CASE 340-01
TO-218AC

MJ16006
MJH16006

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.25	
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 3.0 Adc, I_B = 0.4 Adc)		—	—	2.5	
(I_C = 5.0 Adc, I_B = 0.66 Adc)		—	—	3.0	
(I_C = 5.0 Adc, I_B = 0.66 Adc, T_C = 100°C)		—	—	3.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 5.0 Adc, I_B = 0.66 Adc)		—	—	1.5	
(I_C = 5.0 Adc, I_B = 0.66 Adc, T_C = 100°C)		—	—	1.5	
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 5.0 Vdc	h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	350	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 5.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.66 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 1.3 Adc, R_{B2} = 4.0 Ω)	t_d	—	20	50	ns
Rise Time			t_r	—	85	250	
Storage Time			t_s	—	1000	2500	
Fall Time			t_f	—	70	250	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	500	—	
Fall Time			t_f	—	100	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 5.0 Adc, I_{B1} = 0.66 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	700	1800	ns
Fall Time			t_{fi}	—	80	200	
Crossover Time			t_c	—	150	250	
Storage Time		(T_J = 150°C)	t_{sv}	—	800	—	
Fall Time			t_{fi}	—	80	—	
Crossover Time			t_c	—	200	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

1.3

MJ16008
MJH16008

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)			I_{CEV}	—	—	0.25	mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)				—	—	1.5	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 16			
ON CHARACTERISTICS (1)							
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)			$V_{CE(sat)}$	—	—	2.5	Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)				—	—	3.0	
(I_C = 5.0 Adc, I_B = 0.5 Adc, T_C = 100°C)				—	—	3.0	
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc)			$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc, T_C = 100°C)				—	—	1.5	
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 5.0 Vdc			h_{FE}	7.0	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	—	—	350	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(I_C = 5.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.5 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 1.0 Adc, R_{B2} = 4.0 Ω)	t_d	—	20	50	ns
Rise Time			t_r	—	100	250	
Storage Time			t_s	—	900	2200	
Fall Time			t_f	—	70	250	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	400	—	
Fall Time			t_f	—	50	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 5.0 Adc, I_{B1} = 0.5 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	500	1400	ns
Fall Time			t_{fi}	—	70	150	
Crossover Time			t_c	—	100	200	
Storage Time		(T_J = 150°C)	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	100	—	
Crossover Tjme			t_c	—	150	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

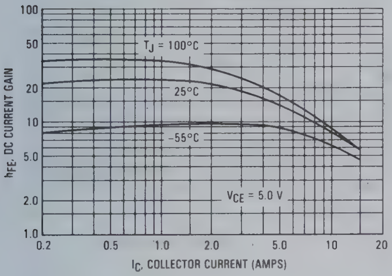


FIGURE 2 — COLLECTOR SATURATION REGION

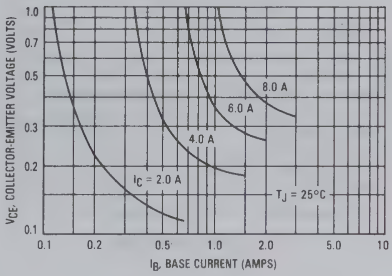


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

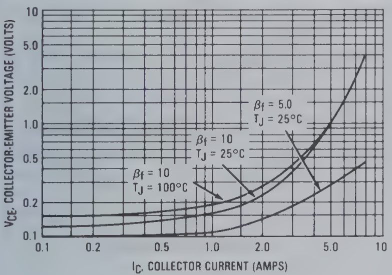


FIGURE 4 — BASE-EMITTER VOLTAGE

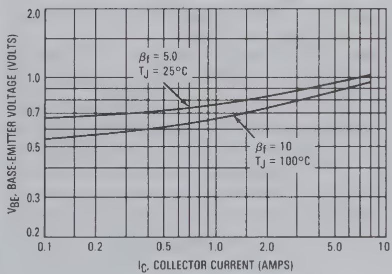


FIGURE 5 — COLLECTOR CUTOFF REGION

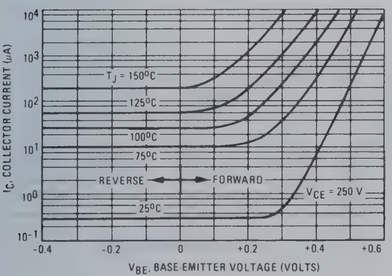
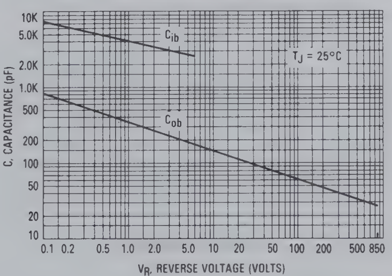


FIGURE 6 — CAPACITANCE



1.3

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

FIGURE 7 — STORAGE TIME

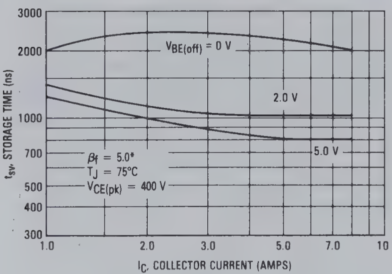


FIGURE 8 — STORAGE TIME

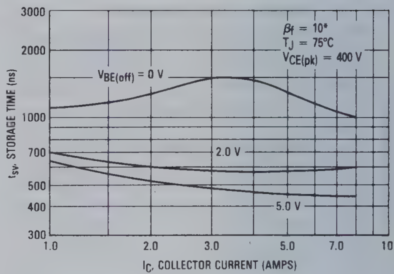


FIGURE 9 — COLLECTOR CURRENT FALL TIME

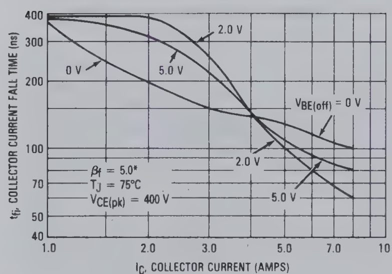


FIGURE 10 — COLLECTOR CURRENT FALL TIME

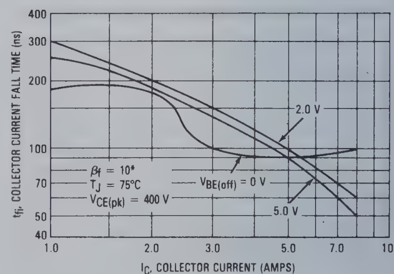


FIGURE 11 — CROSSOVER TIME

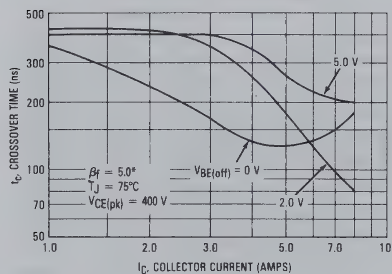
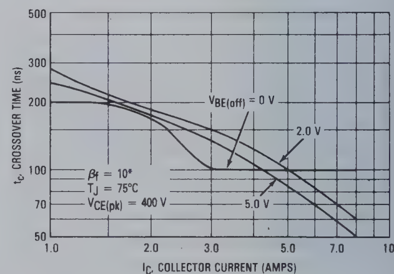


FIGURE 12 — CROSSOVER TIME



$*\beta_f = \frac{I_C}{I_{B1}}$

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

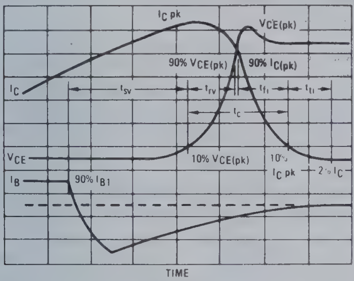


FIGURE 14 — PEAK REVERSE BASE CURRENT

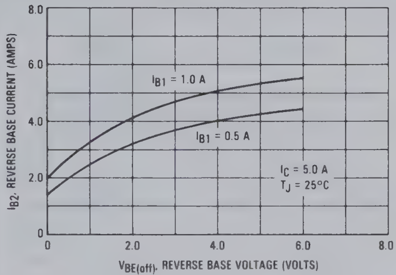
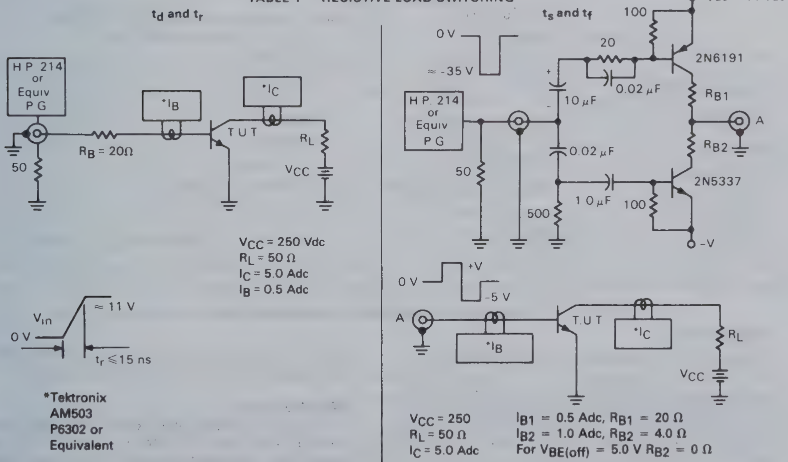


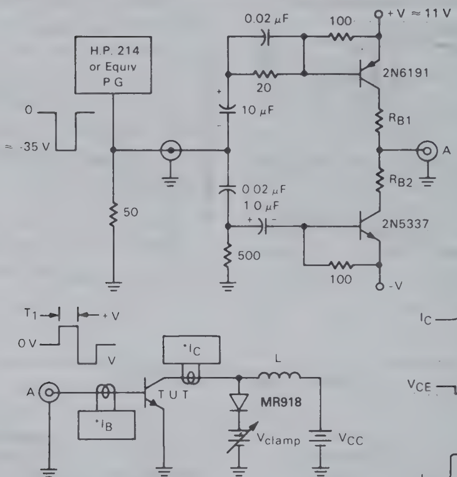
TABLE 1 — RESISTIVE LOAD SWITCHING

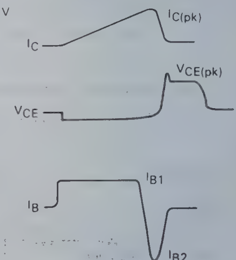


Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

1.3

TABLE 2 — INDUCTIVE LOAD SWITCHING





$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO(sus)}$
$L = 10$ mH
$R_{B2} = \infty$
$V_{CC} = 20$ Volts
$I_{C(pk)} = 100$ mA
*Tektronix AM503 P6302 or Equivalent

Inductive Switching
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

Scope - Tektronix 7403 or Equivalent

RBSOA
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 and 15A are based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 and 15A may be found at any case temperature by using the appropriate curve on Figure 17.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

1.3

GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA, MJ16006 & MJ16008

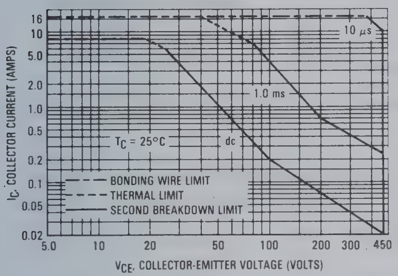


FIGURE 15A — SAFE OPERATING AREA, MJH16006 & MJH16008

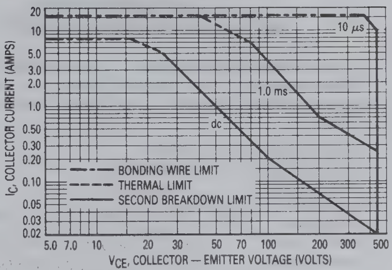


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA

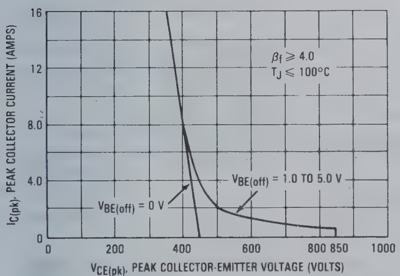


FIGURE 17 — POWER DERATING

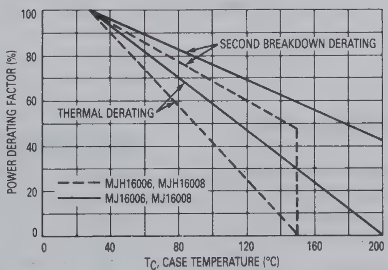
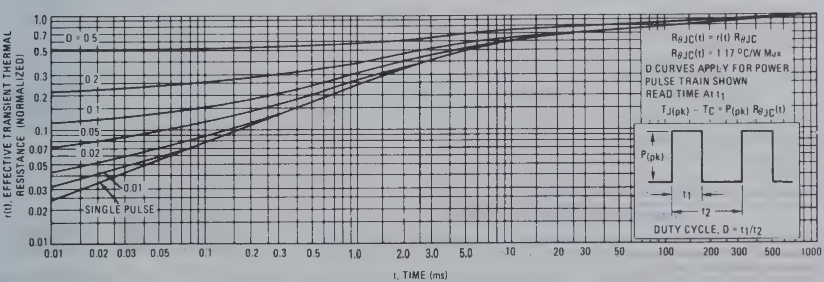


FIGURE 18 — THERMAL RESPONSE



MOTOROLA

1.3

Designer's Data Sheet

1.0 kV SWITCHMODE III SERIES NPN SILICON POWER TRANSISTORS

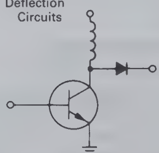
These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:

- Collector-Emitter Voltage — V_{CEX} = 1000 Vdc
- Fast Turn-Off Times
  80 ns Inductive Fall Time – 100°C (Typ)
  120 ns Inductive Crossover Time – 100°C (Typ)
  800 ns Inductive Storage Time – 100°C (Typ)
- 100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Load
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage currents

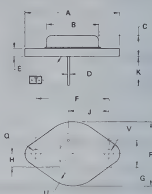


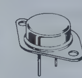
8.0 AMPERE

NPN SILICON POWER TRANSISTORS

500 VOLTS
125 and 150 WATTS

MJ16006A





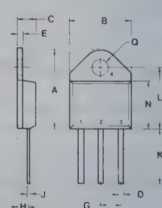
STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. [-T-] IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
| ⌖ | Ø 0.13 (0.005) Ⓜ | T | V Ⓜ |
FOR LEADS
| ⌖ | Ø 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI,Y14.5, 1973

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(Formerly TO-3)

MJH16006A



STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20 32	21 08	0 800	0 830
B	15 49	15.90	0.610	0.626
C	4.19	5.08	0 165	0 200
D	1.02	1.65	0.040	0 065
E	1.35	1.65	0.053	0 065
G	5.21	5 72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0 015	0.025
K	12.70	15.49	0 500	0 610
L	15.88	16 51	0 625	0 650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MJ16006A	MJH16006A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	500		Vdc
Collector-Emitter Voltage	V_{CEV}	1000		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8.0 16		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6.0 12		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	150 85 0.86	125 50 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	–65 to 200	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	1.0	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit Curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)							
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 1000 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$		See Figures 14 or 15		
Clamped Inductive SOA with Base Reverse Biased			RBSOA		See Figure 16		
ON CHARACTERISTICS (1)							
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)			$V_{CE(sat)}$	— — —	— — —	1.0 1.5 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)			$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 5.0 Vdc)			h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	—	—	350	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1) MJ16006A							
Delay Time	(I_C = 5.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.66 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I_{B2} = 1.3 Adc, R_{B2} = 4.0 Ω)	t_d	—	25	100	ns
Rise Time			t_r	—	400	700	
Storage Time			t_s	—	1400	3000	
Fall Time			t_f	—	175	400	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	475	—	
Fall Time			t_f	—	100	—	
Inductive Load (Table 2) MJ16006A							
Storage Time	(I_C = 5.0 Adc, I_{B1} = 0.66 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	800	2000	ns
Fall Time			t_{fi}	—	80	200	
Crossover Time			t_c	—	120	300	
Storage Time		(T_J = 150°C)	t_{sv}	—	1000	—	
Fall Time			t_{fi}	—	90	—	
Crossover Time			t_c	—	150	—	

(1) Pulse Test: PW – 300 μs, Duty Cycle ≤ 2.0%.

1.3

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

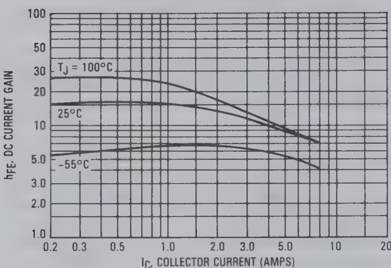


FIGURE 2 — COLLECTOR-EMITTER SATURATION VOLTAGE

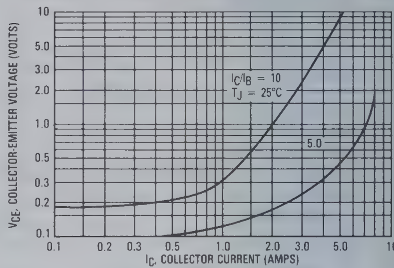


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

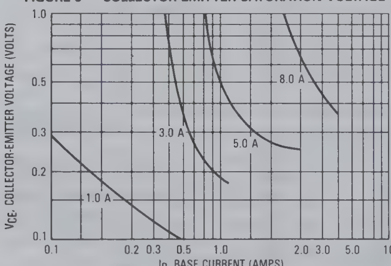


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

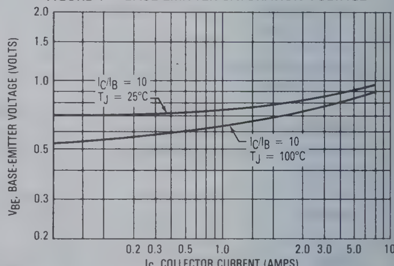


FIGURE 5 — CAPACITANCE

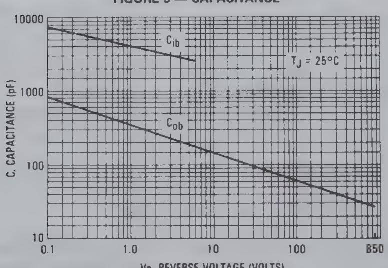


FIGURE 6 — PEAK REVERSE BASE CURRENT

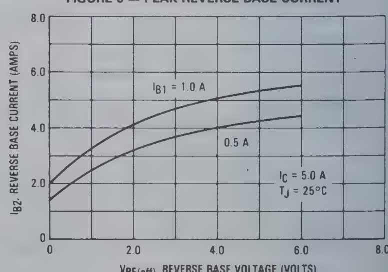
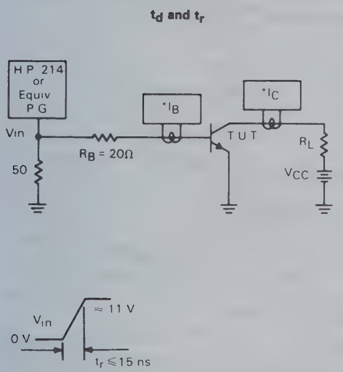
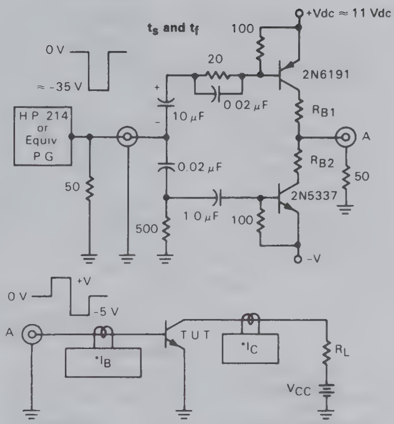


TABLE 1 — RESISTIVE LOAD SWITCHING





*Tektronix
AM503
P6302 or Equivalent

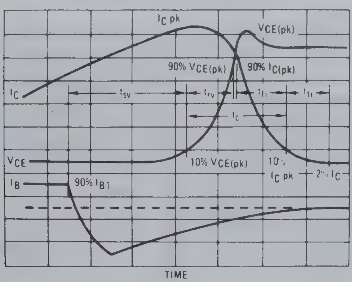
V_{CC}	250 V
R_L	50 Ω
I_C	5.0 A
I_B	0.66 A

V_{CC}	250 V
R_L	50 Ω
I_C	5.0 A
I_{B1}	0.66 A
I_{B2}	1.0 A
R_{B1}	20 Ω
R_{B2}	4.0 Ω

*Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

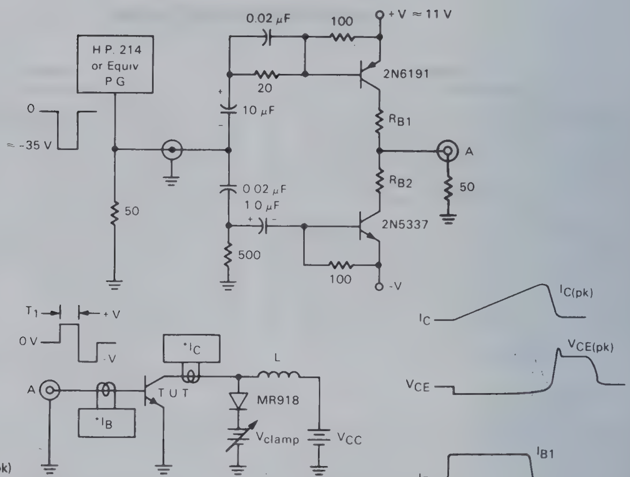
For $V_{BE(off)} = 5.0$ V, $R_{B2} = 0$

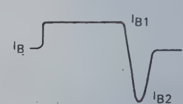
FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS



1.3

TABLE 2 — INDUCTIVE LOAD SWITCHING





$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

BV_{CEO}
$L = 10$ mH
$R_{B2} = \infty$
$V_{CC} = 20$ Volts

Inductive Switching
$L = 750\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

RBSOA
$L = 750\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

*Tektronix AM503
P6302 or Equivalent

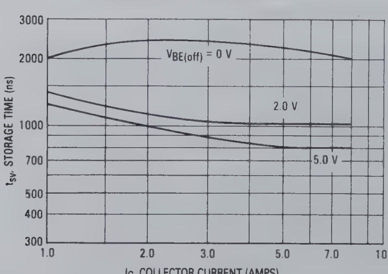
Scope — Tektronix
7403 or
Equivalent

Note: Adjust $-V$ to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

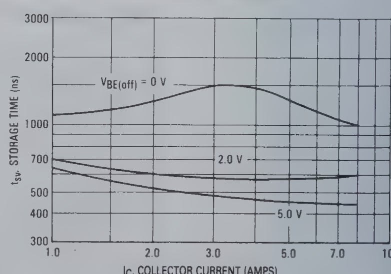
$I_C/I_{B1} = 5.0$, $T_C = 100°C$, $V_{CE(pk)} = 400$ V

FIGURE 8 — STORAGE TIME



$I_C/I_{B1} = 10$, $T_C = 100°C$, $V_{CE(pk)} = 400$ V

FIGURE 9 — STORAGE TIME



GUARANTEED SAFE OPERATING AREA LIMITS (Continued)

FIGURE 16 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

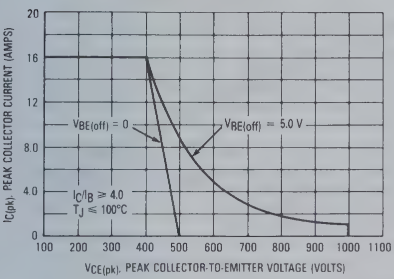
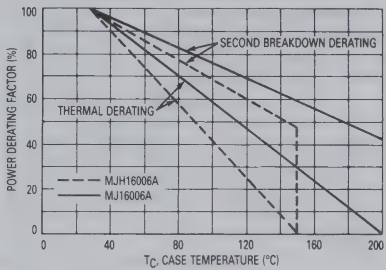


FIGURE 17 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

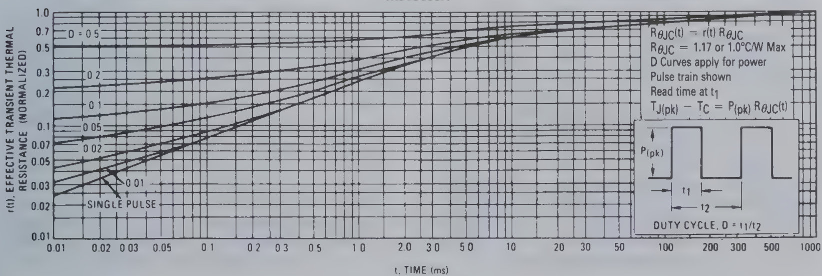
The data of Figures 14 and 15 are based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 14 and 15 may be found at any case temperature by using the appropriate curve on Figure 17.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable putting reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

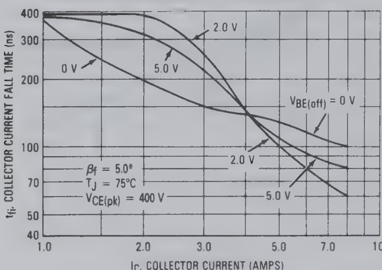
FIGURE 18 — THERMAL RESPONSE
MJ16006A



TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS (Continued)

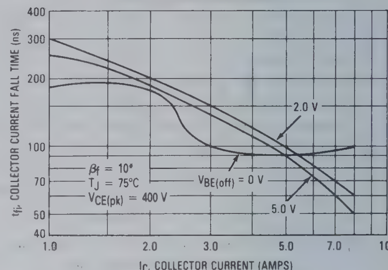
$I_C/I_{B1} = 5.0$, $T_C = 100°C$, $V_{CE(pk)} = 400$ V

FIGURE 10 — COLLECTOR CURRENT FALL TIME



$I_C/I_{B1} = 10$, $T_C = 100°C$, $V_{CE(pk)} = 400$ V

FIGURE 11 — COLLECTOR CURRENT FALL TIME



$$^*\beta_f = \frac{I_C}{I_{B1}}$$

FIGURE 12 — CROSSOVER TIME

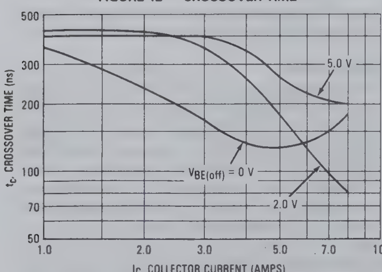
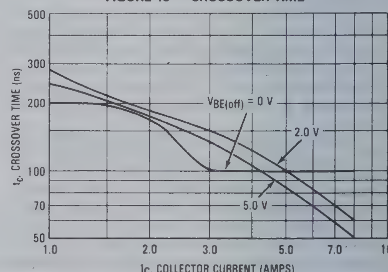


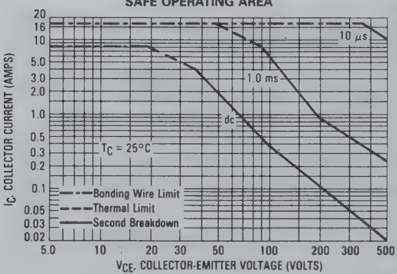
FIGURE 13 — CROSSOVER TIME



GUARANTEED SAFE OPERATING AREA LIMITS

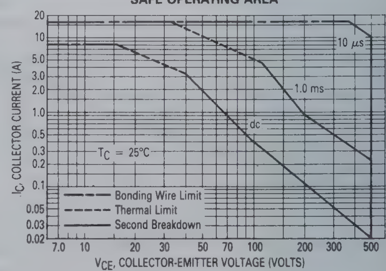
MJ16006A

FIGURE 14 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



MJH16006A

FIGURE 15 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



MOTOROLA

MJ16010
MJ16012
MJH16010
MJH16012

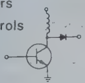
Designer's Data Sheet

SWITCHMODE III SERIES NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16012 and MJH16012 are selected high gain versions of the MJ16010 and MJH16010 for applications where drive current is limited.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits



Features:

- Fast Turn-Off Times — $T_C = 100°C$
  - 50 ns Inductive Fall Time (Typ)
  - 90 ns Inductive Crossover Time (Typ)
  - 800 ns Inductive Storage Time (Typ)
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

15 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
135 AND 175 WATTS

MAXIMUM RATINGS

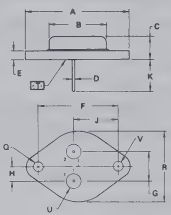
Rating	Symbol	MJ16010 MJ16012	MJH16010 MJH16012	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450		Vdc
Collector-Emitter Voltage	V_{CEV}	850		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15		Adc
Total Device Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	 175 100 1.0	 135 53.8 1.11	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	−55 to 150	°C

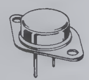
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	0.93	°C/W
Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width ≤ 5.0 µs, Duty Cycle ≥ 10%.

MJ16010
MJ16012





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. $\boxed{-T-}$ IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

⌖	⌀0.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS.

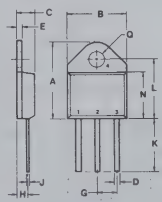
⌖	⌀0.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B		21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA
(Formerly TO-3)

MJH16010
MJH16012



1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

1.3

MJ16010
MJH16010

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 16			
ON CHARACTERISTICS (1)							
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.7 Adc) (I_C = 10 Adc, I_B = 1.3 Adc) (I_C = 10 Adc, I_B = 1.3 Adc, T_C = 100°C)			$V_{CE(sat)}$	— — —	— — —	2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.3 Adc) (I_C = 10 Adc, I_B = 1.3 Adc, T_C = 100°C)			$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 15 Adc, V_{CE} = 5.0 Vdc)			h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	—	—	400	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.3 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 2.6 Adc, R_B = 1.6 Ω)	t_d	—	20	—	ns
Rise Time			t_r	—	200	—	
Storage Time			t_s	—	1200	—	
Fall Time			t_f	—	200	—	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	650	—	
Fall Time			t_f	—	80	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.3 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	800	1800	ns
Fall Time			t_{fi}	—	50	200	
Crossover Time			t_c	—	90	250	
Storage Time		(T_C = 150°C)	t_{sv}	—	1050	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

1.3

MJ16012
MJH16012

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	 — —	 — —	 0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 1.5 1.5	Vdc
DC Current Gain (I_C = 15 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	7.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	400	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.0 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 2.0 Adc, R_B = 1.6 Ω)	t_d	—	20	—	ns
Rise Time			t_r	—	200	—	
Storage Time			t_s	—	900	—	
Fall Time			t_f	—	150	—	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	500	—	
Fall Time			t_f	—	40	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	650	1500	ns
Fall Time			t_{fi}	—	30	150	
Crossover Time			t_c	—	50	200	
Storage Time		(T_C = 150°C)	t_{sv}	—	850	—	
Fall Time			t_{fi}	—	30	—	
Crossover Time			t_c	—	70	—	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

1.3

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

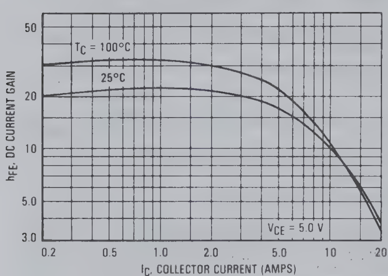


FIGURE 2 — COLLECTOR SATURATION REGION

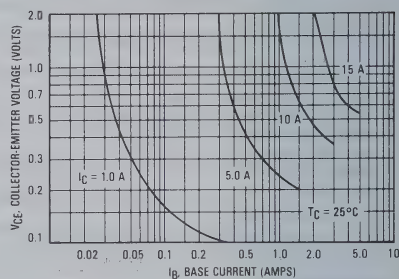


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

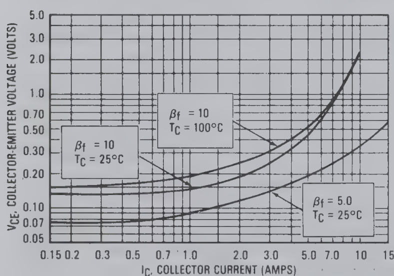


FIGURE 4 — BASE-EMITTER VOLTAGE

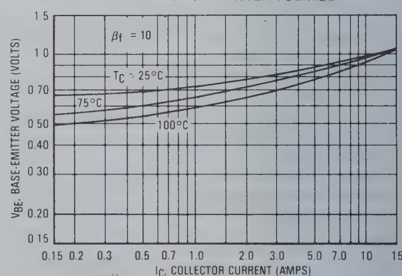


FIGURE 5 — COLLECTOR CUTOFF REGION

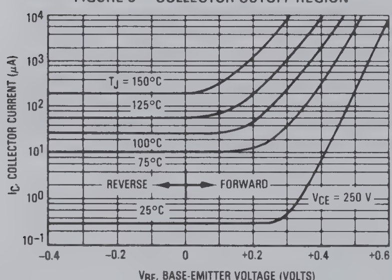
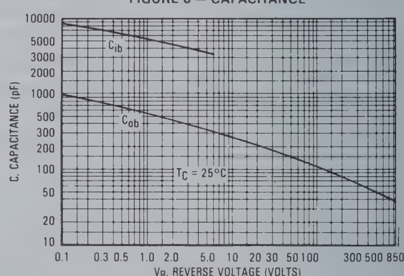


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

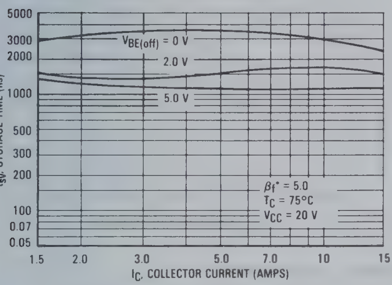


FIGURE 8 — STORAGE TIME

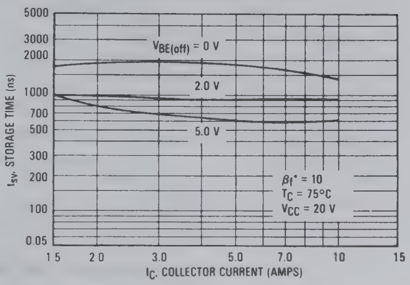


FIGURE 9 — COLLECTOR CURRENT FALL TIME

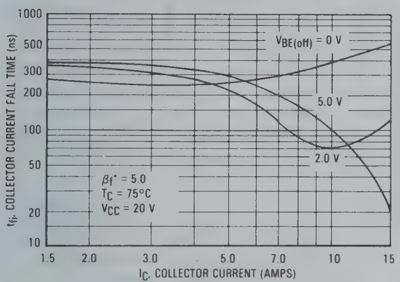


FIGURE 10 — COLLECTOR CURRENT FALL TIME

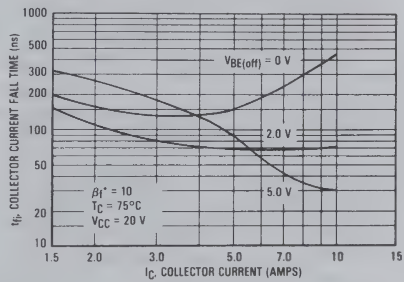


FIGURE 11 — CROSSOVER TIME

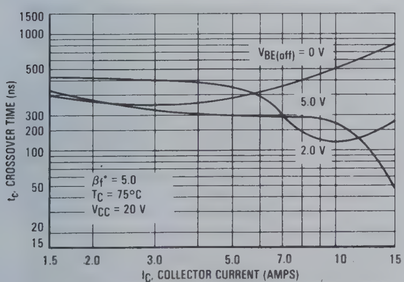
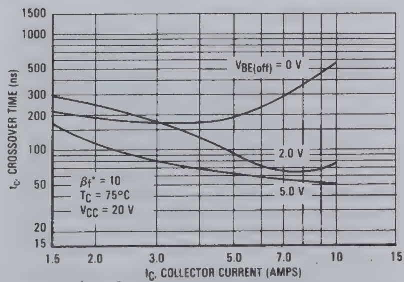


FIGURE 12 — CROSSOVER TIME



$*\beta_f = \dfrac{I_C}{I_{B1}}$

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

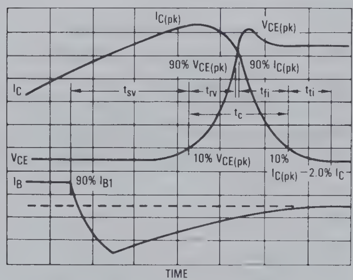
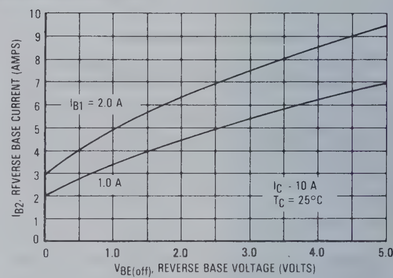


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

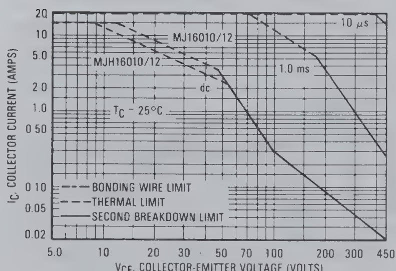
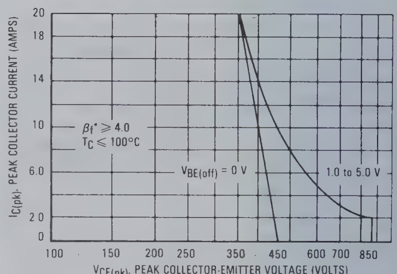


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



$^*\beta_f = \frac{I_C}{I_{B1}}$

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

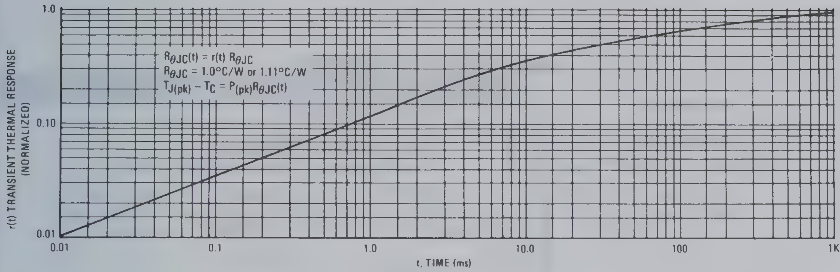


FIGURE 18 — POWER DERATING

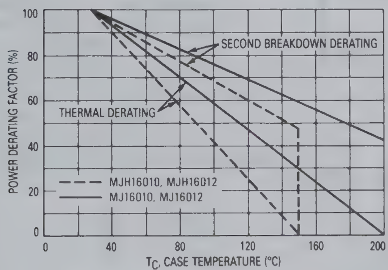
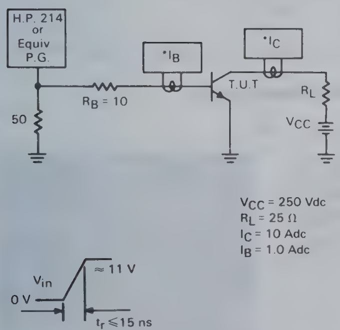


TABLE 1 — RESISTIVE LOAD SWITCHING

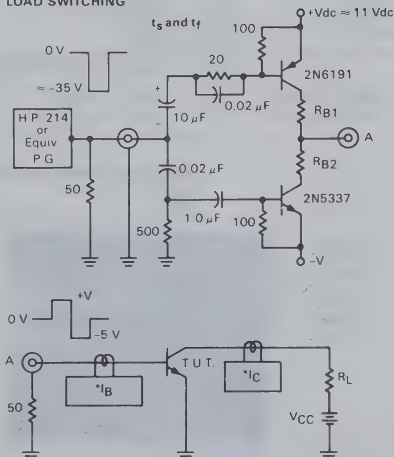
t_d and t_r



$V_{CC} = 250$ Vdc
$R_L = 25\ \Omega$
$I_C = 10$ Adc
$I_B = 1.0$ Adc

*Tektronix AM503
P6302 or Equivalent

t_s and t_f



$V_{CC} = 250$ Vdc
$R_L = 25\ \Omega$
$I_C = 10$ Adc

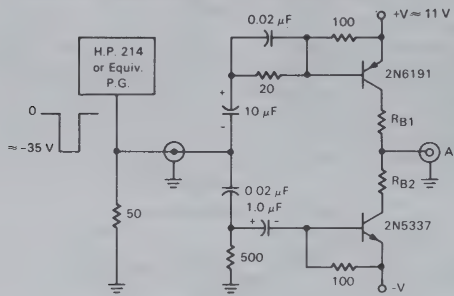
$I_{B1} = 1.0$ Adc
$I_{B2} = 2.0$ Adc
For $V_{BE(off)} = 5.0$ V, $R_{B2} = 0\ \Omega$

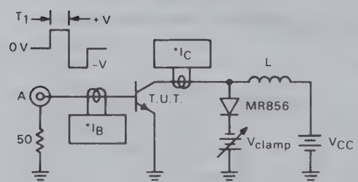
$R_{B1} = 10\ \Omega$
$R_{B2} \doteq 1.6\ \Omega$

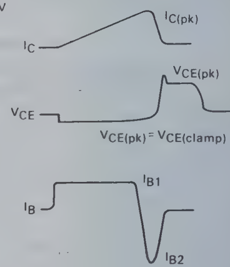
Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

1.3

TABLE 2 — INDUCTIVE LOAD SWITCHING







$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

BV_{CEO}
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 V lts

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 V
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 V
R_{B1} selected for desired I_{B1}

*Tektronix AM503
P6302 or Equivalent

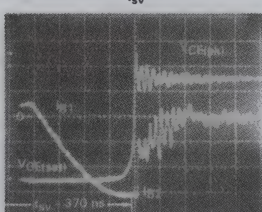
Scope — Tektronix
7403 or Equivalent

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

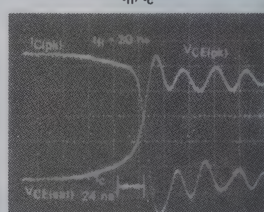
t_{sv}

$I_{C(pk)}$ = 10 A
I_{B1} = 1.0 A
$V_{BE(off)}$ = 5.0 V
$V_{CE(pk)}$ = 400 V
T_C = 25°C
Time Base =
100 ns/cm



t_{fi}, t_c

$I_{C(pk)}$ = 10 A
I_{B1} = 1.0 A
$V_{BE(off)}$ = 5.0 V
$V_{CE(pk)}$ = 400 V
T_C = 25°C
Time Base =
20 ns/cm



MOTOROLA

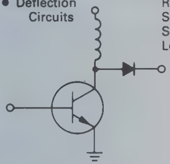
Designer's Data Sheet

1.0 kV SWITCHMODE III SERIES NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:
- Collector-Emitter Voltage — V_{CEX} = 1000 Vdc
- Fast Turn-Off Times
  50 ns Inductive Fall Time – 100°C (Typ)
  90 ns Inductive Crossover Time – 100°C (Typ)
  900 ns Inductive Storage Time – 100°C (Typ)
- 100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Load
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage currents

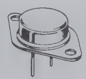


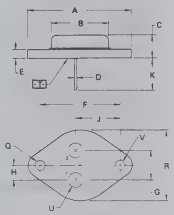
15 AMPERE

NPN SILICON POWER TRANSISTORS

500 VOLTS
125 and 175 WATTS

MJ16010A





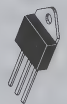
STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

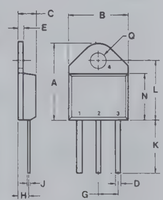
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B		21 08	–	0 830
C	6 35	7 62	0 250	0 300
D	0 97	1 09	0 038	0 043
E	1 40	1 78	0 055	0 070
F	30.15 BSC		1 187 BSC	
G	10 92 BSC		0 430 BSC	
H	5 46 BSC		0 215 BSC	
J	16.89 BSC		0 665 BSC	
K	11 18	12 19	0.440	0 480
Q	3 81	4 19	0.151	0 165
R	–	26 67	–	1 050
U	4.83	5.33	0 190	0.210
V	3.81	4 19	0.151	0 165

NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. -T- IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
   ⌖ ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS
   ⌖ ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

CASE 1-05
TO-204AA
(Formerly TO-3)

MJH16010A





STYLE 1
PIN 1 BASE
2 COLLECTOR
3. EMITTER
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20 32	21 08	0 800	0 830
B	15 49	15 90	0 610	0 626
C	4 19	5 08	0 165	0 200
D	1.02	1 65	0 040	0 065
E	1 35	1 65	0 053	0 065
G	5 21	5 72	0 205	0 225
H	2 41	3 20	0.095	0 126
J	0 38	0 84	0 015	0 025
K	12 70	15 49	0 500	0 610
L	15 88	16 51	0 625	0 650
N	12 19	12 70	0.480	0.500
Q	4.04	4 22	0.159	0.166

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MJ16010A	MJH16010A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	500		Vdc
Collector-Emitter Voltage	V_{CEV}	1000		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	175 100 1.0	135 54 1.09	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	0.92	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit Curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)							
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 1000 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$		See Figures 14 or 15		
Clamped Inductive SOA with Base Reverse Biased			RBSOA		See Figure 16		
ON CHARACTERISTICS (1)							
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)			$V_{CE(sat)}$	— — —	— — —	1.0 1.5 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)			$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 15 Adc, V_{CE} = 5.0 Vdc)			h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	—	—	400	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.3 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I_{B2} = 2.6 Adc, R_{B2} = 1.6 Ω)	t_d	—	25	100	ns
Rise Time			t_r	—	325	600	
Storage Time			t_s	—	1300	3000	
Fall Time			t_f	—	175	400	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	700	—	
Fall Time			t_f	—	80	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.3 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	900	2000	ns
Fall Time			t_{fi}	—	50	250	
Crossover Time			t_c	—	90	300	
Storage Time		(T_J = 150°C)	t_{sv}	—	1100	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: PW – 300 μs, Duty Cycle ≤ 2.0%.

1.3

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

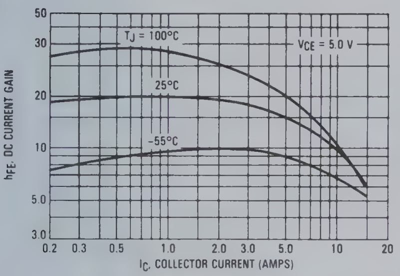


FIGURE 2 — COLLECTOR-EMITTER SATURATION VOLTAGE

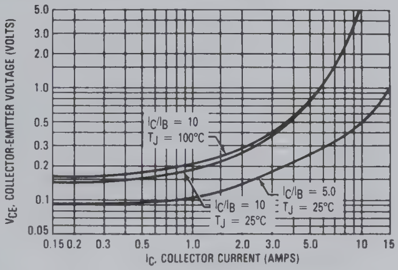


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

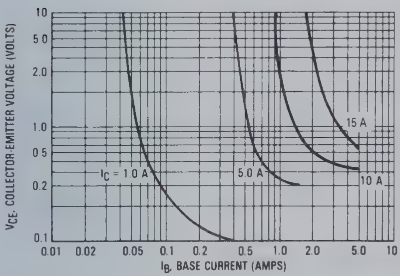


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

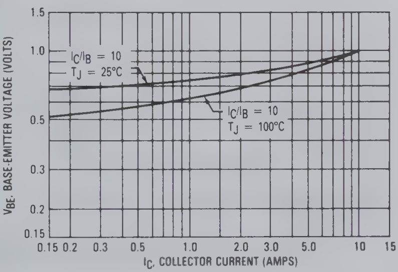


FIGURE 5 — CAPACITANCE

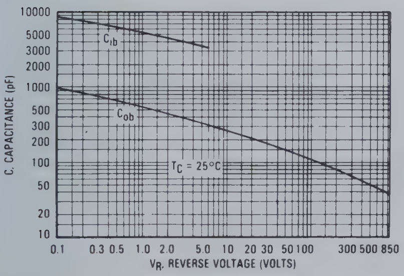


FIGURE 6 — PEAK REVERSE BASE CURRENT

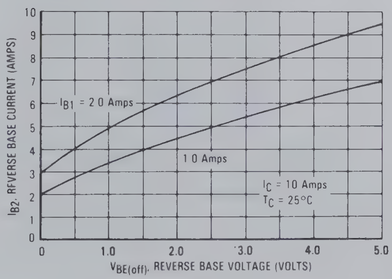
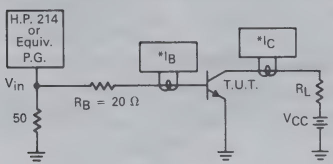
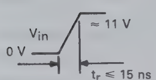


TABLE 1 — RESISTIVE LOAD SWITCHING

t_d and t_r



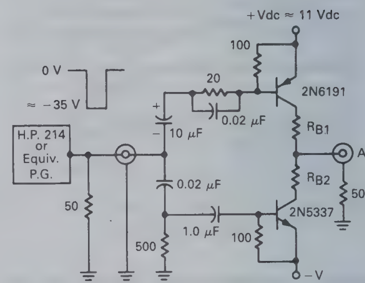


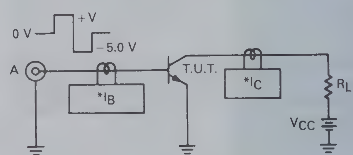
*Tektronix
AM503
P6302 or
Equivalent

V_{CC}	250 V
R_L	50 Ω
I_C	5.0 A
I_{B1}	0.66 A
I_{B2}	1.0 A
R_{B1}	20 Ω
R_{B2}	4.0 Ω

*Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.
For $V_{BE(off)} = 5.0$ V, $R_{B2} = 0$

t_s and t_f

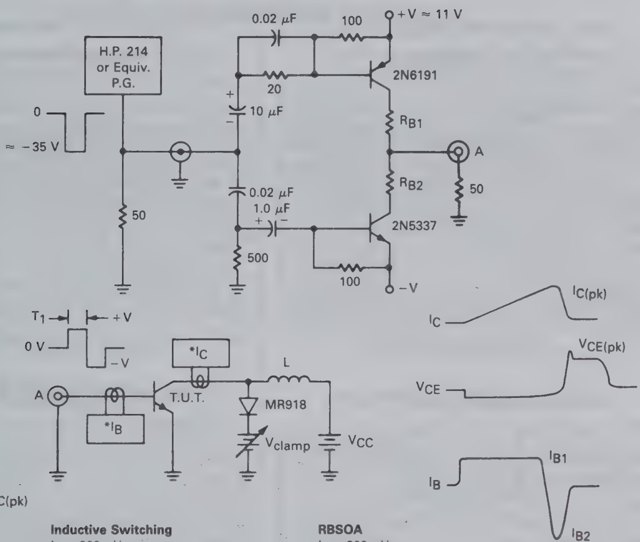




V_{CC}	250 V
R_L	50 Ω
I_C	5.0 A
I_B	0.66 A

1.3

TABLE 2 — INDUCTIVE LOAD SWITCHING



$T_1 \approx \dfrac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

BV_{CEO}
$L = 10$ mH
$R_{B2} = \infty$
$V_{CC} = 20$ Volts

Inductive Switching
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

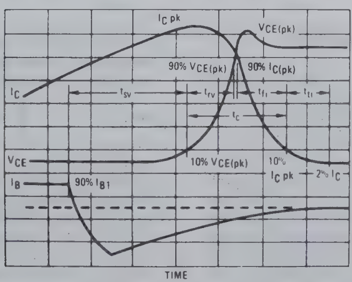
RBSOA
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

*Tektronix AM503
P6302 or Equivalent

Scope — Tektronix
7403 or
Equivalent

Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS



1.3

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

I_C/I_{B1} = 5.0, T_C = 100°C, $V_{CE(pk)}$ = 400 V

I_C/I_{B1} = 10, T_C = 100°C, $V_{CE(pk)}$ = 400 V

FIGURE 8 — STORAGE TIME

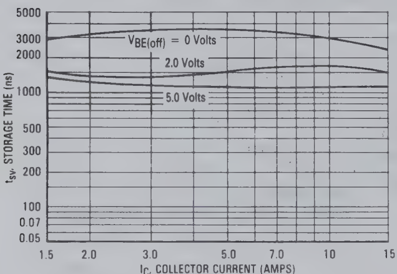


FIGURE 9 — STORAGE TIME

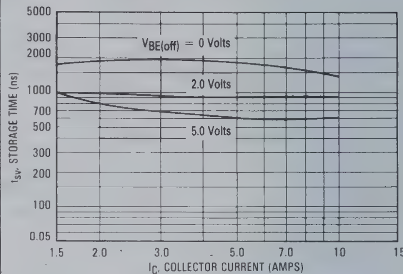


FIGURE 10 — COLLECTOR CURRENT FALL TIME

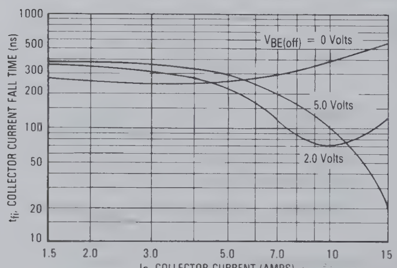


FIGURE 11 — COLLECTOR CURRENT FALL TIME

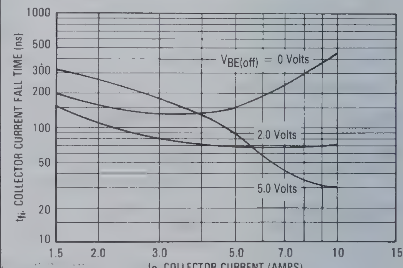


FIGURE 12 — CROSSOVER TIME

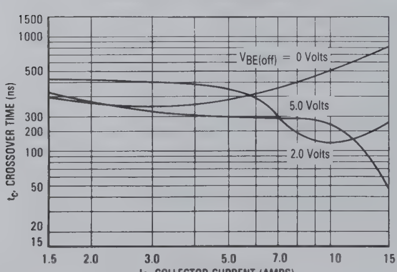
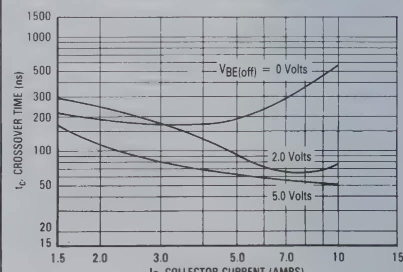


FIGURE 13 — CROSSOVER TIME



GUARANTEED OPERATING AREA INFORMATION

FIGURE 14 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA — MJ16010A

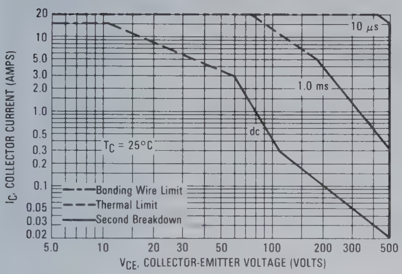


FIGURE 15 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA — MJH16010A

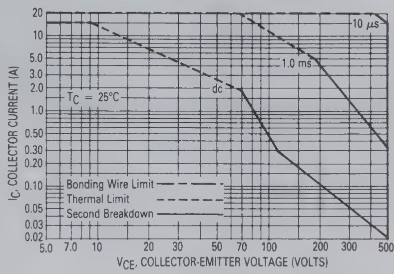


FIGURE 16 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

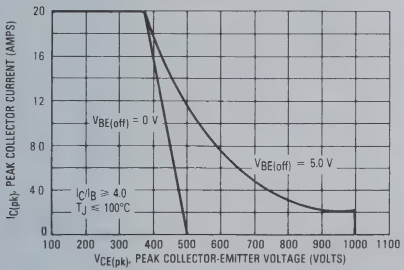
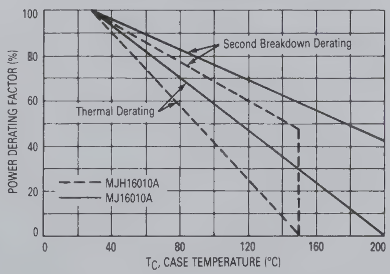


FIGURE 17 — POWER DERATING



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

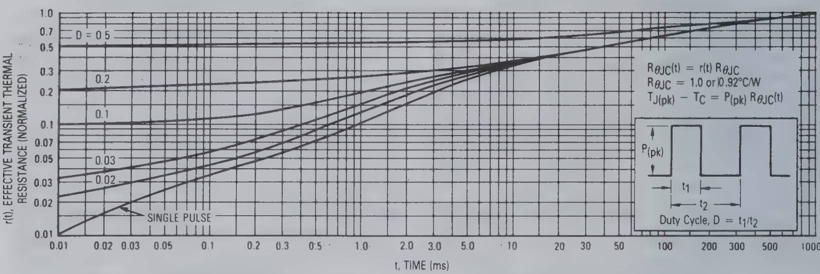
The data of Figures 14 and 15 are based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 14 and 15 may be found at any case temperature by using the appropriate curve on Figure 17.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable putting reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 18 — THERMAL RESPONSE



MJ16014
MJ16016

MOTOROLA

1.3

Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16016 is a selected high-gain version of the MJ16014 for applications where drive current is limited.

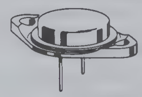
Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  - 40 ns Inductive Fall Time — 75°C (Typ)
  - 40 ns Inductive Crossover Time — 75°C (Typ)
  - 800 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range −65 to +200°C
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

20 AMPERE

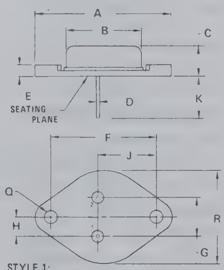
NPN SILICON POWER TRANSISTORS

450 VOLTS
250 WATTS



Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO-3

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 20	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

MJ16014

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.25	
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 1.3 Adc)		—	—	2.5	
(I_C = 15 Adc, I_B = 2.0 Adc)		—	—	3.0	
(I_C = 15 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	—	3.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 15 Adc, I_B = 2.0 Adc)		—	—	1.5	
(I_C = 15 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	—	1.5	
DC Current Gain (I_C = 20 Adc, V_{CE} = 5.0 Vdc	h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	500	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1) — (I_C = 15 Adc, V_{CC} = 250 Vdc, I_{B1} = 2.0 Adc, PW = 30 μs, Duty Cycle ≤2.0%)					ns
Delay Time (I_{B2} = 4.0 Adc, R_B = 1.6 Ω)	t_d	—	20	50	
Rise Time (I_{B2} = 4.0 Adc, R_B = 1.6 Ω)	t_r	—	200	500	
Storage Time (I_{B2} = 4.0 Adc, R_B = 1.6 Ω)	t_s	—	1200	2700	
Fall Time (I_{B2} = 4.0 Adc, R_B = 1.6 Ω)	t_f	—	200	350	
Storage Time ($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	650	—	
Fall Time ($V_{BE(off)}$ = 5.0 Vdc)	t_f	—	80	—	
Inductive Load (Table 2) — (I_C = 15 Adc, I_{B1} = 2.0 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)					ns
Storage Time (T_C = 100°C)	t_{sv}	—	800	2700	
Fall Time (T_C = 100°C)	t_{fi}	—	50	200	
Crossover Time (T_C = 100°C)	t_c	—	90	250	
Storage Time (T_C = 150°C)	t_{sv}	—	1050	—	
Fall Time (T_C = 150°C)	t_{fi}	—	70	—	
Crossover Time (T_C = 150°C)	t_c	—	120	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$^{*}\beta_f = \frac{I_C}{I_{B1}}$

MJ16016

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	 — —	 — —	 0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 15 Adc, I_B = 1.5 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 15 Adc, I_B = 1.5 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 1.5 1.5	Vdc
DC Current Gain (I_C = 20 Adc, V_{CE} = 5.0 Vdc	h_{FE}	7.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	500	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 15 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.5 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 3.0 Adc, R_B = 1.6 Ω)	t_d	—	20	50	ns
Rise Time			t_r	—	200	500	
Storage Time			t_s	—	900	2200	
Fall Time			t_f	—	100	250	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	500	—	
Fall Time			t_f	—	40	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 15 Adc, I_{B1} = 1.5 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	750	2500	ns
Fall Time			t_{fi}	—	30	150	
Crossover Time			t_c	—	50	200	
Storage Time		(T_C = 150°C)	t_{sv}	—	900	—	
Fall Time			t_{fi}	—	30	—	
Crossover Time			t_c	—	70	—	

(1) Pulse Test: PW · 300 μs, Duty Cycle ≤2%.

$^{*}\beta_f = \frac{I_C}{I_{B1}}$

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

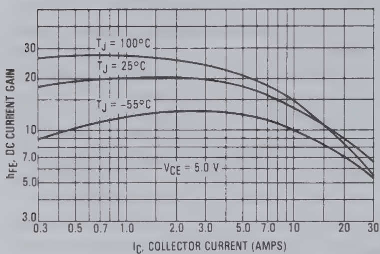


FIGURE 2 — COLLECTOR SATURATION REGION

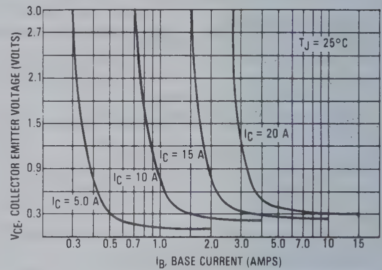


FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION

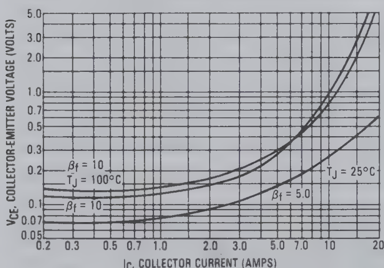


FIGURE 4 — BASE-EMITTER VOLTAGE

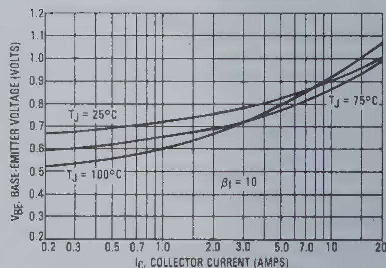


FIGURE 5 — COLLECTOR CUTOFF REGION

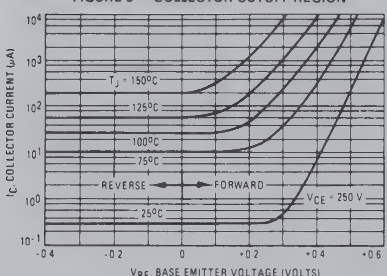
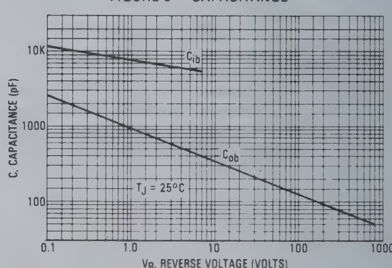


FIGURE 6 — CAPACITANCE



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TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

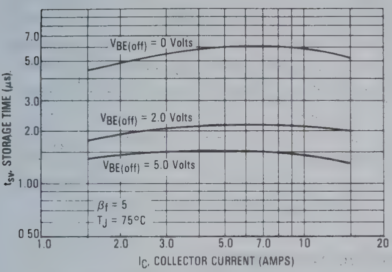


FIGURE 8 — STORAGE TIME

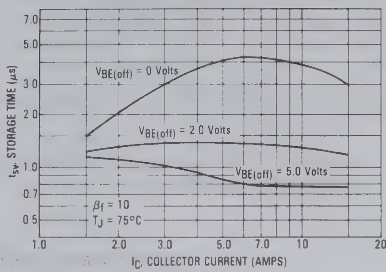


FIGURE 9 — COLLECTOR CURRENT FALL TIME

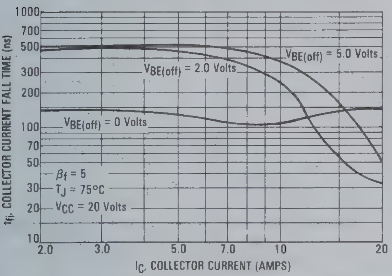


FIGURE 10 — COLLECTOR CURRENT FALL TIME

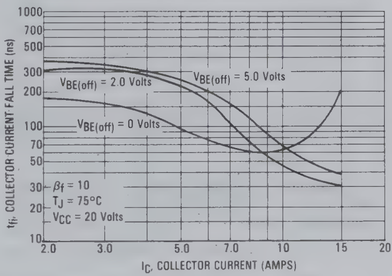


FIGURE 11 — CROSSOVER TIME

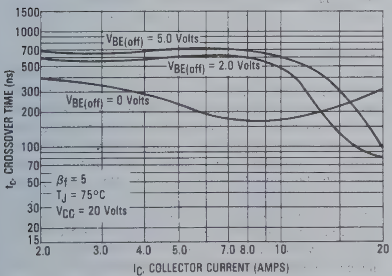


FIGURE 12 — CROSSOVER TIME

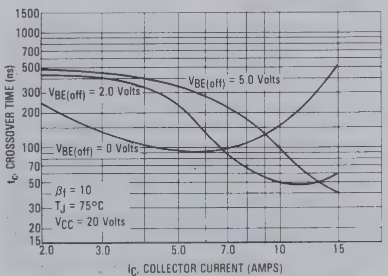


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

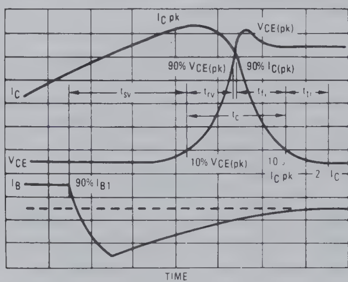
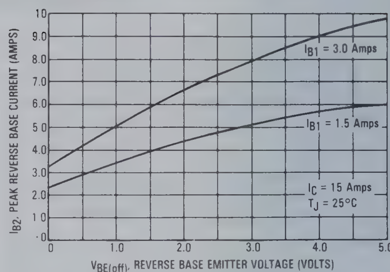


FIGURE 14 — REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

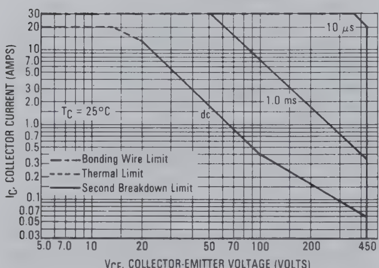
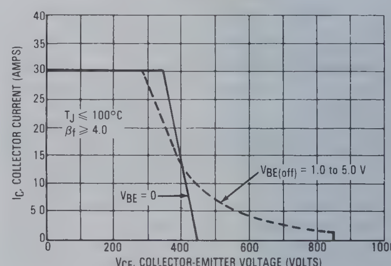


FIGURE 16 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

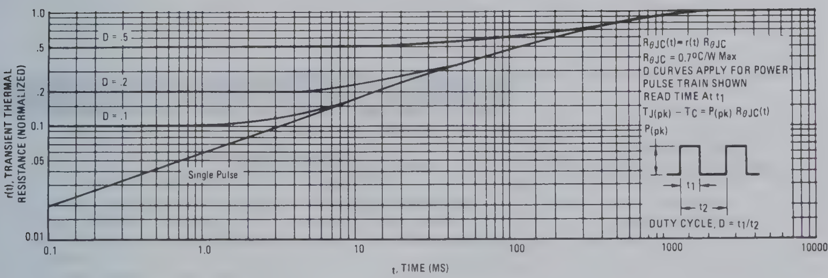


FIGURE 18 — POWER DERATING

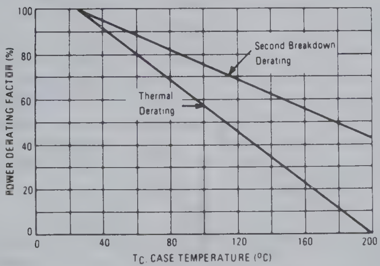
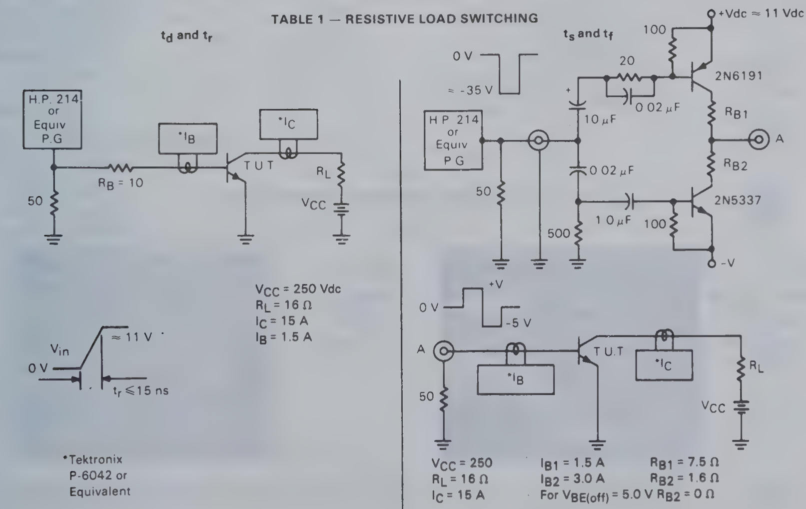


TABLE 1 — RESISTIVE LOAD SWITCHING



*Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

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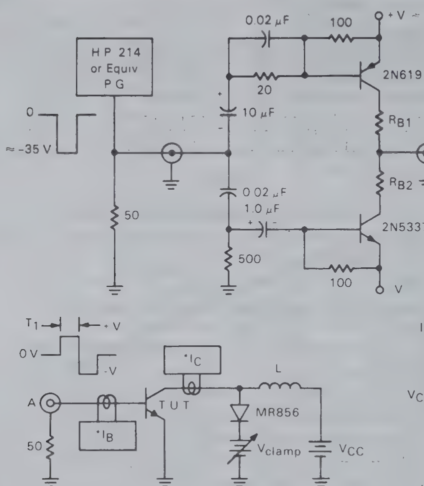
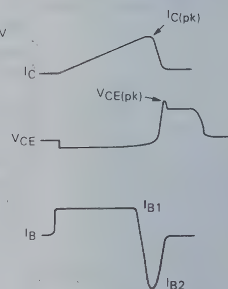
TABLE 2 — INDUCTIVE LOAD SWITCHING





$T_1 \approx \dfrac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

BV_{CEO}
$L = 10$ mH
$R_{B2} = \infty$
$V_{CC} = 20$ Volts

Inductive Switching
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

RBSOA
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

*Tektronix
P-6042 or
Equivalent

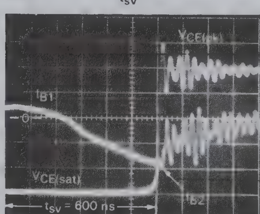
Scope - Tektronix
7403 or
Equivalent

Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

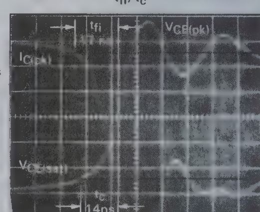
t_{sv}

$I_{C(pk)} = 15$ A
$I_{B1} = 1.5$ A
$V_{BE(off)} = 5.0$ Volts
$V_{CE(pk)} = 400$ Volts
$T_C = 25°C$
Time Base = 100 ns/cm



t_{fi}, t_c

$I_{C(pk)} = 15$ A
$I_{B1} = 1.5$ A
$V_{BE(off)} = 5.0$ Volts
$V_{CE(pk)} = 400$ Volts
$T_C = 25°C$
Time Base = 10 ns/cm



MJ16018
MJH16018

MOTOROLA

1.3

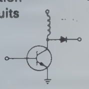
Designers Data Sheet

1.5 kV SWITCHMODE III SERIES NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:
- Collector-Emitter Voltage — V_{CEX} = 1500 Vdc
- Fast Turn-Off Times
  - 280 ns Inductive Fall Time – 100°C (Typ)
  - 470 ns Inductive Crossover Time – 100°C (Typ)
  - 2.6 μs Inductive Storage Time – 100°C (Typ)
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Load
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



10 AMPERE

NPN SILICON POWER TRANSISTORS

800 VOLTS
150 AND 175 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJ16018	MJH16018	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	800		Vdc
Collector-Emitter Voltage	V_{CEX}	1500		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 15		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	8.0 12		Adc
Total Device Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	150 50 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	−55 to 150	°C

THERMAL CHARACTERISTICS

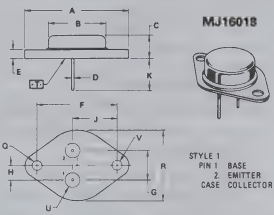
Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	1.0	°C/W
Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds.	T_L	275		°C

(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit Curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MJ16018



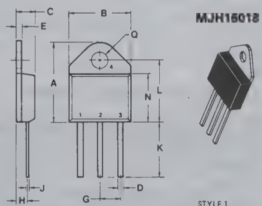
STYLE 1
PIN 1 BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
   | ⌖ | ∅0.13 (0.005) Ⓜ | T | V Ⓜ |
   FOR LEADS.
   | ⌖ | ∅0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39 37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1 187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

**CASE 1-05
TO-204AA
(TO-3 TYPE)**

MJH16018



STYLE 1.
1 BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0 830
B	15.49	15.90	0.610	0 626
C	4.19	5.08	0 165	0 200
D	1.02	1.65	0.040	0 065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0 225
H	2.41	3.20	0.095	0 126
J	0.38	0.64	0.015	0 025
K	12.70	15.49	0 500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

**CASE 340-01
TO-218AC**

MJ16018
MJH16018

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	800	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = 1500 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.25	
(V_{CEV} = 1500 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5	
Collector Cutoff Current (V_{CE} = 1500 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)		—	—	1.5	
(I_C = 10 Adc, I_B = 4.0 Adc)		—	—	1.5	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		—	—	2.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)		—	—	1.5	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		—	—	1.5	
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	7.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	400	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 5.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.0 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I_{B2} = 2.0 Adc, R_{B2} = 3.0 Ω)	t_d	—	50	100	ns
Rise Time			t_r	—	300	400	
Storage Time			t_s	—	2000	3000	
Fall Time			t_f	—	900	1200	
Storage Time		($V_{BE(off)}$ = 2.0 Vdc)	t_s	—	1600	2400	
Fall Time			t_f	—	500	650	
Inductive Load (Table 2)							
Storage Time	(I_C = 5.0 Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 2.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 25°C)	t_{sv}	—	2000	3000	ns
Fall Time			t_{fi}	—	200	400	
Crossover Time			t_c	—	350	500	
Storage Time		(T_J = 100°C)	t_{sv}	—	2600	3600	
Fall Time			t_{fi}	—	280	460	
Crossover Time			t_c	—	470	620	

(1) Pulse Test: PW — 300 μs, Duty Cycle ≤ 2.0%.

1.3

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

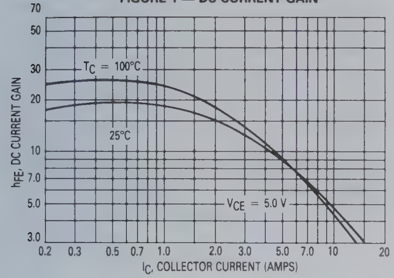


FIGURE 2 — COLLECTOR SATURATION REGION

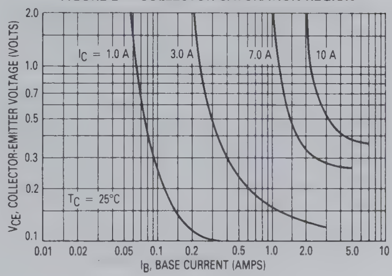


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

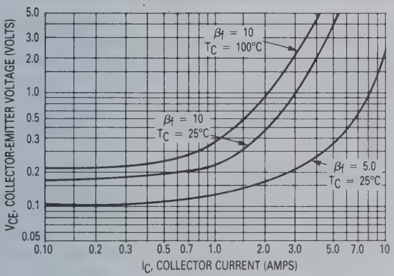


FIGURE 4 — BASE-EMITTER VOLTAGE

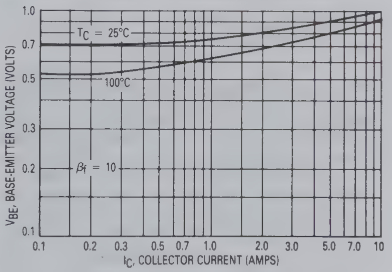


FIGURE 5 — COLLECTOR CUTOFF REGION

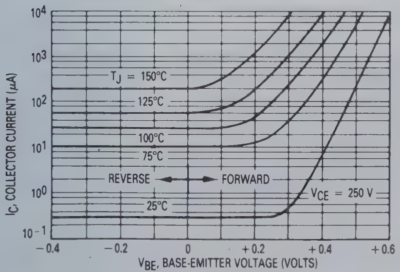
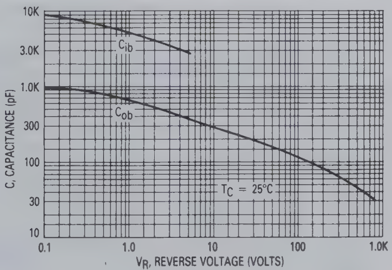


FIGURE 6 — CAPACITANCE



1.3

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

FIGURE 7 — STORAGE TIME

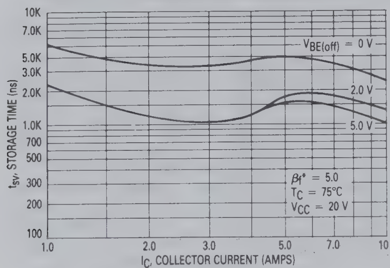


FIGURE 8 — COLLECTOR CURRENT FALL TIME

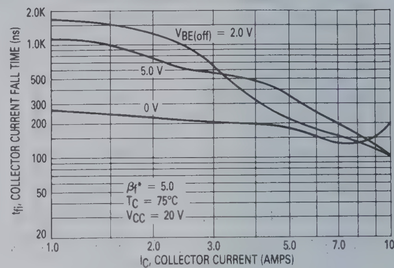


FIGURE 9 — CROSSOVER TIME

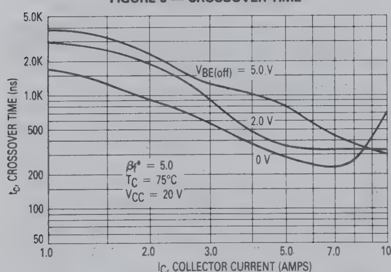


FIGURE 10 — INDUCTIVE SWITCHING MEASUREMENTS

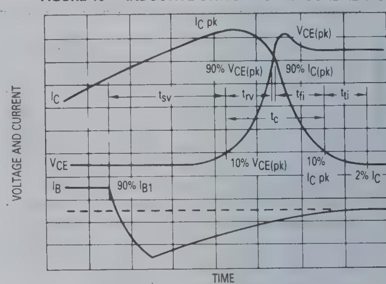
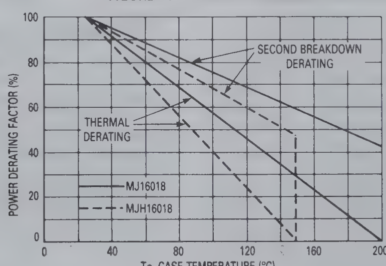


FIGURE 11 — POWER DERATING



$*\beta_f = \frac{I_C}{I_{B1}}$

1.3

GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 12 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

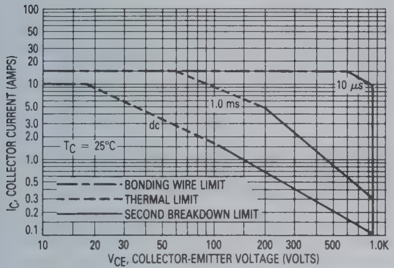
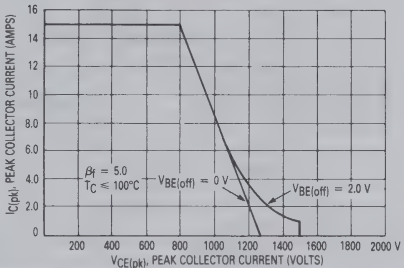


FIGURE 13 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

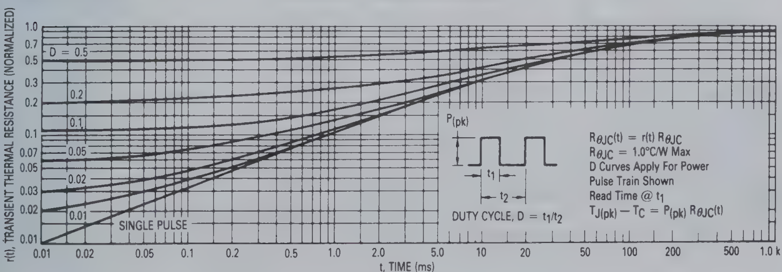
The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 14. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

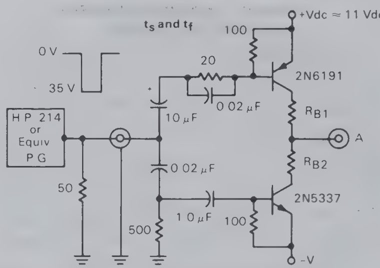
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

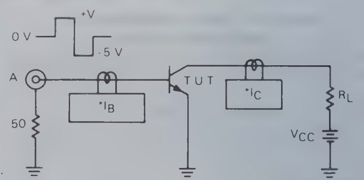
FIGURE 14 — THERMAL RESPONSE



1.3

TABLE 1 — RESISTIVE LOAD SWITCHING

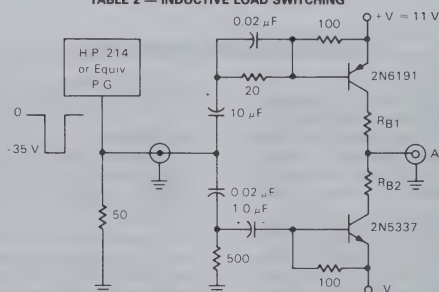


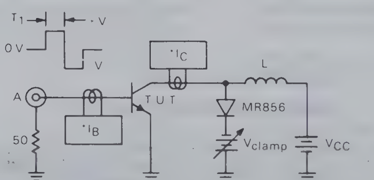


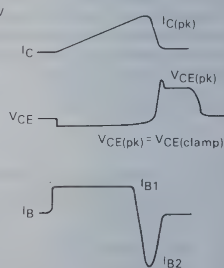
V_{CC} = 250 | I_{B1} = 1.0 Adc | R_{B1} = 10 Ω
R_L = 50 Ω | I_{B2} = 2.0 Adc | R_{B2} = 3.0 Ω
I_C = 5.0 Adc | For $V_{BE(off)}$ = 2.0 V R_{B2} = 0 Ω

*Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING







$$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO(sus)}$
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 Volts

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

***Tektronix**
AM503
P6302 or
Equivalent

Scope - Tektronix
7403 or
Equivalent

Note. Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

MOTOROLA

MEDIUM-POWER PNP SILICON TRANSISTOR

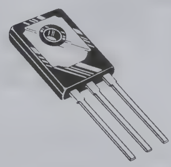
. . . for use as an output device in complementary audio amplifiers up to 20-Watts music power per channel.

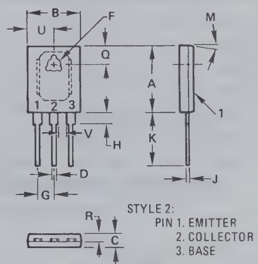
- High DC Current Gain – h_{FE} = 25-100 @ I_C = 2.0 A
- Thermopad High-Efficiency Compact Package
- Complementary to NPN MJE205

5 AMPERE

POWER TRANSISTOR
PNP SILICON

50 VOLTS
65 WATTS





STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	5.0	Adc
Base Current	I_B	2.5	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D(1)	65 0.522	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.92	°C/W

(1) Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

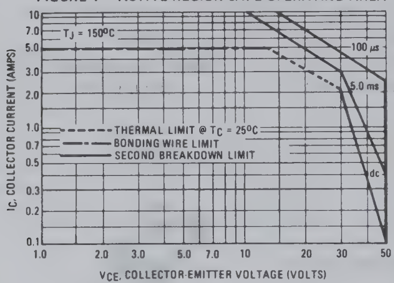
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (2) (I_C = 100 mAdc, I_B = 0)	BV_{CEO}	50	–	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 50 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 – –	 0.1 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter Voltage (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	V_{BE}	–	1.2	Vdc

(2) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

1.3

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C \cdot V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 1 is based on $T_{J(pk)} = 150^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – "ON" VOLTAGES

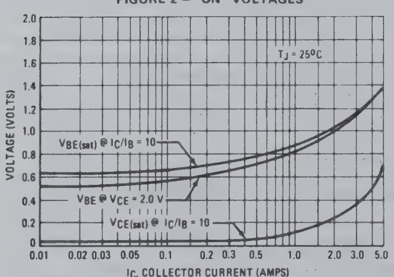


FIGURE 3 – DC CURRENT GAIN

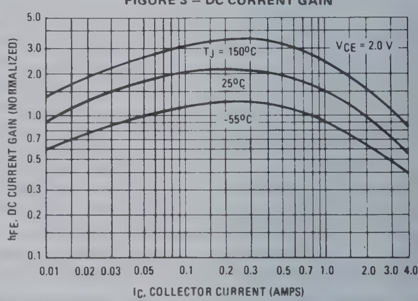
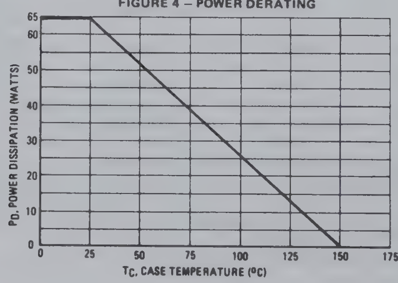


FIGURE 4 – POWER DERATING



MJE170 thru MJE172 PNP
MJE180 thru MJE182 NPN

MOTOROLA

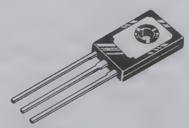
1.3

COMPLEMENTARY PLASTIC SILICON POWER TRANSISTORS

. . . designed for low power audio amplifier and low current, high speed switching applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc — MJE170, MJE180
  = 60 Vdc — MJE171, MJE181
  = 80 Vdc — MJE172, MJE182
- DC Current Gain —
  h_{FE} = 30 (Min) @ I_C = 0.5 Adc
  = 12 (Min) @ I_C = 1.5 Adc
- Current-Gain — Bandwidth Product —
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages —
  I_{CBO} = 100 nA (Max) @ Rated V_{CB}

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
40-60-80 VOLTS
12.5 WATTS



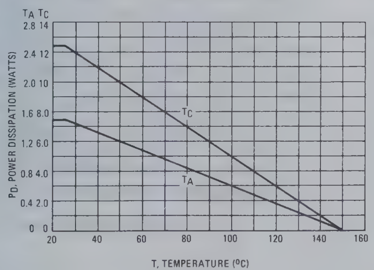
MAXIMUM RATINGS

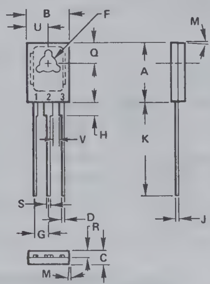
Rating	Symbol	MJE170 MJE180	MJE171 MJE181	MJE172 MJE182	Unit
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 3.0 → ← 6.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 1.5 → ← 0.012 →			Watts W/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 12.5 → ← 0.1 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +150 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	—	0.040	—

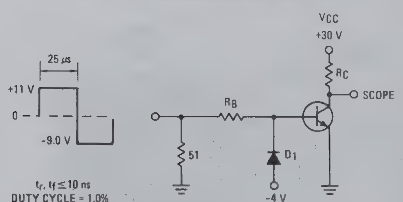
CASE 77-04
TO-126

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	MJE170, MJE180		40	–	
	MJE171, MJE181		60	–	
	MJE172, MJE182		80	–	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 60 Vdc, I_E = 0)	MJE170, MJE180		–	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	MJE171, MJE181		–	0.1	
(V_{CB} = 100 Vdc, I_E = 0)	MJE172, MJE182		–	0.1	
(V_{CB} = 60 Vdc, I_E = 0, T_C = 150°C)	MJE170, MJE180		–	0.1	mAdc
(V_{CB} = 80 Vdc, I_E = 0, T_C = 150°C)	MJE171, MJE181		–	0.1	
(V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	MJE172, MJE182		–	0.1	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			50	250	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			30	–	
(I_C = 1.5 Adc, V_{CE} = 1.0 Vdc)			12	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			–	0.3	
(I_C = 1.5 Adc, I_B = 150 mAdc)			–	0.9	
(I_C = 3.0 Adc, I_B = 600 mAdc)			–	1.7	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 150 mAdc)			–	1.5	
(I_C = 3.0 Adc, I_B = 600 mAdc)			–	2.0	
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	50	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJE170/MJE172		–	60	
	MJE180/MJE182		–	40	

(1) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

For PNP test circuit, reverse all polarities.

FIGURE 3 – TURN-ON TIME

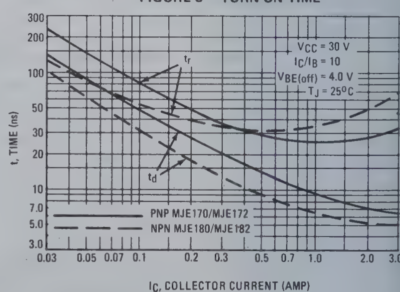
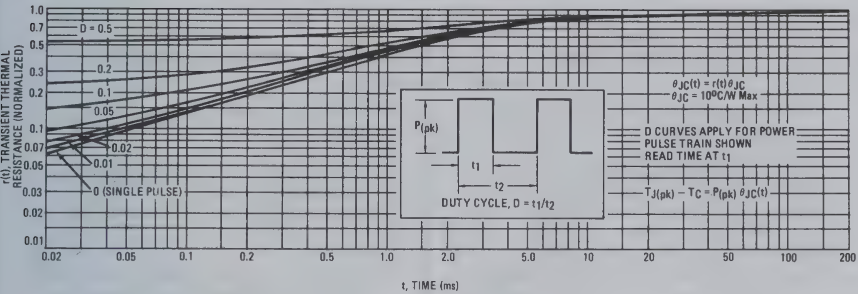


FIGURE 4 — THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 — MJE170, MJE171, MJE172

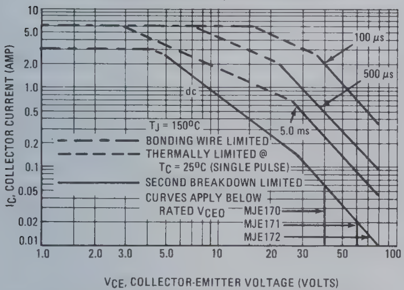
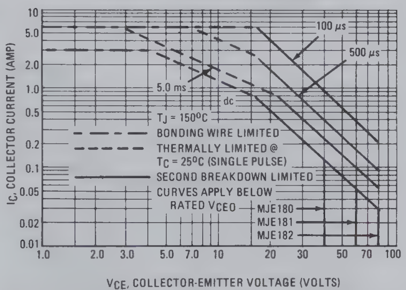


FIGURE 6 — MJE180, MJE181, MJE182



There are two limitations on the power handling ability of a transistor — average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperature, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 — TURN-OFF TIME

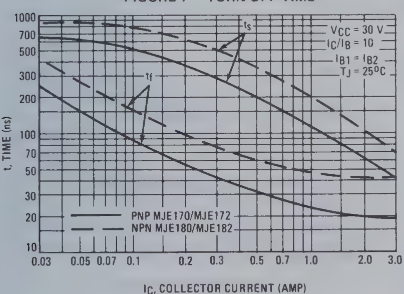
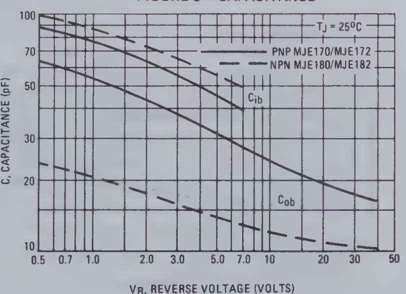


FIGURE 8 — CAPACITANCE



PNP	NPN
MJE170, MJE171, MJE172	MJE180, MJE181, MJE182

FIGURE 9 – DC CURRENT GAIN

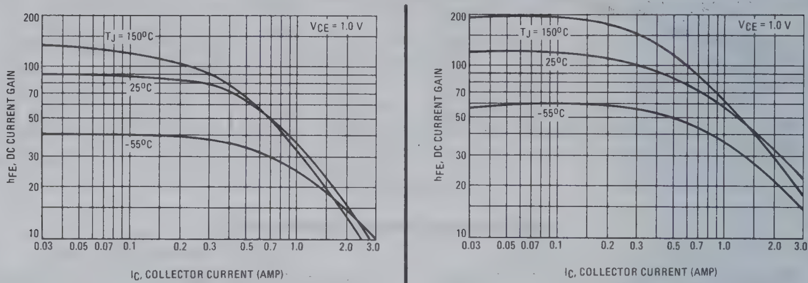


FIGURE 10 – "ON" VOLTAGES

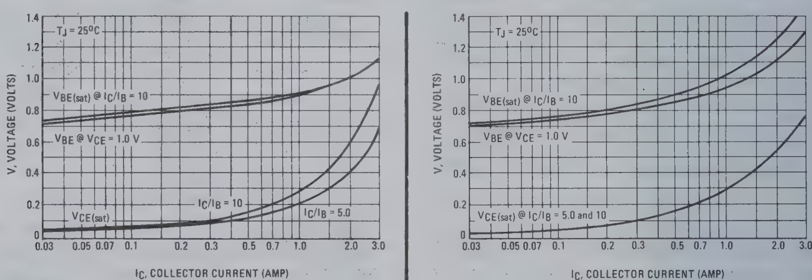
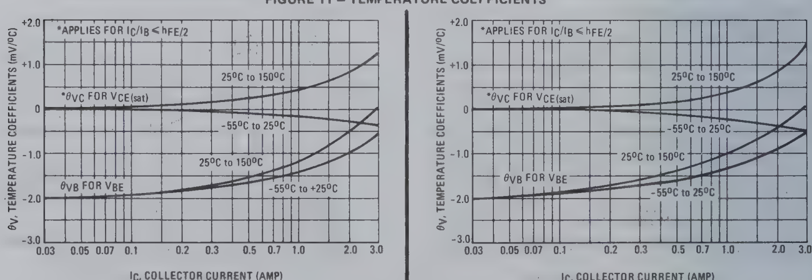


FIGURE 11 – TEMPERATURE COEFFICIENTS



MOTOROLA

MJE200 NPN
MJE210 PNP

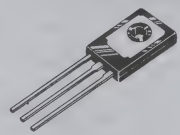
1.3

COMPLEMENTARY SILICON POWER PLASTIC TRANSISTORS

. . . designed for low voltage, low-power, high-gain audio amplifier applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain — h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2.0 Adc
  = 10 (Min) @ I_C = 5.0 Adc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.75 Vdc (Max) @ I_C = 2.0 Adc
- High Current-Gain — Bandwidth Product —
  f_T = 65 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage — I_{CBO} = 100 nAdc @ Rated V_{CB}

5 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
25 VOLTS
15 WATTS



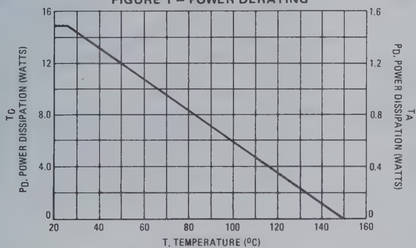
MAXIMUM RATINGS

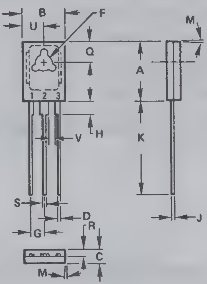
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	40	Vdc
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Emitter-Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous Peak	I_C	5.0 10	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

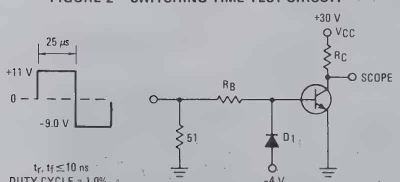
CASE 77-04
TO-126

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	– –	100 100	nAdc μAdc
Emitter Cutoff Current (V_{BE} = 8.0 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	70 45 10	– 180 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	– – –	0.3 0.75 1.8	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	–	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJE200 MJE210	C_{ob}	– –	80 120	pF

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle ≈ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE IB ≈100 mA
MSD6100 USED BELOW IB ≈100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

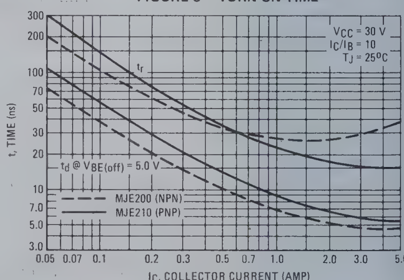


FIGURE 4 – THERMAL RESPONSE

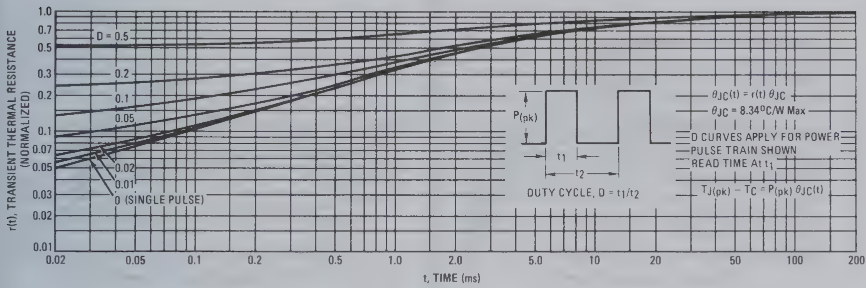
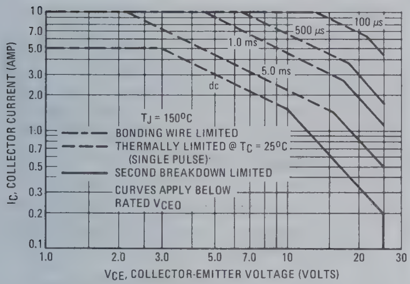


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

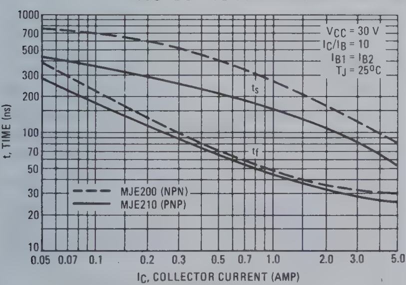
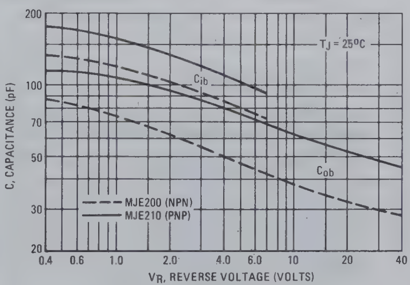


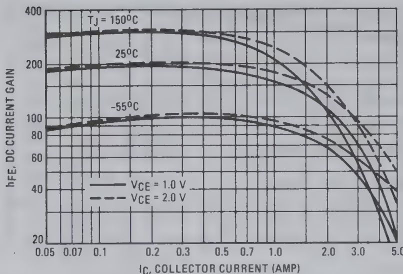
FIGURE 7 – CAPACITANCE



1.3

NPN MJE200	PNP MJE210

FIGURE 8 – DC CURRENT GAIN



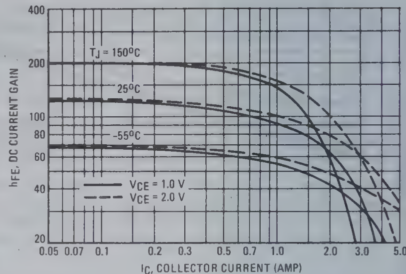
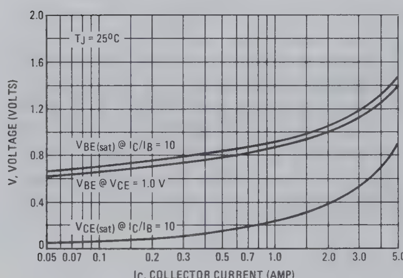


FIGURE 9 – "ON" VOLTAGE



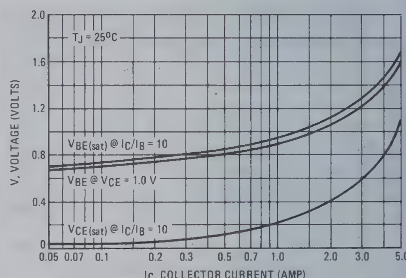
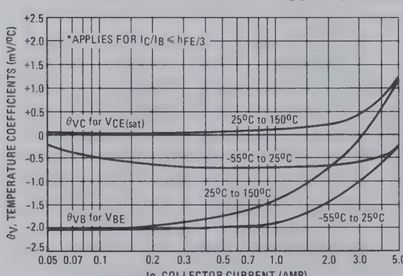
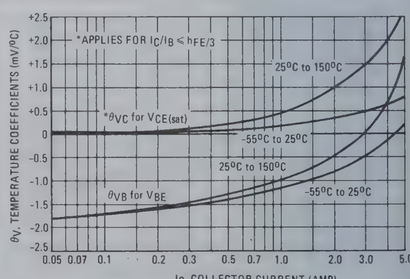


FIGURE 10 – TEMPERATURE COEFFICIENTS





MOTOROLA

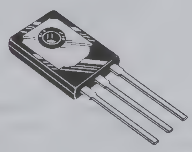
MEDIUM-POWER NPN SILICON TRANSISTOR

. . . for use as an output device in complementary audio amplifiers up to 20-Watts music power per channel.

- High DC Current Gain — h_{FE} = 25-100 @ I_C = 2.0 A
- Thermopad High-Efficiency Compact Package
- Complementary to PNP MJE 105

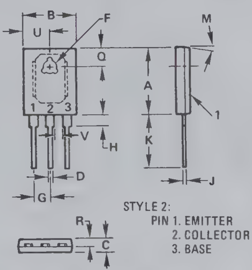
5 AMPERE
POWER TRANSISTOR
NPN SILICON

50 VOLTS
65 WATTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	5.0	Adc
Base Current	I_B	2.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D†	65 0.522	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C



STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.92	°C/W

†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

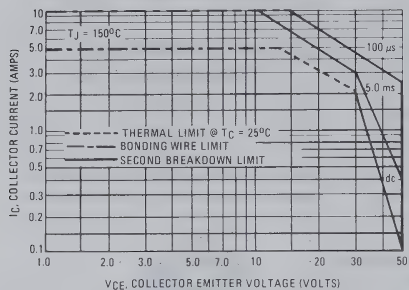
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage‡ (I_C = 100 mAdc, I_B = 0)	BV_{CEO}‡	50	–	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 50 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 – –	 0.1 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter Voltage (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	V_{BE}	–	1.2	Vdc

‡Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

1.3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^oC$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – "ON" VOLTAGES

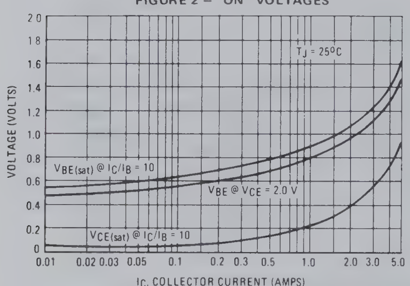


FIGURE 3 – DC CURRENT GAIN

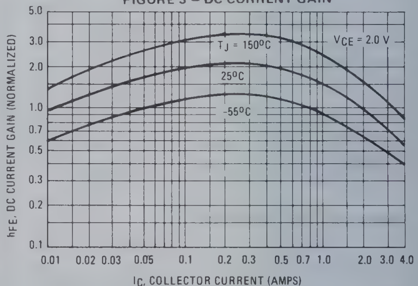
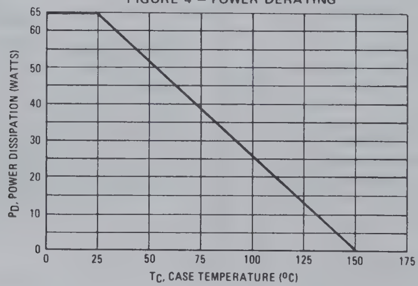


FIGURE 4 – POWER DERATING



MOTOROLA

NPN
MJE240 thru MJE244
PNP
MJE250 thru MJE254

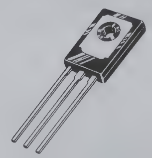
1.3

COMPLEMENTARY SILICON POWER PLASTIC TRANSISTORS

. . . designed for low power audio amplifier and low-current, high-speed switching applications.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — MJE240/2, MJE250/2
  = 100 Vdc (Min) — MJE243/4, MJE253/4
- High DC Current Gain @ I_C = 200 mAdc
  h_{FE} = 40-200 — MJE240, MJE250
  = 40-120 — MJE241,243, MJE251,253
  = 25 (Min) — MJE242,44, MJE252,54
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
- High Current Gain Bandwidth Product —
  f_T = 40 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages
  I_{CBO} = 100 nAdc (Max) @ Rated V_{CB}

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
80, 100 VOLTS
15 WATTS



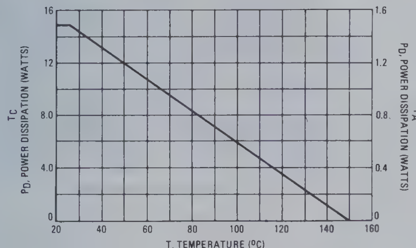
MAXIMUM RATINGS

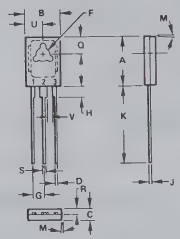
Rating	Symbol	MJE240 MJE241 MJE242 MJE250 MJE251 MJE252	MJE243 MJE244 MJE253 MJE254	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	4.0 8.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

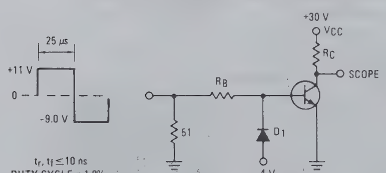
CASE 77-04
TO-126

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	MJE240,MJE241,MJE242, MJE250,MJE251,MJE252	$V_{CEO(sus)}$	80	–	Vdc
	MJE243,MJE244 MJE253,MJE254		100	–	
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	MJE240,MJE241,MJE242, MJE250,MJE251,MJE252	I_{CBO}	–	0.1	μAdc
(V_{CB} = 100 Vdc, I_E = 0)	MJE243,MJE244, MJE253,MJE254,		–	0.1	
(V_{CE} = 80 Vdc, I_E = 0, T_C = 125°C)	MJE240,MJE241,MJE242 MJE250,MJE251,MJE252,		–	0.1	mAdc
(V_{CE} = 100 Vdc, I_E = 0, T_C = 125°C)	MJE243,MJE244 MJE253,MJE254		–	0.1	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 1.0 Vdc)	MJE240,MJE250	h_{FE}	40	200	–
	MJE241,MJE251,		40	120	
	MJE243,MJE253		40	180	
	MJE242,MJE252, MJE244,MJE254		25	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	MJE241,MJE251,		20	–	
	MJE243,MJE253		15	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	MJE242,MJE252 MJE244,MJE254		10	–	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)	MJE240,MJE250		15	–	
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	All Types	$V_{CE(sat)}$	–	0.3	Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc)	MJE241,MJE251, MJE243,MJE253		–	0.6	
(I_C = 2.0 Adc, I_B = 200 mAdc)	MJE240, MJE250		–	0.8	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	1.8	Vdc
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJE240/MJE244	C_{ob}	–	50	pF
	MJE250/MJE254		–	70	

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 — TURN-ON TIME

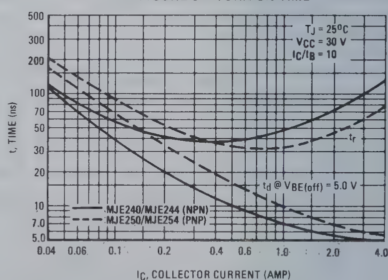


FIGURE 4 – THERMAL RESPONSE

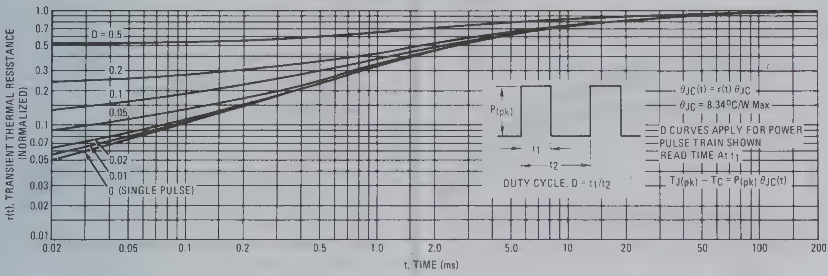
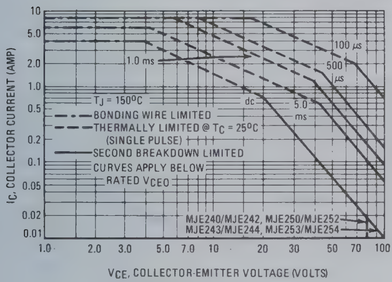


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

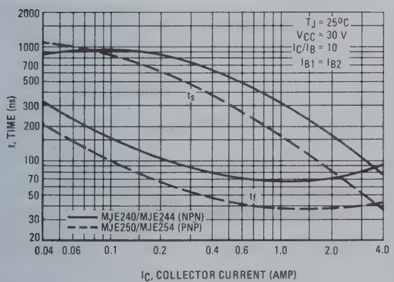
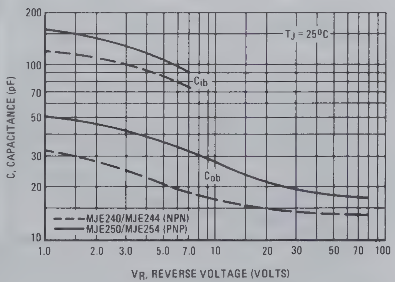


FIGURE 7 – CAPACITANCE



1.3

NPN	PNP
MJE240 thru MJE244	MJE250 thru MJE254

FIGURE 8 – DC CURRENT GAIN

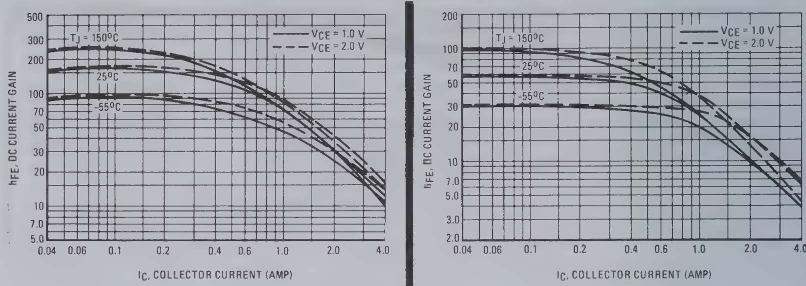


FIGURE 9 – "ON" VOLTAGES

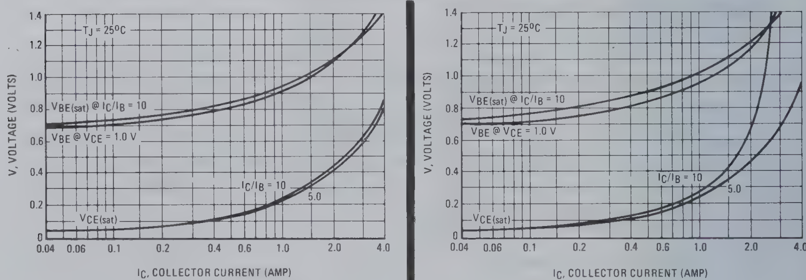
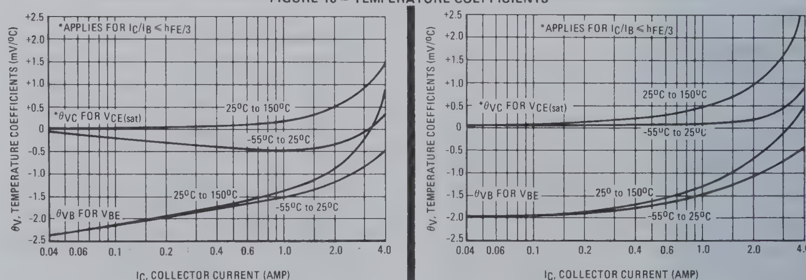


FIGURE 10 – TEMPERATURE COEFFICIENTS



MOTOROLA

PLASTIC MEDIUM POWER NPN SILICON TRANSISTOR

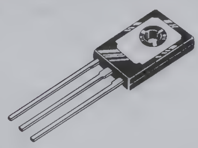
. . . useful for high-voltage general purpose applications.

- Suitable for Transformerless, Line-Operated Equipment
- Thermopad Construction Provides High Power Dissipation Rating for High Reliability

0.5 AMPERE

POWER TRANSISTOR NPN SILICON

300 VOLTS
20 WATTS



MAXIMUM RATINGS

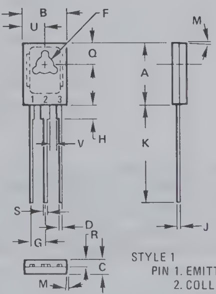
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	20 0.16	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ($I_C = 1.0$ mAdc, $I_B = 0$)	$V_{CEO(sus)}$	300		Vdc
Collector Cutoff Current ($V_{CB} = 300$ Vdc, $I_E = 0$)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current ($V_{EB} = 3.0$ Vdc, $I_C = 0$)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 50$ mAdc, $V_{CE} = 10$ Vdc)	h_{FE}	30	240	—



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	—	0.040	—

CASE 77-04
TO-126

FIGURE 1 – POWER TEMPERATURE DERATING

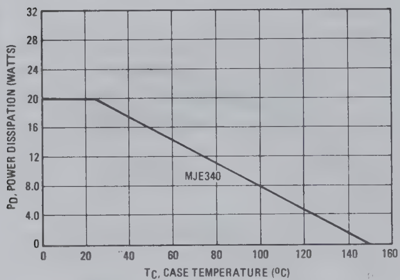
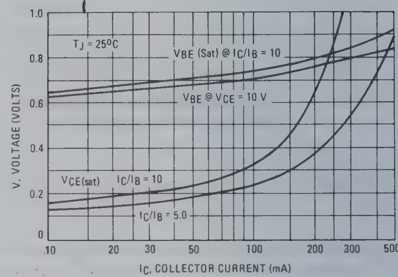
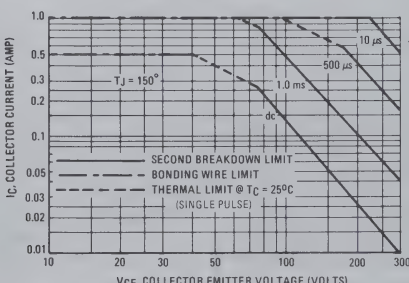


FIGURE 2 – "ON" VOLTAGES



ACTIVE-REGION SAFE OPERATING AREA

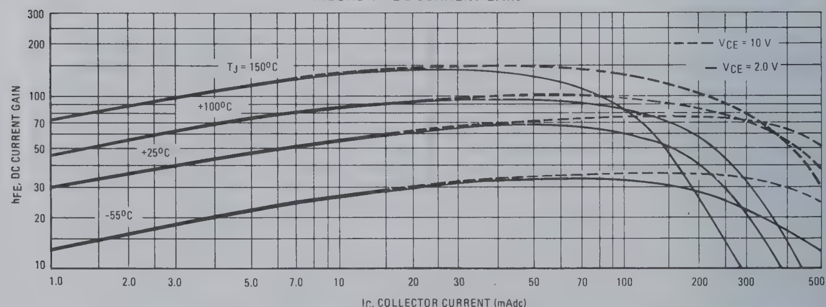
FIGURE 3 – MJE340



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 – DC CURRENT GAIN



MJE341
MJE344

MOTOROLA

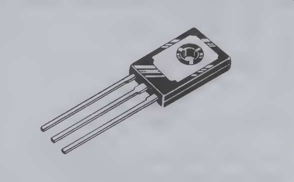
1.3

PLASTIC NPN SILICON MEDIUM-POWER TRANSISTORS

. . .useful for medium voltage applications requiring high f_T such as converters and extended range amplifiers.

0.5 AMPERE POWER TRANSISTORS NPN SILICON

150-200 VOLTS 20 WATTS

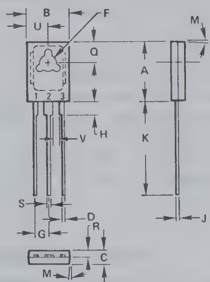


MAXIMUM RATINGS

Rating	Symbol	MJE341	MJE344	Unit
Collector-Emitter Voltage	V_{CEO}	150	200	Vdc
Collector-Base Voltage	V_{CB}	175	200	Vdc
Emitter-Base Voltage	V_{EB}	3.0	5.0	Vdc
Collector Current — Continuous	I_C	← 500 →		mAdc
Base Current	I_B	← 250 →		mAdc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	20 0.16		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

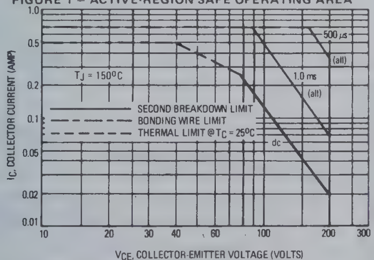


STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	MJE341 MJE344	$V_{CEO(sus)}$	150 200	– –	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0)	MJE341 MJE344	I_{CEO}	– –	1.0 1.0	mAdc
Collector Cutoff Current (V_{CB} = 175 Vdc, I_E = 0) (V_{CB} = 200 Vdc, I_E = 0)	MJE341 MJE344	I_{CBO}	– –	0.3 0.1	mAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0) (V_{EB} = 5.0 Vdc, I_C = 0)	MJE341 MJE344	I_{EBO}	– –	0.1 0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 50 mAdc, V_{CE} = 10 Vdc) (I_C = 150 mAdc, V_{CE} = 10 Vdc)	MJE341 MJE341 MJE344 MJE341	h_{FE}	20 25 30 20	– 200 300 –	–
Collector-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc) (I_C = 150 mAdc, I_B = 15 mAdc)	MJE344 MJE341	$V_{CE(sat)}$	– –	1.0 2.3	Vdc
Base-Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 25 Vdc, f = 10 MHz)		f_T	15	–	MHz
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	15	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

FIGURE 2 – DC CURRENT GAIN

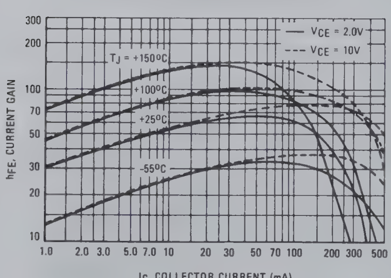
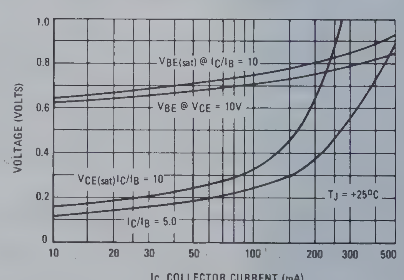


FIGURE 3 – "ON" VOLTAGES



MOTOROLA

PLASTIC MEDIUM POWER PNP SILICON TRANSISTOR

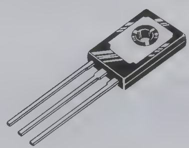
. . . designed for use in line-operated applications such as low power, line-operated series pass and switching regulators requiring PNP capability.

- High Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 300 Vdc @ I_C = 1.0 mAdc
- Excellent DC Current Gain — h_{FE} = 30-240 @ I_C = 50 mAdc
- Plastic Thermopad Package

0.5 AMPERE

POWER TRANSISTOR PNP SILICON

300 VOLTS
20 WATTS



MAXIMUM RATINGS

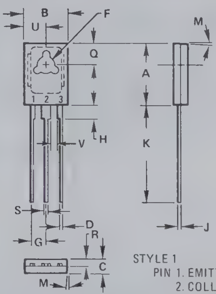
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current - Continuous	I_C	500	mAdc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	20 0.16	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	–	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	–



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3^o TYP		3^o TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

FIGURE 1 – DC CURRENT GAIN

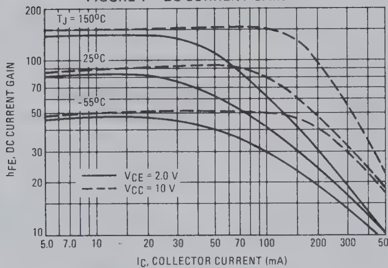


FIGURE 2 – "ON" VOLTAGES

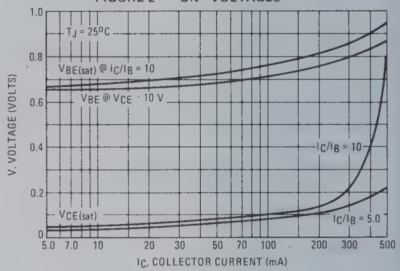


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA

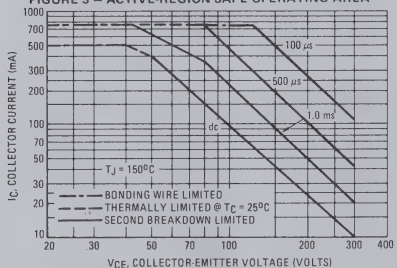


FIGURE 4 – TEMPERATURE COEFFICIENTS

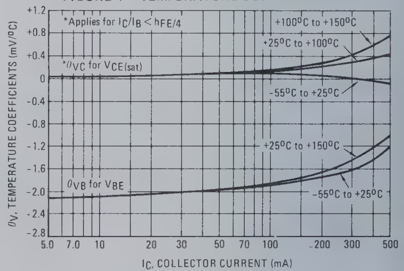
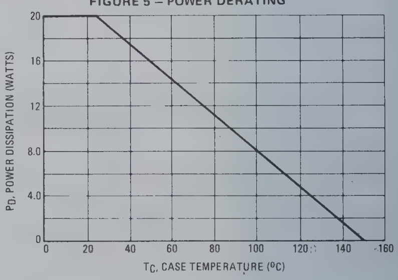


FIGURE 5 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA

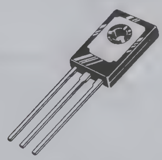
PLASTIC MEDIUM-POWER PNP SILICON TRANSISTOR

. . . designed for use in general-purpose amplifiers and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain — h_{FE} = 25 (Min) @ I_C = 1.0 Adc
- Complementary to NPN MJE520

3 AMPERE POWER TRANSISTOR PNP SILICON

30 VOLTS 25 WATTS

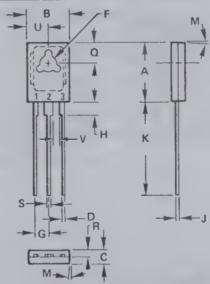


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	3.0	Adc
— Peak		7.0	
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ $T_C = 25^{\circ}C$ Derate above $25^{\circ}C$	P_D	25 0.2	Watts $W/^{\circ}C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^{\circ}C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	$^{\circ}C/W$



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	—	0.040	—

CASE 77-04
TO-126

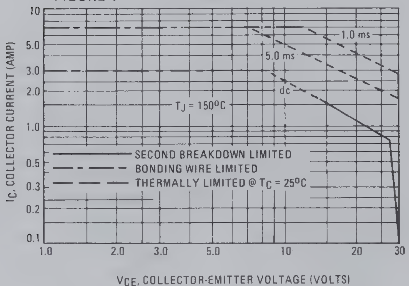
ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	—	Vdc
Collector-Base Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter-Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	25	—	—

(1) Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2.0%.

1.3

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 — DC CURRENT GAIN

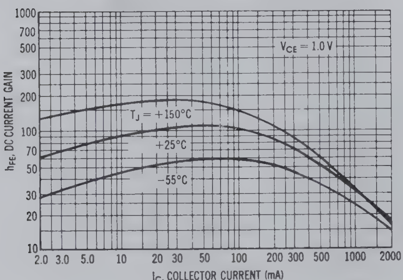


FIGURE 3 — "ON" VOLTAGE

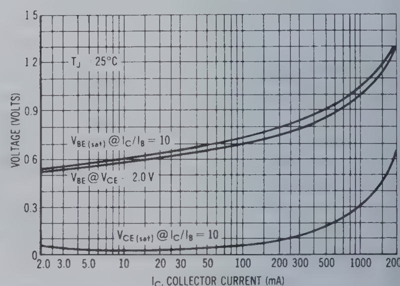
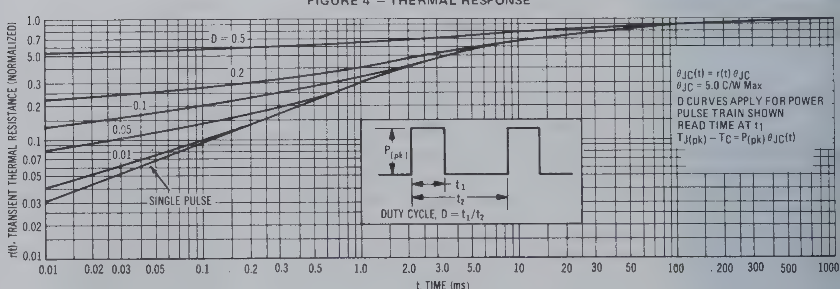


FIGURE 4 — THERMAL RESPONSE



MOTOROLA

1.3

PLASTIC MEDIUM-POWER PNP SILICON TRANSISTORS

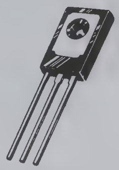
. . . designed for use in general-purpose amplifier and switching circuits. Recommended for use in 5 to 20 Watt audio amplifiers utilizing complementary symmetry circuitry.

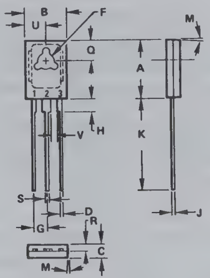
- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- MJE371 is Complementary to NPN MJE521

4 AMPERE

POWER TRANSISTORS PNP SILICON

40 VOLTS
40 WATTS





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	4.0 8.0	Adc
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

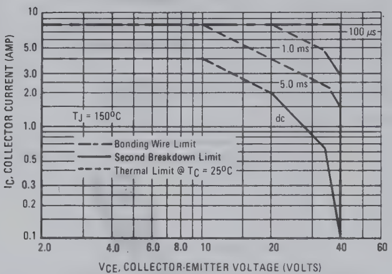
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter-Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs Duty Cycle ≤ 2.0%.

1.3

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – DC CURRENT GAIN

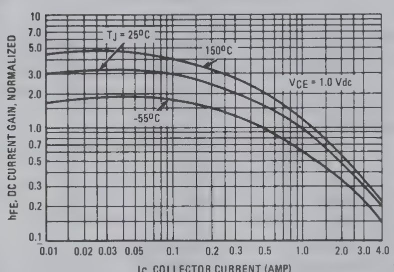


FIGURE 3 – "ON" VOLTAGE

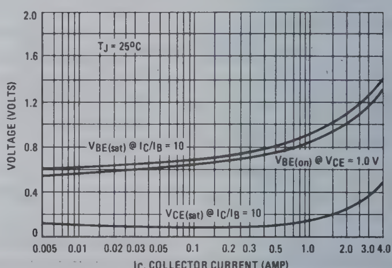
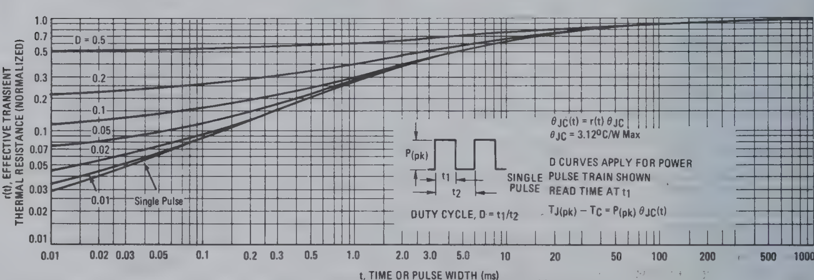


FIGURE 4 – THERMAL RESPONSE



MOTOROLA

PLASTIC MEDIUM-POWER NPN SILICON TRANSISTOR

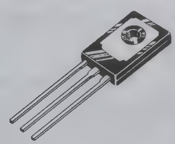
. . . designed for use in general-purpose amplifier and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

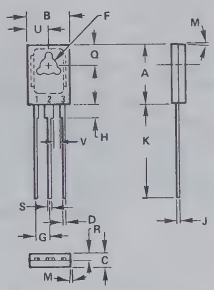
- DC Current Gain — h_{FE} = 25 (Min) @ I_C = 1.0 Adc
- Complementary to PNP MJE370

3 AMPERE

POWER TRANSISTOR NPN SILICON

30 VOLTS
25 WATTS





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3^o TYP		3^o TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	—	0.040	—

CASE 77-04
TO-126

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	3.0 7.0	Adc
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.2	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

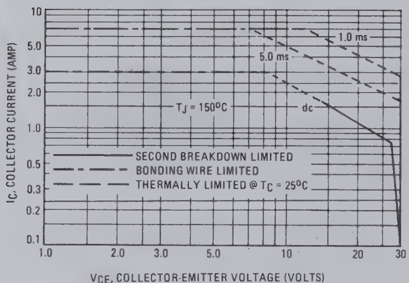
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	—	Vdc
Collector-Base Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter-Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	25	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 ACTIVE-REGION SAFE OPERATING AREA



The data of Figure 1 based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided (T_{Jpk}) ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

FIGURE 2 – DC CURRENT GAIN

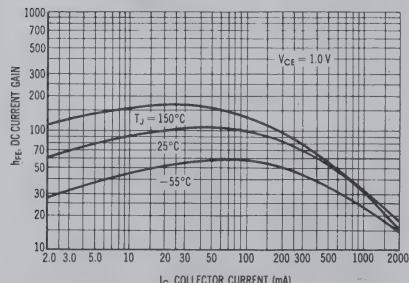


FIGURE 3 – "ON" VOLTAGE

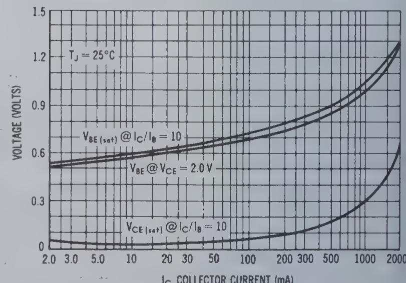
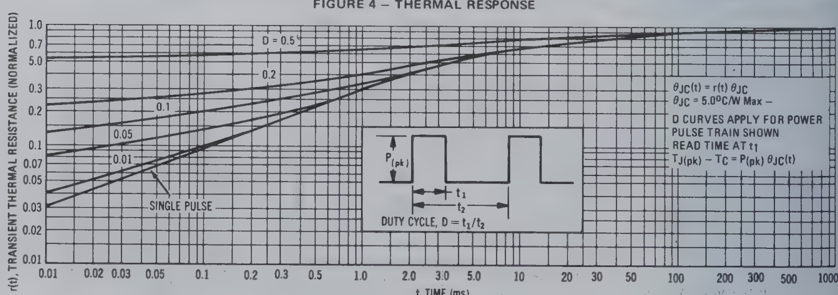


FIGURE 4 – THERMAL RESPONSE



PNP
MJE700, T thru MJE703, T

NPN
MJE800, T thru MJE803, T

MOTOROLA

1.3

PLASTIC DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain — h_{FE} = 2000 (Typ) @ I_C = 2.0 Adc
- Monolithic Construction with Built-in Base-Emitter Resistors to Limit Leakage Muliplication
- Choice of Packages — TO126, MJE700 and MJE800 series; TO220AB, MJE700T and MJE800T series

4.0 AMPERE

DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

40 WATT – TO-126
50 WATT – TO-220AB

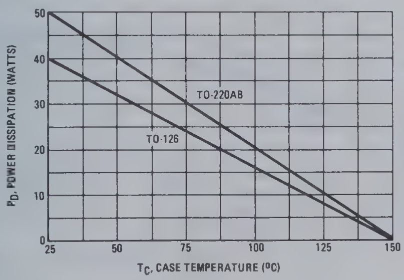
MAXIMUM RATINGS

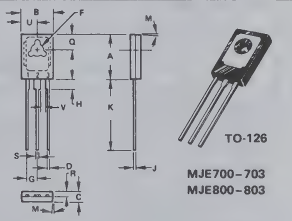
Rating	Symbol	MJE700,T MJE701,T MJE800,T MJE801,T	MJE702,T MJE703,T MJE802,T MJE803,T	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	0.1		Adc
		TO-126	TO-220	
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	50 0.40	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
TO-126		3.13	
TO-220		2.50	

FIGURE 1 — POWER DERATING





TO-126

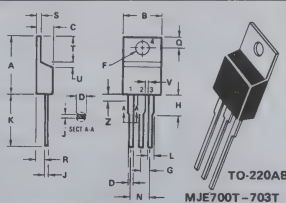
MJE700–703
MJE800–803

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10 80	11.05	0.425	0.435
B	7.49	7 75	0.295	0.305
C	2 41	2.67	0 095	0 105
D	0 51	0.66	0 020	0.026
F	2.92	3 18	0.115	0.125
G	2 31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0 38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3 76	4.01	0 148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0 145	0.155
V	1.02	–	0.040	–

STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES
1. MT = MAIN TERMINAL
2. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. TO DIM. "A" & "B" AT MAXIMUM MATERIAL CONDITION

CASE 77-04



TO-220AB

MJE700T–703T
MJE800T–803T

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15 75	0.575	0.620
B	9 65	10 29	0 380	0.405
C	4.06	4.82	0.160	0 190
D	0 64	0.89	0 025	0 035
F	3 61	3 73	0.142	0 147
G	2 41	2.67	0 095	0.105
H	2 79	3.93	0.110	0.155
J	0 36	0.56	0.014	0.022
K	12 70	14.27	0.500	0.562
L	1 14	1.39	0 045	0.055
N	4.83	5.33	0 190	0.210
Q	2.54	3.04	0 100	0.120
R	2.04	2 79	0 080	0.110
S	1.14	1.39	0 045	0 055
T	5.97	6.48	0 235	0 255
U	0.00	1.27	0.000	0.050
V	1.14	–	0 045	–
Z	–	2.03	–	0.080

STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3

CASE 221A-02

PNP MJE700,T thru MJE703,T
NPN MJE800,T thru MJE803,T

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 50 mAdc, I_B = 0)	MJE700,T, MJE701,T, MJE800,T, MJE801,T		60	–	
	MJE702,T, MJE703,T, MJE802,T, MJE803,T		80	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 60 Vdc, I_B = 0)	MJE700,T, MJE701,T, MJE800,T, MJE801,T		–	100	
(V_{CE} = 80 Vdc, I_B = 0)	MJE702,T, MJE703,T, MJE802,T, MJE803,T		–	100	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = Rated BV_{CEO}, I_E = 0)			–	100	
(V_{CB} = Rated BV_{CEO}, I_E = 0, $T_C = 100^oC$)			–	500	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc)	MJE700,T, MJE702,T, MJE800,T, MJE802,T		750	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	MJE701,T, MJE703,T, MJE801,T, MJE803,T		750	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	All devices		100	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 30 mAdc)	MJE700,T, MJE702,T, MJE800,T, MJE802,T		–	2.5	
(I_C = 2.0 Adc, I_B = 40 mAdc)	MJE701,T, MJE703,T, MJE801,T, MJE803,T		–	2.8	
(I_C = 4.0 Adc, I_B = 40 mAdc)	All Device		–	3.0	
Base-Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc)	MJE700,T, MJE702,T, MJE800,T, MJE802,T		–	2.5	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	MJE701,T, MJE703,T, MJE801,T, MJE803,T		–	2.5	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	All Devices		–	3.0	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	1.0	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

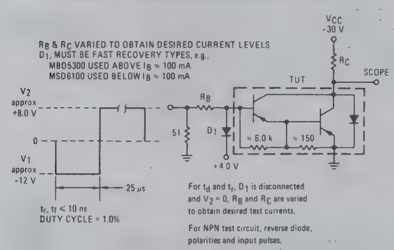


FIGURE 3 – SWITCHING TIMES

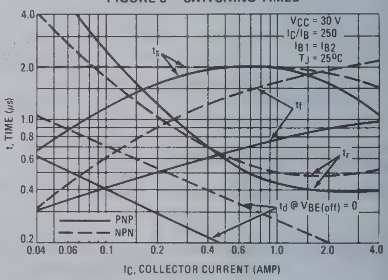


FIGURE 4 – THERMAL RESPONSE (MJE700T, 800T series)

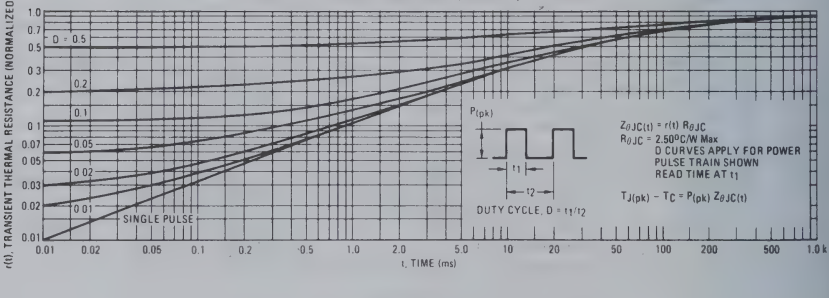
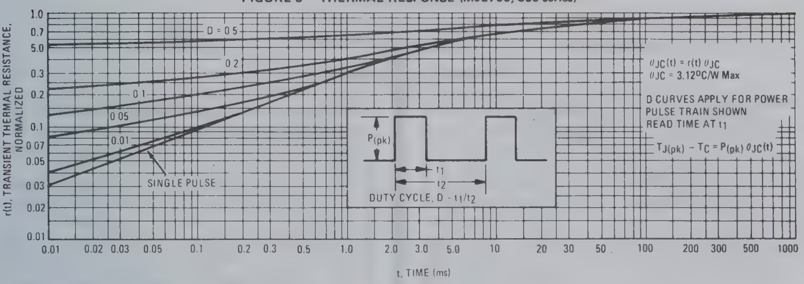


FIGURE 5 – THERMAL RESPONSE (MJE700, 800 series)



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 6 – MJE700 series

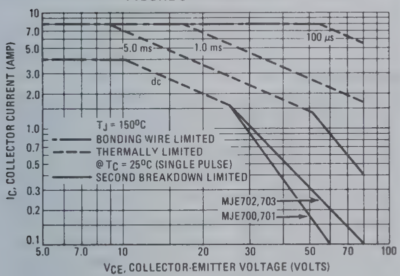
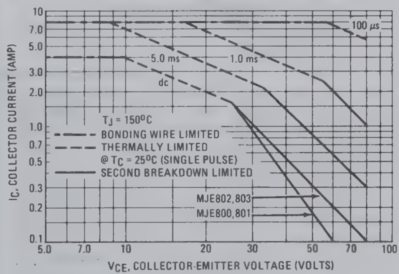


FIGURE 7 – MJE800 series



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 6 and 7 are based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4 or 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 – MJE700T series

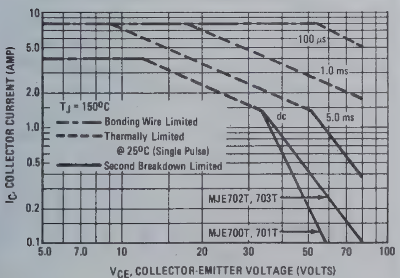
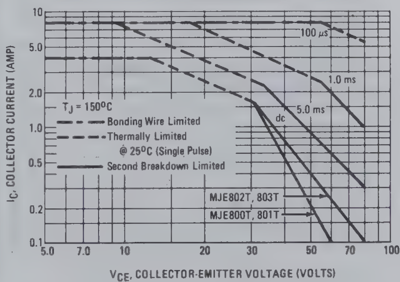


FIGURE 9 – MJE800T series



1.3

PNP
MJE700,T series

NPN
MJE800,T series

FIGURE 10 — DC CURRENT GAIN

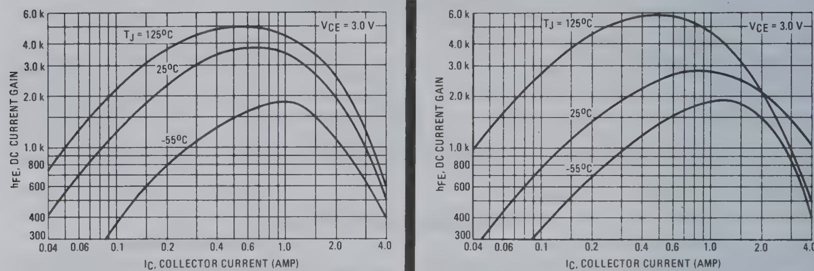


FIGURE 11 — COLLECTOR SATURATION REGION

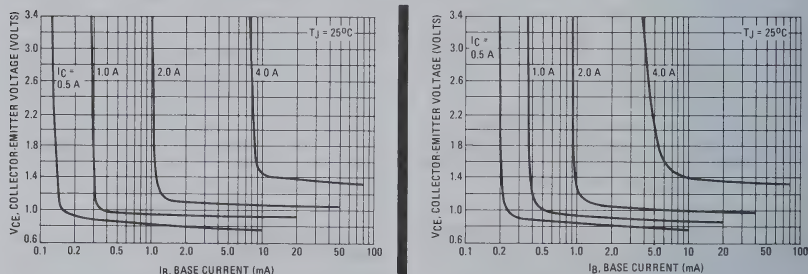
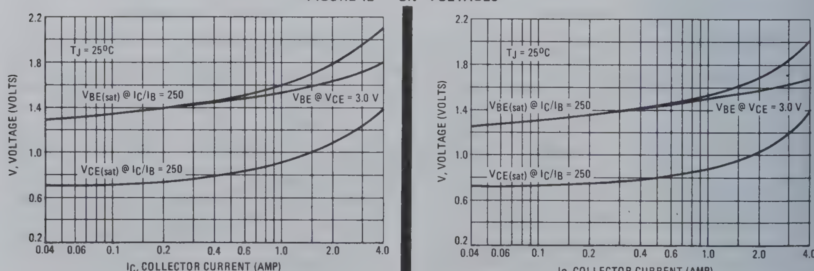


FIGURE 12 — "ON" VOLTAGES



MJE1290 MJE1291 PNP
MJE1660 MJE1661 NPN

MOTOROLA

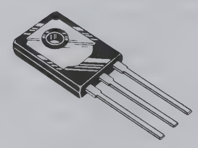
COMPLEMENTARY SILICON MEDIUM-POWER TRANSISTORS

. . . designed for use in power amplifier and switching applications.

- High Collector Current — I_C = 15 Adc
- High DC Current Gain — h_{FE} = 10 (Min) @ I_C = 15 Adc

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON

40-60 VOLTS
90 WATTS

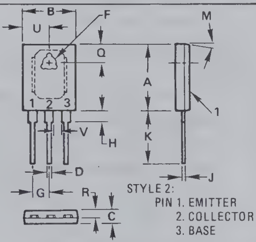


MAXIMUM RATINGS

Rating	Symbol	MJE1290 MJE1660	MJE1291 MJE1661	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Base Voltage	V_{CB}	40	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current-Continuous	I_C	15		Adc
Base Current	I_B	5.0		Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	90 0.72		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		^oC

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	$^oC/W$



STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

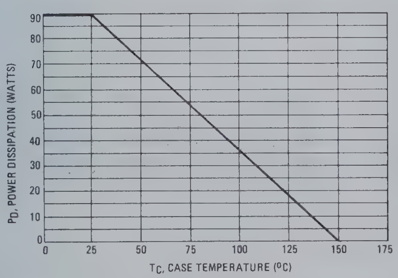
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9^0 TYP		9^0 TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

When mounting the device, torque not to exceed 8.0 in.-lb.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

FIGURE 1 — POWER TEMPERATURE DERATING CURVE



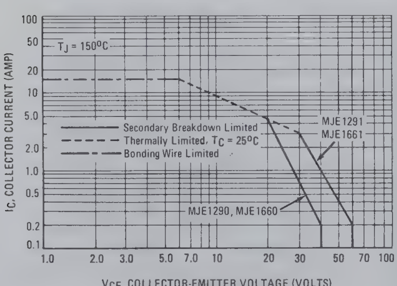
1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	MJE1290, MJE1660 MJE1291, MJE1661	$V_{CEO(sus)}$	40 60	– –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)		I_{CEO}	–	1.0	mAdc
Collector Cutoff Current (V_{CE} = 40 Vdc, V_{BE} = 0) (V_{CE} = 60 Vdc, V_{BE} = 0)	MJE1290, MJE1660 MJE1291, MJE1661	I_{CES}	– –	0.7 0.7	mAdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0)	MJE1290, MJE1660 MJE1291, MJE1661	I_{CBO}	– –	0.7 0.7	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_E = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	20 10	100 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 15 Adc, I_B = 1.5 Adc)		$V_{CE(sat)}$	–	1.8	Vdc
Base-Emitter on Voltage (1) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs. Duty Cycle ≤ 2.0%.

FIGURE 2 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

MOTOROLA

MJE2360T
MJE2361T

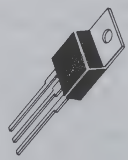
NPN SILICON HIGH-VOLTAGE TRANSISTOR

. . . useful for general-purpose, high voltage applications requiring high f_T.

- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 350 Vdc (Min) @ I_C = 2.5 mAdc
- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 100 mAdc – MJE2361T
- Current-Gain—Bandwidth Product — f_T = 10 MHz (Typ) @ I_C = 50 mAdc

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON

350 VOLTS
30 WATTS



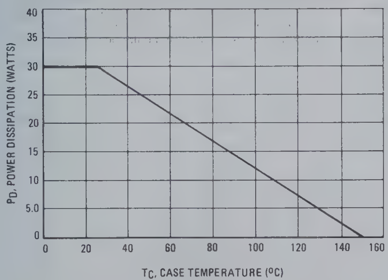
MAXIMUM RATINGS

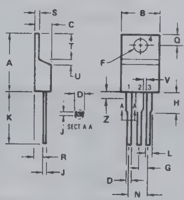
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	350	Vdc
Collector-Base Voltage	V_{CB}	375	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	0.5	Adc
Base Current	I_B	0.25	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	30 0.24	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.167	$^oC/W$

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE





STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
(TO-220 AB)

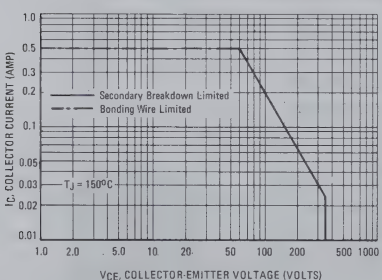
1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage(1) (I_C = 2.5 mAdc, I_B = 0)	$V_{CEO(sus)}$	350	–	–	Vdc
Collector Cutoff Current (V_{CE} = 250 Vdc, I_B = 0)	I_{CEO}	–	–	0.25	mAdc
Collector Cutoff Current (V_{CE} = 375 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}			0.5	mAdc
Collector Cutoff Current (V_{CB} = 375 Vdc, I_E = 0)	I_{CBO}	–		0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				–
(I_C = 50 mAdc, V_{CE} = 10 Vdc) MJE2360T		25		200	
MJE2361T		50	–	250	
(I_C = 100 mAdc, V_{CE} = 10 Vdc) MJE2360T		15		–	
MJE2361T		40		–	
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$			1.5	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$			1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		10		MHz
Output Capacitance (V_{CB} = 100 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	20	–	pF

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

NPN
MJE2801, MJE2801T
PNP
MJE2901, MJE2901T

MOTOROLA

1.3

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . for use as an output device in complementary audio amplifiers up to 35-Watts music power per channel.

- High DC Current Gain — h_{FE} = 25-100 @ I_C = 3.0 A
- Choice of Packages — MJE2801, 2901 — TO-225AB (TO-127)
  MJE2801T, 2901T — TO-220AB

10 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS

60 VOLTS
75, 90 WATTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	5.0	Adc
Total Power Dissipation @ $T_C = 25^oC$	P_D†		Watts
MJE2801, 2901		90	
MJE2801T, 2901T		75	
Derate above 25°C			
MJE2801, 2901		0.72	W/°C
MJE2801T, 2901T		0.6	
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

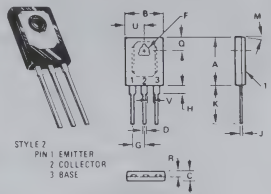
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		°C/W
MJE2801, 2901		1.39	
MJE2801T, 2901T		1.67	

†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 200 mAdc, I_B = 0)	BV_{CEO}	60	–	Vdc
Collector-Cutoff Current	I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)		–	0.1	
(V_{CB} = 60 Vdc, I_E = 0, $T_C = 150^oC$)		–	2.0	
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter Voltage (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	V_{BE}	–	1.4	Vdc

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

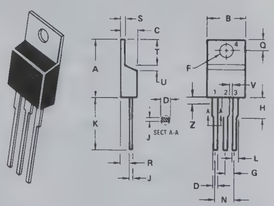


STYLE 2
PIN 1 EMITTER
2 COLLECTOR
3 BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03		0.080	

MJE2801
MJE2901

CASE 90-05
TO-225AB
(TO-127)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

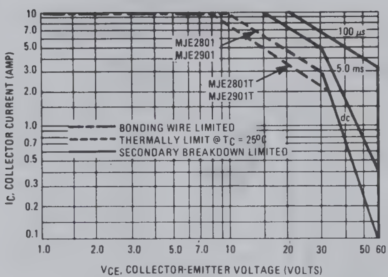
STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3
3 DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4 DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
5 CONTROLLING DIMENSION INCH

CASE 221A-02
TO-220AB

1.3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – DC CURRENT GAIN

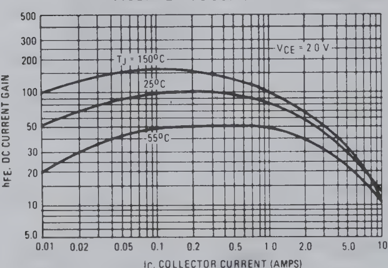


FIGURE 3 – POWER DERATING

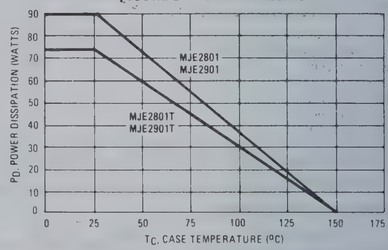
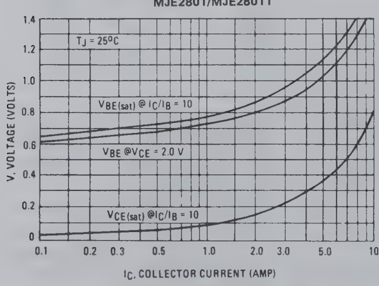
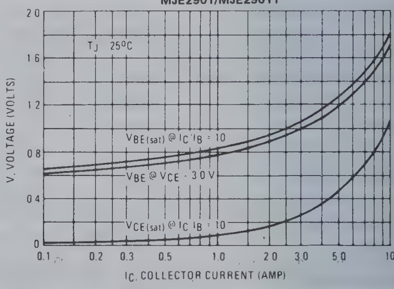


FIGURE 4 – "ON" VOLTAGES

MJE2801/MJE2801T



MJE2901/MJE2901T



MJE2955, MJE2955T PNP
MJE3055, MJE3055T NPN

MOTOROLA

1.3

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 10 Amperes
- High Current Gain — Bandwidth Product — f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Choice of Packages — MJE3055, MJE2955 — TO-225AB (TO-127)
  MJE3055T, MJE2955T — TO-220AB

10 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60 VOLTS
75, 90 WATTS

MAXIMUM RATINGS

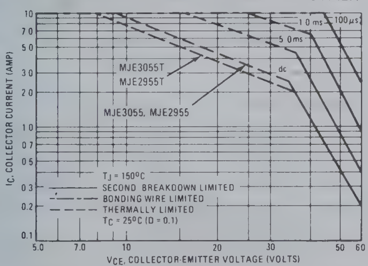
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	70	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6.0	Adc
Total Power Dissipation @ T_C = 25°C MJE3055, MJE2955 MJE3055T, MJE2955T Derate above 25°C MJE3055, MJE2955 MJE3055T, MJE2955T	P_D†	 90 75 0.72 0.6	Watts W/°C W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case MJE3055, MJE2955 MJE3055T, MJE2955T	θ_{JC}	 1.39 1.67	°C/W

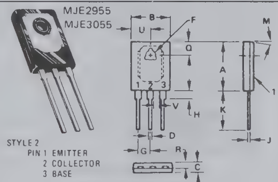
†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



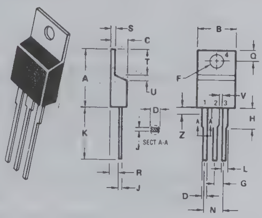
There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown Safe operating area curves indicate I_C V_{CE} limits of the transistor that must be observed for reliable operation i e , the transistor must not be subjected to greater dissipation than the curves indicate

The data of Figure 1 is based on $T_{J(pk)}$ 150°C. T_C is variable depending on conditions Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$ At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (See AN 415A)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16 38	0.635	0 645
B	12 57	12.83	0 495	0 505
C	3 18	3.43	0 125	0 135
D	1 09	1 24	0 043	0 049
F	3 51	3 76	0 138	0 148
G	4 22 BSC		0 166 BSC	
H	2 67	2.92	0 105	0 115
J	0 813	0 864	0 032	0 034
K	15 11	16 38	0 595	0 645
M	9° TYP		9° TYP	
Q	4 70	4 95	0 185	0 195
R	1 91	2 16	0 075	0 085
U	6.22	6 48	0 245	0.255
V	2 03		0 080	

CASE 90-05
TO-225AB
(TO-127)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14 60	15.75	0 575	0.620
B	9 65	10 29	0 380	0 405
C	4.06	4.82	0.160	0 190
D	0 64	0 89	0.025	0 035
F	3 61	3 73	0 142	0 147
G	2 41	2 67	0 095	0 105
H	2.79	3 93	0.110	0 155
J	0.36	0 56	0 014	0 022
K	12 70	14.27	0.500	0 562
L	1.14	1 39	0.045	0.055
N	4.83	5 33	0 190	0.210
Q	2.54	3.04	0 100	0 120
R	2.04	2.79	0.080	0 110
S	1.14	1 39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1 27	0.000	0 050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3
3 DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4 DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
5 CONTROLLING DIMENSION INCH

MJE2955T
MJE3055T

CASE 221A-02
TO 220AB

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}		700	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	–	1.0	mAdc
(V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			5.0	
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	–	1.0	mAdc
(V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)		–	10	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20	100	-
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)		5 0	–	
Collector-Emitter Saturation Voltage (1) (I_C = 4.0 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	–	1.1	Vdc
(I_C = 10 Adc, I_B = 3.3 Adc)			8.0	
Base-Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1 8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — DC CURRENT GAIN

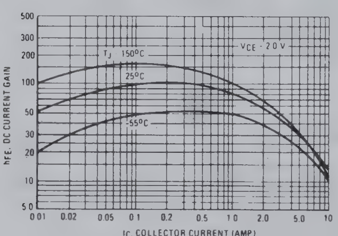


FIGURE 3 — POWER DERATING

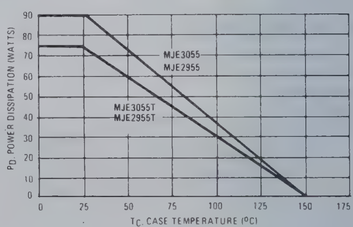
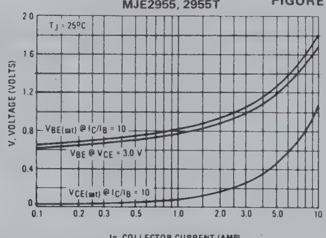
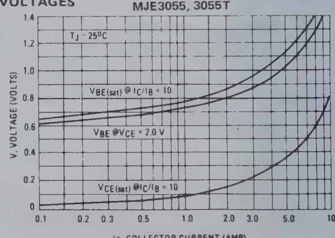


FIGURE 4 — "ON" VOLTAGES

MJE2955, 2955T



MJE3055, 3055T



MJE3300 MJE3301 MJE3302 NPN
MJE3310 MJE3311 MJE3312 PNP

MOTOROLA

PLASTIC DARLINGTON COMPLEMENTARY SILICON ANNULAR POWER TRANSISTORS

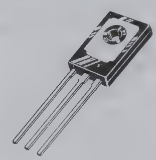
. . . designed for general-purpose amplifier and high-speed switching applications.

- High DC Current Gain —
  h_{FE} = 2000 (Typ) @ I_C = 1.0 Adc
- Collector-Emitter Sustaining Voltage — @ 10 mAdc
  $V_{CEO(sus)}$ = 40 Vdc (Min) — MJE3310/MJE3300
  = 60 Vdc (Min) — MJE3311/MJE3301
  = 80 Vdc (Min) — MJE3312/MJE3302
- Reverse Voltage Protection Diode
- Pinout Compatible with TO-220 Package
- Monolithic Construction with Built-In Base-Emitter Output Resistor
- Thermopad II Construction With Hard Solder for High Reliability

DARLINGTON
4-AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40, 60, 80 VOLTS
15 WATTS



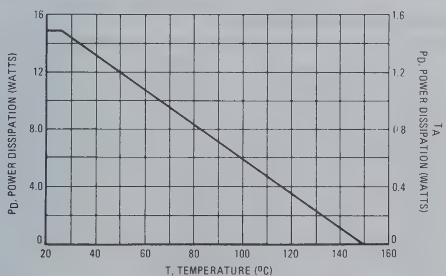
MAXIMUM RATINGS

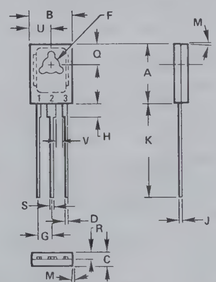
Rating	Symbol	MJE3310 MJE3300	MJE3311 MJE3301	MJE3312 MJE3302	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	4.0 6.0			Adc
Base Current	I_B	100			mAdc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	15 0.12			Watts $W/^oC$
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	1.5 0.012			Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83.3	$^oC/W$

FIGURE 1 — POWER DERATING





STYLE 3.
PIN 1. BASE
2. COLLECTOR
3. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3^o TYP		3^o TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

MJE3300, MJE3301, MJE3302 NPN
MJE3310, MJE3311, MJE3312 PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	MJE3310,MJE3300		40	–	
	MJE3311,MJE3301		60	–	
	MJE3312,MJE3302		80	–	
Collector-Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 20 Vdc, I_B = 0)	MJE3310,MJE3300		–	100	
(V_{CE} = 30 Vdc, I_B = 0)	MJE3311,MJE3301		–	100	
(V_{CE} = 40 Vdc, I_B = 0)	MJE3312,MJE3302		–	100	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = Rated $V_{CEO(sus)}$, I_E = 0)			–	1.0	
(V_{CB} = Rated $V_{CEO(sus)}$, I_E = 0, T_C = 100°C)			–	100	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	μAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)			1000	–	
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			750	–	
Collector-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 6.0 mAdc)		$V_{CE(sat)}$	–	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 6.0 mAdc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	2.5	Vdc
Output Diode Voltage Drop (I_{EC} = 2.0 Adc)		V_{EC}	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)		f_T	20	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — ACTIVE-REGION SAFE OPERATING AREA

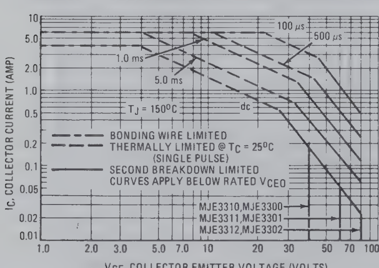


FIGURE 3 — TYPICAL DC CURRENT GAIN

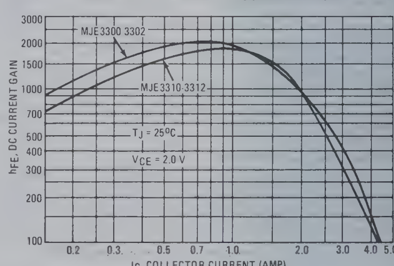
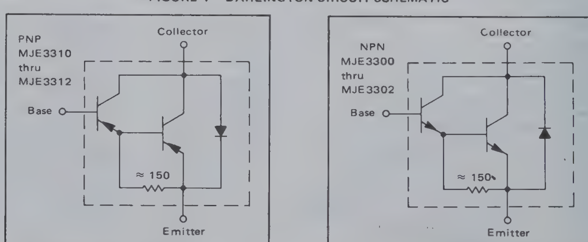


FIGURE 4 — DARLINGTON CIRCUIT SCHEMATIC



MJE3439
MJE3440

MOTOROLA

1.3

NPN SILICON HIGH-VOLTAGE POWER TRANSISTORS

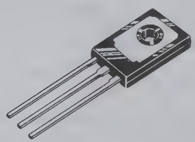
. . . designed for use in line-operated equipment requiring high f_T.

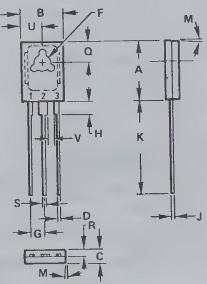
- High DC Current Gain — h_{FE} = 40–160 @ I_C = 20 mAdc
- Current-Gain—Bandwidth Product — f_T = 15 MHz (Min) @ I_C = 10 mAdc
- Low Output Capacitance — C_{ob} = 10 pF (Max) @ f = 1.0 MHz

0.3 AMPERE

POWER TRANSISTORS
NPN SILICON

250–350 VOLTS
15 WATTS





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

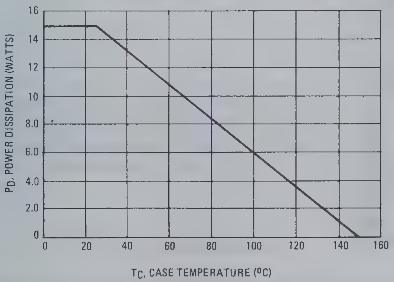
MAXIMUM RATINGS

Rating	Symbol	MJE3439	MJE3440	Unit
Collector-Emitter Voltage	V_{CEO}	350	250	Vdc
Collector-Base Voltage	V_{CB}	450	350	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	0.3		Adc
Base Current	I_B	150		mAdc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.33	°C/W

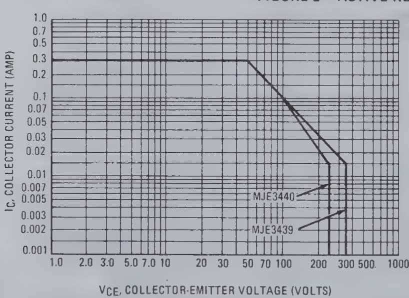
FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 5.0 mAdc, I_B = 0)	MJE3439		350	–	
(I_C = 50 mAdc, I_B = 0)	MJE3440		250	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 300 Vdc, I_B = 0)	MJE3439		–	20	
(V_{CE} = 200 Vdc, I_B = 0)	MJE3440		–	50	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 450 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	MJE3439		–	500	
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	MJE3440		–	500	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 350 Vdc, I_E = 0)	MJE3439		–	20	
(V_{CB} = 250 Vdc, I_E = 0)	MJE3440		–	20	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	20	μAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 2.0 mAdc, V_{CE} = 10 Vdc)			30	–	
(I_C = 20 mAdc, V_{CE} = 10 Vdc)			50	200	
Collector-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)		$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)		$V_{BE(sat)}$	–	1.3	Vdc
Base-Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	0.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 5.0 MHz)		f_T	15	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	10	pF
Small-Signal Current Gain (I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

FIGURE 2 — ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

MOTOROLA

NPN MJE4340 MJE4341 MJE4342 MJE4343
PNP MJE4350 MJE4351 MJE4352 MJE4353

HIGH-VOLTAGE — HIGH POWER TRANSISTORS

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

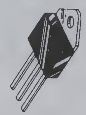
- High Collector-Emitter Sustaining Voltage —

		NPN	PNP
$V_{CEO(sus)}$	= 100 Vdc —	MJE4340	MJE4350
	= 120 Vdc —	MJE4341	MJE4351
	= 140 Vdc —	MJE4342	MJE4352
	= 160 Vdc —	MJE4343	MJE4353

- High DC Current Gain — @ I_C = 8.0 Adc
  h_{FE} = 35 (Typ)
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 8.0 Adc

16 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

100-160 VOLTS



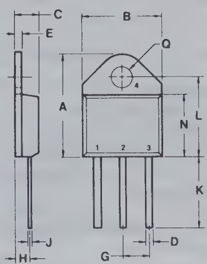
MAXIMUM RATINGS

Rating	Symbol	MJE4340 MJE4350	MJE4341 MJE4351	MJE4342 MJE4352	MJE4343 MJE4353	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	160	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	160	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →				Vdc
Collector Current — Continuous Peak (1)	I_C	← 16 → ← 20 →				Adc
Base Current — Continous	I_B	← 5.0 →				Adc
Total Device Dissipation @ T_C = 25°C	P_D	← 125 →				Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%

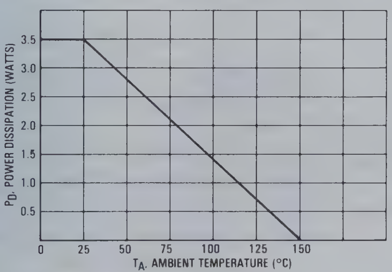


STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

FIGURE 1 — POWER DERATING
REFERENCE: AMBIENT TEMPERATURE



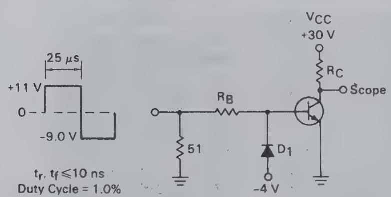
1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	MJE4340, MJE4350		100	—	
	MJE4341, MJE4351		120	—	
	MJE4342, MJE4352		140	—	
	MJE4343, MJE4353		160	—	
Collector-Emitter Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	MJE4340, MJE4350		—	750	
(V_{CE} = 60 Vdc, I_B = 0)	MJE4341, MJE4351		—	750	
(V_{CE} = 70 Vdc, I_B = 0)	MJE4342, MJE4352		—	750	
(V_{CE} = 80 Vdc, I_B = 0)	MJE4343, MJE4353		—	750	
Collector-Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)			—	1.0	
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			—	5.0	
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	750	μAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)			15	35 (Typ)	
(I_C = 16 Adc, V_{CE} = 4.0 Vdc)			8.0	15 (Typ)	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 8.0 Adc, I_B = 800 mA)			—	2.0	
(I_C = 16 Adc, I_B = 2.0 Adc)			—	3.5	
Base-Emitter Saturation Voltage (I_C = 16 Adc, I_B = 2.0 Adc)		$V_{BE(sat)}$	—	3.9	Vdc
Base-Emitter On Voltage (I_C = 16 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	3.9	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	800	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT

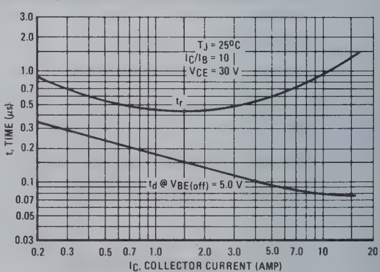


R_B and R_C varied to obtain desired current levels

D_1 must be fast recovery type, eg:
MBD5300 used above $I_B \approx$ 100 mA
MSD6100 used below $I_B \approx$ 100 mA

Note: Reverse polarities to test PNP devices.

FIGURE 3 — TYPICAL TURN-ON TIME



TYPICAL CHARACTERISTICS

FIGURE 4 — TURN-OFF TIME

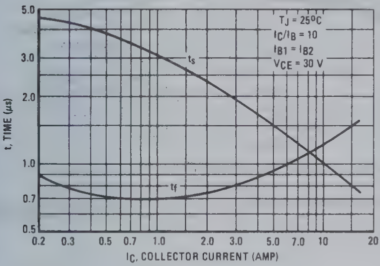
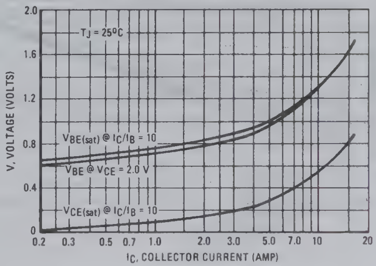


FIGURE 5 — ON VOLTAGES



DC CURRENT GAIN

FIGURE 6 — MJE4340 SERIES (NPN)

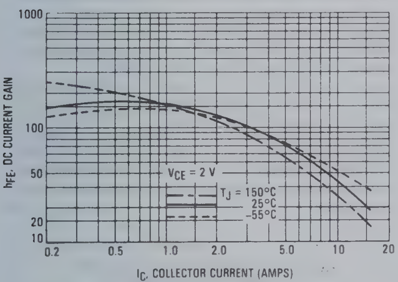


FIGURE 7 — MJE4350 SERIES (PNP)

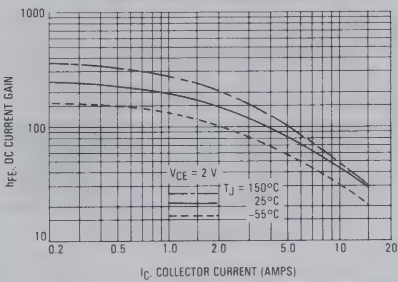
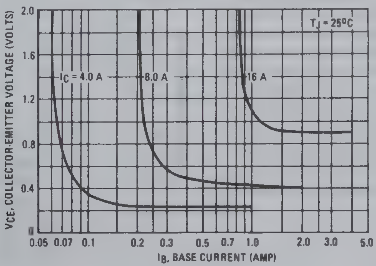


FIGURE 8 — COLLECTOR SATURATION REGION



1.3

FIGURE 9 — THERMAL RESPONSE

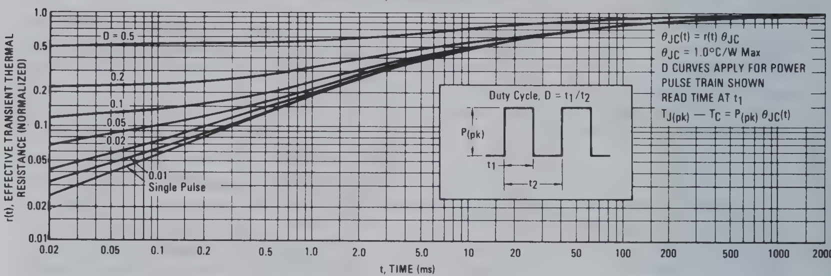
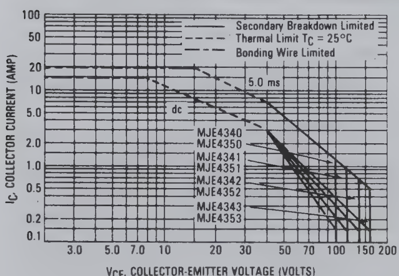


FIGURE 10 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



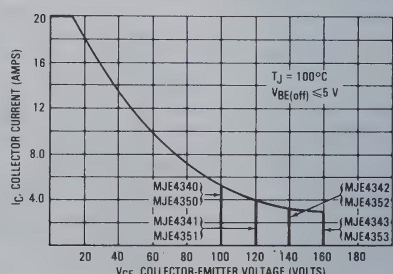
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 11 gives RBSOA characteristics.

FIGURE 11 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



MOTOROLA

NPN | PNP
MJE5180 MJE5170
MJE5181 MJE5171
MJE5182 MJE5172

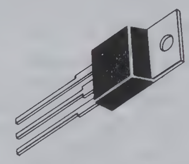
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTOR

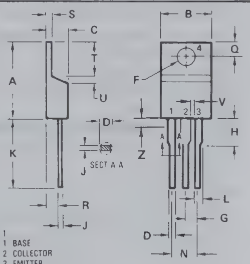
. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage — $V_{CEO(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 120 Vdc (Min) — MJE5170, MJE5180
  = 140 Vdc (Min) — MJE5171, MJE5181
  = 160 Vdc (Min) — MJE5172, MJE5182
- Compact TO-220 AB Package
- TO-66 Leadform Also Availability

6.0 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON

120, 140, 160 VOLTS
65 WATTS





STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3
3 DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4 DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
5. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
(TO-220AB)

MAXIMUM RATINGS

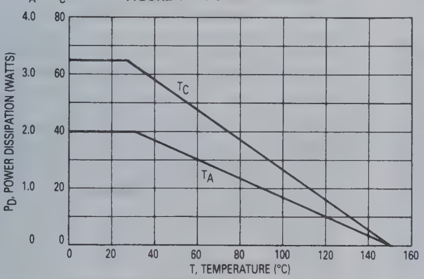
Rating	Symbol	MJE5180 MJE5170	MJE5181 MJE5171	MJE5182 MJE5172	Unit
Collector-Emitter Voltage	V_{CEO}	120	140	160	Vdc
Collector-Base Voltage	V_{CB}	120	140	160	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 6 → ← 10 →			Adc
Base Current	I_B	← 2.0 →			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 65 → ← 0.52 →			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 0.016 →			Watts W/°C
Unclamped Inductive Load Energy (1)	E	← 62.5 →			mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +150 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 2.8 A, L = 50 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω.

FIGURE 1 — POWER DERATING

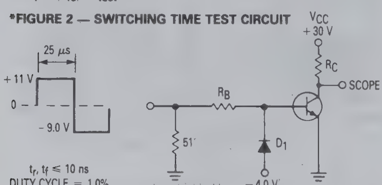


ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	MJE5170, MJE5180 MJE5171, MJE5181 MJE5172, MJE5182	$V_{CEO(sus)}$	120 140 160	— — —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 70 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	MJE5170, MJE5180 MJE5171, MJE5181 MJE5172, MJE5182	I_{CEO}	— — —	0.7 0.7 0.7	mAdc
Collector Cutoff Current (V_{CE} = 120 Vdc, V_{EB} = 0) (V_{CE} = 140 Vdc, V_{EB} = 0) (V_{CE} = 160 Vdc, V_{EB} = 0)	MJE5170, MJE5180 MJE5171, MJE5181 MJE5172, MJE5182	I_{CES}	— — —	400 400 400	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	30 15	— 100	—
Collector-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 600 mAdc)		$V_{CE(sat)}$	—	1.5	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	1.0	—	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		$\|h_{fe}\|$	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$

*FIGURE 2 — SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

*FOR PNP'S REVERSE ALL POLARITIES

FIGURE 3 — TURN-ON SWITCHING TIMES

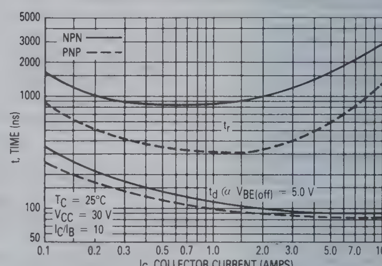


FIGURE 4 — TURN-OFF SWITCHING TIMES

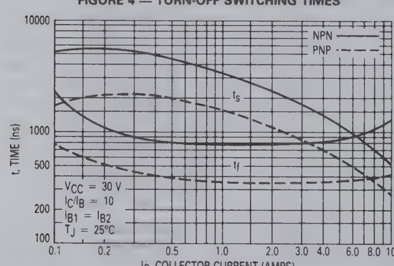
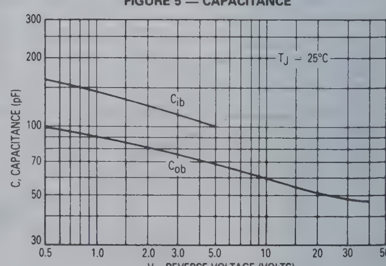


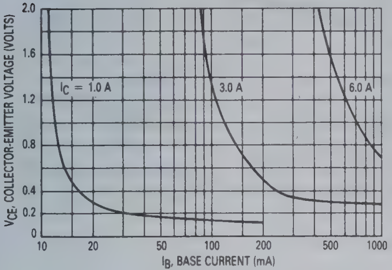
FIGURE 5 — CAPACITANCE



TYPICAL ELECTRICAL CHARACTERISTICS

NPN — MJE5180, MJE5181, MJE5182

FIGURE 10 — COLLECTOR SATURATION REGION



PNP — MJE5170, MJE5171, MJE5172

FIGURE 11 — COLLECTOR SATURATION REGION

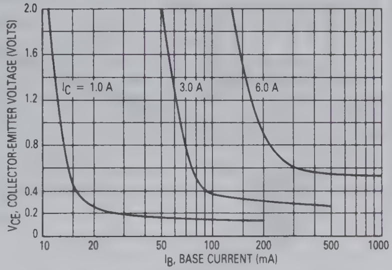


FIGURE 12 — COLLECTOR-EMITTER SATURATION REGION

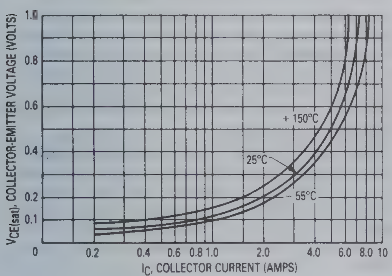


FIGURE 13 — COLLECTOR-EMITTER SATURATION REGION

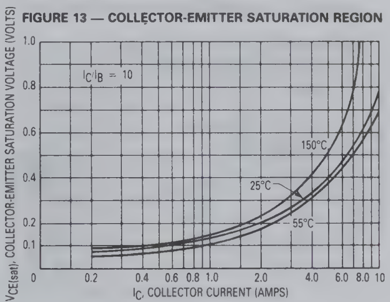


FIGURE 14 — BASE-EMITTER VOLTAGE

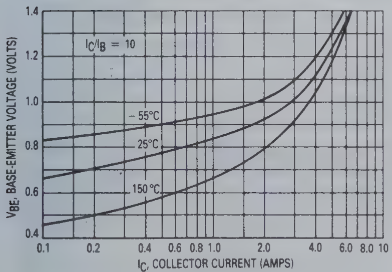


FIGURE 15 — BASE-EMITTER VOLTAGE

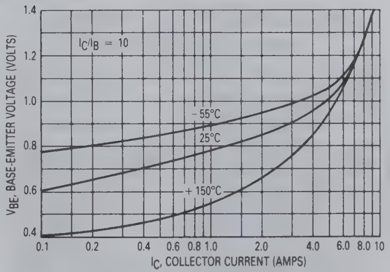


FIGURE 6 — THERMAL RESPONSE

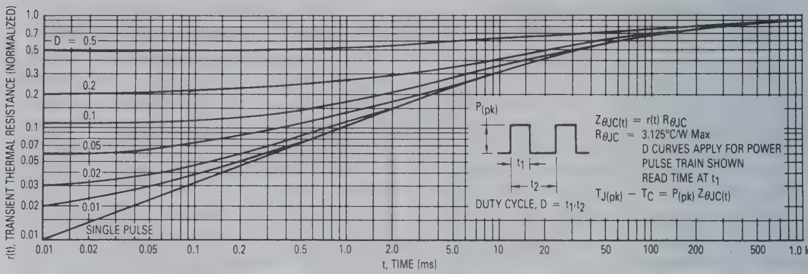
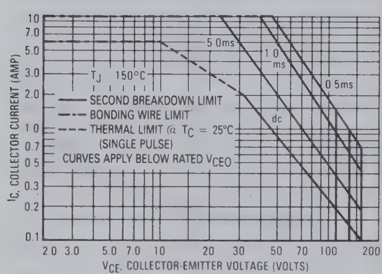


FIGURE 7 — ACTIVE-REGION SAFE OPERATING AREA



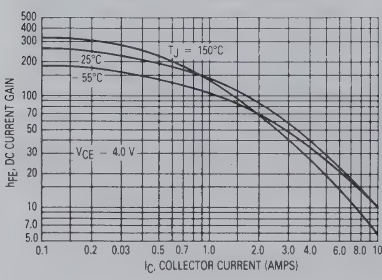
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL ELECTRICAL CHARACTERISTICS

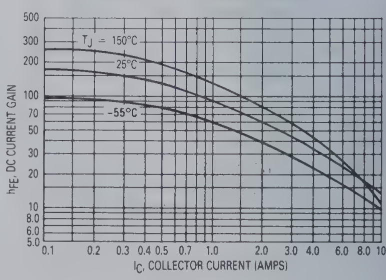
NPN — MJE5180, MJE5181, MJE5182

FIGURE 8 — DC CURRENT GAIN



PNP — MJE5170, MJE5171, MJE5172

FIGURE 9 — DC CURRENT GAIN



MJE5730
MJE5731
MJE5732

MOTOROLA

1.3

HIGH VOLTAGE PNP SILICON POWER TRANSISTORS

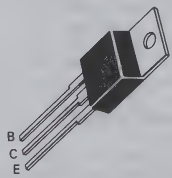
. . . designed for line operated audio output amplifier, SWITCHMODE power supply drivers and other switching applications.

- 300 V to 400 V (Min) — $V_{CEO(sus)}$
- 1.0 A Rated Collector Current
- Popular TO-220 Plastic Package
- TO-66 Leadform Available
- PNP Complements to the TIP47 thru TIP50 Series

1.0 AMPERE

POWER TRANSISTORS
PNP SILICON

300-350-400 VOLTS
40 WATTS

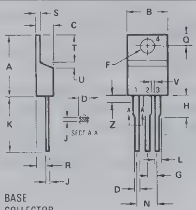


MAXIMUM RATINGS

Rating	Symbol	MJE5730	MJE5731	MJE5732	Unit
Collector-Emitter Voltage	V_{CEO}	300	350	400	Vdc
Collector-Base Voltage	V_{CB}	300	350	400	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 1.0 → ← 3.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	← 40 → ← 0.32 →			Watts W/°C
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	← 2.0 → ← 0.016 →			Watts W/°C
Unclamped Inducting Load Energy (See Figure 10)	E	← 20 →			mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +150 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W



STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3
3 DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4. DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
5 CONTROLLING DIMENSION INCH

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	MJE5730	$V_{CEO(sus)}$	300	—	Vdc
	MJE5731		350	—	
	MJE5732		400	—	
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	MJE5730	I_{CEO}	—	1.0	mAdc
(V_{CE} = 250 Vdc, I_B = 0)	MJE5731		—	1.0	
(V_{CE} = 300 Vdc, I_B = 0)	MJE5732		—	1.0	
Collector Cutoff Current (V_{CE} = 300 Vdc, V_{BE} = 0)	MJE5730	I_{CES}	—	1.0	mAdc
(V_{CE} = 350 Vdc, V_{BE} = 0)	MJE5731		—	1.0	
(V_{CE} = 400 Vdc, V_{BE} = 0)	MJE5732		—	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc)		h_{FE}	30	150	—
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)			10	—	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	—	1.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)		f_T	10	—	MHz
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

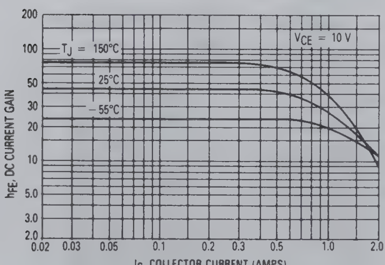


FIGURE 2 — COLLECTOR-EMITTER SATURATION VOLTAGE

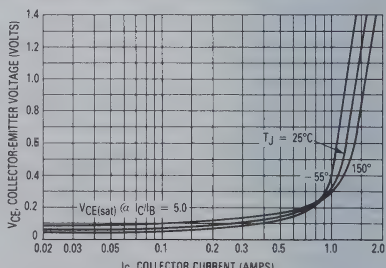


FIGURE 3 — BASE-EMITTER VOLTAGE

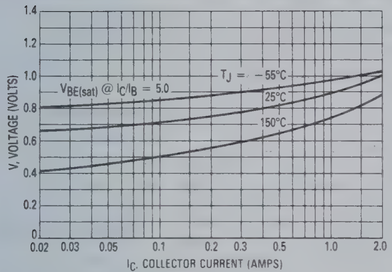


FIGURE 4 — NORMALIZED POWER DERATING

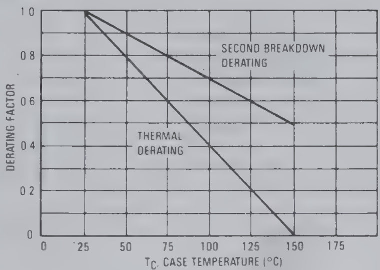
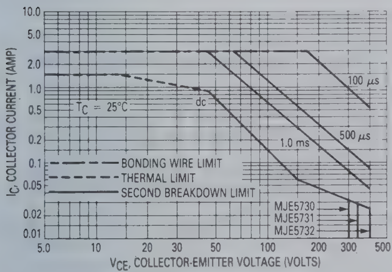


FIGURE 5 — FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — THERMAL RESPONSE

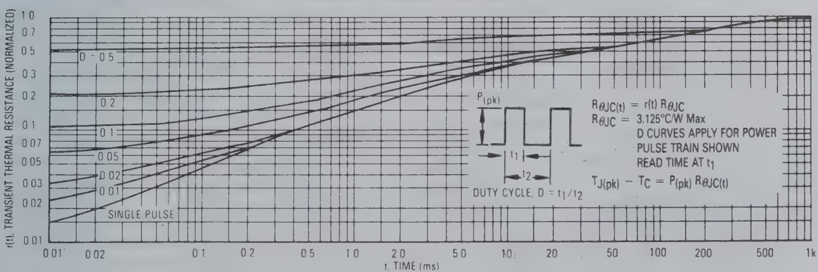


FIGURE 7 — SWITCHING TIME EQUIVALENT CIRCUIT

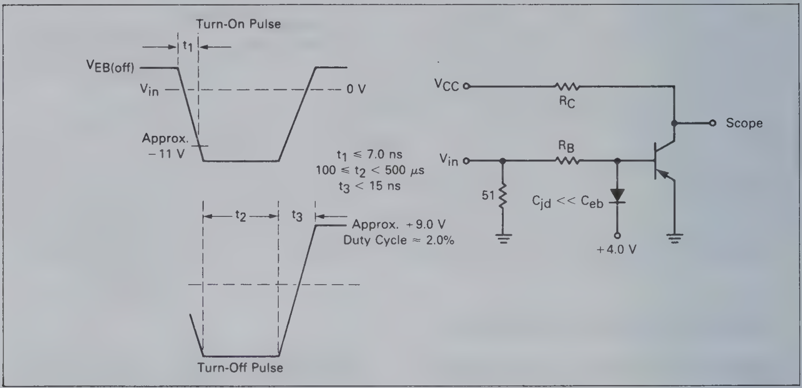


FIGURE 8 — TURN-ON RESISTIVE SWITCHING TIMES

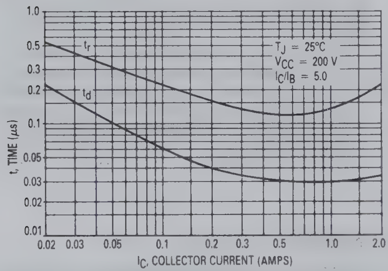


FIGURE 9 — RESISTIVE TURN-OFF SWITCHING TIMES

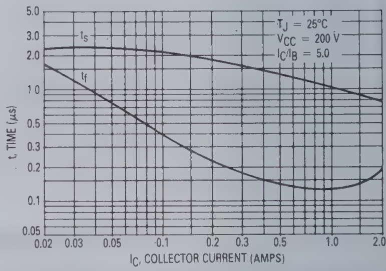
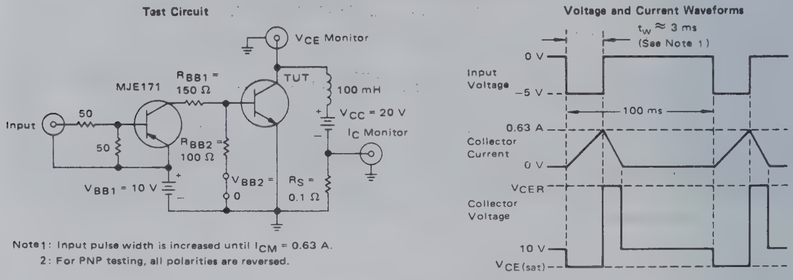


FIGURE 10 — INDUCTIVE LOAD SWITCHING



Note 1: Input pulse width is increased until I_{CM} = 0.63 A.
2: For PNP testing, all polarities are reversed.

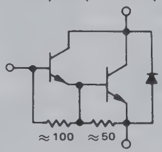
MOTOROLA

MJE5740
MJE5741
MJE5742

NPN SILICON POWER DARLINGTON TRANSISTORS

The MJE5740, 41, 42 darlington transistors are designed for high-voltage power switching in inductive circuits. They are particularly suited for operation in applications such as:

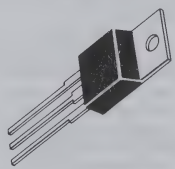
- Small Engine Ignition
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls



8 AMPERE

NPN SILICON POWER DARLINGTON TRANSISTORS

300, 350, 400 VOLTS
80 WATTS



MAXIMUM RATINGS

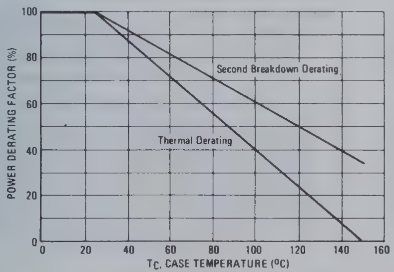
Rating	Symbol	MJE5740	MJE5741	MJE5742	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	800	Vdc
Emitter Base Voltage	V_{EB}	← 8 →			Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	← 8 → ← 16 →			Adc
Base Current—Continuous —Peak (1)	I_B I_{BM}	← 2.5 → ← 5 →			Adc
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	← 2 → ← 16 →			Watts mW/°C
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	← 80 → ← 640 →			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +150 →			°C

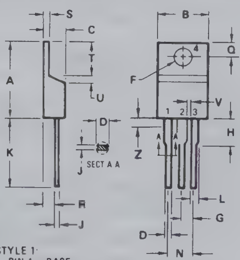
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ⩽ 10%.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mA, I_B = 0) MJE5740	$V_{CEO(sus)}$	300	–	–	Vdc
MJE5741		350	–	–	
MJE5742		400	–	–	
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	5	
Emitter Cutoff Current (V_{EB} = 8 Vdc, I_C = 0)	I_{EBO}	–	–	75	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 6			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 7			
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				–
(I_C = 0.5 Adc, V_{CE} = 5 Vdc)		50	100	–	
(I_C = 4 Adc, V_{CE} = 5 Vdc)		200	400	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 4 Adc, I_B = 0.2 Adc)		–	–	2	
(I_C = 8 Adc, I_B = 0.4 Adc)		–	–	3	
(I_C = 4 Adc, I_B = 0.2 Adc, T_C = 100°C)		–	–	2.2	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 4 Adc, I_B = 0.2 Adc)		–	–	2.5	
(I_C = 8 Adc, I_B = 0.4 Adc)		–	–	3.5	
(I_C = 4 Adc, I_B = 0.2 Adc, T_C = 100°C)		–	–	2.4	
Diode Forward Voltage (2) (I_F = 5 Adc)	V_f	–	–	2.5	Vdc

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Typical Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, $I_{C(pk)}$ = 6A	t_d	–	0.04	–	μs
Rise Time	$I_{B1} = I_{B2}$ = 0.25A, t_p = 25 μs,	t_r	–	0.5	–	μs
Storage Time	Duty Cycle ≤ 1%)	t_s	–	8.0	–	μs
Fall Time		t_f	–	2.0	–	μs
Inductive Load, Clamped (Table 1)						
Voltage Storage Time	($I_{C(pk)}$ = 6A, $V_{CE(pk)}$ = 250 Vdc	t_{sv}	–	4.0	–	μs
Crossover Time	I_{B1} = 0.06 A, $V_{BE(off)}$ = 5 Vdc)	t_c	–	2.0	–	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

(2) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

FIGURE 2 – INDUCTIVE SWITCHING MEASUREMENTS

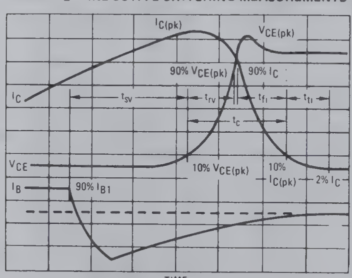
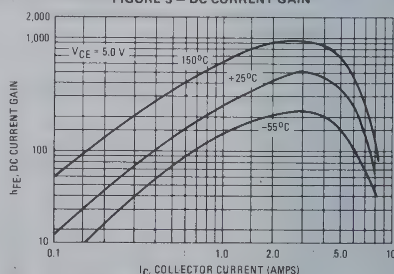
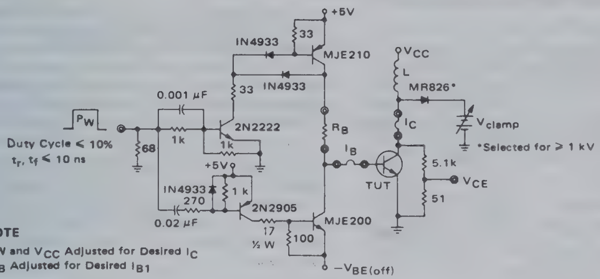
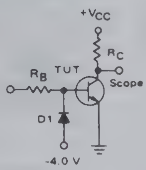
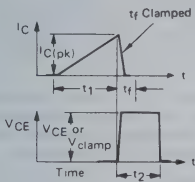
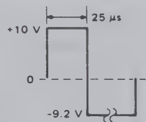


FIGURE 3 – DC CURRENT GAIN



1.3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 **NOTE** PW and V_{CC} Adjusted for Desired I_C; R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656, Full Bobbin (~16 Turns) #16; GAP for 200 μH/20A, L_{coil} = 200 μH; V_{CC} = 30 V, $V_{CE(pk)}$ = 250 Vdc, $I_{C(pk)}$ = 6A	V_{CC} = 250 V; D1 = 1N5820 or Equiv.
TEST WAVEFORMS	 **OUTPUT WAVEFORMS** t_1 Adjusted to Obtain I_C; $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$; $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$; Test Equipment Scope — Tektronix 475 or Equivalent	 t_r, t_f < 10 ns; Duty Cycle = 1.0%; R_B and R_C adjusted for desired I_B and I_C

TYPICAL CHARACTERISTICS

FIGURE 4 — BASE-EMITTER VOLTAGE

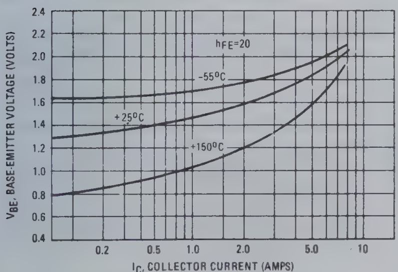
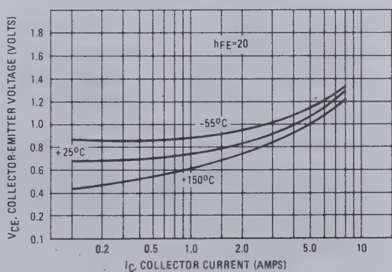


FIGURE 5 — COLLECTOR SATURATION VOLTAGE



1.3

The Safe Operating Area figures shown in Figures 6 and 7 are specified ratings for these devices under the test conditions shown.

FIGURE 6 – FORWARD BIAS SAFE OPERATING AREA

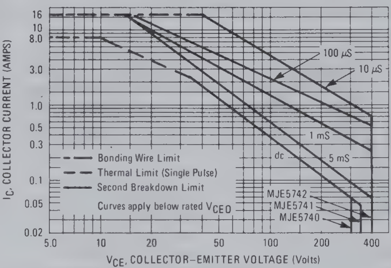
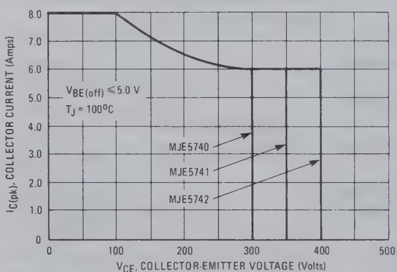


FIGURE 7 – REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 1 .

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives the complete RBSOA characteristics.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

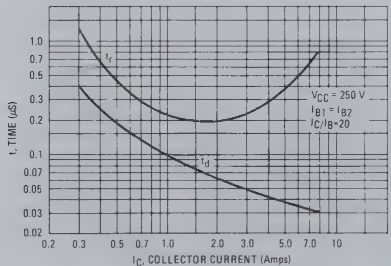
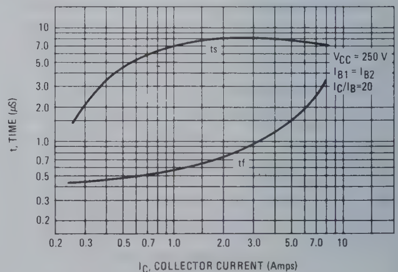


FIGURE 9 – TURN-OFF TIME



MJE5850
MJE5851
MJE5852

MOTOROLA

1.3

Designers Data Sheet

SWITCHMODE SERIES
PNP SILICON POWER TRANSISTORS

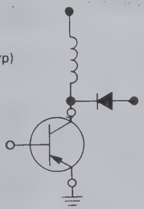
The MJE5850, MJE5851 and the MJE5852 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Delfection Circuits

Fast Turn-Off Times
  100 ns Inductive Fall Time @ 25°C (Typ)
  125 ns Inductive Crossover Time @ 25°C (Typ)

Operating Temperature Range -65 to +150°C

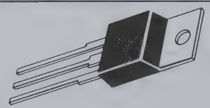
100°C Performance Specified for:
  Reversed Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents



8 AMPERE

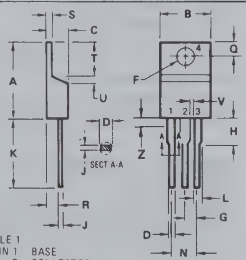
PNP SILICON POWER TRANSISTORS

300, 350, 400 VOLTS
80 WATTS



Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES
1. DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MJE 5850	MJE 5851	MJE 5852	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	350	400	450	Vdc
Emitter Base Voltage	V_{EB}		6.0		Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}		8.0 16		Adc
Base Current — Continuous Peak (1)	I_B I_{BM}		4.0 8.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		80 0.640		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE5850	$V_{CEO(sus)}$	300			Vdc
MJE5851		350	—	—	
MJE5852		400	—	—	
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.5	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 12		
Clamped Inductive SOA with base reverse biased	RBSOA		See Figure 13		
***ON CHARACTERISTICS**					
DC Current Gain	h_{FE}				—
(I_C = 2.0 Adc, V_{CE} = 5 Vdc)		15	—	—	
(I_C = 5.0 Adc, V_{CE} = 5 Vdc)		5	—	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 4.0 Adc, I_B = 1.0 Adc)		—	—	2.0	
(I_C = 8.0 Adc, I_B = 3.0 Adc)		—	—	5.0	
(I_C = 4.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		—	—	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 4.0 Adc, I_B = 1.0 Adc)		—	—	1.5	
(I_C = 4.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	270	—	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, t_p = 50 μs, Duty Cycle ≤ 2%)	t_d	—	0.025	0.1	μs
Rise Time	t_r	—	0.100	0.5	μs
Storage Time (V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%)	t_s	—	0.60	2.0	μs
Fall Time	t_f	—	0.11	0.5	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_{CM} = 4 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	0.8	3.0	μs
Crossover Time	t_c	—	0.4	1.5	μs
Fall Time	t_{fi}	—	0.1	—	μs
Storage Time (I_{CM} = 4 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	—	0.5	—	μs
Crossover Time	t_c	—	0.125	—	μs
Fall Time	t_{fi}	—	0.1	—	μs

* Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%

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TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

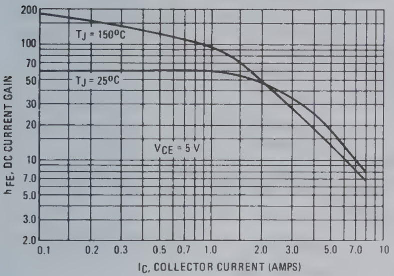

FIGURE 2 – COLLECTOR SATURATION REGION

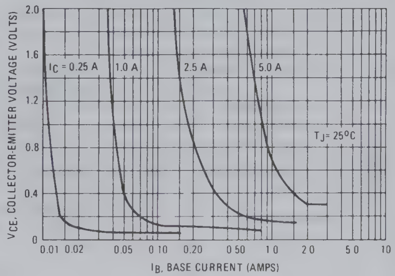

FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

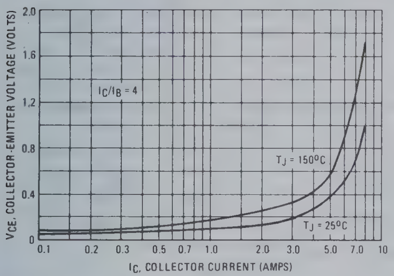

FIGURE 4 – BASE-EMITTER VOLTAGE

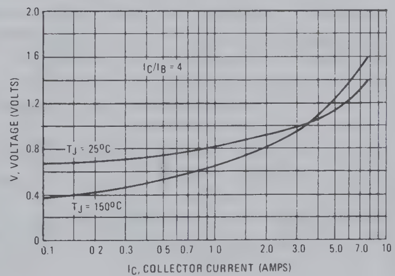

FIGURE 5 – COLLECTOR CUTOFF REGION

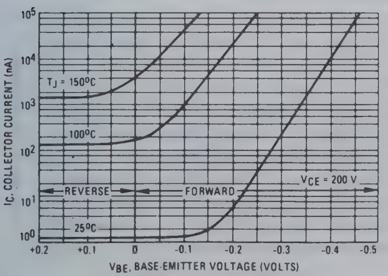

FIGURE 6 – CAPACITANCE

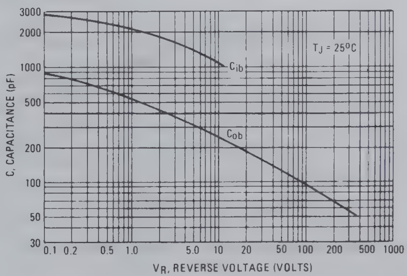

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TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

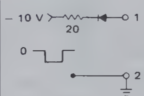
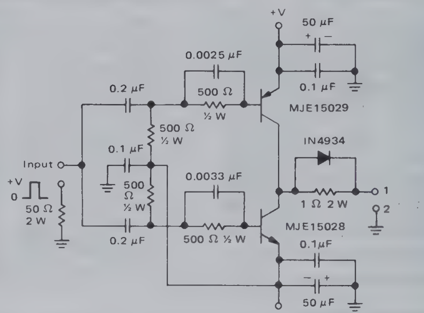
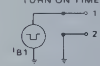
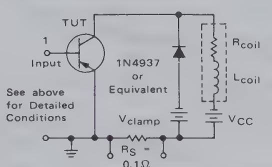
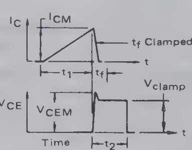
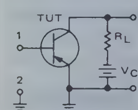
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 –V adjusted to obtain desired I_{B1} +V adjusted to obtain desired $V_{BE(off)}$	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain I_{B1}	V_{CC} = 250 V R_L = 62 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

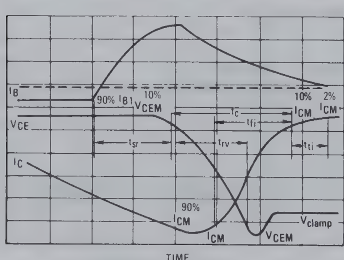
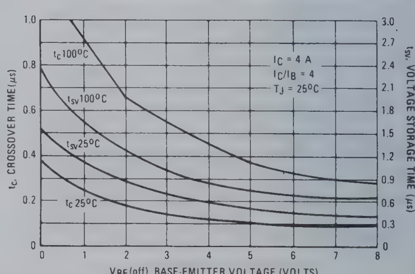


FIGURE 8 – INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user orinented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 9 – TURN-ON SWITCHING TIMES

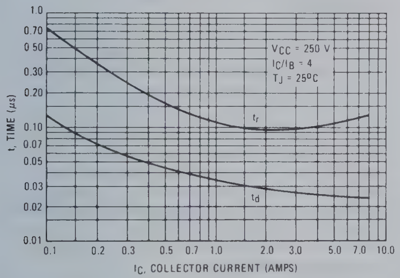


FIGURE 10 – TURN-OFF SWITCHING TIMES

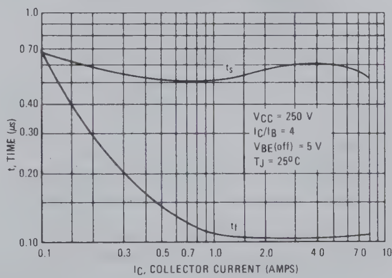
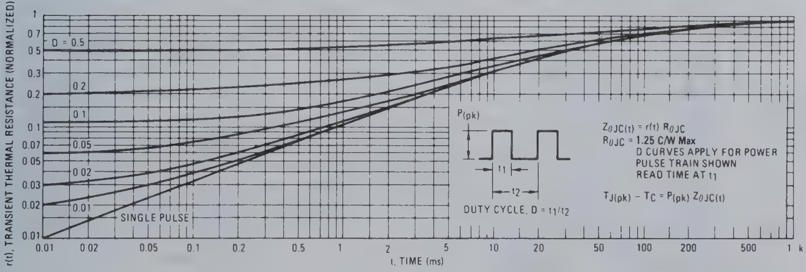


FIGURE 11 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]



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The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA

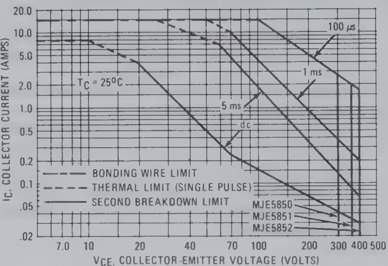
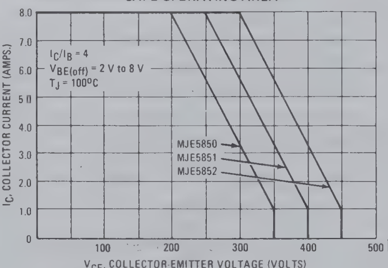


FIGURE 13 – RBSOA, MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

FIGURE 14 PEAK REVERSE BASE CURRENT

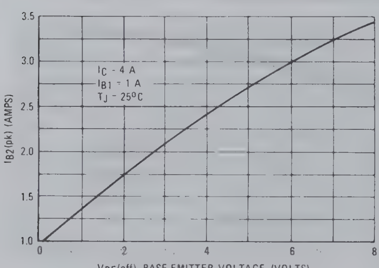
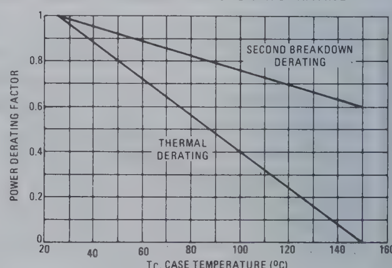


FIGURE 15 – FORWARD BIAS POWER DERATING



MJE8500
MJE8501

MOTOROLA

1.3

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE8500 and MJE8501 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
300 ns Inductive Fall Time — 25°C (Typ)
500 ns Inductive Crossover Time — 25°C (Typ)
900 ns Inductive Storage Time — 25°C (Typ)

Operating Temperature Range –65 to +125°C

100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

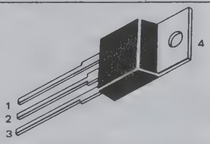
2.5 AMPERE

NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
65 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



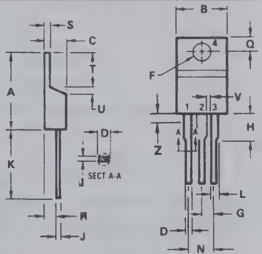
MAXIMUM RATINGS

Rating	Symbol	MJE8500	MJE8501	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	2.5 5.0	2.5 5.0	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	2.0 4.0	2.0 4.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	65 17 0.65	65 17 0.65	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +125		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.54	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

CASE 221A-02 TO-220

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJE8500	$V_{CEO(sus)}$	700	–	–	Vdc
	MJE8501		800	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	–	5.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	7.5	–	–	–
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 1.0 Adc, I_B = 0.33 Adc)			–	–	2.0	
(I_C = 2.5 Adc, I_B = 1.0 Adc)			–	–	5.0	
(I_C = 1.0 Adc, I_B = 0.33 Adc, T_C = 100°C)			–	–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 1.0 Adc, I_B = 0.33 Adc)			–	–	1.5	
(I_C = 1.0 Adc, I_B = 0.33 Adc, TC = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	50	–	250	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 500 Vdc, I_C = 1.0 A, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.045	0.20	μs
Rise Time		t_r	–	0.2	2.0	μs
Storage Time		t_s	–	1.0	4.0	μs
Fall Time		t_f	–	0.5	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 1.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	1.3	4.0	μs
Crossover Time		t_c	–	0.6	2.0	μs
Storage Time	(I_C = 1.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	0.9	–	μs
Crossover Time		t_c	–	0.5	–	μs
Fall Time		t_{fi}	–	0.3	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

1.3

FIGURE 1 — DC CURRENT GAIN

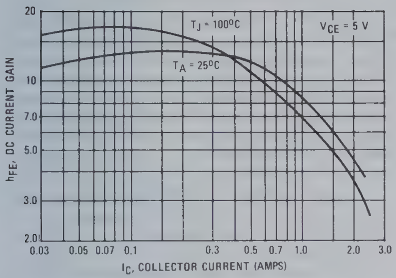


FIGURE 2 — COLLECTOR SATURATION REGION

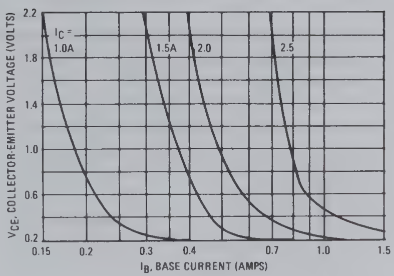


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

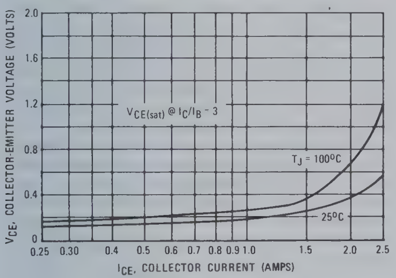


FIGURE 4 — BASE-EMITTER VOLTAGE

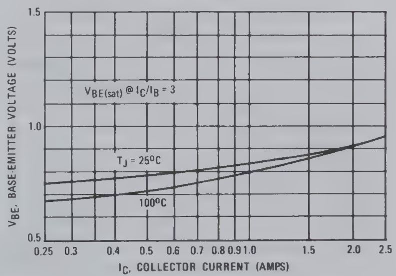


FIGURE 5 — COLLECTOR CUTOFF REGION

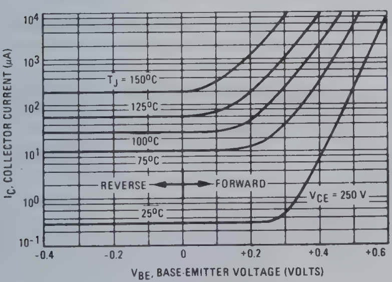


FIGURE 6 — CAPACITANCE

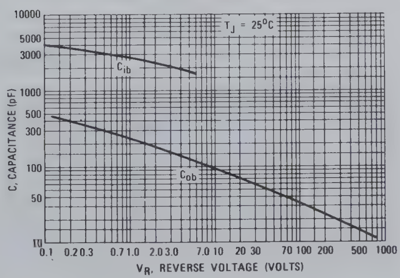


FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

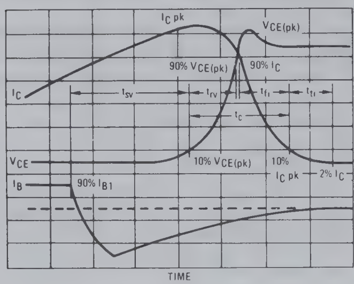
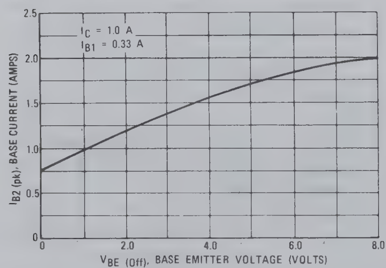


FIGURE 8 — PEAK REVERSE BASE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE\ (pk)}$
t_{rv} = Voltage Rise Time, 10–90% $V_{CE\ (pk)}$
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% $V_{CE\ (pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

TYPICAL RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 — TURN - ON SWITCHING TIMES

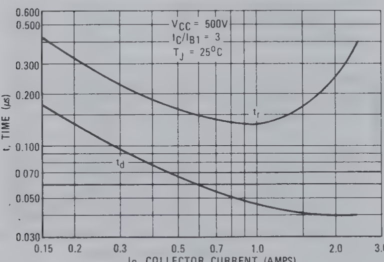


FIGURE 10 — TURN - OFF SWITCHING TIMES

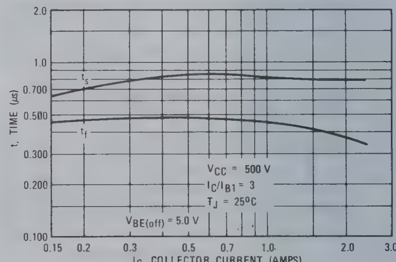


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

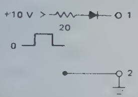
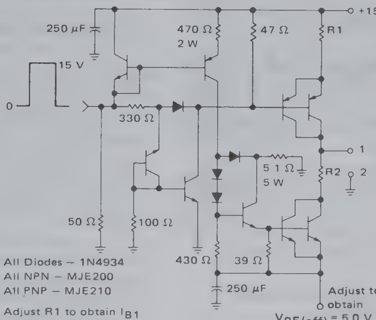
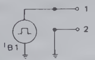
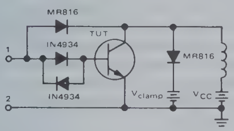
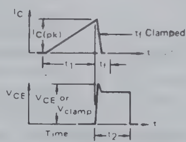
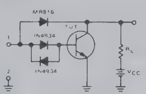
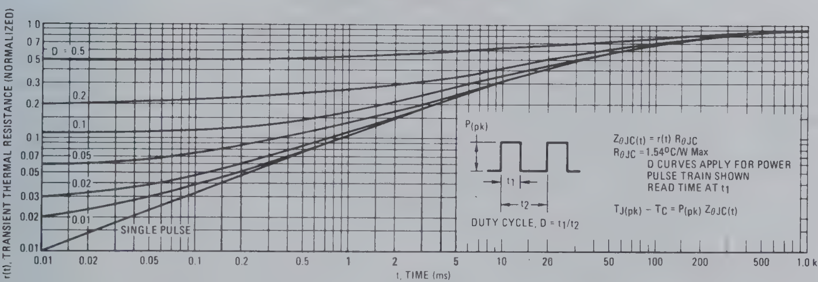
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞ Adjust to obtain $V_{BE(off)}$ = 5.0 V	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0 05 Ω V_{CC} = 20 V V_{clamp} = 500 V	V_{CC} = 500 V R_L = 500 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 11 – THERMAL RESPONSE



1.3

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

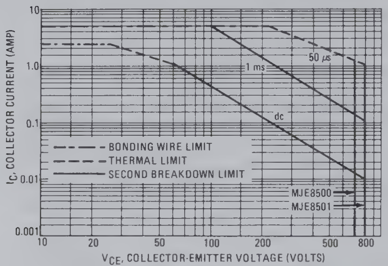
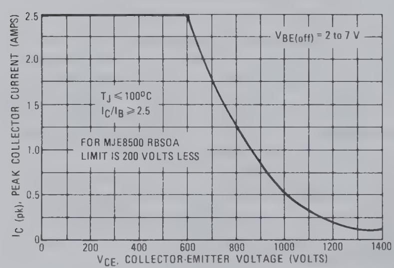


FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

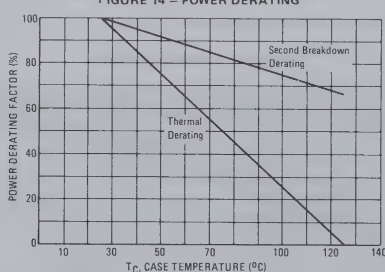
The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 — POWER DERATING



MOTOROLA

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE8502 and MJE8503 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 150 ns Inductive Fall Time—25°C (Typ)
- 400 ns Inductive Crossover Time—25°C (Typ)
- 1200 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range −65 to +125°C

100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

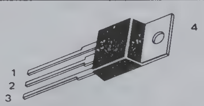
5.0 AMPERE

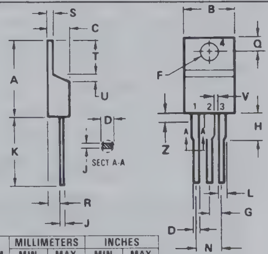
NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
80 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-02 TO-220

MAXIMUM RATINGS

Rating	Symbol	MJE8502	MJE8503	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	5.0 10	5.0 10	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	4.0 8.0	4.0 8.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	80 21 0.80	80 21 0.80	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +125		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJE8502 MJE8503	$V_{CEO(sus)}$	700 800		–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	– –	– –	0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	7.5		–	–
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 2.0 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	– – –	– – –	2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{BE(sat)}$	– –	– –	1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	60		300	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 500 Adc, IC = 2.5 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.040	0.20	μs
Rise Time		t_r	–	0.125	2.0	μs
Storage Time		t_s	–	1.2	4.0	μs
Fall Time		t_f		0.65	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 2.5 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, TC = 100°C)	t_{sv}	–	1.6	5.0	μs
Crossover Time		t_c	–	0.60	2.0	μs
Storage Time	(I_C = 2.5 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	1.2	–	μs
Crossover Time		t_c	–	0.4	–	μs
Fall Time		t_{fi}	–	0.15	–	μs

(1) Pulse Test: PW · 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

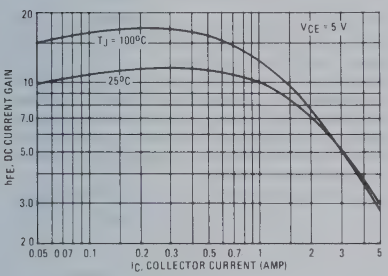


FIGURE 2 – COLLECTOR SATURATION REGION

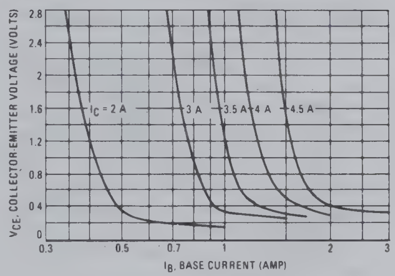


FIGURE 3 – COLLECTOR-EMITTER SATURATION REGION

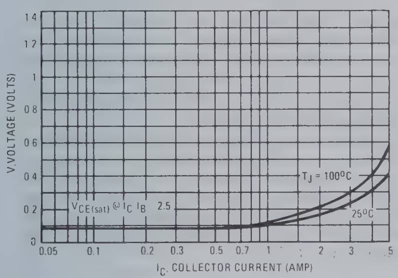


FIGURE 4 – BASE-EMITTER VOLTAGE

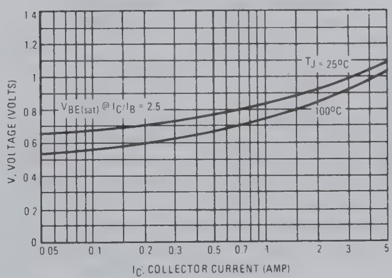


FIGURE 5 – COLLECTOR CUTOFF REGION

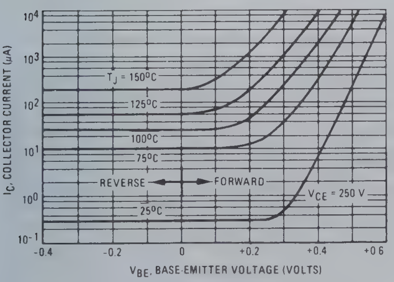


FIGURE 6 – CAPACITANCE

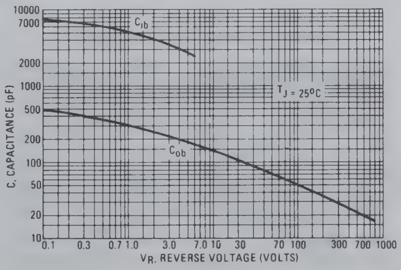


FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

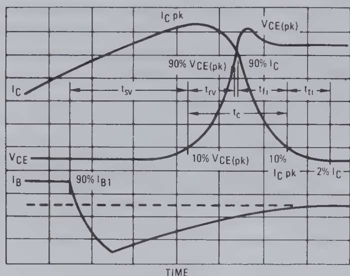
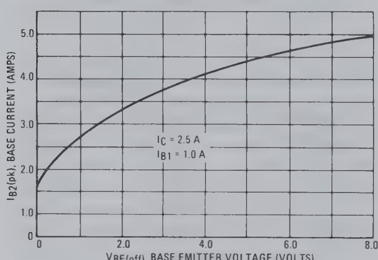


FIGURE 8 — PEAK REVERSE BASE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$
t_{rv} = Voltage Rise Time, 10–90% $V_{CE(pk)}$
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

TYPICAL RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 — TURN-ON SWITCHING TIMES

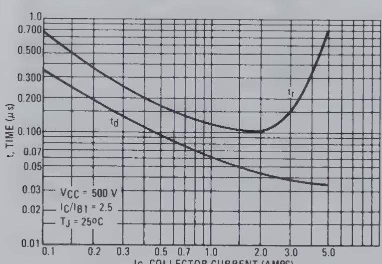


FIGURE 10 — TURN-OFF SWITCHING TIMES

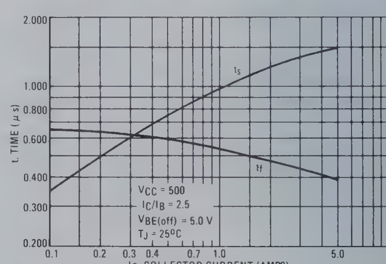


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

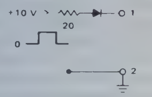
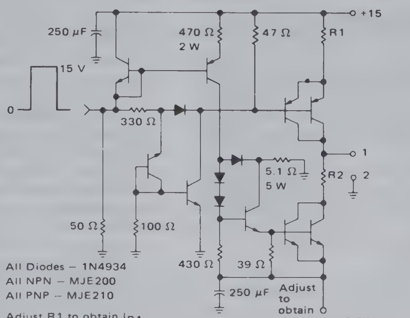
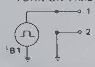
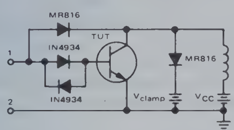
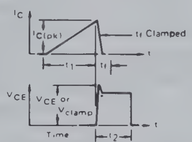
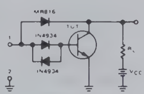
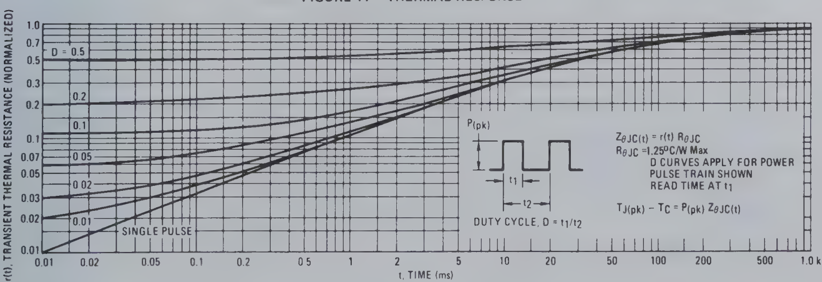
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} 180 µH R_{coil} 0.05 Ω V_{CC} 20 V V_{clamp} = 500 V	V_{CC} = 500 V R_L = 200 Ω Pulse Width = 10 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 11 – THERMAL RESPONSE



1.3

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

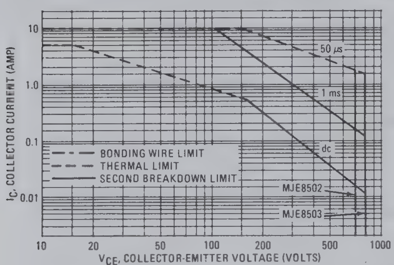
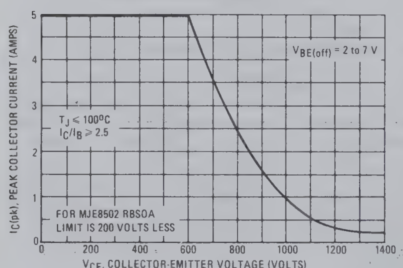


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

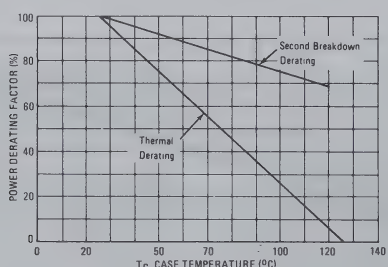
The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



MOTOROLA

HORIZONTAL DEFLECTION TRANSISTOR

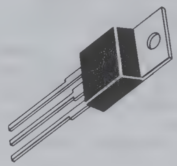
. . . specifically designed for use in small screen black and white deflection circuits.

- Collector-Emitter Voltage — V_{CEX} = 1500 Volts
- Glassivated Base-Collector Junction
- Switching Times with Inductive Loads — t_f = 0.65 μs (Typ) @ I_C = 2.0 A

2.5 AMPERE

NPN SILICON POWER TRANSISTOR

1500 VOLTS
65 WATTS

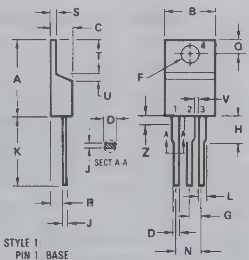


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous	I_C	2.5	Adc
Base Current — Continuous	I_B	2.0	Adc
Emitter Current — Continuous	I_E	4.5	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.65	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.54	°C/W

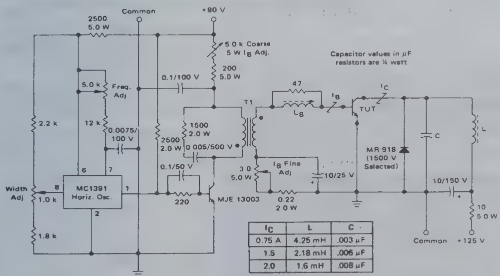


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

FIGURE 1 — TEST CIRCUIT



I_C	L	C
0.75 A	4.25 mH	.003 μF
1.5	2.18 mH	.006 μF
2.0	1.6 mH	.008 μF

DRIVER TRANSFORMER (T1)
Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance – 39 mH, Secondary Inductance – 22 mH, Leakage Inductance with primary shorted – 2.0 μH, Primary 260 turns #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.8 Adc)	$V_{CE(sat)}$	–	–	5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.8 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	50	–	pF
Current Gain – Bandwidth Product (1) (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	–	4.0	–	MHz
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 2.0 Adc, I_{B1} = 1.0 Adc, L_B = 12 μH)	t_f	–	0.65	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 2 – DC CURRENT GAIN

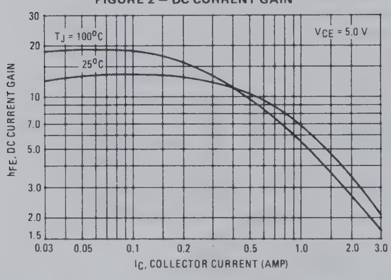


FIGURE 3 – "ON" VOLTAGE

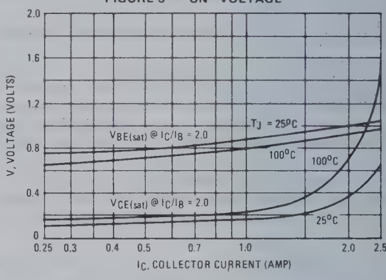
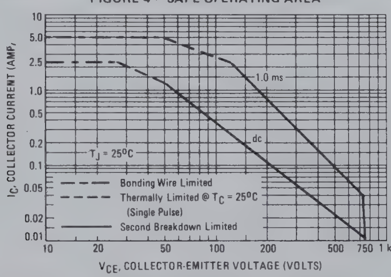


FIGURE 4 – SAFE OPERATING AREA



MJE13002
MJE13003

MOTOROLA

1.3

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

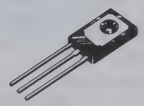
SPECIFICATION FEATURES:

- Reverse Biased SOA with Inductive Loads @ $T_C = 100^{\circ}C$
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and $100^{\circ}C$ . . . t_c @ 1 A, $100^{\circ}C$ is 290 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

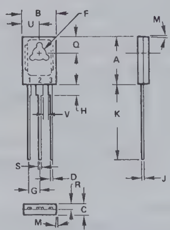
1.5 AMPERE

NPN SILICON
POWER TRANSISTORS

300 and 400 VOLTS
40 WATTS



CASE 77-04
TO-126



STYLE 3
PIN 1. BASE
2. COLLECTOR
3. EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

MAXIMUM RATINGS

Rating	Symbol	MJE13002	MJE13003	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	1.5 3		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	0.75 1.5		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	2.25 4.5		Adc
Total Power Dissipation @ $T_A = 25^{\circ}C$ Derate above $25^{\circ}C$	P_D	1.4 11.2		Watts $mW/^{\circ}C$
Total Power Dissipation @ $T_C = 25^{\circ}C$ Derate above $25^{\circ}C$	P_D	40 320		Watts $mW/^{\circ}C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		$^{\circ}C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	$^{\circ}C/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	89	$^{\circ}C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	$^{\circ}C$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13002 / MJE13003	$V_{CEO(sus)}$	300 / 400	– / –	– / –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 100^oC$)		–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 12			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 2 Vdc)	h_{FE}	8	–	40	–
(I_C = 1 Adc, V_{CE} = 2 Vdc)		5	–	25	
Collector-Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	–	–	0.5	Vdc
(I_C = 1 Adc, I_B = 0.25 Adc)		–	–	1	
(I_C = 1.5 Adc, I_B = 0.5 Adc)		–	–	3	
(I_C = 1 Adc, I_B = 0.25 Adc, $T_C = 100^oC$)		–	–	1	
Base-Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	–	–	1	Vdc
(I_C = 1 Adc, I_B = 0.25 Adc)		–	–	1.2	
(I_C = 1 Adc, I_B = 0.25 Adc, $T_C = 100^oC$)		–	–	1.1	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	10	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	21	–	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 125 Vdc, I_C = 1 A, $I_{B1} = I_{B2}$ = 0.2 A, t_p - 25 µs, Duty Cycle ≤ 1%)	t_d	–	0.05	0.1	µs
Rise Time	t_r	–	0.5	1	µs
Storage Time	t_s	–	2	4	µs
Fall Time	t_f	–	0.4	0.7	µs
Inductive Load, Clamped (Table 1, Figure 13)					
Storage Time (I_C = 1 A, V_{clamp} = 300 Vdc, I_{B1} = 0.2 A, $V_{BE(off)}$ = 5 Vdc, $T_C = 100^oC$)	t_{sv}	–	1.7	4	µs
Crossover Time	t_c	–	0.29	0.75	µs
Fall Time	t_{fi}	–	0.15	–	µs

(1) Pulse Test: PW = 300 µs, Duty Cycle ≤2%.

FIGURE 1 – DC CURRENT GAIN

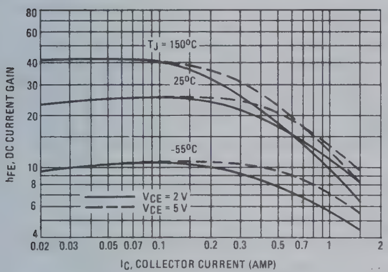


FIGURE 2 – COLLECTOR SATURATION REGION

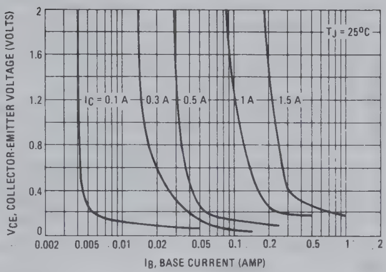


FIGURE 3 – BASE-EMITTER VOLTAGE

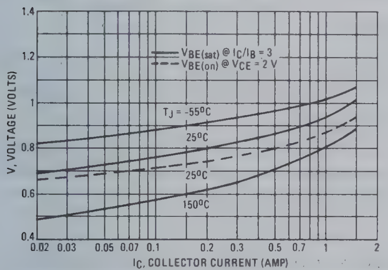


FIGURE 4 – COLLECTOR-EMITTER SATURATION REGION

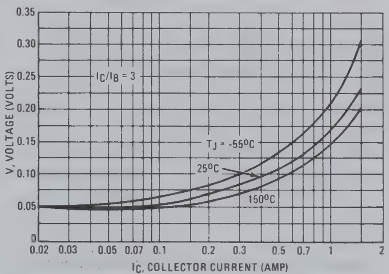


FIGURE 5 – COLLECTOR CUTOFF REGION

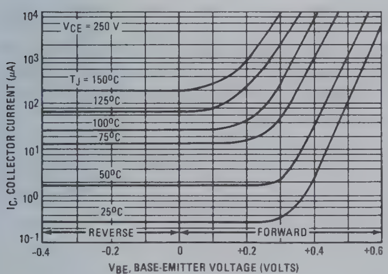
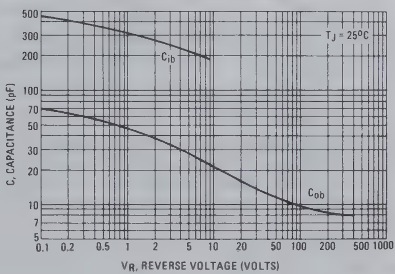


FIGURE 6 – CAPACITANCE

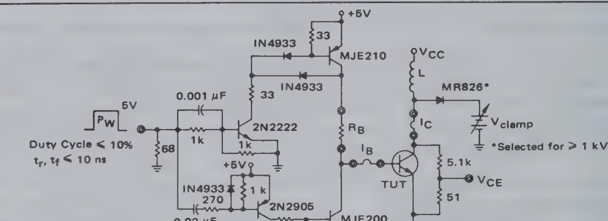


1.3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

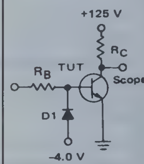
REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING

TEST CIRCUITS



NOTE
PW and V_{CC} Adjusted for Desired I_C
R_B Adjusted for Desired I_{B1}

RESISTIVE SWITCHING



CIRCUIT VALUES

Coil Data:
Ferroxcube Core #6656
Full Bobbin (~200 Turns) #20

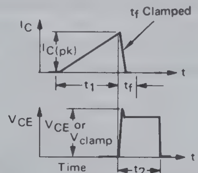
GAP for 30 mH/2A
L_{coil} = 50 mH

V_{CC} = 20 V
V_{clamp} = 300 Vdc

Resistive switching:
V_{CC} = 125 V
R_C = 125 Ω
D1 = 1N5820 or Equiv.
R_B = 47 Ω

TEST WAVEFORMS

OUTPUT WAVEFORMS

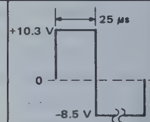


t_1 Adjusted to Obtain I_C

$$t_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$$

$$t_2 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{clamp}}$$

Test Equipment
Scope-Tektronics
475 or Equivalent



t_r, t_f < 10 ns
Duty Cycle = 1.0%
R_B and R_C adjusted for desired I_B and I_C

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

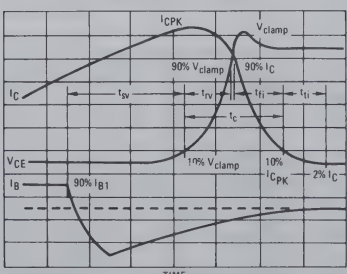


TABLE 2 — TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

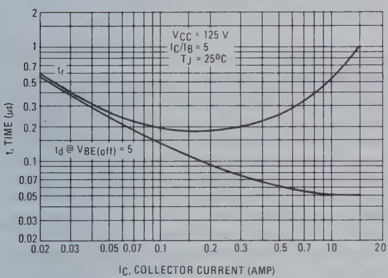


FIGURE 9 — TURN-OFF TIME

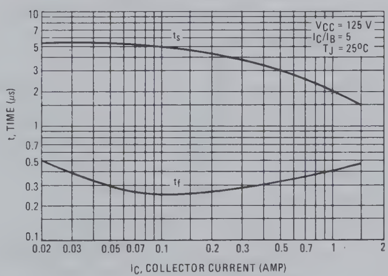
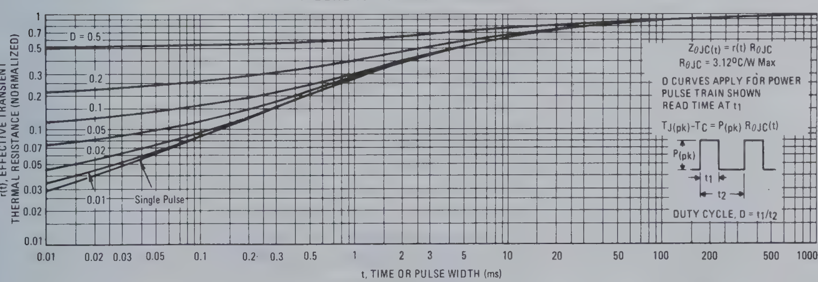


FIGURE 10 — THERMAL RESPONSE



1.3

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATION AREA

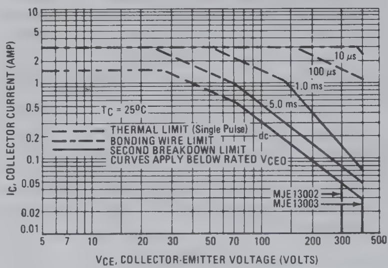
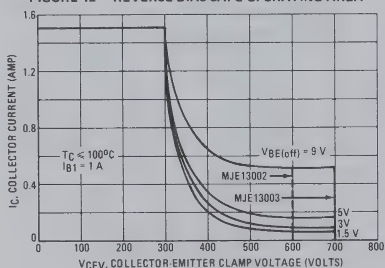


FIGURE 12 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

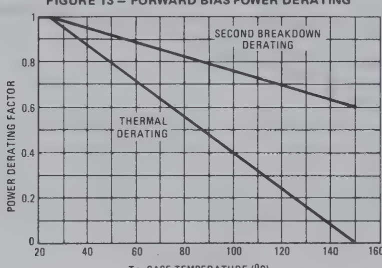
The data of Figure 11 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

FIGURE 13 — FORWARD BIAS POWER DERATING



MOTOROLA

MJE13004
MJE13005

1.3

Designer's Data Sheet

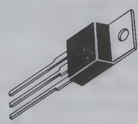
SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

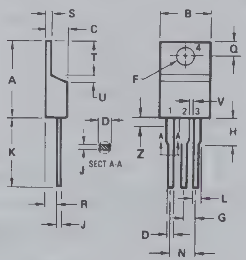
These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulator's, Inverters, Motor Controls, Solenoid / Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 2 to 4 Amp, 25 and 100°C
  . . . t_c @ 3A, 100°C is 180 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information.

4 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
75 WATTS





STYLE 1:
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MJE13004	MJE13005	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	4 8		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	6 12		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 600		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**						
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13004		$V_{CEO(sus)}$	300	–	–	Vdc
MJE13005			400	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	–	1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 100^oC$)			–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$		See Figure 11		
Clamped Inductive SOA with Base Reverse Biased		RBSOA		See Figure 12		
***ON CHARACTERISTICS**						
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)		h_{FE}	10	–	60	–
(I_C = 2 Adc, V_{CE} = 5 Vdc)			8	–	40	
Collector-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	–	–	0.5	Vdc
(I_C = 2 Adc, I_B = 0.5 Adc)			–	–	0.6	
(I_C = 4 Adc, I_B = 1 Adc)			–	–	1	
(I_C = 2 Adc, I_B = 0.5 Adc, $T_C = 100^oC$)			–	–	1	
Base-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)		$V_{BE(sat)}$	–	–	1.2	Vdc
(I_C = 2 Adc, I_B = 0.5 Adc)			–	–	1.6	
(I_C = 2 Adc, I_B = 0.5 Adc, $T_C = 100^oC$)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	–	–	MHz
Output Capacitance (V_{CB} - 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	65	–	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 2)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 2 A,	t_d	–	0.025	0.1	μs
Rise Time	$I_{B1} = I_{B2}$ = 0.4 A, t_p = 25 μs,	t_r	–	0.3	0.7	μs
Storage Time	Duty Cycle ≤ 1%)	t_s	–	1.7	4	μs
Fall Time		t_f	–	0.4	0.9	μs
Inductive Load, Clamped (Table 2, Figure 13)						
Voltage Storage Time	(I_C = 2 A, V_{clamp} = 300 Vdc,	t_{sv}	–	0.9	4	μs
Crossover Time	I_{B1} = 0.4 A, $V_{BE(off)}$ = 5 Vdc, $T_C = 100^oC$)	t_c	–	0.32	0.9	μs
Fall Time		t_{fi}	–	0.16	–	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 — DC CURRENT GAIN

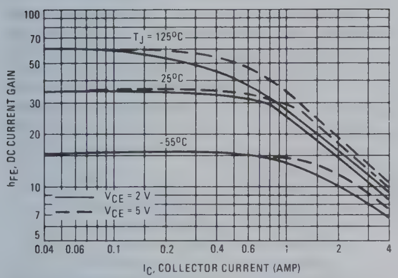


FIGURE 2 — COLLECTOR SATURATION REGION

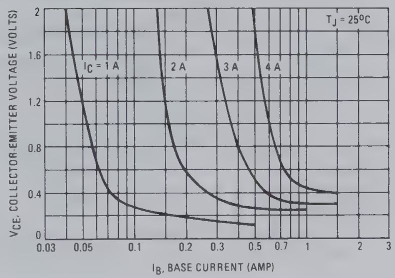


FIGURE 3 — BASE-EMITTER VOLTAGE

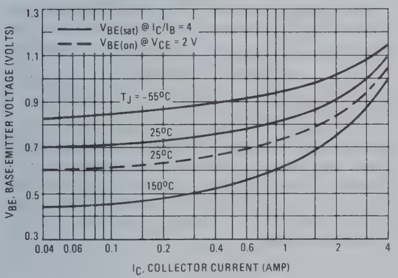


FIGURE 4 — COLLECTOR–EMITTER SATURATION VOLTAGE

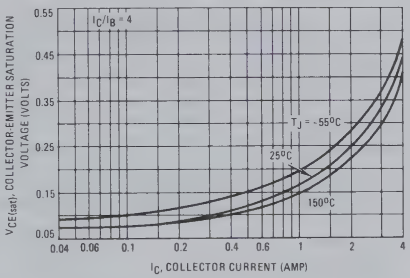


FIGURE 5 — COLLECTOR CUTOFF REGION

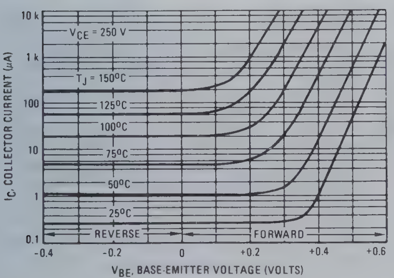
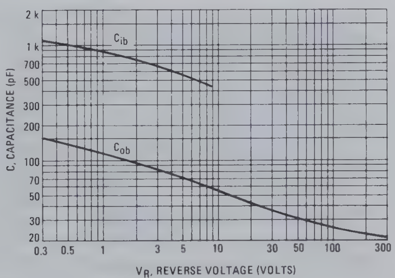
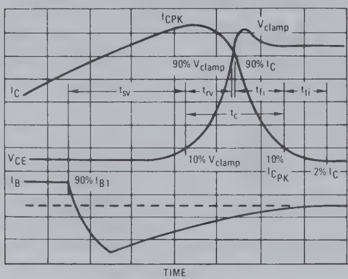


FIGURE 6 — CAPACITANCE



1.3

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

TABLE 1 — TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
2	25	600	70	100	80	180
	100	900	110	240	130	320
3	25	650	60	140	60	200
	100	950	100	330	100	350
4	25	550	70	160	100	220
	100	850	110	350	160	390

NOTE: All Data recorded in the inductive Switching Circuit in Table 2.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

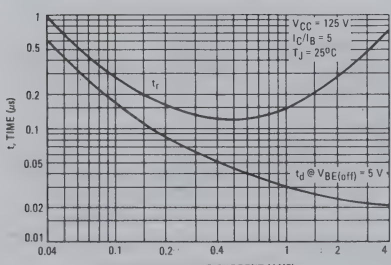


FIGURE 9 — TURN-OFF TIME

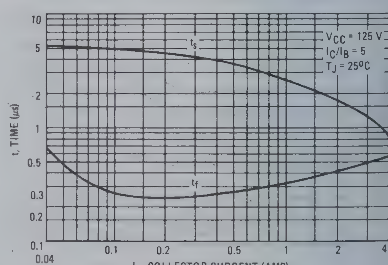
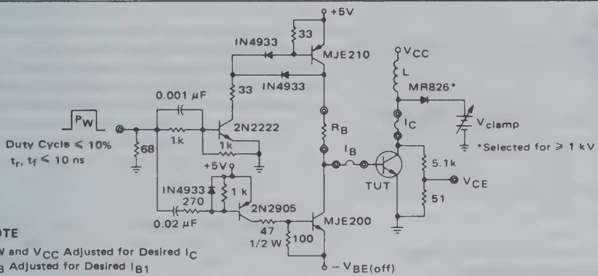


TABLE 2 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING

TEST CIRCUITS



NOTE
PW and V_{CC} Adjusted for Desired I_C
R_B Adjusted for Desired I_{B1}

CIRCUIT VALUES

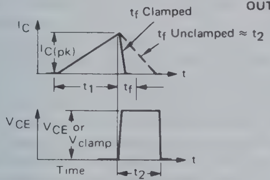
Coil Data:
Ferroxcube Core #6656
Full Bobbin (~16 Turns) #16

GAP for 200 μH/20A
L_{coil} = 200 μH

V_{CC} = 20 V
V_{clamp} = 300 Vdc

TEST WAVEFORMS

OUTPUT WAVEFORMS



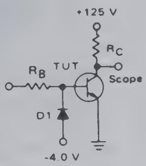
t_1 Adjusted to Obtain I_C

$$t_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$$

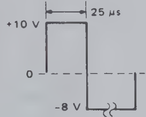
$$t_2 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{clamp}}$$

Test Equipment
Scope — Tektronix
475 or Equivalent

RESISTIVE SWITCHING

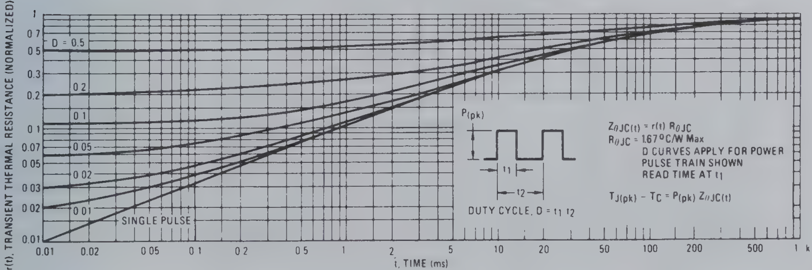


V_{CC} = 125 V
R_C = 62 Ω
D1 = 1N5820 or Equiv
R_B = 22 Ω



t_r, t_f < 10 ns
Duty Cycle = 1.0%
R_B and R_C adjusted for desired I_B and I_C

FIGURE 10 — TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]



1.3

The Safe Operating Area Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

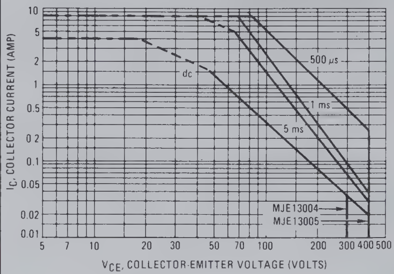
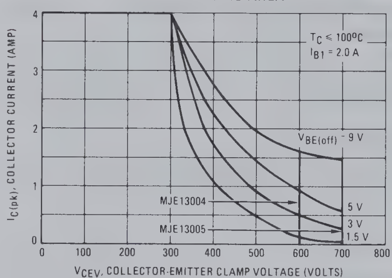


FIGURE 12– REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

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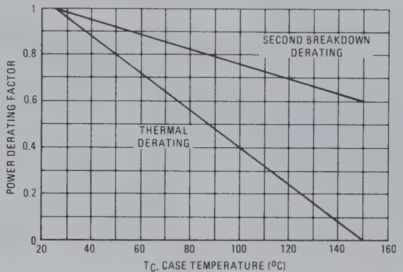
$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.

FIGURE 13 – FORWARD BIAS POWER DERATING



MJE13006
MJE13007

MOTOROLA

1.3

Designer's Data Sheet

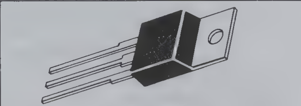
SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE13006 and MJE13007 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ $T_C = 100^oC$
- Inductive Switching Matrix 3 to 8 Amp, 25 and 100°C ... t_c @ 5A, 100°C is 136 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

8 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
80 WATTS



Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

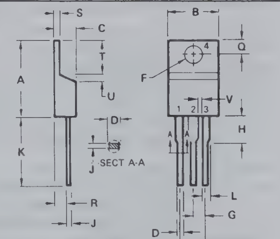
MAXIMUM RATINGS

Rating	Symbol	MJE13006	MJE13007	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8 16		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4 8		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 24		Adc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25°C	P_D	80 640		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES
1. DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13006	$V_{CEO(sus)}$	300	–	–	Vdc
MJE13007		400	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 100^oC$)		–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased	–	See Figure 2			
***ON CHARACTERISTICS**					
DC Current Gain (I_C = 2 Adc, V_{CE} = 5 Vdc)	h_{FE}	8	–	60	–
(I_C = 5 Adc, V_{CE} = 5 Vdc)		5	–	30	
Collector-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	–	–	1	Vdc
(I_C = 5 Adc, I_B = 1 Adc)		–	–	2	
(I_C = 8 Adc, I_B = 2 Adc)		–	–	3	
(I_C = 5 Adc, I_B = 1 Adc, $T_C = 100^oC$)		–	–	3	
Base-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.4 Adc)	$V_{BE(sat)}$	–	–	1.2	Vdc
(I_C = 5 Adc, I_B = 1 Adc)		–	–	1.6	
(I_C = 5 Adc, I_B = 1 Adc, $T_C = 100^oC$)		–	–	1.5	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	–	–	MHz
Output Capacitance (V_{CB} · 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	110	–	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 5 A,	t_d	–	0.05	0.1	μs
Rise Time	$I_{B1} = I_{B2}$ = 1 A, t_p = 25 μs,	t_r	–	0.8	1.5	μs
Storage Time	Duty Cycle ≤ 1%)	t_s	–	1	3	μs
Fall Time		t_f	–	0.15	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Voltage Storage Time	(I_C = 5 A, V_{clamp} = 300 Vdc,	t_{sv}	–	0.86	2.3	μs
Crossover Time	I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, $T_C = 100^oC$)	t_c	–	0.14	0.7	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA

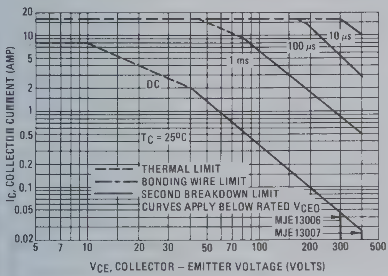
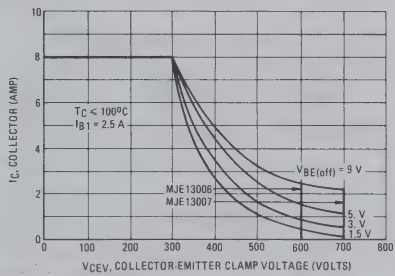
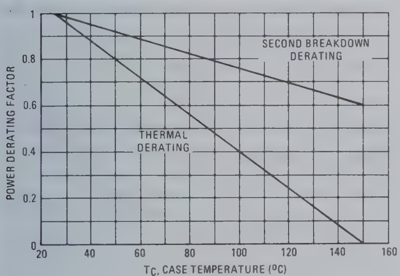


FIGURE 2 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 – FORWARD BIAS POWER DERATING



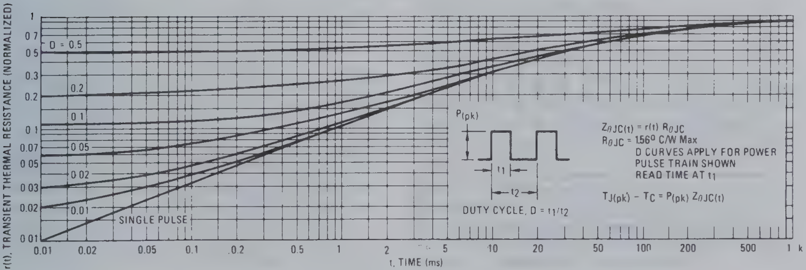
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]



1.3

FIGURE 5 – DC CURRENT GAIN

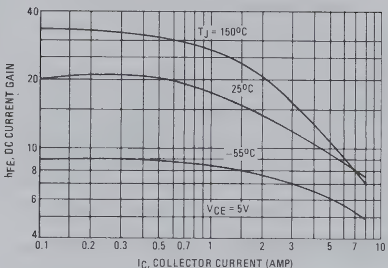


FIGURE 6 – COLLECTOR SATURATION REGION

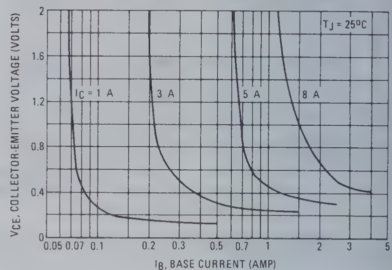


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE

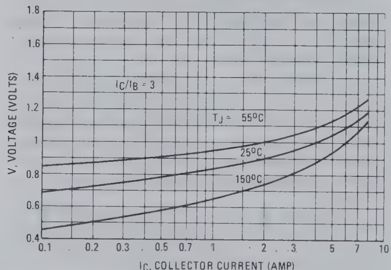


FIGURE 8 – COLLECTOR-EMITTER SATURATION VOLTAGE

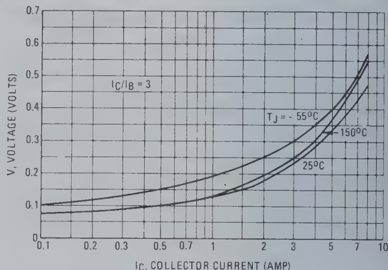


FIGURE 9 – COLLECTOR CUTOFF REGION

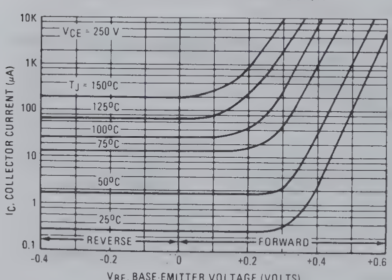


FIGURE 10 – CAPACITANCE

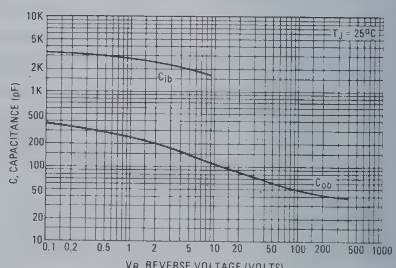


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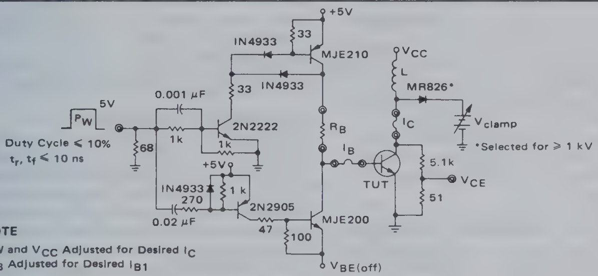
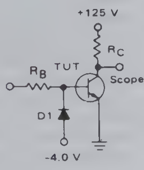
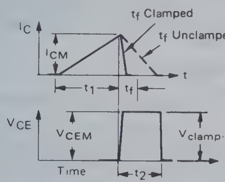
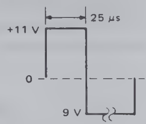
TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 **NOTE** PW and V_{CC} Adjusted for Desired I_C; R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656, Full Bobbin (~16 Turns) #16; GAP for 200 µH/20A; L_{coil} = 200 µH; V_{CC} = 20 V; V_{clamp} = 300 V	V_{CC} = 125 V; R_C = 25 Ω; D1 = 1N5820 or Equiv.; R_B = 10Ω
TEST WAVEFORMS	**OUTPUT WAVEFORMS**  t_1 Adjusted to Obtain I_C; $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$; $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$; Test Equipment Scope — Tektronix 475 or Equivalent	 $t_r, t_f < 10$ ns; Duty Cycle = 1.0%; R_B and R_C adjusted for desired I_B and I_C

APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737A, AN-767, and AN-752.

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).

(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

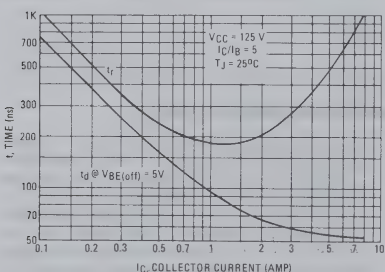


FIGURE 12 – TURN-OFF TIME

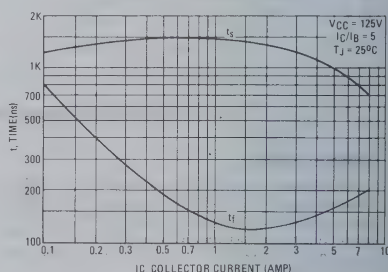


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

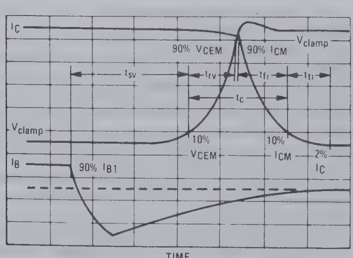


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS (at 300 V and 8A with I_{B1} = 1.6A and $V_{BE(off)}$ = 5 V)

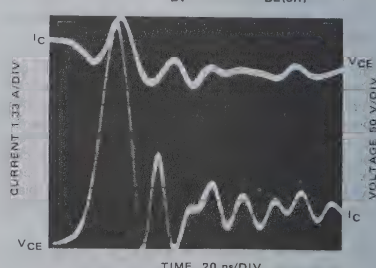


TABLE 2 — APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

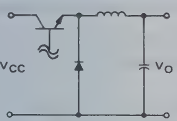
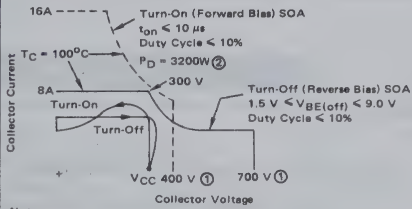
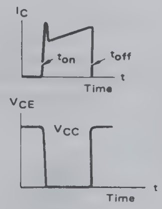
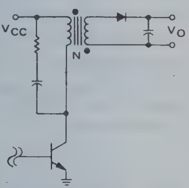
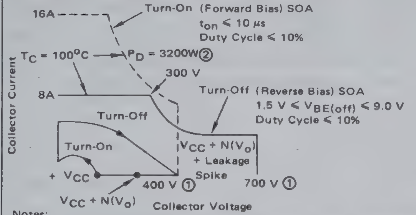
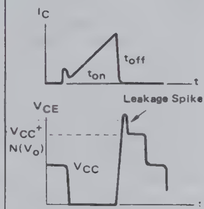
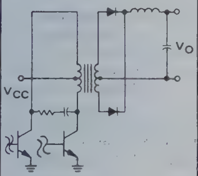
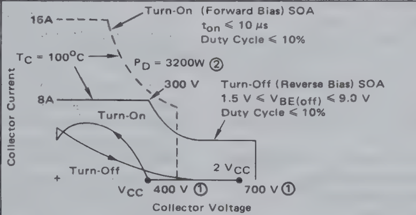
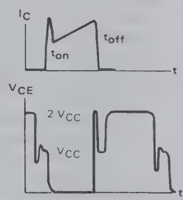
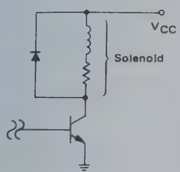
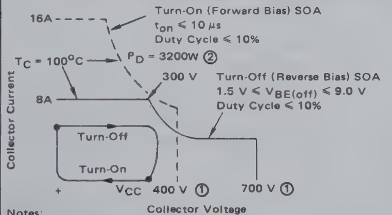
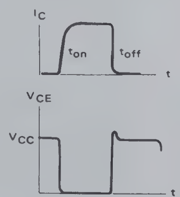
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	SERIES SWITCHING REGULATOR 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13006 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
B	RINGING CHOKE INVERTER 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown. MJE13006 Ratings Are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure	
C	PUSH-PULL INVERTER/CONVERTER 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
D	SOLENOID DRIVER 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	

TABLE 3 — TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25	730	115	100	110	200
	100	1000	150	100	150	250
5	25	600	60	23	4	85
	100	860	84	50	10	136
8	25	650	25	26	4	42
	100	880	52	80	20	160

NOTE: All Data recorded in the inductive Switching Circuit in Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
t_{fi} = Current Fall Time, 90–10% I_{CM}
t_{ti} = Current Tail, 10–2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

MJE13008
MJE13009

MOTOROLA

1.3

Designers Data Sheet

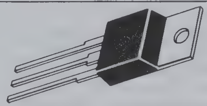
SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE13008 and MJE13009 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 12 Amp, 25 and 100°C . . . t_c @ 8 A, 100°C is 120 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

12 AMPERE
NPN SILICON POWER TRANSISTORS
300 and 400 VOLTS
100 WATTS



Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

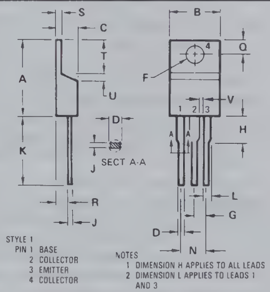
MAXIMUM RATINGS

Rating	Symbol	MJE13008	MJE13009	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	12 24		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6 12		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	18 36		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 800		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13008	$V_{CEO(sus)}$	300	–	–	Vdc
MJE13009		400	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased	–	See Figure 2			
***ON CHARACTERISTICS**					
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)	h_{FE}	8		40	
(I_C = 8 Adc, V_{CE} = 5 Vdc)		6		30	
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1Adc)	$V_{CE(sat)}$	-	-	1	Vdc
(I_C = 8 Adc, I_B = 1.6 Adc)			-	1.5	
(I_C = 12 Adc, I_B = 3 Adc)				3	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		–	–	2	
Base-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc)	$V_{BE(sat)}$	–	–	1.2	Vdc
(I_C = 8 Adc, I_B = 1.6 Adc)		–	–	1.6	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		–	–	1.5	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	–	–	MHz
Output Capacitance (V_{CB} · 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	180	–	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 125 Vdc, I_C = 8 A,	t_d	–	0.06	0.1	μs
Rise Time I_{B1} = I_{B2} = 1.6 A, t_p = 25 μs,	t_r	–	0.45	1	μs
Storage Time Duty Cycle ≤ 1%)	t_s	–	1.3	3	μs
Fall Time	t_f	–	0.2	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time (I_C = 8 A, V_{clamp} = 300 Vdc,	t_{sv}	–	0.92	2.3	μs
Crossover Time I_{B1} = 1.6 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.12	0.7	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 — FORWARD BIAS SAFE OPERATING AREA

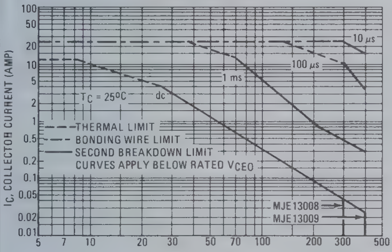
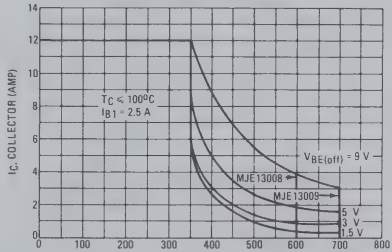
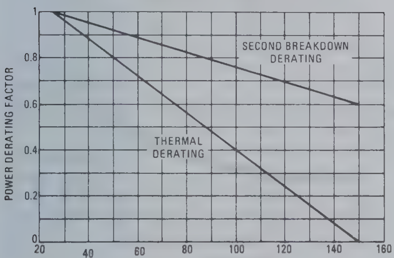


FIGURE 2 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 — FORWARD BIAS POWER DERATING



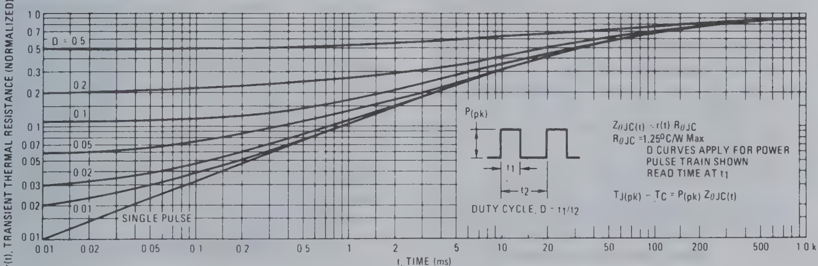
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 — TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]



1.3

FIGURE 5 – DC CURRENT GAIN

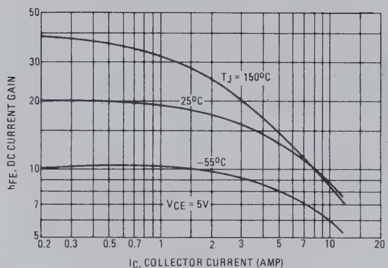


FIGURE 6 – COLLECTOR SATURATION REGION

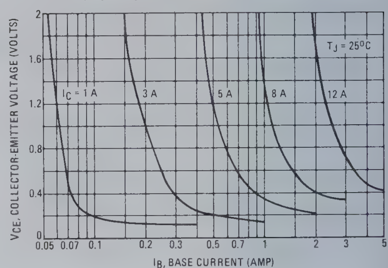


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE

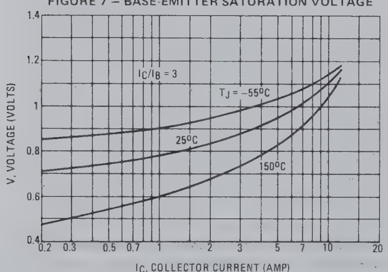


FIGURE 8 – COLLECTOR-EMITTER SATURATION VOLTAGE

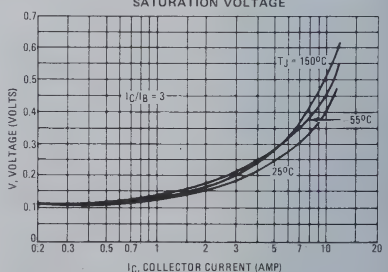


FIGURE 9 – COLLECTOR CUTOFF REGION

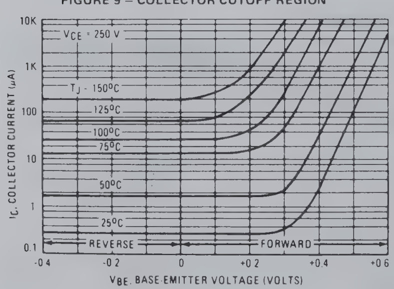


FIGURE 10 – CAPACITANCE

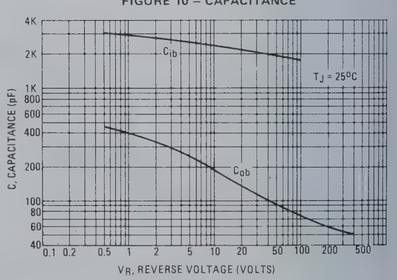


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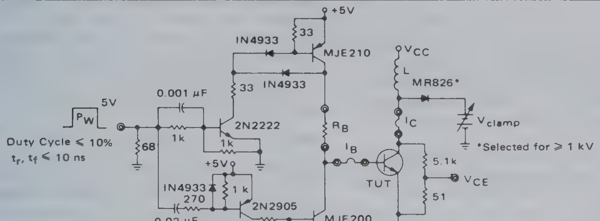
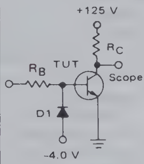
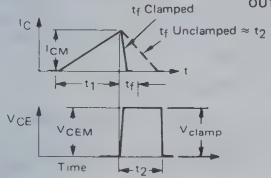
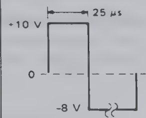
TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 **NOTE** PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 μH/20A L_{coil} = 200 μH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 15 Ω D1 = 1N5820 or Equiv R_B = 5.6 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}\,(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}\,(I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes An-719, AN-737A, AN-752, AN-767.

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VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.
(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).
(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 8 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 — TURN-ON TIME

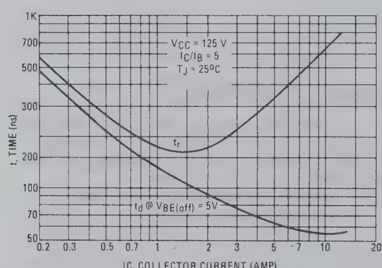


FIGURE 12 — TURN-OFF TIME

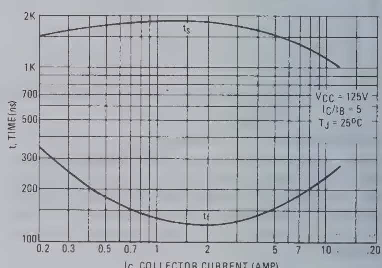


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

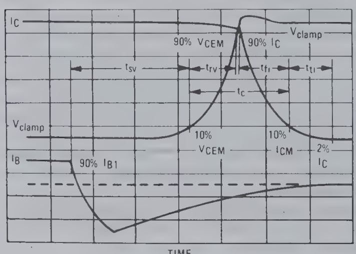


FIGURE 14 — TYPICAL INDUCTIVE SWITCHING WAVEFORMS (at 300 V and 12 A with I_{B1} = 2.4 A and $V_{BE(off)}$ = 5 V)

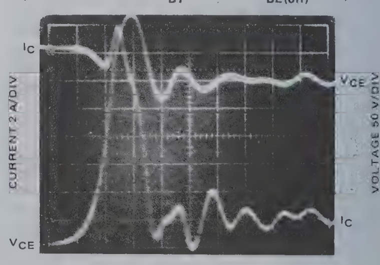
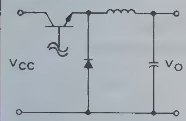
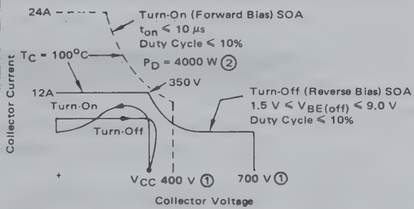
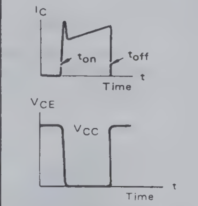
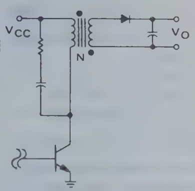
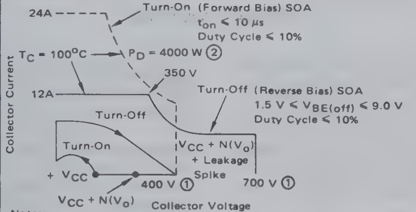
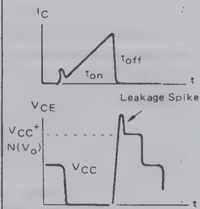
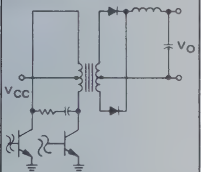
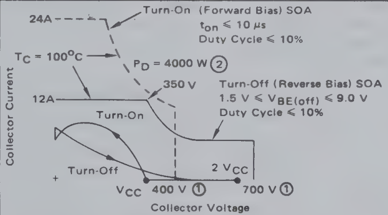
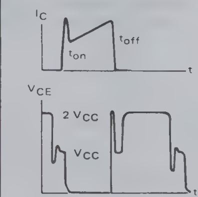
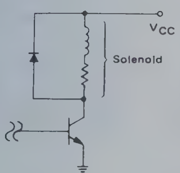
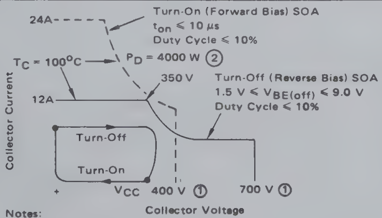


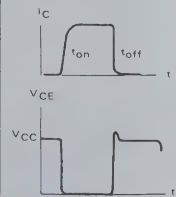
TABLE 2 — APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

<table>
<tr><th></th><th>CIRCUIT</th><th>LOAD LINE DIAGRAMS</th><th>TIME DIAGRAMS</th></tr>
<tr><td>A</td><td>SERIES SWITCHING REGULATOR

</td><td>

Notes:
① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower.
② See AN-569 for Pulse Power Derating Procedure.</td><td>
</td></tr>
<tr><td>B</td><td>RINGING CHOKE INVERTER

</td><td>

Notes:
① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower.
② See AN-569 For Pulse Power Derating Procedure.</td><td>
</td></tr>
<tr><td>C</td><td>PUSH-PULL INVERTER/CONVERTER

</td><td>

Notes:
① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower.
② See AN-569 for Pulse Power Derating Procedure.</td><td>
</td></tr>
<tr><td>D</td><td>SOLENOID DRIVER

</td><td>

Notes:
① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower.
② See AN-569 for Pulse Power Derating Procedure.</td><td>
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</table>

1.3

TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25	770	100	150	200	240
	100	1000	230	160	200	320
5	25	630	72	26	10	100
	100	820	100	55	30	180
8	25	720	55	27	2	77
	100	920	70	50	8	120
12	25	640	20	17	2	41
	100	800	32	24	4	54

NOTE: All Data recorded in the Inductive Switching Circuit in Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
t_{fi} = Current Fall Time, 90–10% I_{CM}
t_{ti} = Current Tail, 10–2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c)\, f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

MJE13070
MJE13071

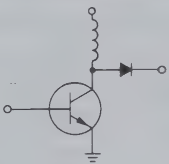
MOTOROLA

Designer's Data Sheet

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The MJE13070 and MJE13071 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
- 100 ns Inductive Fall Time @ 25°C (Typ)
- 150 ns Inductive Crossover Time @ 25°C (Typ)
- 400 ns Inductive Storage Time @ 25°C (Typ)

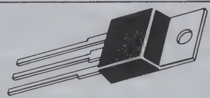
Operating Temperature Range −65 to +150°C

100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

5 AMPERE

NPN SILICON POWER TRANSISTORS

400 AND 450 VOLTS
80 WATTS



Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

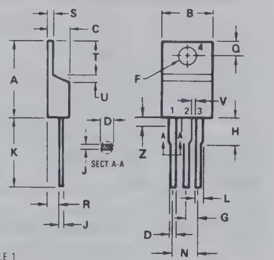
MAXIMUM RATINGS

Rating	Symbol	MJE13070	MJE13071	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	750	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 8.0		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.0 4.0		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	80 32 0.64		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

NOTES
1. DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJE13070	$V_{CEO(sus)}$	400	—	—	Vdc
	MJE13071		450	—	—	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	—	—	0.5	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			—	—	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 5.0 Vdc		h_{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)		$V_{CE(sat)}$	—	—	1.0	Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)			—	—	3.0	
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)			—	—	2.0	
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)		$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)			—	—	1.5	
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	—	—	250	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(V_{CC} = 250 Vdc, I_C = 3.0 Adc, I_{B1} = 0.4 Adc, t_p = 30 μs, Duty Cycle ≤2%, $V_{BE(off)}$ = 5.0 Vdc)		t_d	—	0.03	0.05	μs
Rise Time			t_r	—	0.10	0.40	
Storage Time			t_s	—	0.40	1.50	
Fall Time			t_f	—	0.175	0.50	
Inductive Load, Clamped (Table 1)							
Storage Time	($I_{C(pk)}$ = 3.0 A, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V)	(T_J = 100°C)	t_{sv}	—	0.70	2.0	μs
Crossover Time			t_c	—	0.28	0.50	
Fall Time			t_{fi}	—	0.15	0.30	
Storage Time		(T_J = 25°C)	t_{sv}	—	0.40	—	
Crossover Time			t_c	—	0.15	—	
Fall Time			t_{fi}	—	0.10	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$\beta_f = \frac{I_C}{I_B}$

1.3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

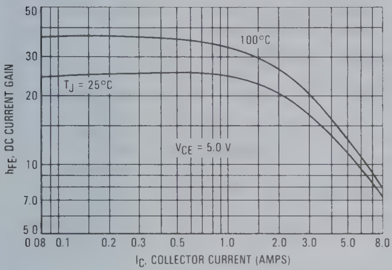


FIGURE 2 — COLLECTOR SATURATION REGION

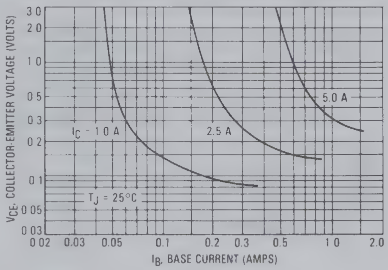


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

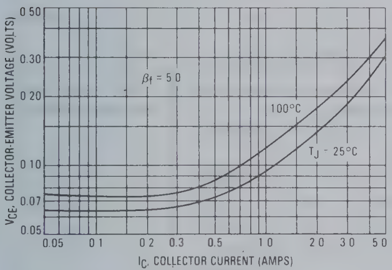


FIGURE 4 — BASE-EMITTER VOLTAGE

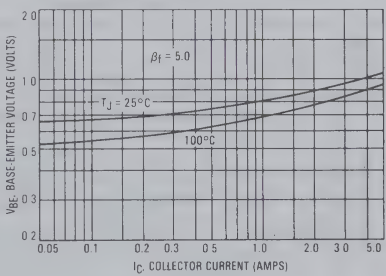


FIGURE 5 — COLLECTOR CUTOFF REGION

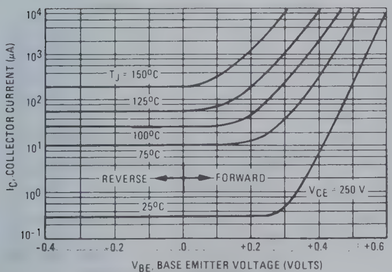


FIGURE 6 — CAPACITANCE

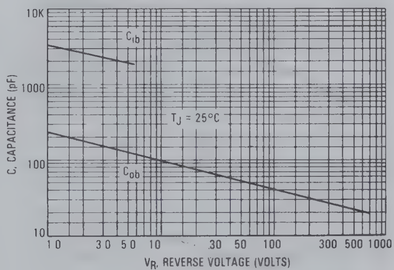


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

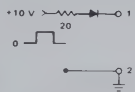
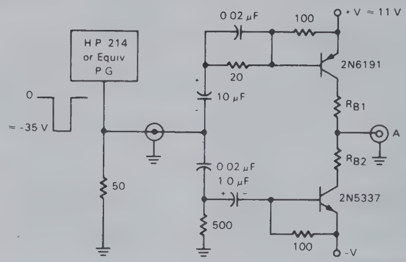
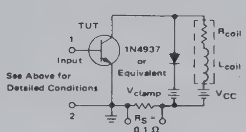
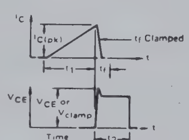
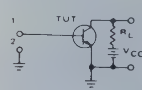
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Adjust R_{B1} to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} - 250 V R_{B1} adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

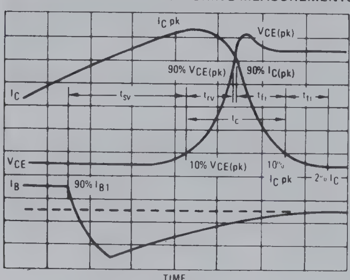
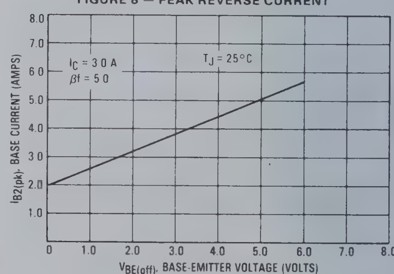


FIGURE 8 — PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

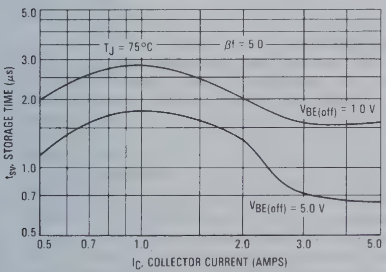


FIGURE 10 — CROSSOVER AND FALL TIMES

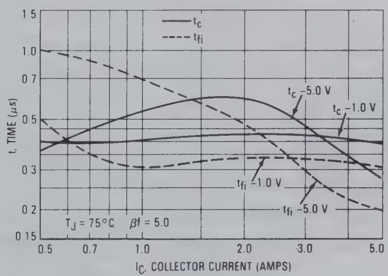
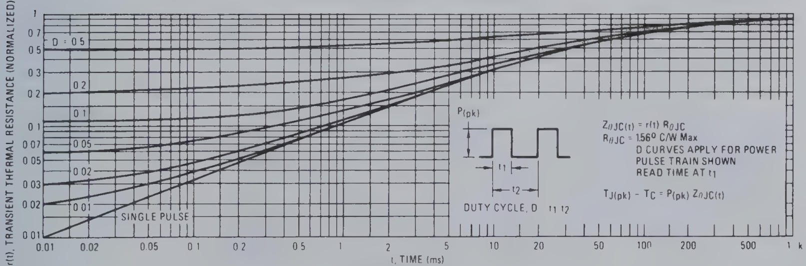


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

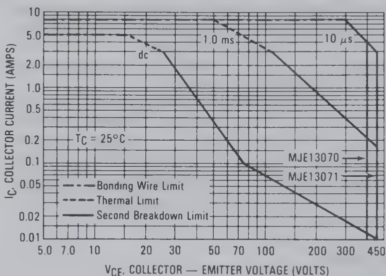
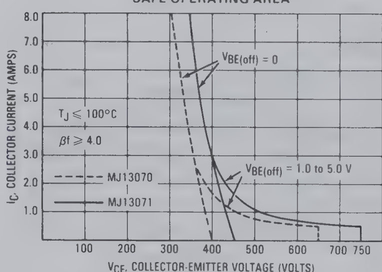


FIGURE 13 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

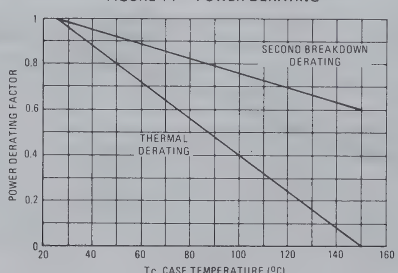
The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 14 — POWER DERATING



MOTOROLA

NPN | PNP

MJE15028 MJE15029
MJE15030 MJE15031

1.3

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

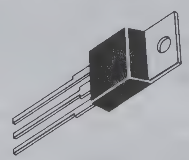
. . . designed for use as high-frequency drivers in audio amplifiers.

- DC Current Gain Specified to 4.0 Amperes
  h_{FE} = 40(Min) @ I_C = 3.0 Adc
  = 20(Min) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 120 Vdc (Min) — MJE15028, MJE15029
  = 150 Vdc (Min) — MJE15030, MJE15031
- High Current Gain — Bandwidth Product
  f_T = 30 MHz (Min) @ I_C = 500 mAdc
- TO-220AB Compact Package
- TO-66 Leadform Also Available

8 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

120–150 VOLTS
50 WATTS



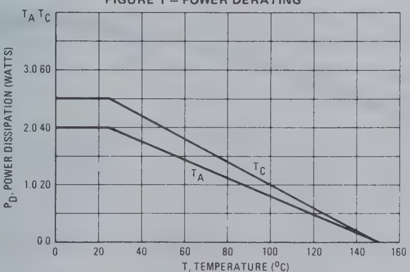
MAXIMUM RATINGS

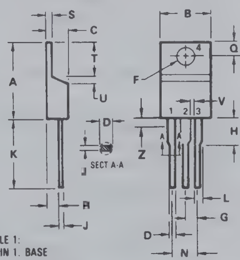
Rating	Symbol	MJE15028 MJE15029	MJE15030 MJE15031	Unit
Collector-Emitter Voltage	V_{CEO}	120	150	Vdc
Collector-Base Voltage	V_{CB}	120	150	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	8.0		Adc
— Peak		16		
Base Current	I_B	2.0		Adc
Total Power Dissipation @ $T_C = 25^oC$	P_D	50		Watts
Derate above 25^oC		0.40		$W/^oC$
Total Power Dissipation @ $T_A = 25^oC$	P_D	2.0		Watts
Derate above 25^oC		0.016		$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^oC/W$

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

1.3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	MJE15028, MJE15029		120	–	
	MJE15030, MJE15031		150	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 120 Vdc, I_B = 0)	MJE15028, MJE15029		–	0.1	
(V_{CE} = 150 Vdc, I_B = 0)	MJE15030, MJE15031		–	0.1	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 120 Vdc, I_E = 0)	MJE15028, MJE15029		–	10	
(V_{CB} = 150 Vdc, I_E = 0)	MJE15030, MJE15031		–	10	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	10	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.1 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)			20	–	
DC Current Gain Linearity (V_{CE} From 2.0V to 20V, I_C From 0.1A to 3A)		h_{FE}	Typ		
			2		
(NPN TO PNP)			3		
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	30	–	MHz

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2)$f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – THERMAL RESPONSE

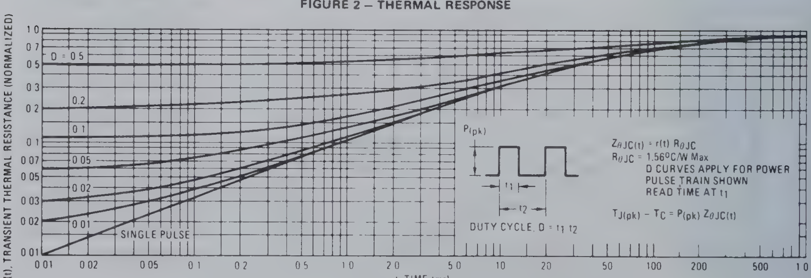
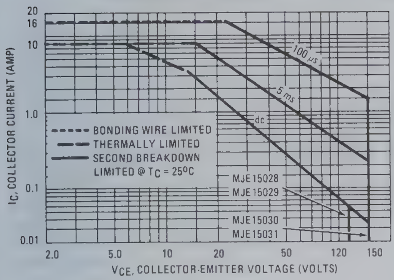


FIGURE 3 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 – REVERSE-BIAS SWITCHING SAFE OPERATING AREA

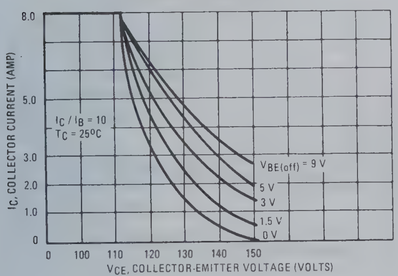


FIGURE 5 – CAPACITANCES

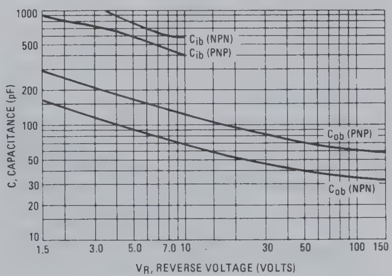


FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

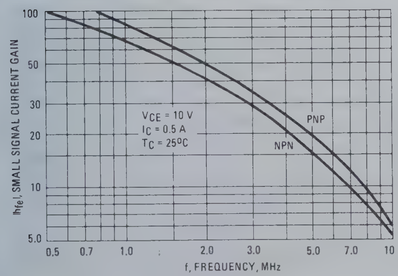
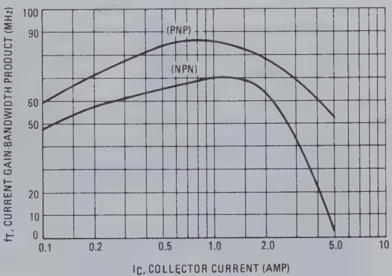
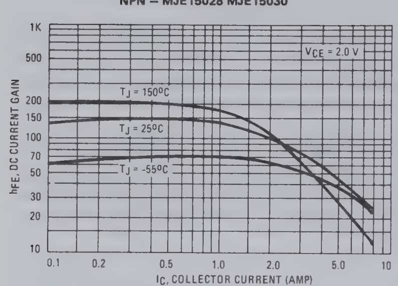


FIGURE 7 – CURRENT GAIN-BANDWIDTH PRODUCT



1.3

FIGURE 8 – DC CURRENT GAIN



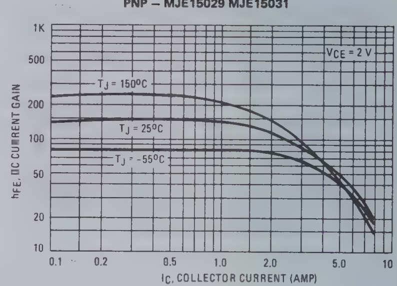
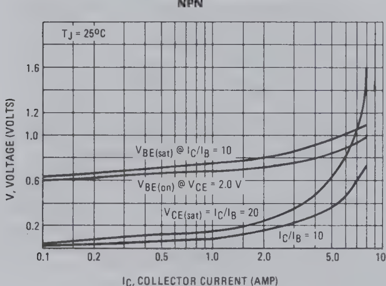


FIGURE 9 – "ON" VOLTAGE



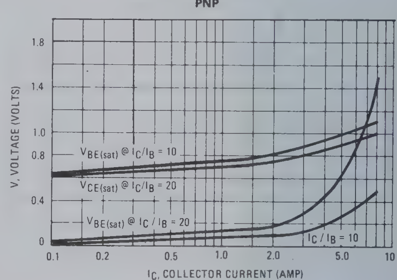


FIGURE 10 – TURN-ON TIMES

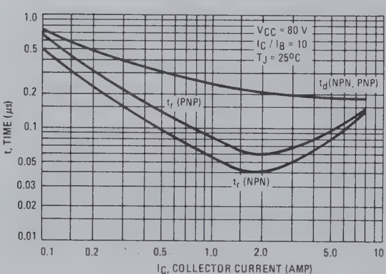
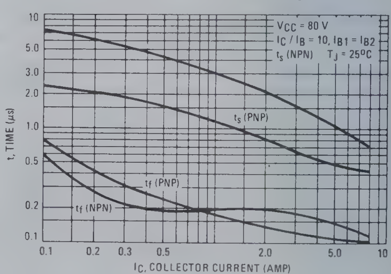


FIGURE 11 – TURN-OFF TIMES



MOTOROLA

MJE16002
MJE16004
MJH16002
MJH16004

Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed switching of inductive circuits where fall time and RBSOA are critical. They are particularly well-suited for line-operated switchmode applications.

The MJE16004 and MJH16004 are high-gain versions of the MJE16002 and MJH16002 for applications where drive current is limited.

Typical Applications:

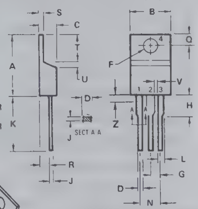
- Switching Regulators
- High Resolution Deflection Circuits
- Inverters
- Motor Drives
- Fast Switching Speeds
  50 ns Inductive Fall Time @ 75°C (Typ)
  70 ns Crossover Time @ 75°C (Typ)
- 100°C Performance Specified for:
  Reverse-Biased SOA
  Inductive Switching Times
  Saturation Voltages
  Leakage Currents

5.0 AMPERE

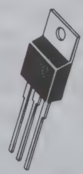
NPN SILICON POWER TRANSISTORS

450 VOLTS
80 and 100 WATTS

MJE16002
MJE16004



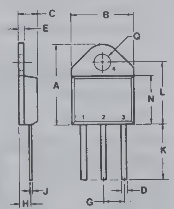
STYLE 1.
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



CASE 221A-02
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14 60	15 75	0 575	0 620
B	9 65	10 29	0 380	0 405
C	4 06	4 82	0 160	0 190
D	0 64	0 89	0 025	0 035
F	3 61	3 73	0 142	0 147
G	2 41	2 67	0 095	0 105
H	2 79	3 93	0 110	0 155
J	0 36	0 56	0 014	0 022
K	12 70	14 27	0 500	0 562
L	1 14	1 39	0 045	0 055
N	4 83	5 33	0 190	0 210
Q	2 54	3 04	0 100	0 120
R	2 04	2.79	0 080	0 110
S	1 14	1 39	0.045	0 055
T	5 97	6 48	0 235	0 255
U	0 00	1 27	0 000	0 050
V	1 14	-	0 045	-
Z	-	2 03	-	0 080

MJH16002
MJH16004



STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340-01
TO-218AC

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

MAXIMUM RATINGS

Rating	Symbol	MJE16002 MJE16004	MJH16002 MJH16004	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450		Vdc
Collector-Emitter Voltage	V_{CEV}	850		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 10		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4.0 8.0		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above $T_C = 25°C$	P_D	80 32 0.64	100 40 0.8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	1.25	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.25	
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 17 or 18		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 19		
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 1.5 Adc, I_B = 0.2 Adc) MJE16002/MJH16002		—	—	1.0	
(I_C = 1.5 Adc, I_B = 0.15 Adc) MJE16004/MJH16004		—	—	1.0	
(I_C = 3.0 Adc, I_B = 0.4 Adc) MJE16002/MJH16002		—	—	2.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc) MJE16004/MJH16004		—	—	2.5	
(I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C) MJE16002/MJH16002		—	—	2.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc, T_C = 100°C) MJE16004/MJH16004		—	—	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 3.0 Adc, I_B = 0.4 Adc) MJE16002/MJH16002		—	—	1.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc) MJE16004/MJH16004		—	—	1.5	
(I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C) MJE16002/MJH16002		—	—	1.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc, T_C = 100°C) MJE16004/MJH16004		—	—	1.5	
DC Current Gain	h_{FE}				—
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc) MJE16002/MJH16002		5.0	—	—	
MJE16004/MJH16004		7.0	—	—	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	200	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1) MJE16002/MJH16002							
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 0.8 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100	ns
Rise Time			t_r	—	100	300	
Storage Time			t_s	—	1000	3000	
Fall Time			t_f	—	60	300	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	400	—	
Fall Time			t_f	—	130	—	
Resistive Load (Table 1) MJE16004/MJH16004							
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.3 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 0.6 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100	ns
Rise Time			t_r	—	130	300	
Storage Time			t_s	—	800	2700	
Fall Time			t_f	—	80	350	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	250	—	
Fall Time			t_f	—	60	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$^*\beta_f = \frac{I_C}{I_{B1}}$

SWITCHING CHARACTERISTICS (continued)

Characteristics			Symbol	Min	Typ	Max	Unit
Inductive Load (Table 2) MJE16002/MJH16002							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	500	1600	ns
Fall Time			t_{fi}	—	100	200	
Crossover Time			t_c	—	120	250	
Storage Time		(T_J = 150°C)	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	
Inductive Load (Table 2) MJE16004/MJH16004							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.3 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	400	1300	ns
Fall Time			t_{fi}	—	80	150	
Crossover Time			t_c	—	90	200	
Storage Time		(T_J = 150°C)	t_{sv}	—	450	—	
Fall Time			t_{fi}	—	100	—	
Crossover Time			t_c	—	110	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$^*\beta_f = \frac{I_C}{I_{B1}}$

FIGURE 1 — DC CURRENT GAIN

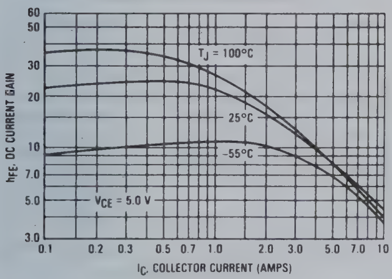


FIGURE 2 — COLLECTOR SATURATION REGION

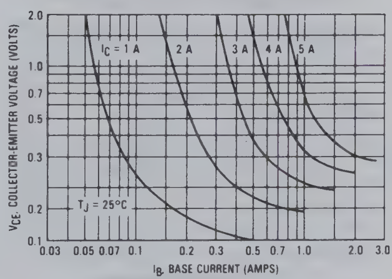


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

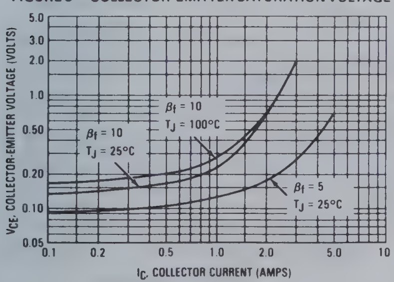
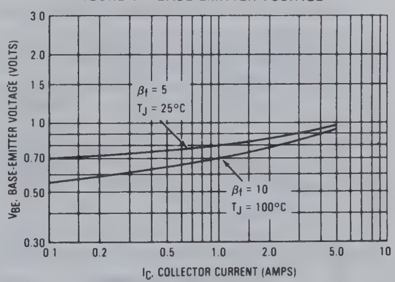


FIGURE 4 — BASE-EMITTER VOLTAGE



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TYPICAL STATIC CHARACTERISTICS (continued)

FIGURE 5 — COLLECTOR CUTOFF REGION

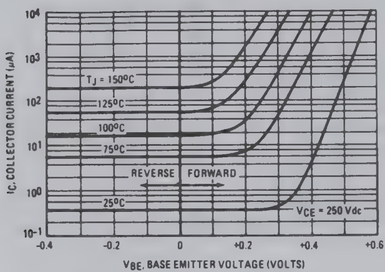
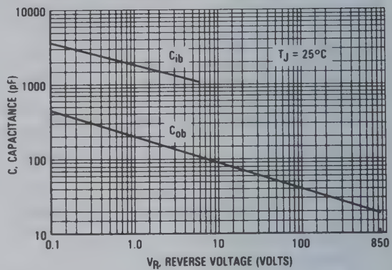


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

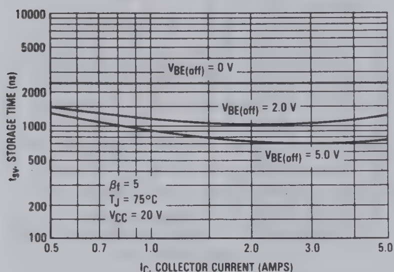


FIGURE 8 — STORAGE TIME

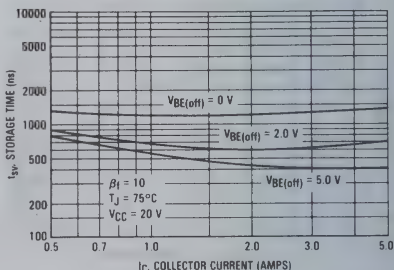


FIGURE 9 — COLLECTOR CURRENT FALL TIME

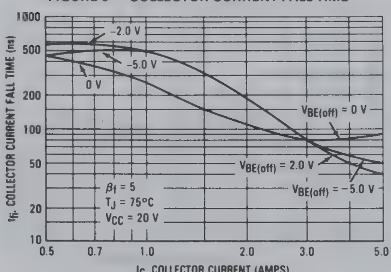
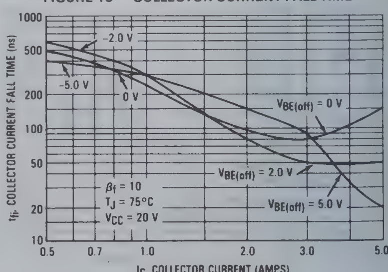


FIGURE 10 — COLLECTOR CURRENT FALL TIME



TYPICAL DYNAMIC CHARACTERISTICS (continued)

FIGURE 11 — CROSSOVER TIME

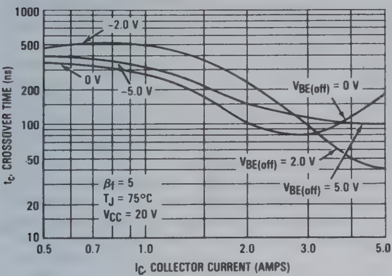
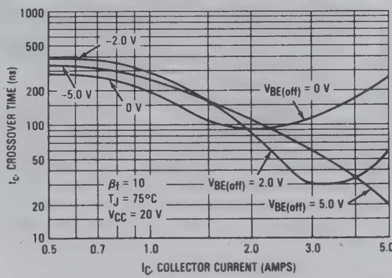


FIGURE 12 — CROSSOVER TIME



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

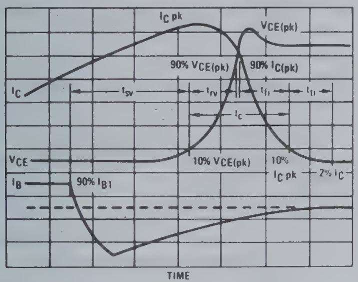


FIGURE 14 — PEAK REVERSE BASE CURRENT

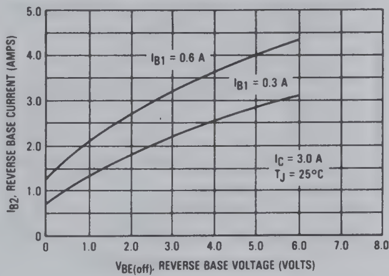
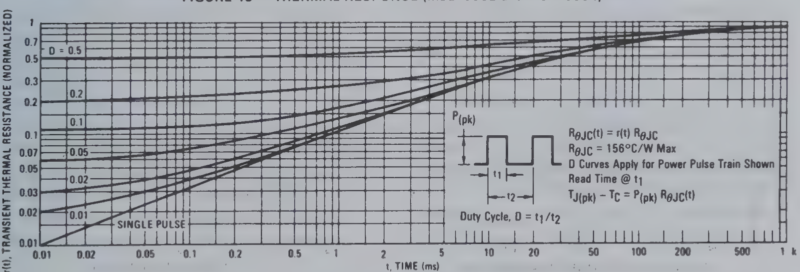


FIGURE 15 — THERMAL RESPONSE (MJE16002 and MJE16004)



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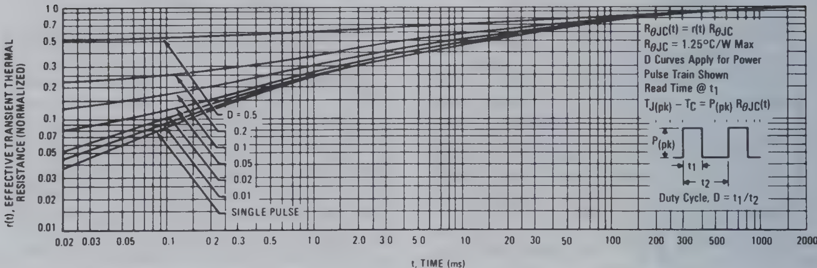
TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 16 — THERMAL RESPONSE (MJH16002 and MJH16004)



SAFE OPERATING AREA INFORMATION

FIGURE 17 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (MJE16002 and MJE16004)

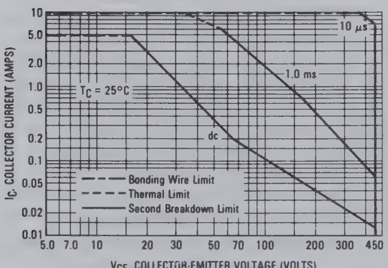


FIGURE 18 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (MJH16002 and MJH16004)

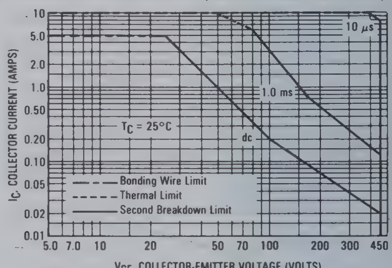


FIGURE 19 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

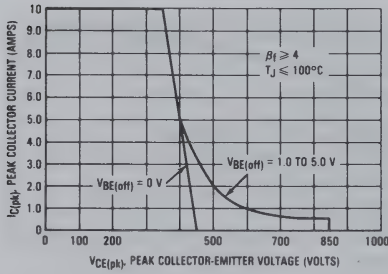
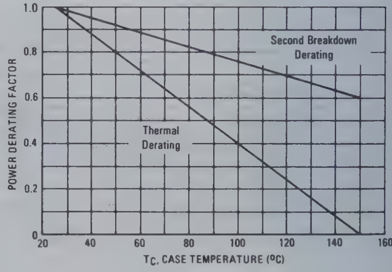


FIGURE 20 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

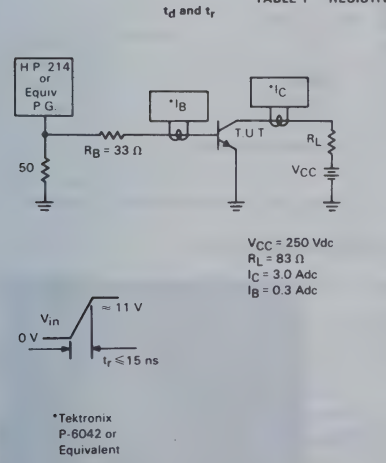
The data of Figures 17 and 18 are based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 17 and 18 may be found at any case temperature by using the appropriate curve on Figure 20.

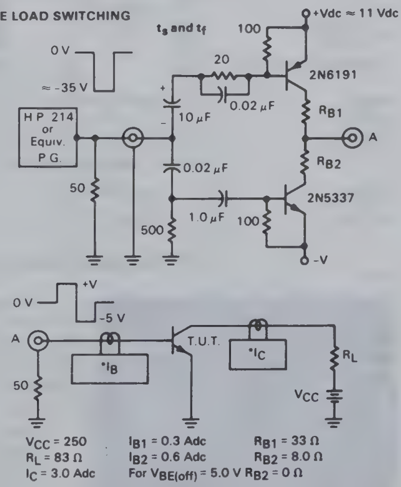
$T_{J(pk)}$ may be calculated from the data in Figures 15 or 16. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneousl during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable putting reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 19 gives the RBSOA characteristics.

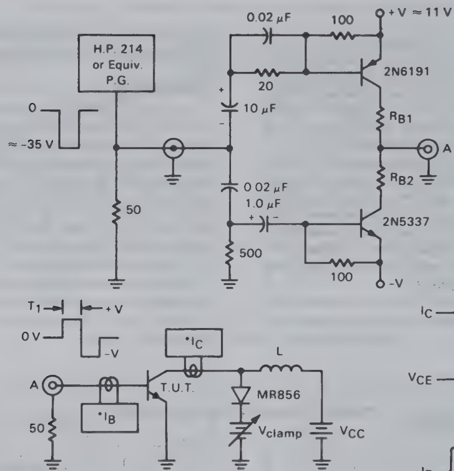
TABLE 1 — RESISTIVE LOAD SWITCHING

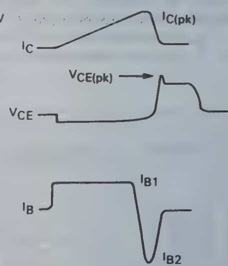




*Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING





$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

BV_{CEO}
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

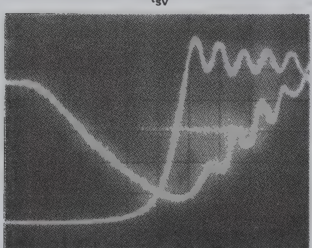
*Tektronix
P-6042 or
Equivalent

Scope - Tektronix
7403 or
Equivalent

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

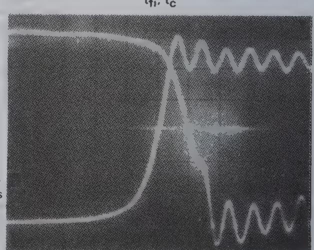
TYPICAL INDUCTIVE SWITCHING WAVEFORMS

t_{sv}



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.3 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 300 Volts
T_C = 25°C
Time Base =
20 ns/cm

t_{fi}, t_c



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.3 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 300 Volts
T_C = 25°C
Time Base =
20 ns/cm

MOTOROLA

MPS-U01
MPS-U01A

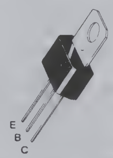
1.3

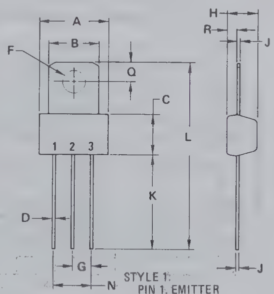
NPN SILICON ANNULAR TRANSISTORS

. . . designed for complementary symmetry audio circuits to 10 Watts output.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 1.0 Adc
- Complements to PNP MPS-U51 and MPS-U51A
- Uniwatt Package for Excellent Thermal Properties — 1.0 Watt @ T_A = 25°C

NPN SILICON
AUDIO TRANSISTORS





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	MPS-U01	MPS-U01A	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Base Voltage	V_{CB}	40	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	2.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	125	°C/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

Uniwatt packages can be To-5 lead formed by adding -5 to the device title and tab formed for flush mounting by adding -1 to the device title.

1.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)	MPS-U01	BV_{CEO}	30	–	Vdc
	MPS-U01A		40	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	MPS-U01	BV_{CBO}	40		Vdc
	MPS-U01A		50	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	MPS-U01	I_{CBO}	–	0.1	μAdc
(V_{CB} = 40 Vdc, I_E = 0)	MPS-U01A		–	0.1	
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 1.0 Vdc)		h_{FE}	55		–
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			50	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$		0.5	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	50	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	20	pF

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

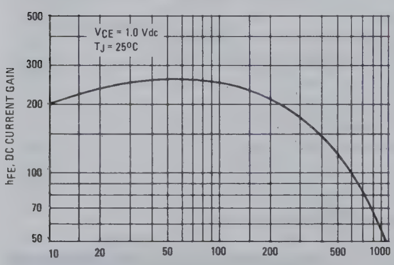


FIGURE 2 — "ON" VOLTAGES

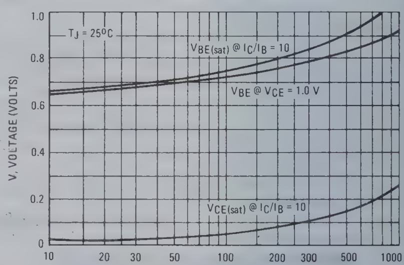
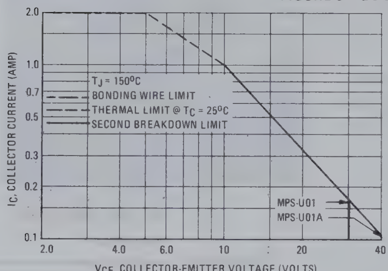


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MPS - U02

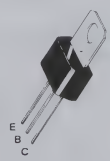
MOTOROLA

NPN SILICON ANNULAR AMPLIFIER TRANSISTOR

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complement to PNP MPS-U52

NPN SILICON AMPLIFIER TRANSISTOR



MAXIMUM RATINGS

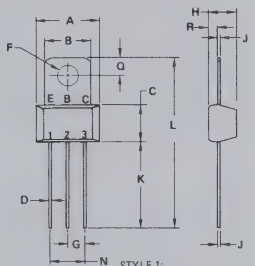
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	800	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	60	-	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	-	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 150 mAdc, V_{CE} = 10 Vdc) (I_C = 500 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 50 50 30	 - 300 -	-
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$	-	0.4	Vdc
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$	-	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	100	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	-	20	pF



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

1.3

FIGURE 1 — NORMALIZED DC CURRENT GAIN

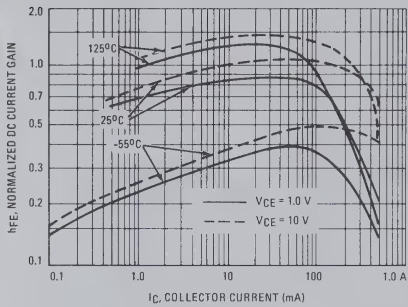


FIGURE 2 — COLLECTOR-EMITTER SATURATION VOLTAGE versus BASE CURRENT

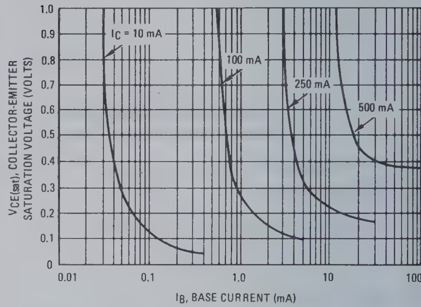


FIGURE 3 — BASE-EMITTER VOLTAGE versus COLLECTOR CURRENT

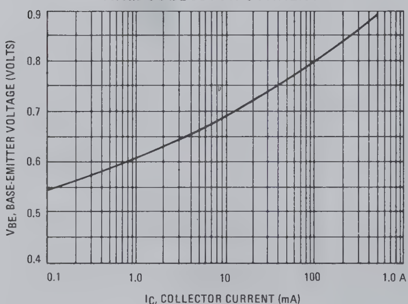


FIGURE 4 — CAPACITANCE versus VOLTAGE

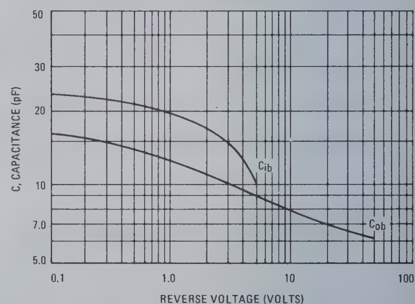


FIGURE 5 — CURRENT-GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

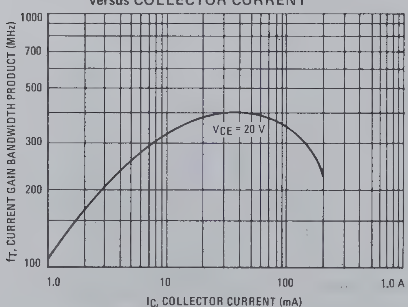
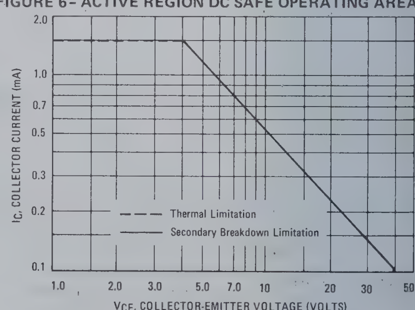


FIGURE 6 - ACTIVE REGION DC SAFE OPERATING AREA



MOTOROLA

MPS-U03
MPS-U04

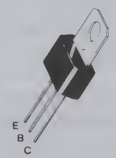
1.3

NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for horizontal drive applications, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 180 Vdc (Min) @ I_C = 1 mAdc — MPS-U04
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 200 mAdc
- High Power Dissipation —
  P_D = 10 W @ T_C = 25°C

NPN SILICON AMPLIFIER TRANSISTORS

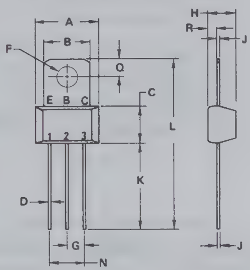


MAXIMUM RATINGS

Rating	Symbol	MPS-U03	MPS-U04	Unit
Collector-Emitter Voltage	V_{CEO}	120	180	Vdc
Collector-Base Voltage	V_{CB}	120	180	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current	I_C	1		Adc
Total Power Dissipation @ T_A = 25°C Derate Above 25°C	P_D	1 8		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C
Solder Temperature, 1/16″ From Case for 10 Seconds	—	260		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

1.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	MPS-U03	BV_{CEO}	120	–	Vdc
	MPS-U04		180	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	MPS-U03	BV_{CBO}	120	–	Vdc
	MPS-U04		180	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	MPS-U03	I_{CBO}	–	0.1	μAdc
(V_{CB} = 150 Vdc, I_E = 0)	MPS-U04		–	0.1	
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc)		h_{FE}	40	–	–
Collector-Emitter Saturation Voltage (I_C = 200 mAdc, I_B = 20 mAdc)		$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter On Voltage (I_C = 200 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	35	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	12	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)		C_{ib}	–	110	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 — CURRENT-GAIN — BANDWIDTH PRODUCT

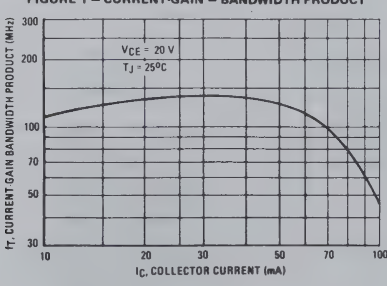
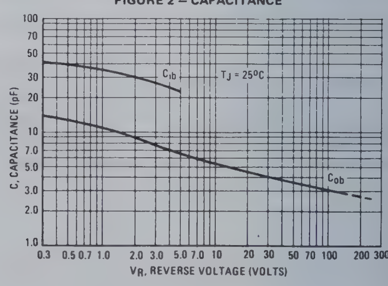


FIGURE 2 — CAPACITANCE



TYPICAL CHARACTERISTICS (Continued)

FIGURE 3 – DC CURRENT GAIN

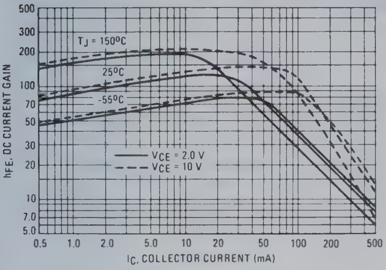


FIGURE 4 – "ON" VOLTAGE

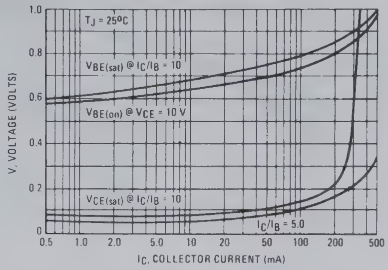


FIGURE 5 – COLLECTOR SATURATION REGION

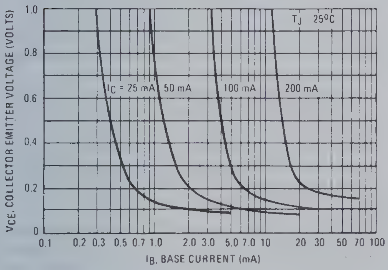


FIGURE 6 – TEMPERATURE COEFFICIENTS

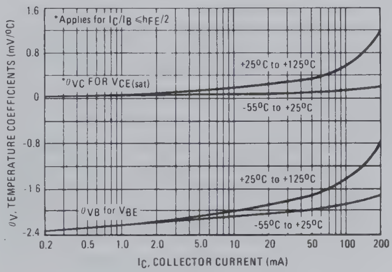


FIGURE 7 – COLLECTOR CHARACTERISTICS

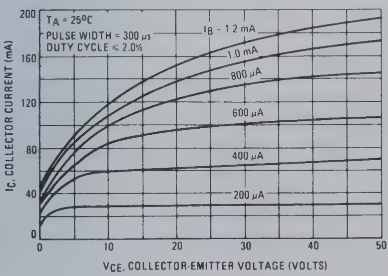
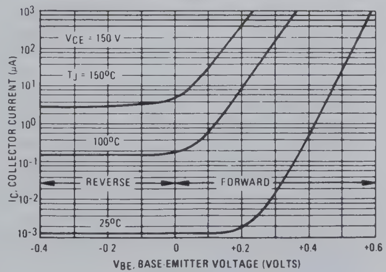


FIGURE 8 – COLLECTOR CUTOFF REGION



1.3

TYPICAL CHARACTERISTICS (Continued)

FIGURE 9 — THERMAL RESPONSE

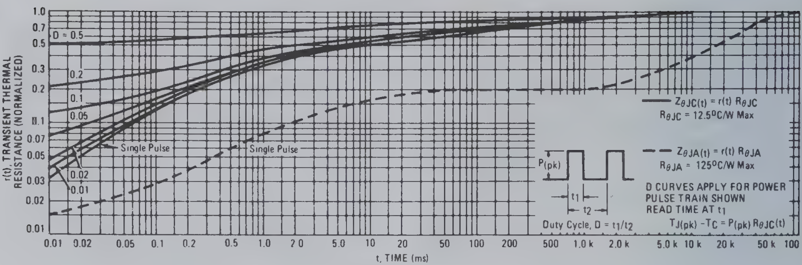
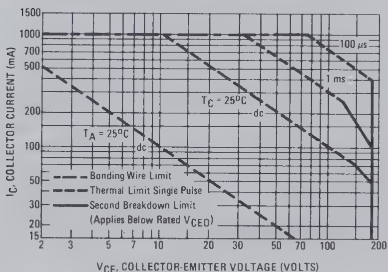


FIGURE 10 — ACTIVE REGION SAFE-OPERATING AREA

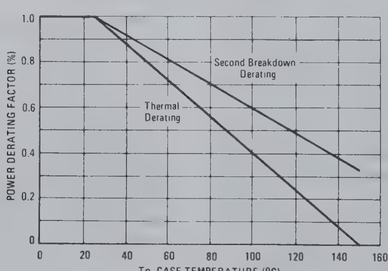


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 — POWER DERATING



MPS-U05
MPS-U06

MOTOROLA

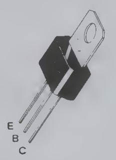
1.3

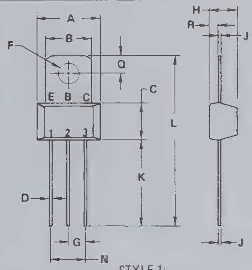
NPN SILICON ANNULAR AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mAdc — MPS-U05
  80 Vdc (Min) @ I_C = 1.0 mAdc — MPS-U06
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complements to PNP MPS-U55 and MPS-U56

NPN SILICON AMPLIFIER TRANSISTORS





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	MPS-U05	MPS-U06	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current — Continuous	I_C	2.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0) MPS-U05	BV_{CEO}	60	–	–	Vdc
MPS-U06		80	–	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) MPS-U05	I_{CBO}	–	–	100	nAdc
(V_{CB} = 60 Vdc, I_E = 0) MPS-U06		–	–	100	
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	80	125	–	–
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		60	100	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		-	55	–	
Collector-Emitter Saturation Voltage(1) (I_C = 250 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	–	0.18	0.4	Vdc
(I_C = 250 mAdc, I_B = 25 mAdc)		–	0.1	–	
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	0.74	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	50	150	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	6.0	12	pF

(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 1 — DC CURRENT GAIN

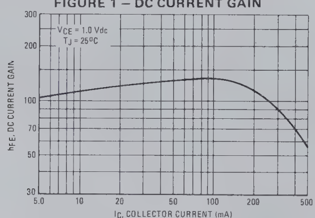


FIGURE 2 — "ON" VOLTAGES

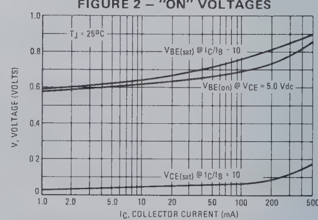


FIGURE 3 — DC SAFE OPERATING AREA

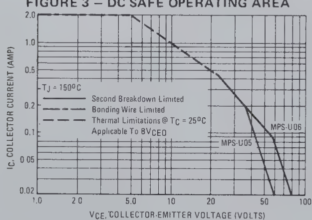
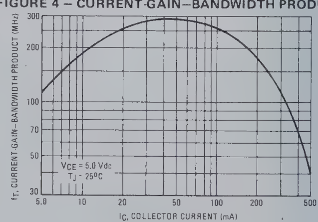


FIGURE 4 — CURRENT-GAIN—BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

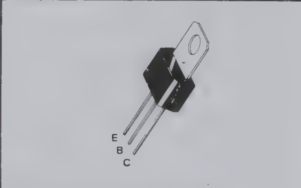
MOTOROLA

NPN SILICON ANNULAR AMPLIFIER TRANSISTOR

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 100 Vdc (Min) @ I_C = 1.0 mAdc
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complement to PNP MPS-U57

NPN SILICON AMPLIFIER TRANSISTOR

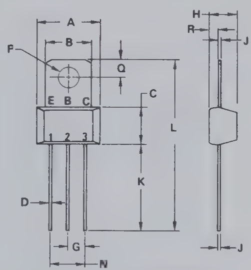


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	2.0	Adc
Total Power Dissipaton @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipaton @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

1.3

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	100	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (1)	h_{FE}				–
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)		60	110	–	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		30	65	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		–	33	–	
Collector-Emitter Saturation Voltage (1)	$V_{CE(sat)}$				Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)		–	0.18	0.4	
(I_C = 250 mAdc, I_B = 25 mAdc)		–	0.1	–	
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	0.76	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	50	150	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	6.0	12	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 – DC CURRENT GAIN

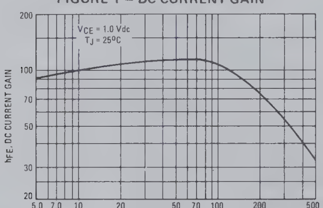


FIGURE 2 – "ON" VOLTAGES

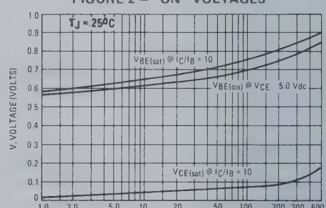


FIGURE 3 – DC SAFE OPERATING AREA

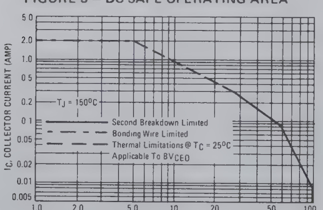
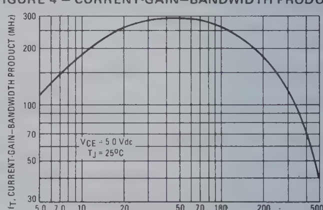


FIGURE 4 – CURRENT-GAIN–BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MPS-U10

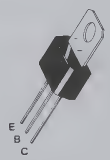
MOTOROLA

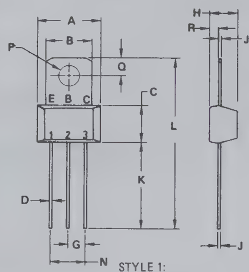
NPN SILICON
HIGH VOLTAGE
AMPLIFIER
TRANSISTOR

NPN SILICON ANNULAR TRANSISTOR

. . . designed for high-voltage video and luminance output stages in TV receivers.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 300 Vdc (Min) @ I_C = 1.0 mAdc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.75 Vdc (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance — C_{cb} = 3.0 pF (Max) @ V_{CB} = 20 Vdc





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	0.5	Adc
Total Power Dissipation @ $T_A = 25^\circ C$ Derate above $25^\circ C$	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA(1)}$	125	°C/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

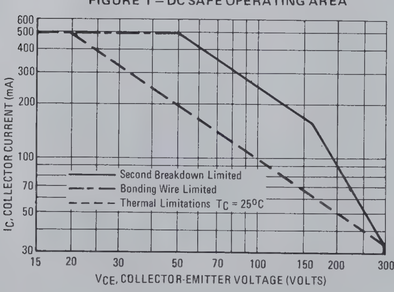
1.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	300	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	300	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	6.0	–	Vdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}		0.2	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			-
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)		25	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)		40	-	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)		40	–	
Collector-Emitter Saturation Voltage (I_C = 30 mAdc, I_B = 3.0 mAdc)	$V_{CE(sat)}$	–	0.75	Vdc
Base-Emitter On Voltage (I_C = 30 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	–	0.85	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (1) (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	45	–	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	3.0	pF

(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle≤ 2%.

FIGURE 1 — DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C—V_{CE} limits below which the device will not enter second breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – DC CURRENT GAIN

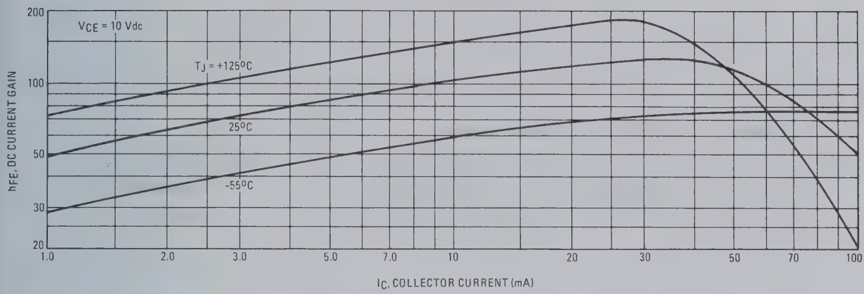


FIGURE 3 – CAPACITANCES

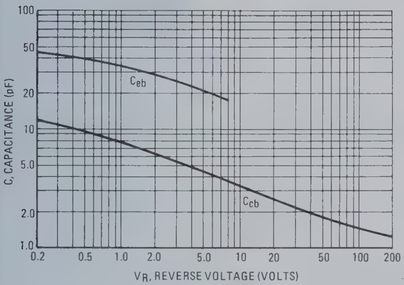


FIGURE 4 – CURRENT-GAIN–BANDWIDTH PRODUCT

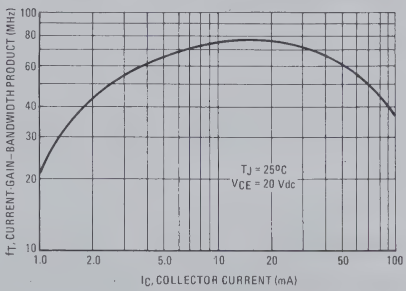
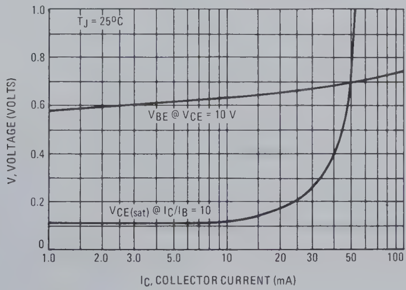


FIGURE 5 – "ON" VOLTAGES



MPS-U31

MOTOROLA

1.3

NPN SILICON ANNULAR RF TRANSISTOR

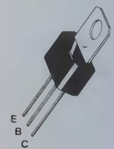
. . . designed for use in Citizen-Band and other high-frequency communications equipment operating to 30 MHz. Higher breakdown voltages allow a high percentage of up-modulation in AM circuits. This device is designed to be used with the MPS8000 driver and the MPS8001 RF oscillator.

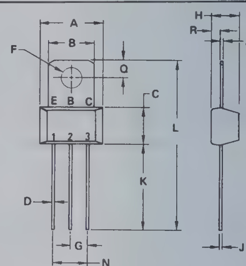
- Output Power = 3.5 W (Min) @ V_{CC} = 13.6 Vdc
- Power Gain = 11.5 dB (Min)
- High Collector-Emitter Breakdown Voltage — $BV_{CES} \geq 65$ Vdc
- DC Current Gain — Linear to 500 mAdc

3.5 W — 27 MHz

RF POWER OUTPUT TRANSISTOR

NPN SILICON





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	65	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	1.0 8.0	Watt $mW/^oC$
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	10 80	Watt $mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JA}$	12.5	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}(1)$	125	$^oC/W$

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 150 mAdc, V_{BE} = 0)	BV_{CES}	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	BV_{EBO}	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	–	–	0.01	mAdc
ON CHARACTERISTICS					
DC Current Gain (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc)	h_{FE}	10	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	40	pF
FUNCTIONAL TEST (Figure 1)					
Common-Emitter Amplifier Power Gain (P_{out} = 3.5 W, V_{CC} = 13.6 Vdc, f = 27 MHz)	G_{PE}	11.5	–	–	dB
Output Power (P_{in} = 250 mW, V_{CC} = 13.6 Vdc, f = 27 MHz)	P_{out}	3.5	–	–	Watts
Collector Efficiency (3) (P_{out} = 3.5 W, V_{CC} = 13.6 Vdc, f = 27 MHz)	η	–	70	–	%
Percentage Up-Modulation (4) (f = 27 MHz)	–	–	85	–	%

(1) Pulsed thru a 25 mH Inductor

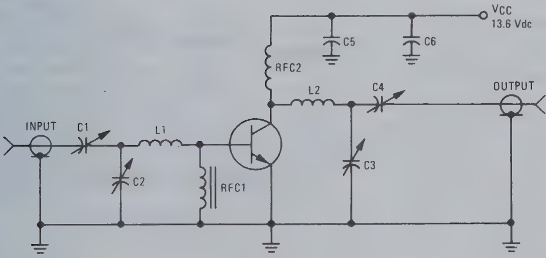
(2) Pulse Test: Pulse Width $\leqslant$300 μs, Duty Cycle $\leqslant$2.0%.

(3) $\eta = \dfrac{R_F\, P_{out}}{(V_{CC})\,(I_C)} \bullet 100$

(4) Percentage Up-Modulation is measured in the test circuit (Figure 1) by setting the Carrier Power (P_c) to 3.5 Watts with V_{CC} = 13.6 Vdc and noting the power input. Then the Peak Envelope Power (PEP) is noted after doubling the original power input to simulate driver modulation (at a 25% duty cycle for thermal considerations) and raising the V_{CC} to 25 Vdc (to simulate the modulating voltage). Percentage Up-Modulation is then determined by the relation:

$$\text{Percentage Up-Modulation} = \left[\left(\frac{PEP}{P_c}\right)^{1/2} - 1\right] \bullet 100$$

FIGURE 1 – 27 MHz TEST CIRCUIT



C1, C2 9.0-180 pF ARCO 463 or Equivalent
C3, C4 5.0-80 pF ARCO 462 or Equivalent
C5 0.02 μF Ceramic Disc
C6 0.1 μF Ceramic Disc
RFC1 4 Turns #30 Enameled Wire Wound on Ferroxcube Bead Type 56-590-65/3B
RFC2 26 Turns #22 Enameled Wire (2 Layers – 13 Turns Each Layer) ¼" Inner Diameter
L1 0.22 μH Molded Choke
L2 0.68 μH Molded Choke

1.3

POWER OUTPUT

FIGURE 2 – V_{CC} = 12.5 Vdc

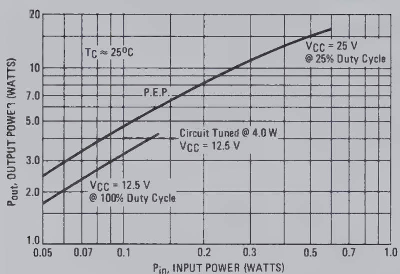


FIGURE 3 – V_{CC} = 13.6 Vdc

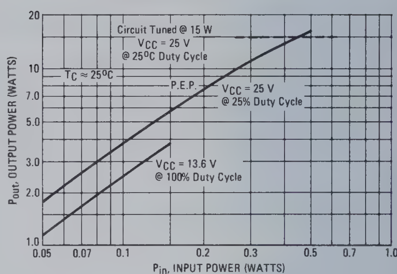


FIGURE 4 – CURRENT-GAIN – BANDWIDTH PRODUCT

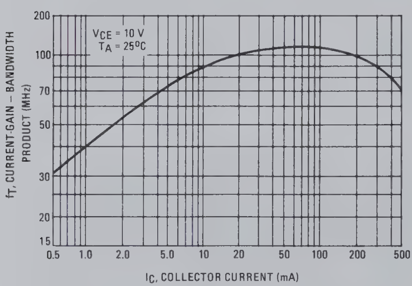


FIGURE 5 – CAPACITANCE

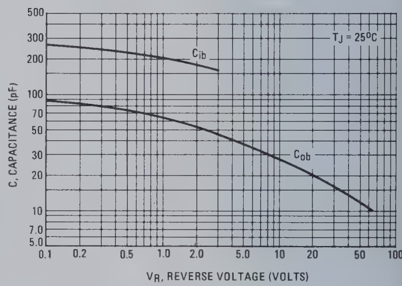


FIGURE 6 – DC CURRENT GAIN

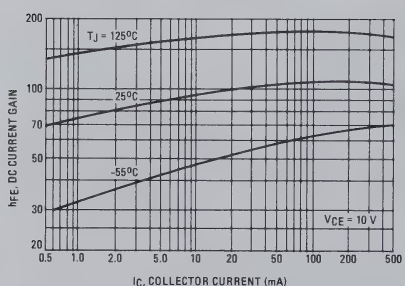
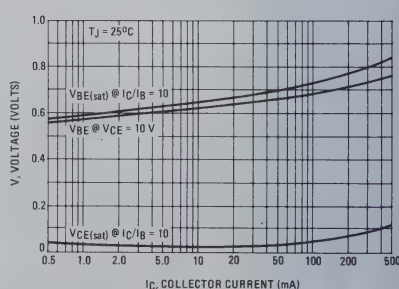


FIGURE 7 – ON VOLTAGES



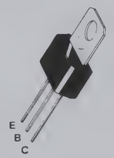
MOTOROLA

NPN SILICON DARLINGTON AMPLIFIER TRANSISTOR

. . . designed for amplifier and driver applications.

- High DC Current Gain –
  h_{FE} = 25,000 (Min) @ I_C = 200 mAdc
  15,000 (Min) @ I_C = 500 mAdc
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc @ I_C = 1.0 Adc
- Monolithic Construction for High Reliability
- Complement to PNP MPS-U95

NPN SILICON DARLINGTON TRANSISTOR



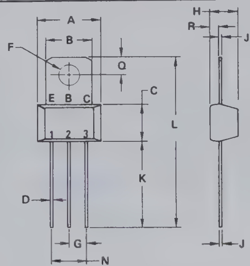
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}(1)	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	12	Vdc
Collector Current	I_C	2.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

(1) Due to the monolithic construction of this device, breakdown voltages of both transistor elements are identical. BV_{CES} is tested in lieu of BV_{CEO} in order to avoid errors caused by noise pickup. The voltage measured during the BV_{CES} test is the BV_{CEO} of the output transistor.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

1.3

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ($I_C = 100\ \mu Adc$, $V_{BE} = 0$)	BV_{CES}	40	–	–	Vdc
Collector-Base Breakdown Voltage ($I_C = 100\ \mu Adc$, $I_E = 0$)	BV_{CBO}	50	–	–	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\ \mu Adc$, $I_C = 0$)	BV_{EBO}	12	–	–	Vdc
Collector Cutoff Current ($V_{CB} = 30$ Vdc, $I_E = 0$)	I_{CBO}	–	–	100	nAdc
Emitter Cutoff Current ($V_{EB} = 10$ Vdc, $I_C = 0$)	I_{EBO}	–	–	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain	h_{FE}				
($I_C = 200$ mAdc, $V_{CE} = 5.0$ Vdc)		25,000	65,000	150,000	
($I_C = 500$ mAdc, $V_{CE} = 5.0$ Vdc)		15,000	35,000	–	
($I_C = 1.0$ Adc, $V_{CE} = 5.0$ Vdc)		4,000	12,000	–	
Collector-Emitter Saturation Voltage ($I_C = 1.0$ Adc, $I_B = 2.0$ mAdc)	$V_{CE(sat)}$	–	1.2	1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0$ Adc, $I_B = 2.0$ mAdc)	$V_{BE(sat)}$	–	1.85	2.0	Vdc
Base-Emitter On Voltage ($I_C = 1.0$ Adc, $V_{CE} = 5.0$ Vdc)	$V_{BE(on)}$	–	1.7	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (1) ($I_C = 200$ mAdc, $V_{CE} = 5.0$ Vdc, f = 100 MHz)	$\lvert h_{fe} \rvert$	1.0	3.2	–	–
Collector Base Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, f = 1.0 MHz)	C_{cb}	–	2.5	6.0	pF

(1)Pulse Test: Pulse Width $\leq 300\ \mu s$, Duty Cycle $\leq 2.0\%$.

Uniwatt darlington transistors can be used in any number of low power applications, such as relay drivers, motor control and as general purpose amplifiers. As an audio amplifier these devices, when used as a complementary pair, can drive 3.5 watts into a 3.2 ohm speaker using a 14 volt supply with less than one per cent distortion. Because of the high gain the base drive requirement is as low as 1 mA in this application. They are also useful as power drivers for high current application such as voltage regulators.

FIGURE 1 — DC CURRENT GAIN

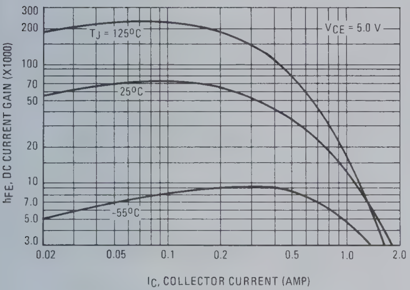


FIGURE 2 — SMALL-SIGNAL CURRENT GAIN

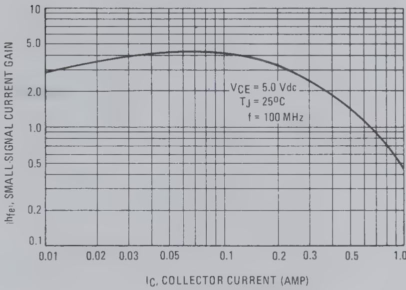


FIGURE 3 — "ON" VOLTAGES

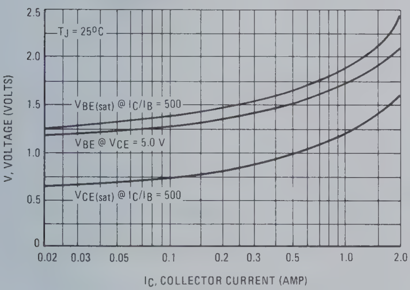


FIGURE 4 — TEMPERATURE COEFFICIENT

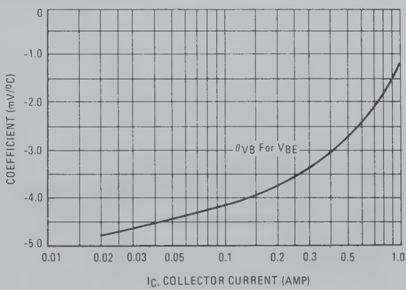
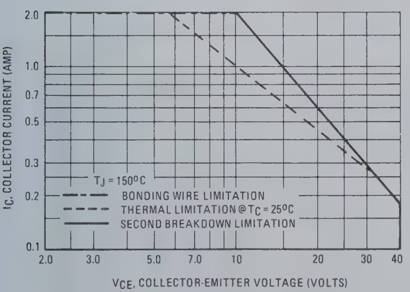


FIGURE 5 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MPS-U51
MPS-U51A

MOTOROLA

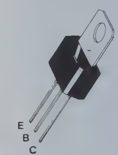
1.3

PNP SILICON ANNULAR TRANSISTORS

. . . designed for complementary symmetry audio circuits to 5 Watts output.

- Excellent Current Gain Linearity — 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 1.0 Adc
- Complements to NPN MPS-U01 and MPS-U01A
- Uniwatt Package for Excellent Thermal Properties — 1.0 Watt @ T_A = 25°C

PNP SILICON AUDIO TRANSISTORS

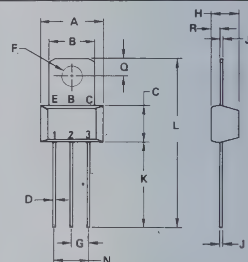


MAXIMUM RATINGS

Rating	Symbol	MPS-U51	MPS-U51A	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Base Voltage	V_{CB}	40	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	2.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	 MPS-U51 MPS-U51A	BV_{CEO}	 30 40	 – –	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	 MPS-U51 MPS-U51A	BV_{CBO}	 40 50		Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0		Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0)	 MPS-U51 MPS-U51A	I_{CBO}	 – 	 0.1 0.1	μAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 1.0 Vdc) (I_C = 100 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	 55 60 50	 – – –	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	–	0.7	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	50	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}		30	pF

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

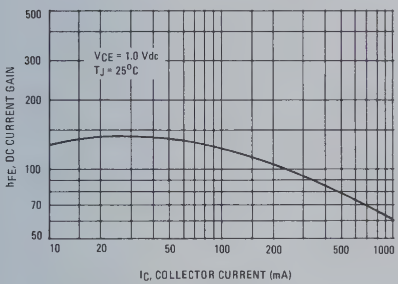


FIGURE 2 — "ON" VOLTAGES

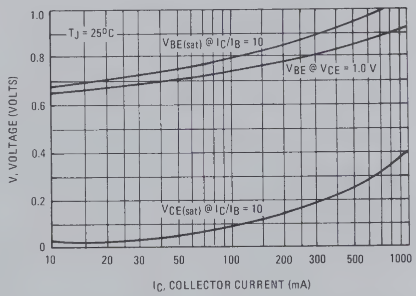
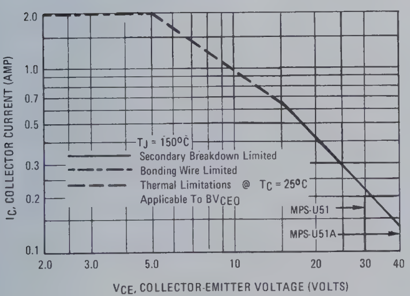


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MPS-U52

MOTOROLA

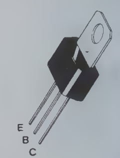
1.3

PNP SILICON ANNULAR TRANSISTOR

. . . designed for general-purpose amplifier and driver applications.

- Complement to NPN MPS-U02

PNP SILICON AMPLIFIER TRANSISTOR



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	1.5	Adc
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg} (1)	-55 to +150	°C

THERMAL CHARACTERISTICS

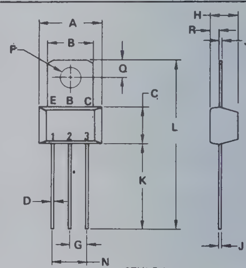
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ (1)	125	°C/W

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	60	-	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	-	100	nAdc
ON CHARACTERISTICS (2)				
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 150 mAdc, V_{CE} = 10 Vdc) (I_C = 500 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 50 50 30	 - 300 -	-
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$	-	0.4	Vdc
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$	-	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (2) (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	100	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	-	24	pF

(1) $R_{\theta JA}$ is measured with device soldered into a typical printed circuit board

(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

FIGURE 1 – DC CURRENT GAIN

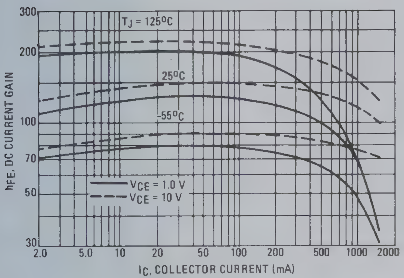


FIGURE 2 – "ON" VOLTAGES

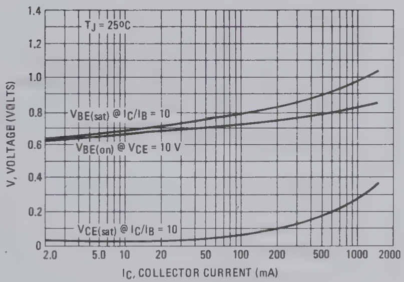


FIGURE 3 – COLLECTOR SATURATION REGION

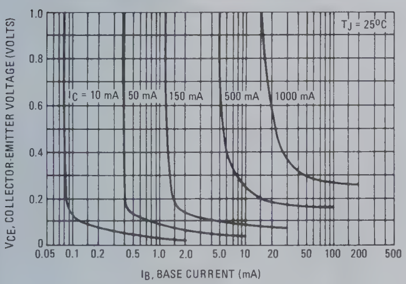


FIGURE 4 – DC SAFE OPERATING AREA

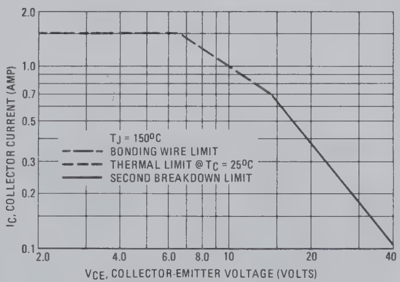


FIGURE 5 – CURRENT-GAIN BANDWIDTH PRODUCT

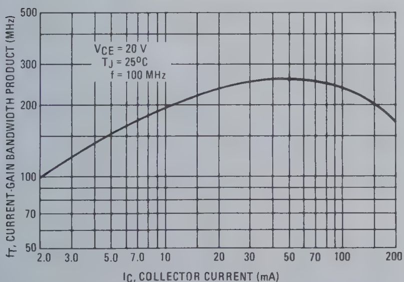
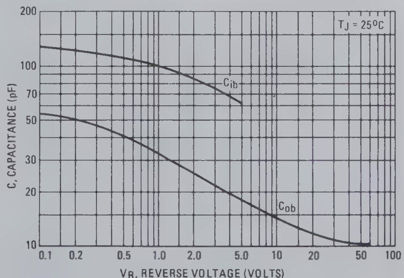


FIGURE 6 – CAPACITANCE



MPS-U55
MPS-U56

MOTOROLA

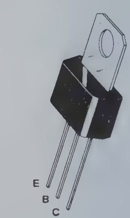
1.3

PNP SILICON ANNULAR AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mAdc – MPS-U55
  80 Vdc (Min) @ I_C = 1.0 mAdc – MPS-U56
- High Power Dissipation – P_D = 10 W @ T_C = 25°C
- Complements to NPN MPS-U05 and MPS-U06

PNP SILICON AMPLIFIER TRANSISTORS



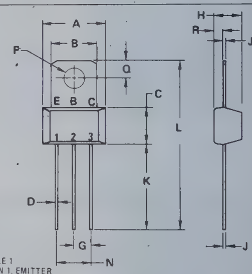
MAXIMUM RATINGS

Rating	Symbol	MPS-U55	MPS-U56	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	2.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0 100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

Collector Connected to Tab

CASE 152-02

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0) MPS-U55	BV_{CEO}	60	–	–	Vdc
MPS-U56		80	–	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) MPS-U55	I_{CBO}	–	–	100	nAdc
(V_{CB} = 60 Vdc, I_E = 0) MPS-U56		–	–	100	
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	80	160	–	–
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		50	130	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		–	80	–	
Collector-Emitter Saturation Voltage(1) (I_C = 250 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	–	0.22	0.5	Vdc
(I_C = 250 mAdc, I_B = 25 mAdc)		–	0.15	–	
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	0.78	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	50	100	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	10	15	pF

(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 1 — DC CURRENT GAIN

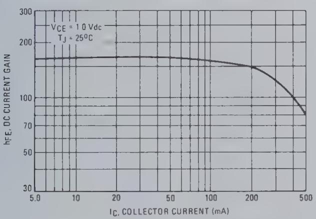


FIGURE 2 — "ON" VOLTAGES

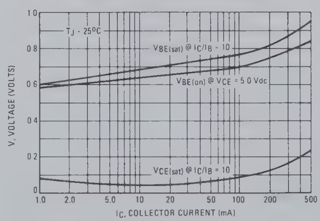


FIGURE 3 — ACTIVE-REGION SAFE OPERATING AREA

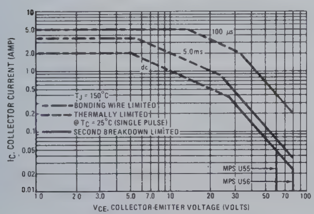
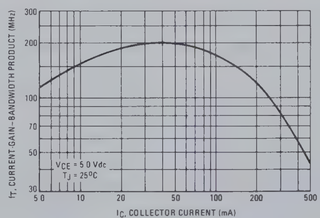


FIGURE 4 — CURRENT-GAIN—BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MPS - U57

MOTOROLA

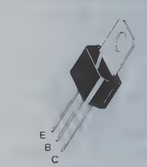
1.3

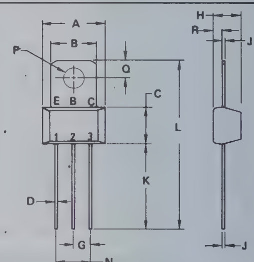
PNP SILICON ANNULAR
AMPLIFIER TRANSISTOR

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 100 Vdc (Min) @ I_C = 1.0 mAdc
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complement to NPN MPS-U07

AMPLIFIER TRANSISTOR
PNP SILICON





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current Continuous	I_C	2.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

1.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	100	–	–	Vdc
Emitter-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				–
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)		60	140	–	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		30	65	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		–	30	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)		–	0.24	0.5	
(I_C = 250 mAdc, I_B = 25 mAdc)		–	0.15	–	
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	0.78	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	50	100	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	10	15	pF

(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2.0%.

FIGURE 1 – DC CURRENT GAIN

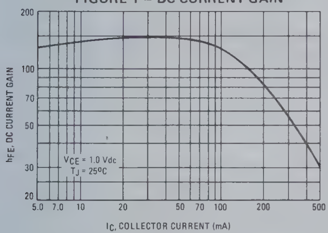


FIGURE 2 – "ON" VOLTAGES

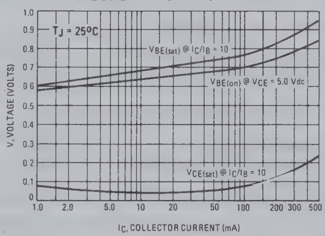


FIGURE 3 – DC SAFE OPERATING AREA

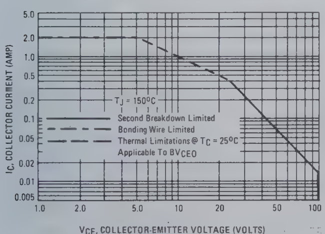
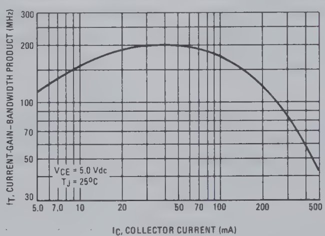


FIGURE 4 – CURRENT-GAIN—BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MPS - U60

MOTOROLA

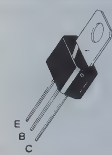
1.3

PNP SILICON ANNULAR TRANSISTOR

. . . designed for general-purpose applications requiring high breakdown voltages, low saturation voltages and low capacitance.

- Complement to NPN Type MPS-U10

PNP SILICON HIGH VOLTAGE TRANSISTOR



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	1.0 8.0	Watt mW/^oC
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	10 80	Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	55 to +150	^oC

THERMAL CHARACTERISTICS

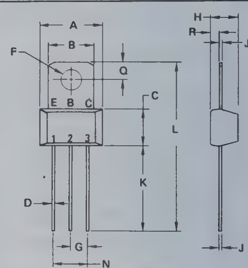
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	125	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Breakdown Voltage (2) (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	300	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	300		Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0		Vdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}	–	0.2	μAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}		0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (2) (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 30 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 25 30 30		
Collector-Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 2.0 mAdc)	$V_{CE(sat)}$	–	0.75	Vdc
Base-Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 2.0 mAdc)	$V_{BE(sat)}$	–	0.9	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (2) (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	60	–	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	8.0	pF

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

(2) Pulse Test: Pulse Width $\leqslant$ 300 μs, Duty Cycle $\leqslant$ 2.0%.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

FIGURE 1 – DC CURRENT GAIN

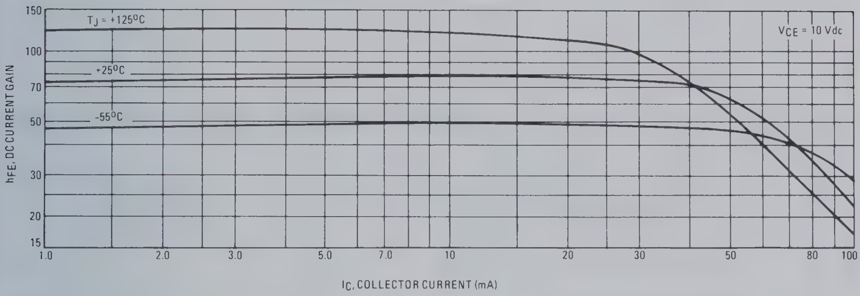


FIGURE 2 – CAPACITANCES

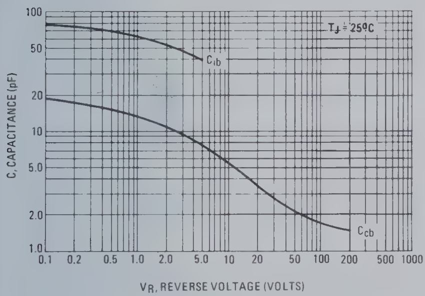


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

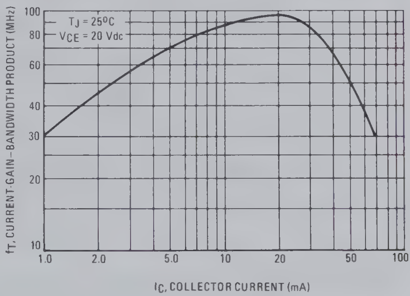


FIGURE 4 – "ON" VOLTAGES

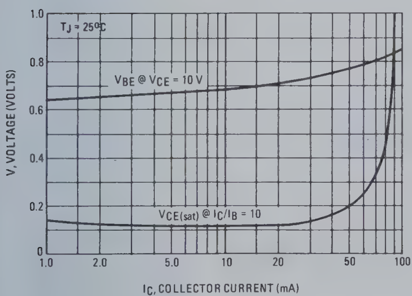
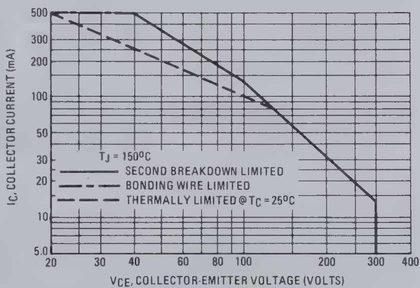


FIGURE 5 – DC SAFE OPERATING AREA



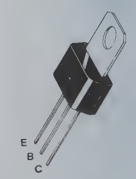
MOTOROLA

PNP SILICON DARLINGTON AMPLIFIER TRANSISTOR

. . . designed for amplifier and driver applications.

- High DC Current Gain –
  h_{FE} = 25,000 (Min) @ I_C = 200 mAdc
  15,000 (Min) @ I_C = 500 mAdc
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc @ I_C = 1.0 Adc
- Monolithic Construction for High Reliability
- Complement to NPN MPS-U45

PNP SILICON DARLINGTON TRANSISTOR



MAXIMUM RATINGS

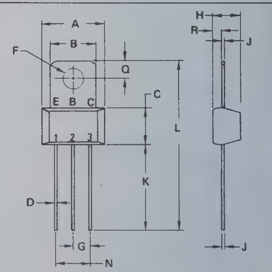
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}(1)	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current -Continuous	I_C	2.0	Adc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	1.0 8.0	Watt mW/^{o}C
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	10 80	Watts mW/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	^{o}C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(2)	125	^{o}C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	^{o}C/W

(1) Due to the monolithic construction of this device, breakdown voltages of both transistor elements are identical. BV_{CES} is tested in lieu of BV_{CEO} in order to avoid errors caused by noise pickup. The voltage measured during the BV_{CES} test is the BV_{CEO} of the output transistor.

(2) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ($I_C = 100\ \mu Adc$, $V_{BE} = 0$)	BV_{CES}	40	–	–	Vdc
Collector-Base Breakdown Voltage ($I_C = 100\ \mu Adc$, $I_E = 0$)	BV_{CBO}	50	–	–	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\ \mu Adc$, $I_C = 0$)	BV_{EBO}	10	–	–	Vdc
Collector Cutoff Current ($V_{CB} = 30$ Vdc, $I_E = 0$)	I_{CBO}	–	–	100	nAdc
Emitter Cutoff Current ($V_{EB} = 8.0$ Vdc, $I_C = 0$)	I_{EBO}	–	–	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain	h_{FE}				–
($I_C = 200$ mAdc, $V_{CE} = 5.0$ Vdc)		25,000	43,000	150,000	
($I_C = 500$ mAdc, $V_{CE} = 5.0$ Vdc)		15,000	41,000	–	
($I_C = 1.0$ Adc, $V_{CE} = 5.0$ Vdc)		4,000	35,000	–	
Collector-Emitter Saturation Voltage ($I_C = 1.0$ Adc, $I_B = 2.0$ mAdc)	$V_{CE(sat)}$	–	1.0	1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0$ Adc, $I_B = 2.0$ mAdc)	$V_{BE(sat)}$	–	1.85	2.0	Vdc
Base-Emitter On Voltage ($I_C = 1.0$ Adc, $V_{CE} = 5.0$ Vdc)	$V_{BE(on)}$	–	1.7	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (1) ($I_C = 200$ mAdc, $V_{CE} = 5.0$ Vdc, f = 100 MHz)	$\|h_{fe}\|$	0.5	1.6	–	–
Collector Base Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, f = 1.0 MHz)	C_{cb}	–	2.5	12	pF

(1)Pulse Test: Pulse Width $\leq 300\ \mu s$, Duty Cycle $\leq 2.0\%$.

Uniwatt darlington transistors can be used in any number of low power applications, such as relay drivers, motor control and as general purpose amplifiers. As an audio amplifier these devices, when used as a complementary pair, can drive 3.5 watts into a 3.2 ohm speaker using a 14 volt supply with less than one per cent distortion. Because of the high gain the base drive requirement is as low as 1 mA in this application. They are also useful as power drivers for high current application such as voltage regulators.

FIGURE 1 — DC CURRENT GAIN

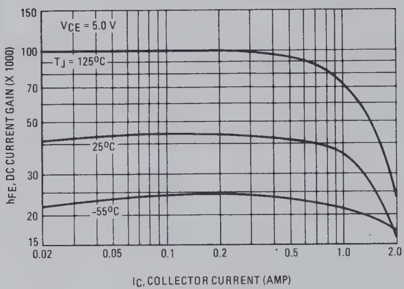


FIGURE 2 — SMALL-SIGNAL CURRENT GAIN

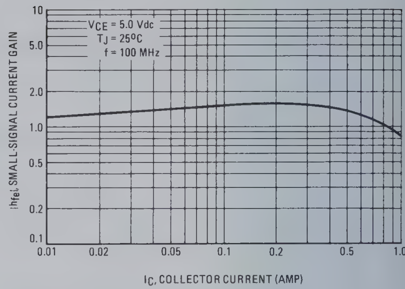


FIGURE 3 — "ON" VOLTAGES

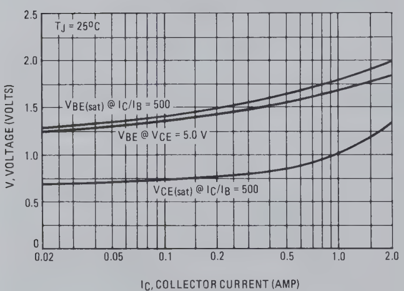


FIGURE 4 — TEMPERATURE COEFFICIENT

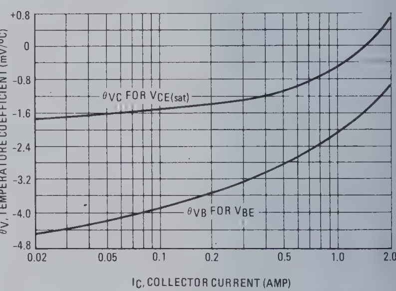
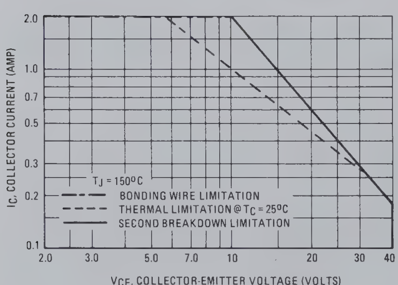


FIGURE 5 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN PNP

TIP29 TIP30
TIP29A TIP30A
TIP29B TIP30B
TIP29C TIP30C

MOTOROLA

1.3

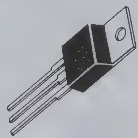
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications. Compact TO-220 AB package. TO-66 leadform also available.

1 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

40-60-80-100 VOLTS
30 WATTS



MAXIMUM RATINGS

Rating	Symbol	TIP29 TIP30	TIP29A TIP30A	TIP29B TIP30B	TIP29C TIP30C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current — Continuous Peak	I_C	← 1.0 → ← 3.0 →				Adc
Base Current	I_B	← 0.4 →				Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	← 30 → ← 0.24 →				Watts W/^oC
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	← 2.0 → ← 0.016 →				Watts W/^oC
Unclamped Inductive Load Energy (See Note 3)	E	← 32 →				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →				^oC

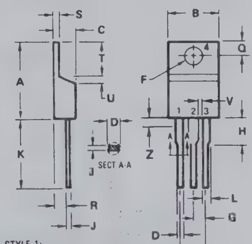
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.167	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP29, TIP30 TIP29A, TIP30A TIP29B, TIP30B TIP29C, TIP30C	$V_{CEO(sus)}$	40 60 80 100	— — — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	 TIP29, TIP29A, TIP30, TIP30A TIP29B, TIP29C, TIP30B, TIP30C	I_{CEO}	 — —	 0.3 0.3	mAdc
Collector Cutoff Current (V_{CE} = 40 Vdc, V_{EB} = 0) (V_{CE} = 60 Vdc, V_{EB} = 0) (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	 TIP29, TIP30 TIP29A, TIP30A TIP29B, TIP30B TIP29C, TIP30C	I_{CES}	 — — — —	 200 200 200 200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.2 Adc, V_{CE} = 4.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 40 15	 — 75	—
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 125 mAdc)		$V_{CE(sat)}$	—	0.7	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	—	MHz
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20	—	—

(1) Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$
(3) This rating based on testing with L_C = 20 mH, R_{BE} = 100 Ω, V_{CC} = 10 V, I_C = 1.8 A, P.R.F. = 10 Hz.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	—	0.045	—
Z	—	2.03	—	0.080

CASE 221A-02
TO-220AB

FIGURE 1 – DC CURRENT GAIN

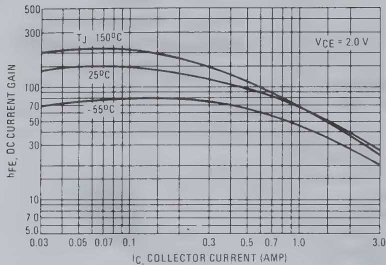


FIGURE 2 – TURN-OFF TIME

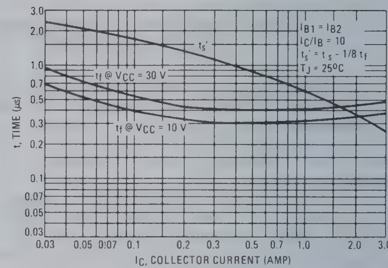


FIGURE 3 – SWITCHING TIME EQUIVALENT CIRCUIT

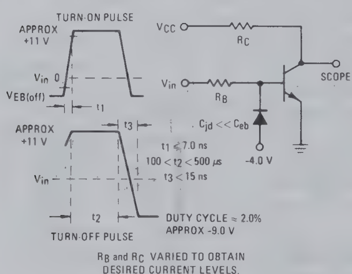


FIGURE 4 – TURN-ON TIME

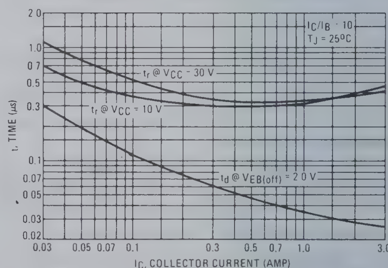
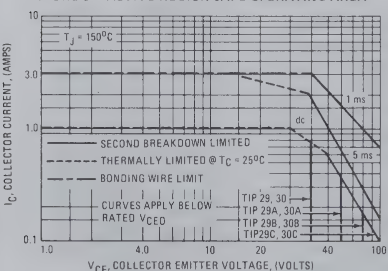


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA

NPN	PNP
TIP31	**TIP32**
TIP31A	**TIP32A**
TIP31B	**TIP32B**
TIP31C	**TIP32C**

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

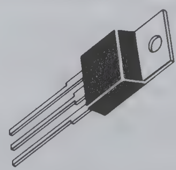
. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc (Min) — TIP31, TIP 32
  = 60 Vdc (Min) — TIP31A, TIP32A
  = 80 Vdc (Min) — TIP31B, TIP32B
  = 100 Vdc (Min) — TIP31C, TIP32C
- High Current Gain — Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220 AB Package
- TO-66 Leadform Also Available

3 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

40-60-80-100 VOLTS
40 WATTS



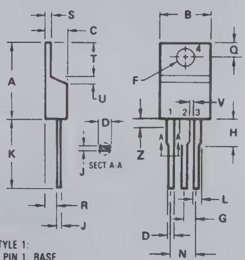
*MAXIMUM RATINGS

Rating	Symbol	TIP31 TIP32	TIP31A TIP32A	TIP31B TIP32B	TIP31C TIP32C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous	I_C	3.0				Adc
Peak		5.0				
Base Current	I_B	1.0				Adc
Total Power Dissipation @ T_C = 25°C	P_D	40				Watts
Derate above 25°C		0.32				W/°C
Total Power Dissipation @ T_A = 25°C	P_D	2.0				Watts
Derate above 25°C		0.016				W/°C
Unclamped Inductive Load Energy (1)	E	32				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1.8 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP31, TIP32	$V_{CEO(sus)}$	40	–	Vdc
	TIP31A, TIP32A		60	–	
	TIP31B, TIP32B		80	–	
	TIP31C, TIP32C		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP31, TIP31A, TIP32, TIP32A		–	0.3	
(V_{CE} = 60 Vdc, I_B = 0)	TIP31B, TIP31C, TIP32B, TIP32C		–	0.3	
Collector Cutoff Current		I_{CES}			µAdc
(V_{CE} = 40 Vdc, V_{EB} = 0)	TIP31, TIP32		–	200	
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP31A, TIP32A		–	200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP31B, TIP32B		–	200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP31C, TIP32C		–	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			25	–	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			10	50	
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 375 mAdc)		$V_{CE(sat)}$	–	1.2	Vdc
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		$\|h_{fe}\|$	20	–	–

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 1 — POWER DERATING

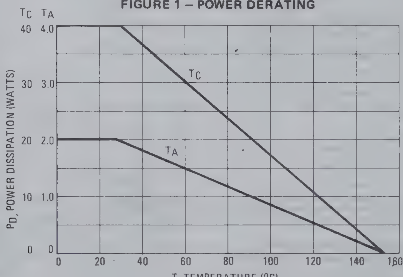
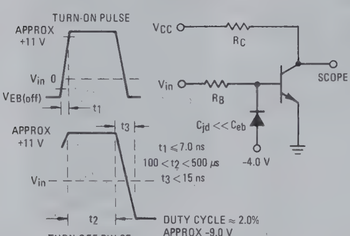


FIGURE 2 — SWITCHING TIME EQUIVALENT CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS.

FIGURE 3 — TURN-ON TIME

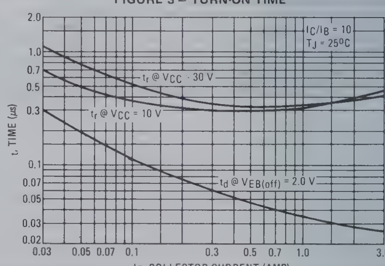


FIGURE 4 — THERMAL RESPONSE

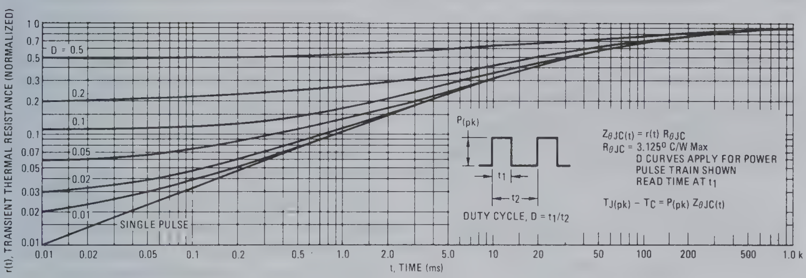
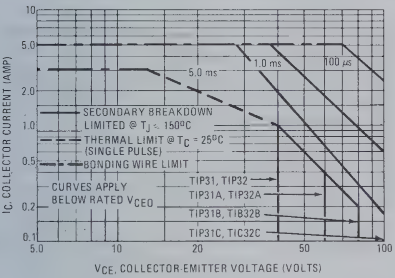


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — TURN-OFF TIME

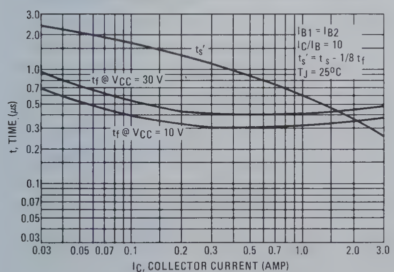


FIGURE 7 — CAPACITANCE

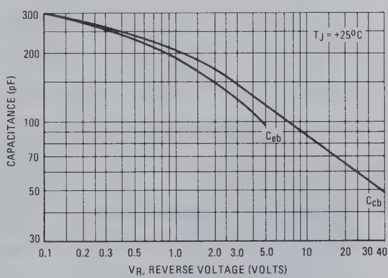


FIGURE 8 – DC CURRENT GAIN

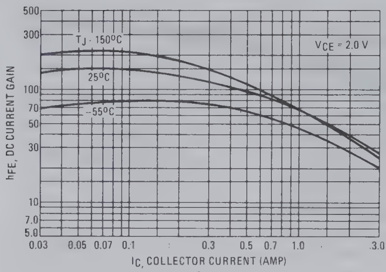


FIGURE 9 – COLLECTOR SATURATION REGION

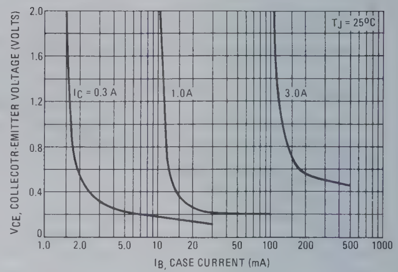


FIGURE 10 – "ON" VOLTAGES

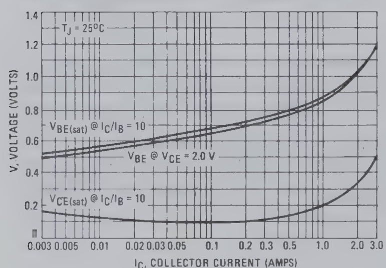


FIGURE 11 – TEMPERATURE COEFFICIENTS

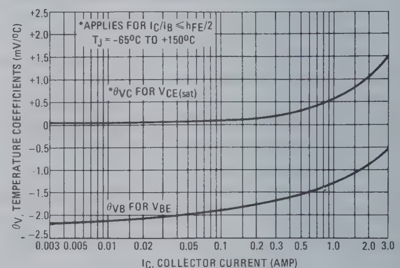


FIGURE 12 – COLLECTOR CUT-OFF REGION

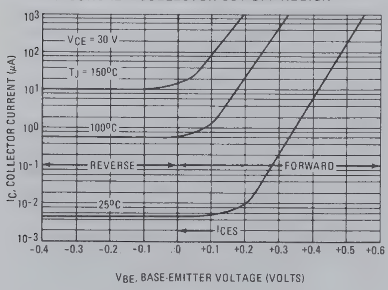
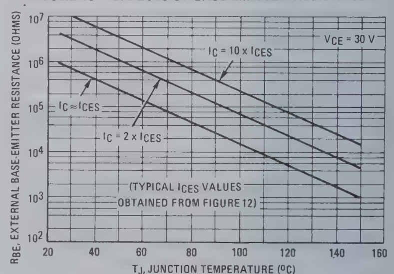


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



MOTOROLA

NPN TIP33, TIP33A, TIP33B, TIP33C
PNP TIP34, TIP34A, TIP34B, TIP34C

1.3

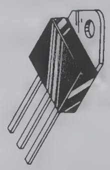
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . for general-purpose power amplifier and switching applications.

- 10 A Collector Current
- Low Leakage Current — I_{CEO} = 0.7 mA @ 30 and 60 V
- Excellent dc Gain — h_{FE} = 40 Typ @ 3.0 A
- High Current Gain Bandwidth Product — h_{fe} = 3.0 min @ I_C = 0.5 A, f = 1.0 MHz

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

40-100 VOLTS
80 WATTS



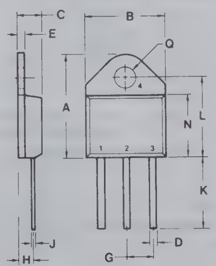
MAXIMUM RATINGS

Rating	Symbol	TIP33 TIP34	TIP33A TIP34A	TIP33B TIP34B	TIP33C TIP34C	Unit
Collector-Emitter Voltage	V_{CEO}	40 V	60 V	80 V	100 V	Vdc
Collector-Base Voltage	V_{CB}	40 V	60 V	80 V	100 V	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current — Continuous Peak (1)	I_C	10 15				Adc
Base Current — Continous	I_B	3.0				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Junction-To-Free-Air Thermal Resistance	$R_{\theta JA}$	35.7	°C/W

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle ≤ 10%.

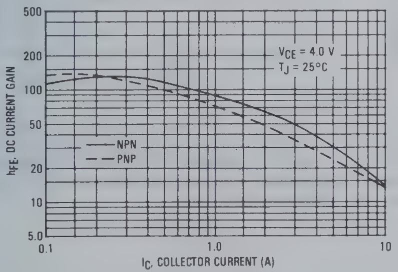


STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

FIGURE 1 — DC CURRENT GAIN



1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mA, I_B = 0)	TIP33, TIP34	BV_{CEO}	40	—	Vdc
	TIP33A, TIP34A		60	—	
	TIP33B, TIP34B		80	—	
	TIP33C, TIP34C		100	—	
Collector-Emitter Cutoff Current (V_{CE} = 30 V, I_B = 0)	TIP33, TIP33A, TIP34, TIP34A	I_{CEO}	—	0.7	mA
(V_{CE} = 60 V, I_B = 0)	TIP33B, TIP33C, TIP34B, TIP34C		—	0.7	
Collector-Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)		I_{CES}	—	0.4	mA
Emitter-Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)		I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 A, V_{CE} = 4.0 V)		h_{FE}	40	—	—
(I_C = 3.0 A, V_{CE} = 4.0 V)			20	100	
Collector-Emitter Saturation Voltage (I_C = 3.0 A, I_B = 0.3 A)		$V_{CE(sat)}$	—	1.0	Vdc
(I_C = 10 A, I_B = 2.5 A)			—	4.0	
Base-Emitter On Voltage (I_C = 3.0 A, V_{CE} = 4.0 V)		$V_{BE(on)}$	—	1.6	Vdc
(I_C = 10 A, V_{CE} = 4.0 V)			—	3.0	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 0.5 A, V_{CE} = 10 V, f = 1.0 kHz)		h_{fe}	20	—	—
Current-Gain—Bandwidth Product (2) (I_C = 0.5 A, V_{CE} = 10 V, f = 1.0 MHz)		f_T	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

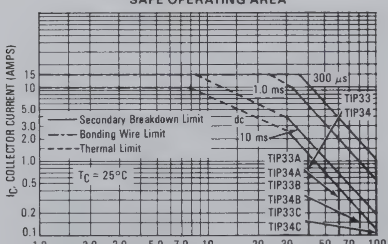
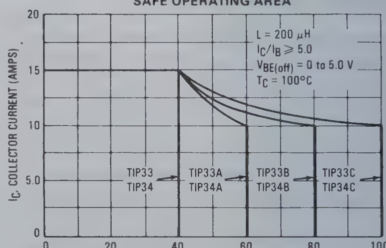


FIGURE 3 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



FORWARD BIAS

The Forward Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during forward bias. The data is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%, and must be derated thermally for T_C > 25°C.

REVERSE BIAS

The Reverse Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during reverse biased turn-off. This rating is verified under clamped conditions so the device is never subjected to an avalanche mode.

MOTOROLA

NPN	PNP
TIP35	TIP36
TIP35A	TIP36A
TIP35B	TIP36B
TIP35C	TIP36C

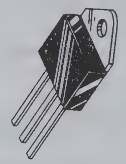
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

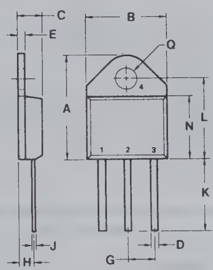
. . . for general-purpose power amplifier and switching applications.

- 25 A Collector Current
- Low Leakage Current — I_{CEO} = 1.0 mA @ 30 and 60 V
- Excellent dc Gain — h_{FE} = 40 Typ @ 15 A
- High Current Gain Bandwidth Product — (h_{fe} = 3.0 min @ I_C = 1.0 A, f = 1.0 MHz

25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

40-100 VOLTS
125 WATTS





STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
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C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

MAXIMUM RATINGS

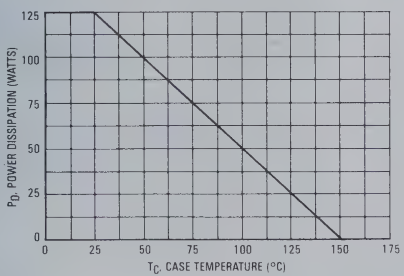
Rating	Symbol	TIP35 TIP36	TIP35A TIP36A	TIP35B TIP36B	TIP35C TIP36C	Unit
Collector-Emitter Voltage	V_{CEO}	40 V	60 V	80 V	100 V	Vdc
Collector-Base Voltage	V_{CB}	40 V	60 V	80 V	100 V	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current — Continuous Peak (1)	I_C	← 25 → ← 40 →				Adc
Base Current — Continous	I_B	← 5.0 →				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 → ← 1.0 →				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C
Unclamped Inductive Load	E_{SB}	90				mJ

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Junction-To-Free-Air Thermal Resistance	$R_{\theta JA}$	35.7	°C/W

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle ≤ 10%.

FIGURE 1 — POWER DERATING

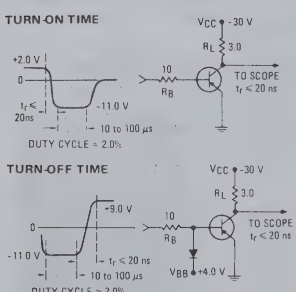


ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mA, I_B = 0)	BV_{CEO}			Vdc
TIP35, TIP36		40	—	
TIP35A, TIP36A		60	—	
TIP35B, TIP36B		80	—	
TIP35C, TIP36C		100	—	
Collector-Emitter Cutoff Current	I_{CEO}			mA
(V_{CE} = 30 V, I_B = 0) TIP35, TIP35A, TIP36, TIP36A		—	1.0	
(V_{CE} = 60 V, I_B = 0) TIP35B, TIP35C, TIP36B, TIP36C		—	1.0	
Collector-Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)	I_{CES}	—	0.7	mA
Emitter-Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)	I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			—
(I_C = 1.5 A, V_{CE} = 4.0 V)		25	—	
(I_C = 15 A, V_{CE} = 4.0 V)		15	75	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 15 A, I_B = 1.5 A)		—	1.8	
(I_C = 25 A, I_B = 5.0 A)		—	4.0	
Base-Emitter On Voltage	$V_{BE(on)}$			Vdc
(I_C = 15 A, V_{CE} = 4.0 V)		—	2.0	
(I_C = 25 A, V_{CE} = 4.0 V)		—	4.0	
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 kHz)	h_{fe}	25	—	—
Current-Gain—Bandwidth Product (2) (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 MHz)	f_T	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2.0%
(2) $f_T = [h_{fe}] \cdot f_{test}$

FIGURE 2 — SWITCHING TIME EQUIVALENT TEST CIRCUITS



FOR CURVES OF FIGURES 3 & 4, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES.

FIGURE 3 — TURN-ON TIME

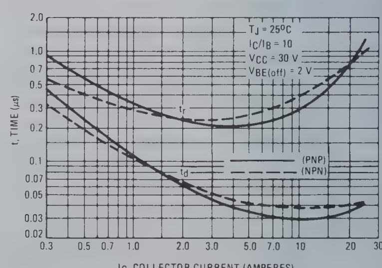


FIGURE 4 — TURN-OFF TIME

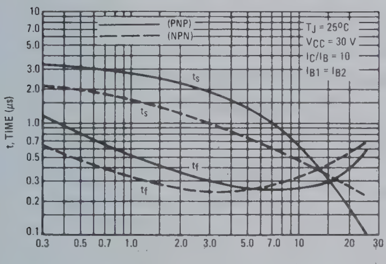
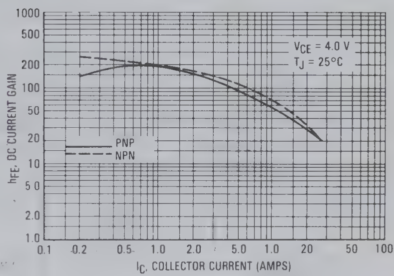


FIGURE 5 — DC CURRENT GAIN



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.

FIGURE 6 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

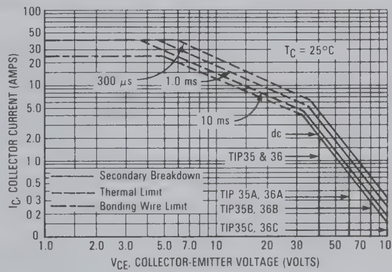
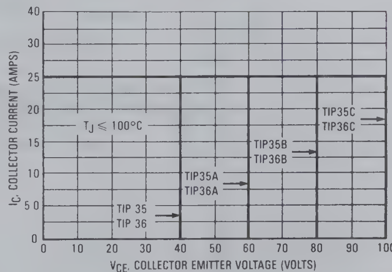
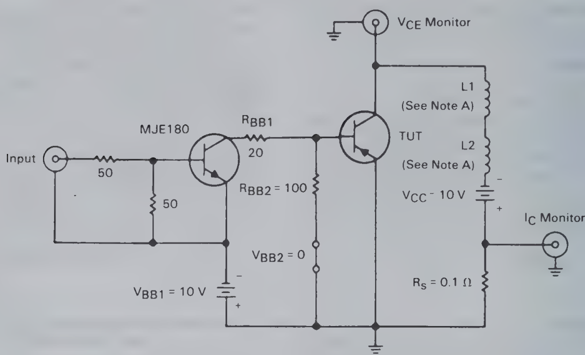


FIGURE 7 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

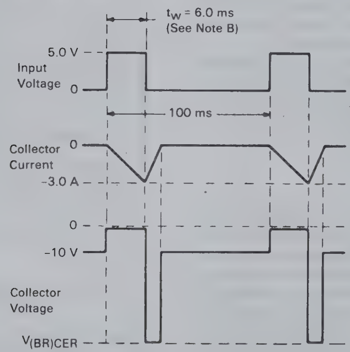


1.3

FIGURE 8 — INDUCTIVE LOAD SWITCHING



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES:

A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C-2688, or equivalent.
B. Input pulse width is increased until $I_{CM} = -3.0$ A.
C. For NPN, reverse all polarities.

NPN TIP41 TIP41A TIP41B TIP41C
PNP TIP42 TIP42A TIP42B TIP42C

MOTOROLA

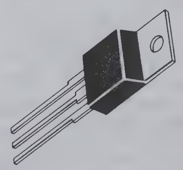
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc (Min) — TIP41, TIP42
  = 60 Vdc (Min) — TIP41A, TIP42A
  = 80 Vdc (Min) — TIP41B, TIP42B
  = 100 Vdc (Min) — TIP41C, TIP42C
- High Current Gain — Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220 AB Package
- TO-66 Leadform Also Available

6 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

40-60-80-100 VOLTS
65 WATTS



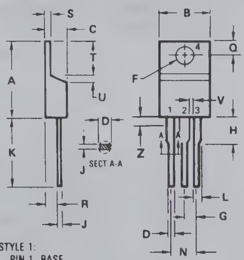
*MAXIMUM RATINGS

Rating	Symbol	TIP41 TIP42	TIP41A TIP42A	TIP41B TIP42B	TIP41C TIP42C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current Continuous	I_C	6				Adc
Peak		10				
Base Current	I_B	2.0				Adc
Total Power Dissipation @ $T_C = 25^oC$	P_D	65				Watts
Derate above 25^oC		0.52				$W/^oC$
Total Power Dissipation @ $T_A = 25^oC$	P_D	2.0				Watts
Derate above 25^oC		0.016				$W/^oC$
Unclamped Inductive Load Energy (1)	E	62.5				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^oC/W$

(1) I_C = 2.5 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10V, R_{BE} = 100 Ω.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	$V_{CEO(sus)}$	40 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	TIP41, TIP41A, TIP42, TIP42A TIP41B, TIP41C, TIP42B, TIP42C	I_{CEO}	– –	0.7 0.7	mAdc
Collector Cutoff Current (V_{CE} = 40 Vdc, V_{EB} = 0) (V_{CE} = 60 Vdc, V_{EB} = 0) (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	I_{CES}	– – – –	400 400 400 400	µAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	30 15	– 75	–
Collector-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 600 mAdc)		$V_{CE(sat)}$	–	1.5	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		$\|h_{fe}\|$	20	–	–

(1) Pulse Test: Pulsewidth ≤ 300 µs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 1 — POWER DERATING

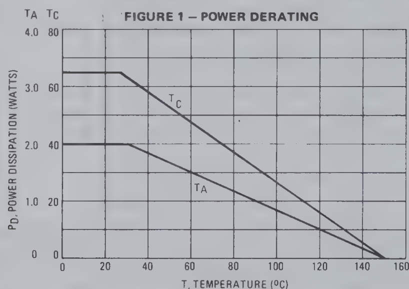


FIGURE 2 — SWITCHING TIME TEST CIRCUIT

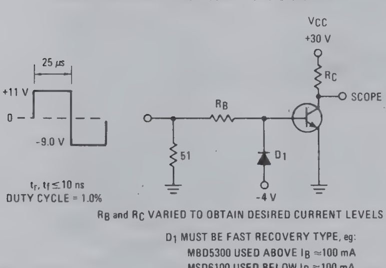


FIGURE 3 — TURN-ON TIME

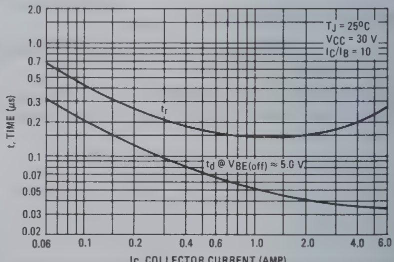


FIGURE 4 – THERMAL RESPONSE

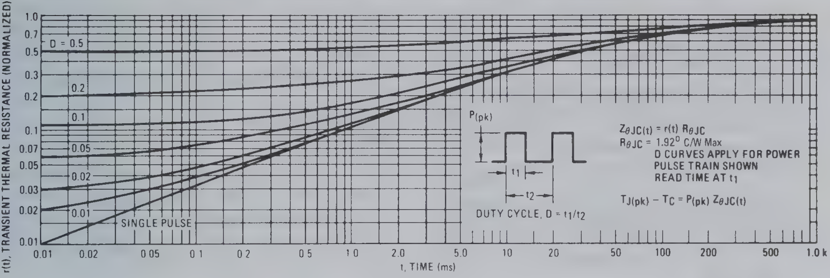
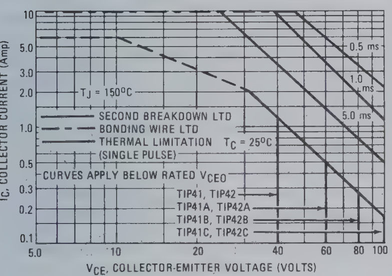


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

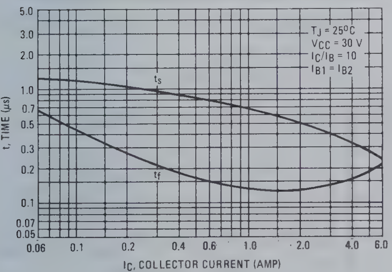


FIGURE 7 – CAPACITANCE

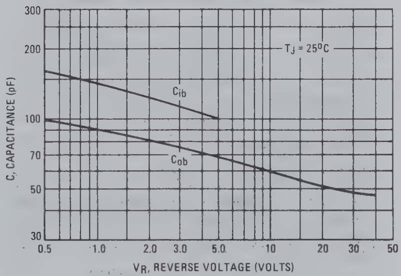


FIGURE 8 — DC CURRENT GAIN

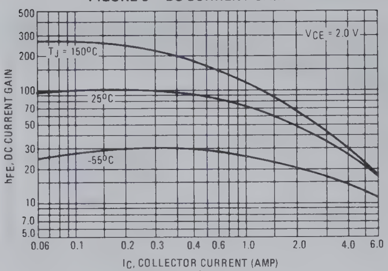


FIGURE 9 — COLLECTOR SATURATION REGION

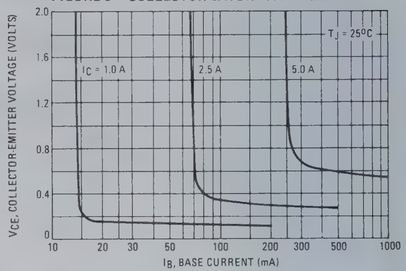


FIGURE 10 — "ON" VOLTAGES

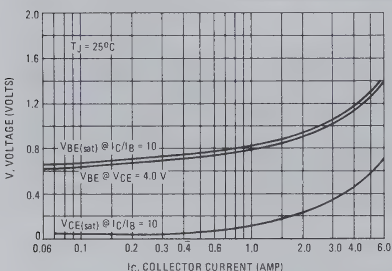


FIGURE 11 — TEMPERATURE COEFFICIENTS

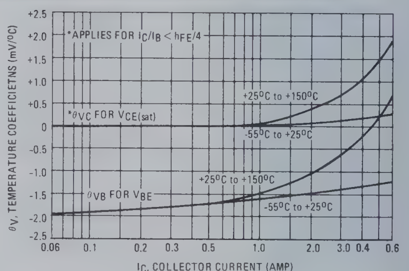


FIGURE 12 — COLLECTOR CUT-OFF REGION

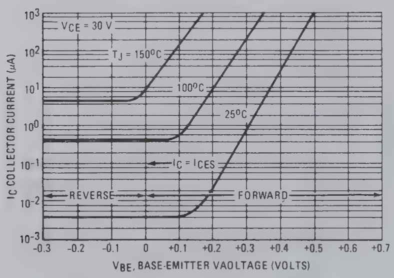
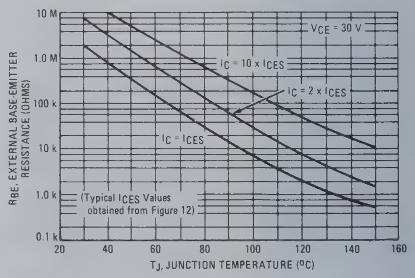


FIGURE 13 — EFFECTS OF BASE-EMITTER RESISTANCE



TIP47 TIP48 TIP49 TIP50

MOTOROLA

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

. . . designed for line operated audio output amplifier, Switchmode power supply drivers and other switching applications.

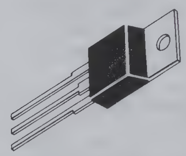
- 250 V to 400 V (Min) — $V_{CEO(sus)}$
- 1 A Rated Collector Current
- Popular TO-220 Plastic Package
- TO-66 Leadform Available

1.0 AMPERE

POWER TRANSISTORS
NPN SILICON

250-300-350-400 VOLTS
40 WATTS

1.3



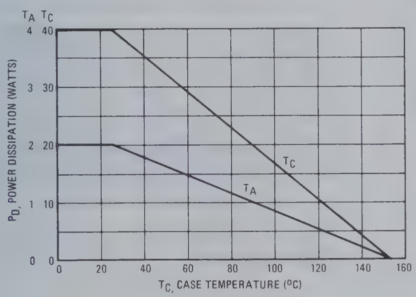
MAXIMUM RATINGS

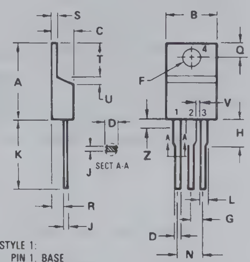
Rating	Symbol	TIP47	TIP48	TIP49	TIP50	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	400	Vdc
Collector-Base Voltage	V_{CB}	350	400	450	500	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current — Continuous Peak	I_C	← 1.0 → ← 2.0 →				Adc
Base Current	I_B	← 0.6 →				Adc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	← 40 → ← 0.32 →				Watts $W/^\circ C$
Total Power Dissipation @ $T_A = 25^\circ C$ Derate above $25^\circ C$	P_D	← 2.0 → ← 0.016 →				Watts $W/^\circ C$
Unclamped Inducting Load Energy (See Figure 8)	E	← 20 →				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +150 →				$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	$^\circ C/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

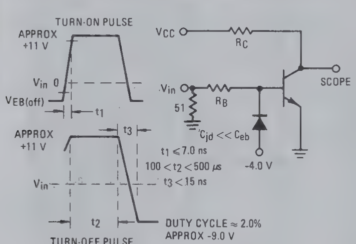
1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)	TIP47	$V_{CEO(sus)}$	250	–	Vdc
(I_C = 30 mAdc, I_B = 0)	TIP48		300	–	
	TIP49		350	–	
	TIP50		400	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 150 Vdc, I_B = 0)	TIP47		–	1.0	
(V_{CE} = 200 Vdc, I_B = 0)	TIP48		–	1.0	
(V_{CE} = 250 Vdc, I_B = 0)	TIP49		–	1.0	
(V_{CE} = 300 Vdc, I_B = 0)	TIP50		–	1.0	
Collector Cutoff Current		I_{CES}			mAdc
(V_{CE} = 350 Vdc, V_{BE} = 0)	TIP47		–	1.0	
(V_{CE} = 400 Vdc, V_{BE} = 0)	TIP48		–	1.0	
(V_{CE} = 450 Vdc, V_{BE} = 0)	TIP49		–	1.0	
(V_{CE} = 500 Vdc, V_{BE} = 0)	TIP50		–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.3 Adc, V_{CE} = 10 Vdc)			30	150	
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)			10	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	–	1.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)		f_T	10	–	MHz
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

(1) Pulse Test: Pulsewidth ⩽ 300 μs, Duty Cycle ⩽ 2.0%.

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS.

FIGURE 3 – TURN-ON TIME

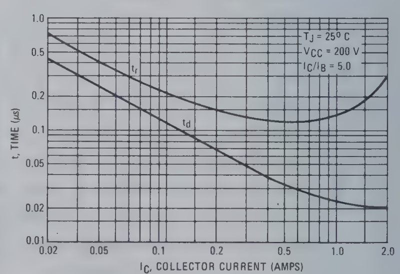


FIGURE 4 — THERMAL RESPONSE

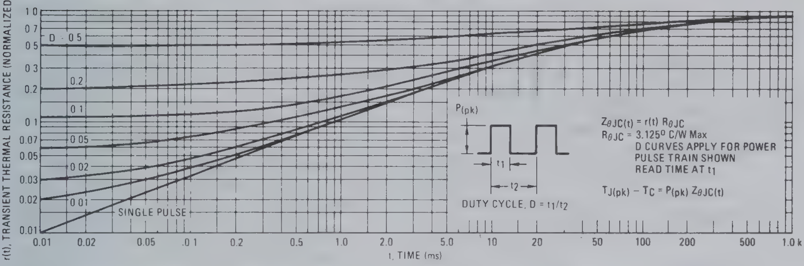
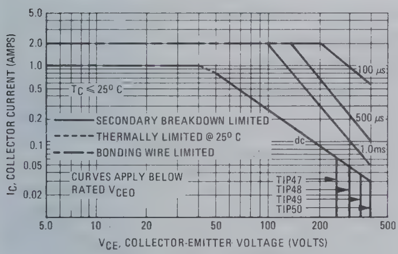


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — TURN-OFF TIME

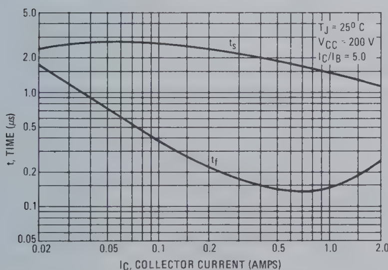


FIGURE 7 — TEMPERATURE COEFFICIENTS

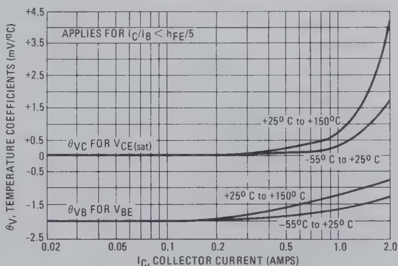
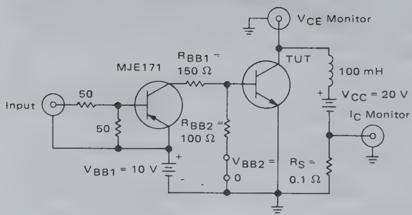
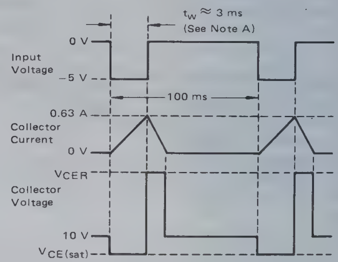


FIGURE 8 — INDUCTIVE LOAD SWITCHING

Test Circuit



Voltage and Current Waveforms



Note A: Input pulse width is increased until I_{CM} = 0.63 A.

FIGURE 9 — DC CURRENT GAIN

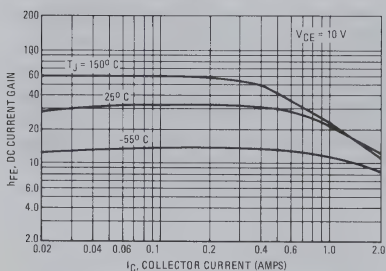
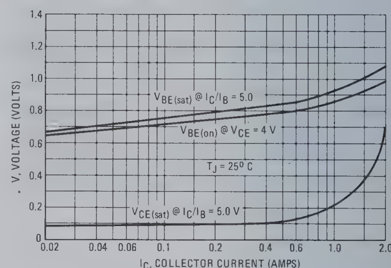


FIGURE 10 — "ON" VOLTAGES



MOTOROLA

NPN | PNP

TIP100 TIP105
TIP101 TIP106
TIP102 TIP107

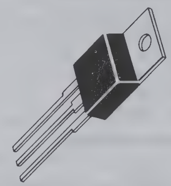
1.3

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP100, TIP105
  = 80 Vdc (Min) — TIP101, TIP106
  = 100 Vdc (Min) — TIP102, TIP107
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 2.5 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
80 WATTS



*MAXIMUM RATINGS

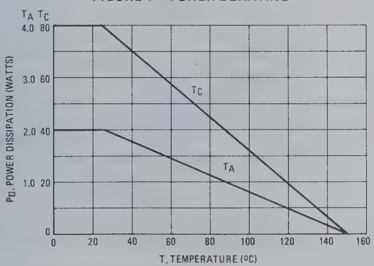
Rating	Symbol	TIP100, TIP105	TIP101, TIP106	TIP102, TIP107	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous / Peak	I_C		8.0 / 15		Adc
Base Current	I_B		1.0		Adc
Total Power Dissipation @ T_C = 25°C / Derate above 25°C	P_D		80 / 0.64		Watts / W/°C
Unclamped Inductive Load Energy (1)	E		30		mJ
Total Power Dissipation @ T_A = 25°C / Derate above 25°C	P_D		2.0 / 0.016		Watts / W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150		°C

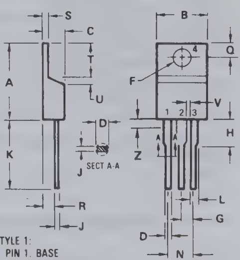
THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1.1 A, L = 50 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

FIGURE 1 — POWER DERATING





STYLE 1:
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2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
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Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	TIP100, TIP105		60	–	
	TIP101, TIP106		80	–	
	TIP102, TIP107		100	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP100, TIP105		–	50	
(V_{CE} = 40 Vdc, I_B = 0)	TIP101, TIP106		–	50	
(V_{CE} = 50 Vdc, I_B = 0)	TIP102, TIP107		–	50	
Collector Cuttoff Current		I_{CBO}			μAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP100, TIP105		–	50	
(V_{CB} = 80 Vdc, I_E = 0)	TIP101, TIP106		–	50	
(V_{CB} = 100 Vdc, I_E = 0)	TIP102, TIP107		–	50	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	8.0	mAdc
ON-CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			1000	20,000	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)			200	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 6.0 mAdc)			–	2.0	
(I_C = 8.0 Adc, I_B = 80 mAdc)			–	2.5	
Base-Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	–
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP105, TIP106, TIP107		–	300	
	TIP100, TIP101, TIP102		–	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

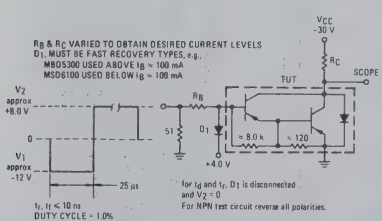


FIGURE 3 – SWITCHING TIMES

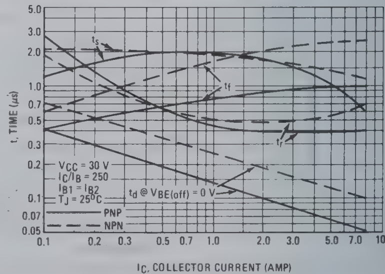


FIGURE 4 – THERMAL RESPONSE

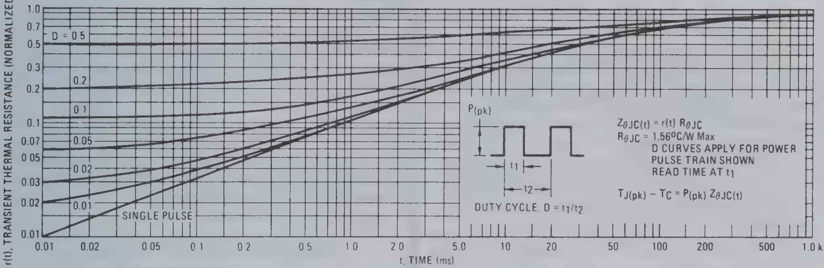
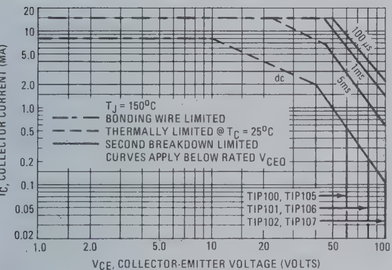


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

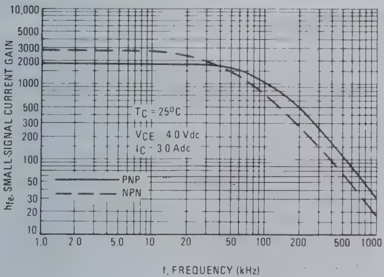
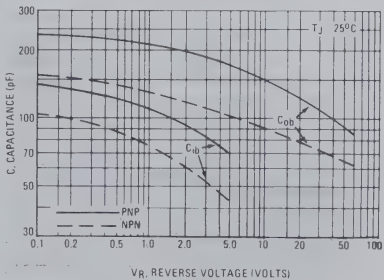


FIGURE 7 – CAPACITANCE



1.3

NPN
TIP100, TIP101, TIP102

PNP
TIP105, TIP106, TIP107

FIGURE 8 — DC CURRENT GAIN

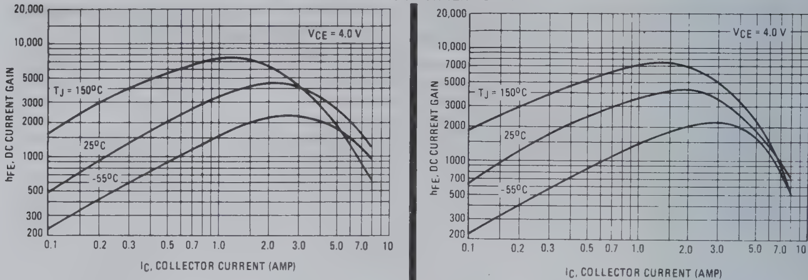


FIGURE 9 — COLLECTOR SATURATION REGION

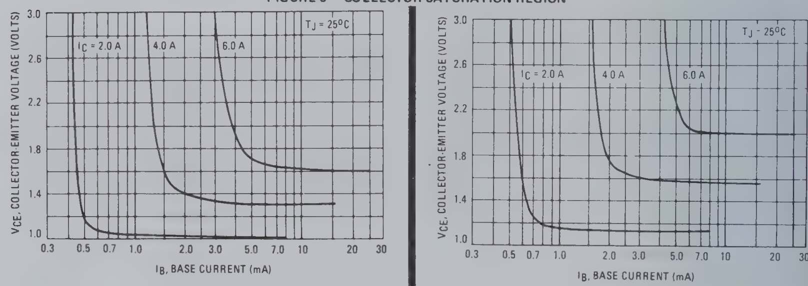
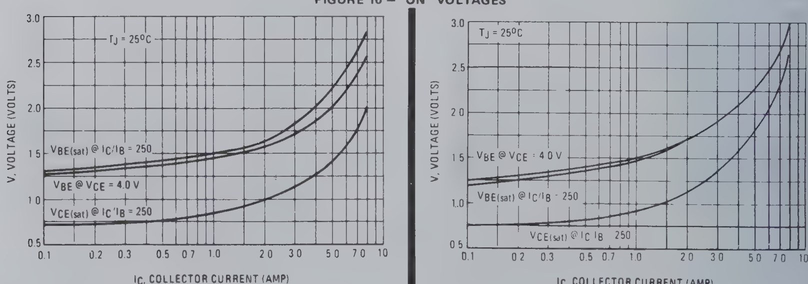


FIGURE 10 — "ON" VOLTAGES



MOTOROLA

NPN | PNP

TIP110 TIP115
TIP111 TIP116
TIP112 TIP117

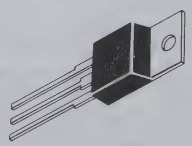
1.3

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 1.0 Adc
- Collector-Emitter Sustaining Voltage — @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP110, TIP115
  = 80 Vdc (Min) — TIP111, TIP116
  = 100 Vdc (Min) — TIP112, TIP117
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C = 2.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON
2 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
50 WATTS



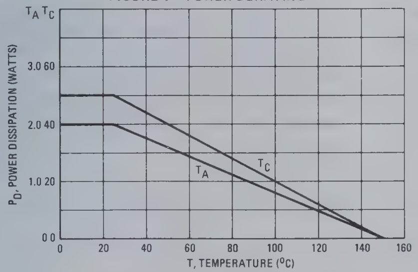
*MAXIMUM RATINGS

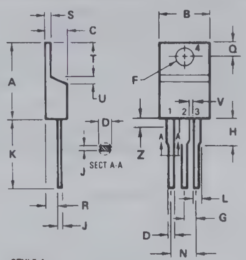
Rating	Symbol	TIP110, TIP115	TIP111, TIP116	TIP112, TIP117	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 2.0 → ← 4.0 →			Adc
Base Current	I_B	← 50 →			mAdc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	← 50 → ← 0.4 →			Watts $W/^oC$
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	← 2.0 → ← 0.016 →			Watts $W/^oC$
Unclamped Inductive Load Energy — Figure 13	E	← 25 →			mJ
Operating and Storage Junction,	T_J, T_{stg}	← −65 to +150 →			^oC

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^oC/W$

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

TIP110, TIP111, TIP112, NPN, TIP115, TIP116, TIP117, PNP

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	TIP110, TIP115		60	–	
	TIP111, TIP116		80	–	
	TIP112, TIP117		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP110, TIP115		–	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	TIP111, TIP116		–	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	TIP112, TIP117		–	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP110, TIP115		–	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	TIP111, TIP116		–	1.0	
(V_{CB} = 100 Vdc, I_E = 0)	TIP112, TIP117		–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			1000	–	
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)			500	–	
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 8.0 mAdc)		$V_{CE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	25	–	–
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP115, TIP116, TIP117		–	200	
	TIP110, TIP111, TIP112		–	100	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

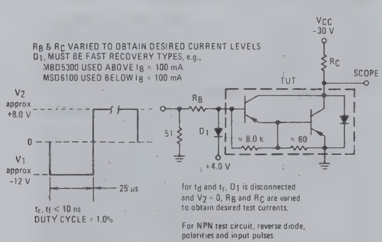


FIGURE 3 – SWITCHING TIMES

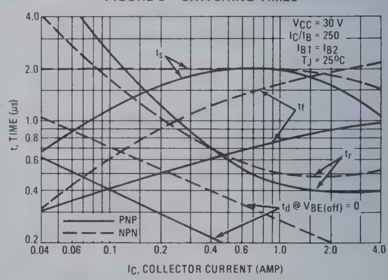
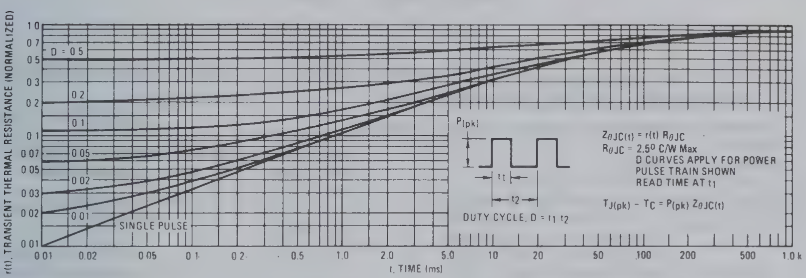


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 5 – TIP115, 116, 117

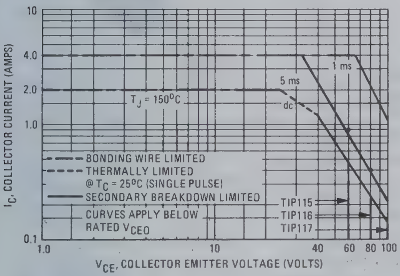
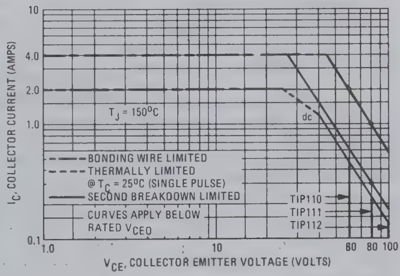


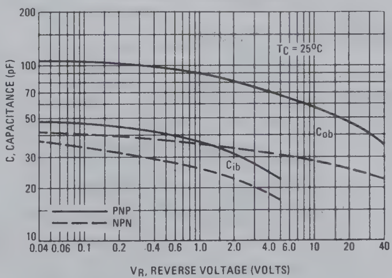
FIGURE 6 – TIP110, 111, 112



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 – CAPACITANCE



NPN PNP

TIP120 TIP125
TIP121 TIP126
TIP122 TIP127

MOTOROLA

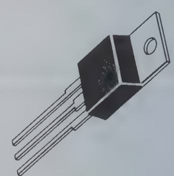
1.3

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP120, TIP125
  = 80 Vdc (Min) — TIP121, TIP126
  = 100 Vdc (Min) — TIP122, TIP127
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
65 WATTS



*MAXIMUM RATINGS

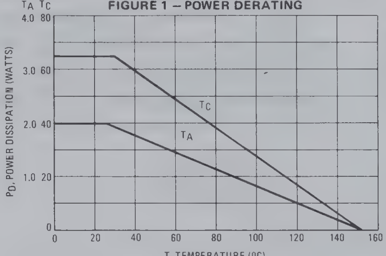
Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 5.0 → ← 8.0 →			Adc
Base Current	I_B	← 120 →			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 65 → ← 0.52 →			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 0.016 →			Watts W/°C
Unclamped Inductive Load Energy (1)	E	← 50 →			mJ
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	← −65 to +150 →			°C

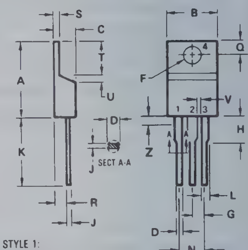
THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1 A, L = 100 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	TIP120, TIP125		60	–	
	TIP121, TIP126		80	–	
	TIP122, TIP127		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP120, TIP125		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	TIP121, TIP126		–	0.5	
(V_{CE} = 50 Vdc, I_B = 0)	TIP122, TIP127		–	0.5	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP120, TIP125		–	0.2	
(V_{CB} = 80 Vdc, I_E = 0)	TIP121, TIP126		–	0.2	
(V_{CB} = 100 Vdc, I_E = 0)	TIP122, TIP127		–	0.2	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 3.0 Vdc)			1000	–	
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			1000	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			–	2.0	
(I_C = 5.0 Adc, I_B = 20 mAdc)			–	4.0	
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	–
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP125, TIP126, TIP127		–	300	
	TIP120, TIP121, TIP122		–	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

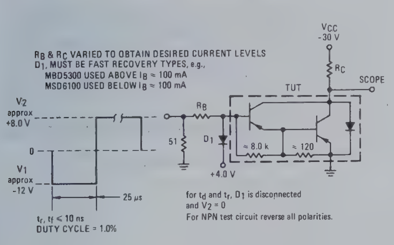
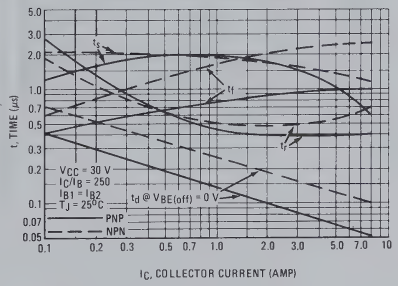


FIGURE 3 – SWITCHING TIMES



1.3

FIGURE 4 – THERMAL RESPONSE

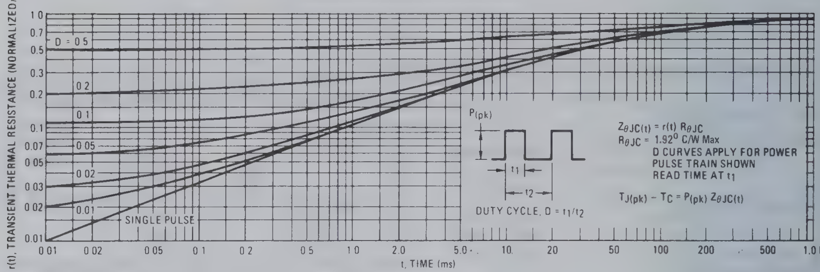
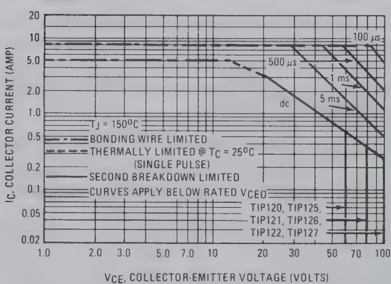


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

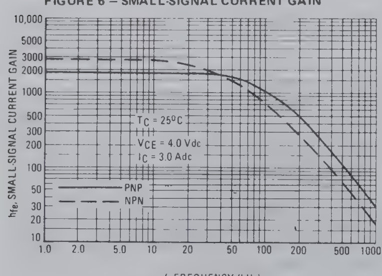
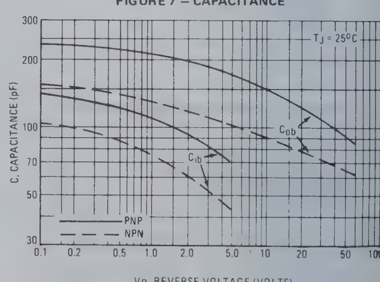


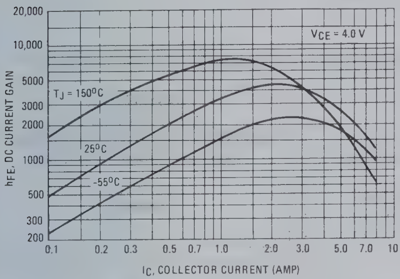
FIGURE 7 – CAPACITANCE



1.3

NPN TIP120, TIP121, TIP122	PNP TIP125, TIP126, TIP127

FIGURE 8 — DC CURRENT GAIN



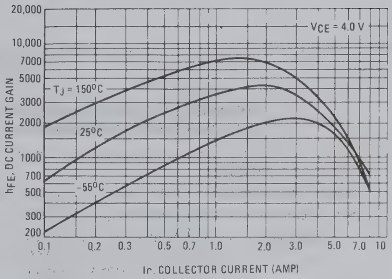
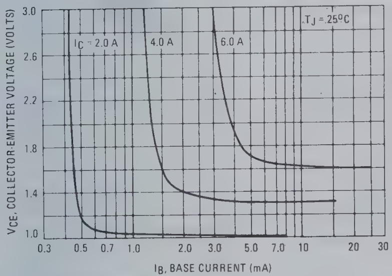


FIGURE 9 — COLLECTOR SATURATION REGION



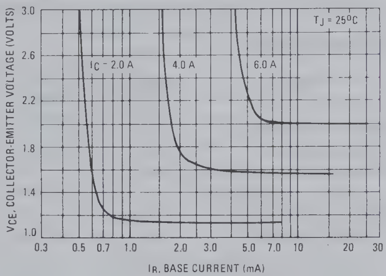
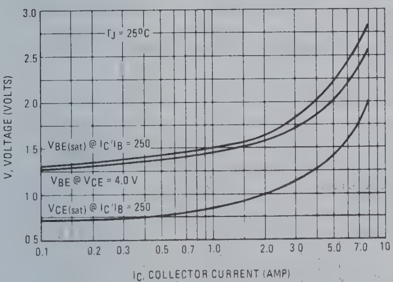
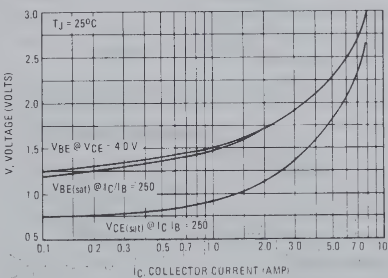


FIGURE 10 — "ON" VOLTAGES





NPN TIP140 TIP141 TIP142 — PNP TIP145 TIP146 TIP147

NPN	PNP
TIP140	TIP145
TIP141	TIP146
TIP142	TIP147

MOTOROLA

1.3

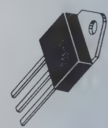
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain — Min $h_{FE} = 1000$ @ $I_C = 5$ A, $V_{CE} = 4$ V
- Collector-Emitter Sustaining Voltage — @ 30 mA
  $V_{CEO(sus)} =$ 60 Vdc (Min) — TIP140, TIP145
  80 Vdc (Min) — TIP141, TIP146
  100 Vdc (Min) — TIP142, TIP147
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor

10 AMPERE DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

60-100 VOLTS
125 WATTS



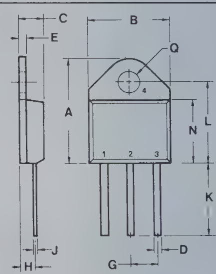
MAXIMUM RATINGS

Rating	Symbol	TIP140 TIP145	TIP141 TIP146	TIP142 TIP147	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous Peak (1)	I_C		10 15		Adc
Base Current — Continuous	I_B		0.5		Adc
Total Device Dissipation @ $T_C = 25°C$	P_D		125		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Case to Ambient	$R_{\theta JA}$	35.7	°C/W

(1) 5 ms, ≤10% Duty Cycle

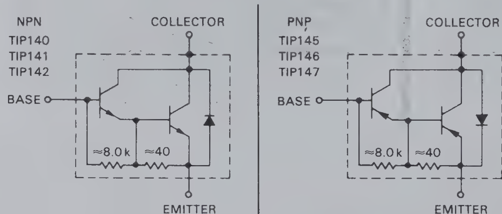


STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

CASE 340-01
TO-218AC

DARLINGTON SCHEMATICS

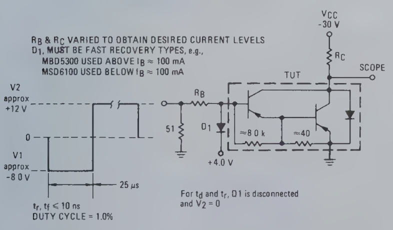


ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$				Vdc
(I_C = 30 mA, I_B = 0)	TIP140, TIP145		60	—	—	
	TIP141, TIP146		80	—	—	
	TIP142, TIP147		100	—	—	
Collector Cutoff Current		I_{CEO}				mA
(V_{CE} = 30 Vdc, I_B = 0)	TIP140, TIP145		—	—	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	TIP141, TIP146		—	—	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	TIP142, TIP147		—	—	2.0	
Collector Cutoff Current		I_{CBO}				mA
(V_{CB} = 60 V, I_E = 0)	TIP140, TIP145		—	—	1.0	
(V_{CB} = 80 V, I_E = 0)	TIP141, TIP146		—	—	1.0	
(V_{CB} = 100 V, I_E = 0)	TIP142, TIP147		—	—	1.0	
Emitter Cutoff Current V_{BE} = 5.0 V		I_{EBO}	—	—	2.0	mA
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				—
(I_C = 5.0 A, V_{CE} = 4.0 V)			1000	—	—	
(I_C = 10 A, V_{CE} = 4.0 V)			500	—	—	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5.0 A, I_B = 10 mA)			—	—	2.0	
(I_C = 10 A, I_B = 40 mA)			—	—	3.0	
Base-Emitter Saturation Voltage (I_C = 10 A, I_B = 40 mA)		$V_{BE(sat)}$	—	—	3.5	Vdc
Base-Emitter On Voltage (I_C = 10 A, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	—	3.0	Vdc
SWITCHING CHARACTERISTICS						
Resistive Load (See Figure 1)						
Delay Time	(V_{CC} = 30 V, I_C = 5.0 A,	t_d	—	0.15	—	μs
Rise Time	I_B = 20 mA, Duty Cycle ≤ 2.0%,	t_r	—	0.55	—	μs
Storage Time	$I_{B1} = I_{B2}$, R_C & R_B Varied, T_J = 25°C)	t_s	—	2.5	—	μs
Fall Time		t_f	—	2.5	—	μs

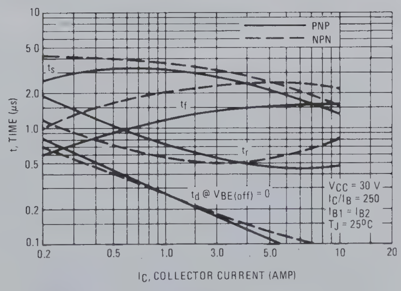
(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

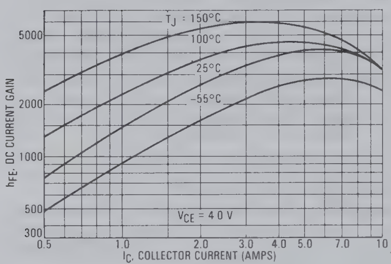
FIGURE 2 — SWITCHING TIMES



TYPICAL CHARACTERISTICS

NPN TIP140, TIP141, TIP142	PNP TIP145, TIP146, TIP147

FIGURE 3 — DC CURRENT GAIN versus COLLECTOR CURRENT



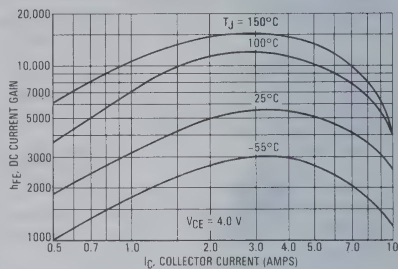
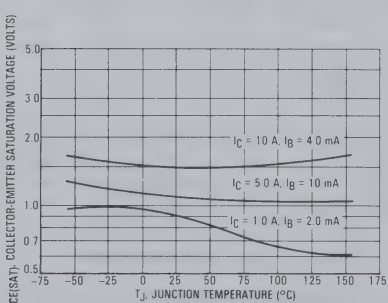


FIGURE 4 — COLLECTOR-EMITTER SATURATION VOLTAGE



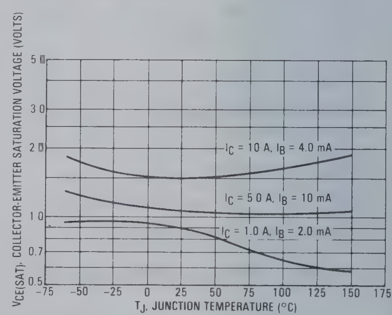
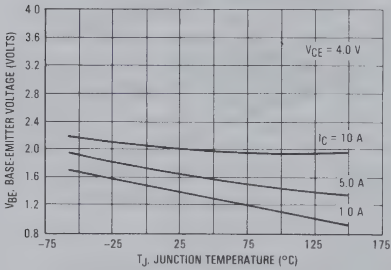
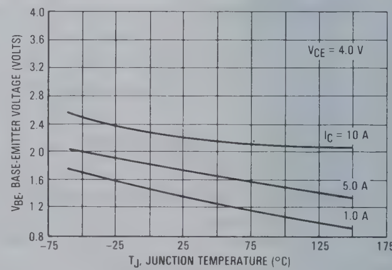


FIGURE 5 — BASE-EMITTER VOLTAGE





ACTIVE-REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — ACTIVE-REGION SAFE OPERATING AREA

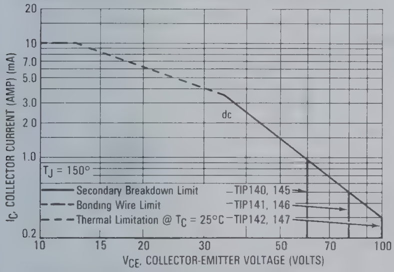


FIGURE 7 — UNCLAMPED INDUCTIVE LOAD

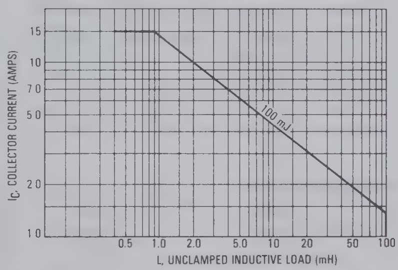
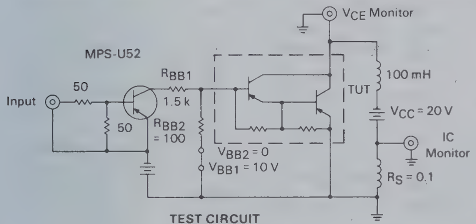
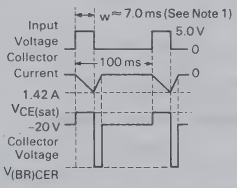


FIGURE 8 — INDUCTIVE LOAD



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTE 1: Input pulse width is increased until $I_{CM} = 1.42$ A.
NOTE 2: For NPN test circuit reverse polarities.

FIGURE 9 — MAGNITUDE OF COMMON EMITTER SMALL-SIGNAL SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO

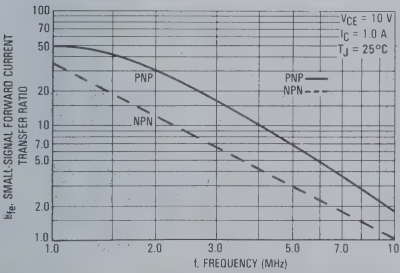
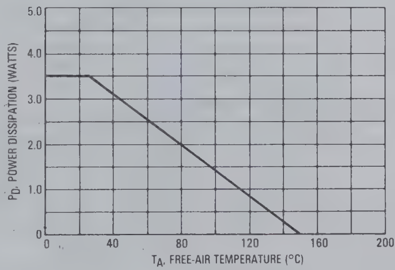


FIGURE 10 — FREE-AIR TEMPERATURE POWER DERATING



NPN **PNP**
TIP3055 **TIP2955**

MOTOROLA

1.3

COMPLEMENTARY SILICON POWER TRANSISTORS

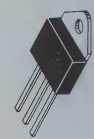
. . . designed for general-purpose switching and amplifier applications.

- DC Current Gain — h_{FE} = 20–70 @ I_C = 4.0 Adc
- Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4.0 Adc
- Excellent Safe Operating Area

15 AMPERE POWER TRANSISTORS

COMPLEMENTARY SILICON

60 VOLTS
90 WATTS

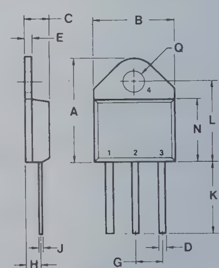


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Emitter Voltage	V_{CER}	70	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current	I_B	7.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	90 0.72	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.39	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	35.7	°C/W

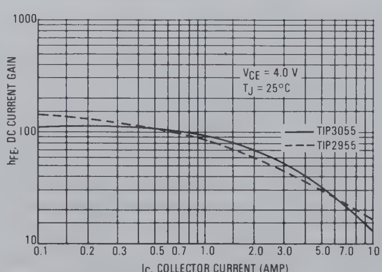


STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
(TO-218AC)

FIGURE 1 — DC CURRENT GAIN



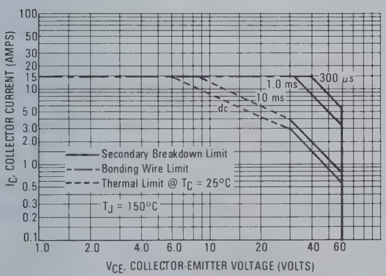
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 70 Vdc, R_{BE} = 100 Ohms)	I_{CER}	—	1.0	mAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			—
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		20	70	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)		5.0	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 400 mAdc)		—	1.1	
(I_C = 10 Adc, I_B = 3.3 Adc)		—	3.0	
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.8	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 30 Vdc, t = 1.0 s; Nonrepetitive)	$I_{s/b}$	3.0	—	Adc
DYNAMIC CHARACTERISTICS				
Current Gain—Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	—	MHz
Small-Signal Current Gain (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	h_{fe}	15	—	kHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2.0%.

Note: For additional design curves, refer to electrical characteristics curves of 2N3055

FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature.

THYRISTORS

TRIGGERED SWITCHES FOR YOUR POWER HANDLING APPLICATION

Thyristors and their trigger devices can take numerous forms, but they share these characteristics:

- They are "open circuits," capable of withstanding rated voltage until triggered.
- They become low-impedance current paths when triggered, and remain so, even after the trigger source is removed, until current through that path stops, or is reduced below a minimum "holding" level.

The regenerative action which "holds" a thyristor in the "on" state is due to multiple layers of opposite P and N silicon, in which part of the load current through the thyristor is injected to supplement the trigger current, and to sustain conduction when the trigger is removed. This characteristic, coupled with the thyristor's low "on resistance," makes it possible to control a portion of each cycle of an ac power waveform into a load in low-dissipation "dimming" or motor speed control applications, to precisely switch capacitive discharge currents in electronic pilot ignition systems, or to efficiently modulate radar systems with high current, fast pulses.

SCRs

Silicon-Controlled Rectifiers (SCRs) are thyristors intended to switch load currents in one direction only, making them useful for dc and half-wave ac applications as well as full-wave applications, in which bidirectional current is routed in one direction through the SCR via a bridge rectifier.

TRIACs

Triacs are bidirectional thyristors, in which a single trigger source turns the device on for load current in either direction. Because they do not require a bridge rectifier in order to handle full-wave ac, triacs are useful in ac power applications that require full source power control capability to be applied to the load.

Trigger Devices

Unijunction Transistors — UJT — are negative resistance, threshold sensitive device especially suited to unidirectional triggering of SCRs, pulse generators, oscillators, and timing circuits.

Programmable Unijunction Transistors — PUT — are similar to the UJT, but capable of adjustable threshold characteristics via a voltage divider.

Bilateral Triggers — DIAC — are low-cost bidirectional trigger which can drive a triac in full-wave ac applications.

Silicon Bidirectional Switches — SBS — are similar to a DIAC but save an added gate electrode for external synchronization.

Optically Coupled Triac Drivers allow bidirectional triac triggering from low-level logic, such as microprocessor outputs, while isolating these sensitive sources by as much as 7500 V from ac line transients.

Motorola Thyristors and Triggers serve a wide variety of applications.

Thyristors

Index and Cross Reference

2.1

The table on the subsequent pages contains an Alphanumeric index of Thyristors currently manufactured and available to the industry.

For devices not manufactured by Motorola, the column headed "Similar" lists units with characteristics that might represent suitable replacements. In cases where such a replacement is contemplated, the Motorola device data sheet should be carefully compared with one for the device being replaced to determine any variations that could affect circuit performance.

INDEX CROSS-REFERENCE

2.1

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
0220100F		C228A	2-179
0220200F		C228B	2-179
0220300F		C228C	2-179
0220400F		C228D	2-179
0220500F		C228E	2-179
0220600F		C228M	2-179
0230100F		C228A	2-179
0230200F		C228B	2-179
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T4101B	T4101B		—
T4101C	T4101C		—
T4101D	T4101D		—
T4101E	T4101E		—
T4101F	T4101F		—
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TY4008		MCR218-6	2-254
TY4010		2N6397	2-161
TY5004		MCR218-7	2-254
TY5008		MCR218-7	2-254
TY5010		MCR220-7	2-161
TY6004		MCR218-8	2-254
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TYAL3815M		MAC15-9	—

Thyristors

Selector Guide

2.2

While all thyristors are, essentially, electronic switches, representing a very high resistance in the off condition and a very low resistance in the "breakover" (on) condition, their applications for the various types are significantly different.

SCRs, for example, will conduct current only in one direction, making them suitable for pulse power control.

TRIACs, in essence, represent inverse parallel connected SCRs and thus can conduct in both directions for the control of ac loads.

C orrespondingly, UJT and PUT Triggers are unidirectional and are normally associated with SCRs, whereas the bidirectional DIACs and SBSs are compatible with TRIACs. The static characteristics curves associated with these components are depicted on page 2-ii together with callouts and definitions related to the most significant parameters associated with each of these components. The range of electrical capabilities of components within each specific group is presented in the corresponding selector guide on the following pages.

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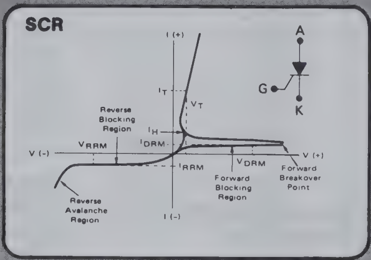
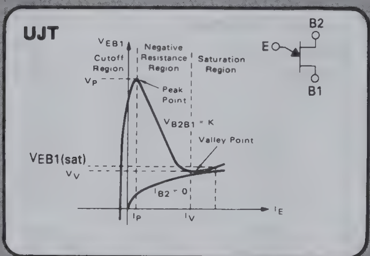
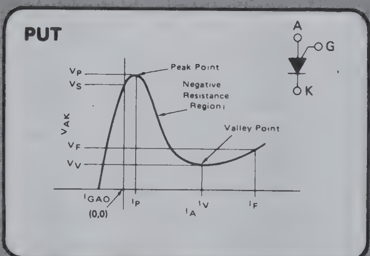
Thyristors

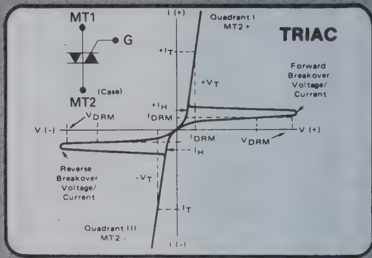
Characteristic Curves

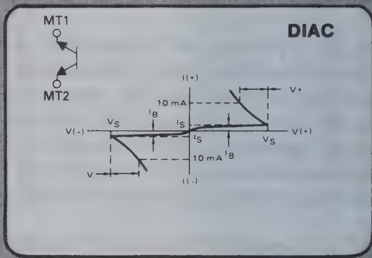
2.2

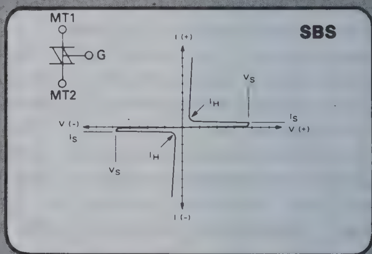


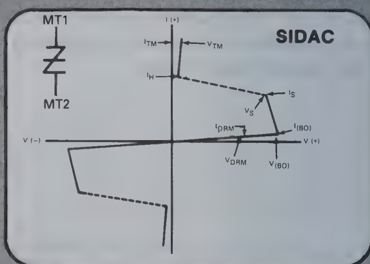










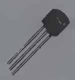


Thyristors — SCRs

Metal/Plastic Packages

0.5 to 55 Amperes RMS
25–800 Volts

NOTE: Industry Standards, with a variety of Custom Specifications and Leadforms available

On-State (RMS) Current							
0.5 AMP	0.8 AMP	1.5 AMPS	1.6 AMPS				
T_C = 65°C	T_C = 58°C	T_C = 50°C	T_C = 80°C	T_C = 85°C			
							
Sensitive Gate				Sensitive Gate			
Case 22-03 TO-206AA (TO-18) Style 6	Case 29-02 TO-226AA (TO-92) Style 10		Case 79-02 TO-205AD (TO-39) Style 3				
MCR202	MCR102 2N5060			2N2322	2N4212	25 V	V_{DRM} V_{RRM}
MCR203	MCR103 2N5061	MCR22-2	2N1595	2N2323	2N4213	50 V	
MCR204	MCR100-3 2N5062	MCR22-3	2N1596	2N2324	2N4214	100 V	
MCR206	MCR100-4 2N5064	MCR22-4	2N1597	2N2326	2N4216	200 V	
	MCR100-5	MCR22-5	2N1598	2N2328	2N4218	300 V	
	MCR100-6	MCR22-6	2N1599	2N2329	2N4219	400 V	
	MCR100-7	MCR22-7				500 V	
	MCR100-8	MCR22-8				600 V	
						700 V	
						800 V	
6.0	10	150(1)	15	15	15	I_{TSM}(Amps) 60 Hz	MAXIMUM ELECTRICAL CHARACTERISTICS
0.2	0.2	0.2	10	0.2	0.1	I_{GT} (mA)	
0.8	0.8	0.8	3.0	0.8	0.8	V_{GT}(V)	
−65 to +125	−65 to +110	−40 to +125	−65 to +125			T_J Operating Range (°C)	

(1) Exponential decay for 1.0 μs, 10 Hz pulse width (CD ignition)

SCRs (continued)

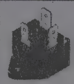
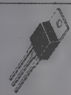
2.2

		On-State (RMS) Current							
		1.6 AMPS	4.0 AMPS		8.0 AMPS				8.0 AMPS
		T_C = 65°C	T_C = 93°C	T_C = 30°C	T_C = 73°C	T_C = 75°C		T_C = 83°C	T_C = 95°C
									
			Sensitive Gate					Sensitive Gate	
		Case 79-02 TO-205AD (TO-39) Style 3	Case 77-04 TO-126 Style 2		Case 90-05 TO-225AB Style 1	Case 221A-02 TO-220AB Style 3			Case 221A-02 TO-220AB Style 3
V_{DRM} / V_{RRM}	25 V	MCR1906-1	MCR106-1 2N6236	C106Y*	MCR3000-1			MCR72-1	
	50 V	MCR1906-2	MCR106-2 2N6237	C106F*	2N4441 MCR3000-2	MCR218-2	C122F1 S2800F	MCR72-2	
	100 V	MCR1906-3	MCR106-3 2N6238	C106A*	MCR3000-3	MCR218-3	C122A1 S2800A	MCR72-3	
	200 V	MCR1906-4	MCR106-4 2N6239	C106B*	2N4442 MCR3000-4	MCR218-4	C122B1 S2800B	MCR72-4	MCR2080-4,A4
	300 V	MCR1906-5	MCR106-5	C106C*	MCR3000-5	MCR218-5	C122C1 S2800C	MCR72-5	MCR2080-5,A5
	400 V	MCR1906-6	MCR106-6 2N6240	C106D*	2N4443 MCR3000-6	MCR218-6	C122D1 S2800D	MCR72-6	MCR2080-6,A6
	500 V	MCR1906-7	MCR106-7	C106E*	MCR3000-7	MCR218-7	C122E1 S2800E	MCR72-7	MCR2080-7,A7
	600 V	MCR1906-8	MCR106-8 2N6241	C106M*	2N4444 MCR3000-8	MCR218-8*	C122M1 S2800M	MCR72-8	MCR2080-8,A8
	700 V				MCR3000-9	MCR218-9	C122S1 S2800S		MCR2080-9,A9
	800 V				MCR3000-10	MCR218-10	C122N1 S2800N		MCR2080-10,A10
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps) 60 Hz	15	25	20 150(1)	80	80	C122/S2800 90/100	100	90
	I_{GT} (mA)	1.0	0.2	0.2	30	15	C122/S2800 25/25	0.2	50
	V_{GT}(V)	1.0	1.0	0.8	1.5	1.5	1.5	1.5	2.5
	T_J Operating Range (°C)	−65 to +110	−40 to +110		−40 to +100	−40 to +125	−40 to +100		−40 to +125

(1) Exponential decay for 1.0 μs, 10 Hz pulse width (CD ignition)
Lead forms available (see page 28)

SCRs (continued)

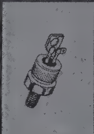
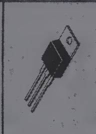
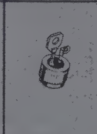
2.2

On-State (RMS) Current									
8.0 AMPS		12 AMPS				12.5 AMPS	15 AMPS		
T_C = 83°C		T_C = 90°C	T_C = 85°C			T_C = 80°C	T_C = 80°C		
									
Case 86-01 Style 1	Case 87L-02 Style 1	Case 221A-02 TO-220AB Style 3	Case 86-01 Style 1	Case 221A-02 TO-220AB Style 3	Case 342-01 Style 1	Case 54-05 Style 2	Case 221A-02 TO-220AB Style 3		
2N4167	2N4183		MCR67-1	MCR68-1	MCR568-1			V_{DRM} V_{RRM}	25 V
2N4168	2N4184	2N6394	MCR67-2	MCR68-2	MCR568-2				50 V
2N4169	2N4185	2N6395	MCR67-3	MCR68-3	MCR568-3	2N3668			100 V
2N4170	2N4186	2N6396				2N3669	MCR2150-4,A4		200 V
2N4171	2N4187	MCR220-5					MCR2150-5,A5		300 V
2N4172	2N4188	2N6397	MCR67-6	MCR68-6	MCR568-6	2N3670	MCR2150-6,A6		400 V
2N4173	2N4189	MCR220-7				2N4103	MCR2150-7,A7		500 V
2N4174	2N4190	2N6398					MCR2150-8,A8		600 V
		MCR220-9					MCR2150-9,A9		700 V
		2N6399					MCR2150-10,A10		800 V
100			300(1)			200	160	MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps) 60 Hz
30						40	50		I_{GT} (mA)
1.5						2.0	2.5		V_{GT} (V)
−40 to +100		−40 to +125				−40 to +100	−40 to +125		T_J Operating Range (°C)

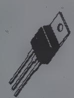
(1) Peak capacitor discharge current for t_w = 1.0 μs. t_w is defined as five time constants of an exponentially decaying current pulse (crowbar applications)

SCRs (continued)

2.2

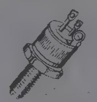
		On-State (RMS) Current						
		16 AMPS		20 AMPS				
		$T_C = 35°C$	$T_C = 90°C$	$T_C = 65°C$			$T_C = 85°C$	$T_C = 65°C$
						 Isolated		
		Case 263-04 Style 1	Case 221A-02 TO-220AB Style 3	Case 310-02 Style 1	Case 263-04 Style 1	Case 311-02 Style 1	Case 54-05 Style 2	Case 174-04 TO-203AA Style 1
V_{DRM} V_{RRM}	25 V	2N1842 2N1842A					MCR649AP1	MCR3818-1
	50 V	2N1843 2N1843A	2N6400	2N5164	2N5168		MCR649AP2	MCR3818-2
	100 V	2N1844 2N1844A	2N6401	S6200A	S6210A	2N6167 S6220A	MCR649AP3	MCR3818-3
	200 V	2N1846 2N1846A	2N6402	2N5165 S6200B	2N5169 S6210B	2N6168 S6220B	MCR649AP4	MCR3818-4
	300 V	2N1848 2N1848A	MCR221-5				MCR649AP5	MCR3818-5
	400 V	2N1849 2N1849A	2N6403	2N5166 S6200D	2N5170 S6210D	2N6169 S6220D	MCR649AP6	MCR3818-6
	500 V	2N1850 2N1850A	MCR221-7				MCR649AP7	MCR3818-7
	600 V		2N6404	2N5167 S6200M	2N5171 S6210M	2N6170 S6220M	MCR649AP8	MCR3818-8
	700 V		MCR221-9				MCR649AP9	MCR3818-9
	800 V		2N6405				MCR649AP10	MCR3818-10
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps) 60 Hz	125	160	240			260	240
	I_{GT} (mA)	80	30	40			40	40
	V_{GT} (V)	2.0	1.5	1.5			3.5	1.5
	T_J Operating Range (°C)	-40 to +100	-40 to +125	-40 to +100			-65 to +125	-40 to +100

SCRs (continued)

On-State (RMS) Current								
20 AMPS	25 AMPS							
T_C = 67°C	T_C = 85°C					T_C = 65°C		
								
Case 175-03 Style 1	Case 221A-02 TO-220AB Style 3		Case 342-01 Style 1		Case 61-03 TO-41 Style 1	Case 263-04 Style 1		
MCR3918-1		MCR69-1		MCR569-1	2N2573	2N681	25 V	
MCR3918-2	2N6504	MCR69-2		MCR569-2	2N2574	2N682	50 V	
MCR3918-3	2N6505	MCR69-3		MCR569-3	2N2575	2N683	100 V	
MCR3918-4	2N6506		MCR525-4		2N2576	2N685	200 V	
MCR3918-5	MCR225-5		MCR525-5		2N2577	2N687	300 V	V_{DRM}
MCR3918-6	2N6507	MCR69-6	MCR525-6	MCR569-6	2N2578	2N688	400 V	
MCR3918-7	MCR225-7		MCR525-7		2N2579	2N689	500 V	V_{RRM}
MCR3918-8	2N6508		MCR525-8		MCR649A8	2N690	600 V	
MCR3918-9	MCR225-9		MCR525-9		MCR649A9	2N691	700 V	
MCR3918-10	2N6509		MCR525-10		MCR649A10	2N692	800 V	
	MCR225-12						1000 V	
240	300	750 (1)	300	750 (1)	260	150	I_{TSM} (Amps) 60 Hz	MAXIMUM ELECTRICAL CHARACTERISTICS
40	40	30	40	30	40	40	I_{GT} (mA)	
1.5					3.5	2.0	V_{GT} (V)	
-40 to +100	-40 to +125				-65 to +125		T_J Operating Range (°C)	

(1) Peak capacitor discharge current for $t_w = 1.0\ \mu s$. t_w is defined as five time constants of an exponentially decaying current pulse (crowbar applications)

SCRs (continued)

		On-State (RMS) Current						
		25 AMPS						
		$T_C = 60°C$		$T_C = 65°C$		$T_C = 70°C$		$T_C = 65°C$
				 Isolated				
		Case 175-03 Style 1		Case 235-03 Style 1		Case 174-04 TO-203AA Style 1		
	25V							MCR3835-1
	50V	C230F	C231F	C230F3	C231F3	C232F	C233F	MCR3835-2
	100 V	C230A	C231A	C230A3	C231A3	C232A	C233A	2N3870
	200 V	C230B	C231B	C230B3	C231B3	C232B	C233B	2N3871
V_{DRM}	300 V	C230C	C231C	C230C3	C231C3	C232C	C233C	MCR3835-5
	400 V	C230D	C231D	C230D3	C231D3	C232D	C233D	2N3872
V_{RRM}	500 V	C230E	C231E	C230E3	C231E3	C232E	C233E	MCR3835-7
	600 V	C230M	C231M	C230M3	C231M3	C232M	C233M	2N3873 MCR3835-8
	700 V							MCR3835-9
	800 V							MCR3835-10
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps) 60 Hz	250						350
	I_{GT} (mA)	25.0	9.0	25.0	9.0	25	9.0	40
	V_{GT} (V)	1.5						1.6
	T_J Operating Range (°C)	-40 to +100						

(1) Peak capacitor discharge current for $t_w = 1.0\ \mu s$. t_w is defined as five time constants of an exponentially decaying current pulse (crowbar applications)

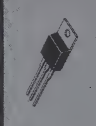
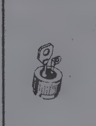
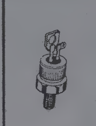
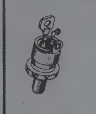
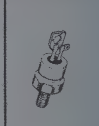
SCRs (continued)

On-State (RMS) Current								
35 AMPS								
T_C = 65°C			T_C = 40°C	T_C = 65°C				
					 Isolated			
Case 175-03 Style 1		Case 310-02 Style 1	Case 263-04 Style 1		Case 311-02 Style 1			
MCR3935-1	MCR70-1						25 V	V_{DRM} V_{RRM}
MCR3935-2	MCR70-2	C229F	C35F	C228F		C228F3	50 V	
2N3896	MCR70-3	C229A	C35A	C228A	2N6171	C228A3	100 V	
2N3897		C229B	C35B	C228B	2N6172	C228B3	200 V	
MCR3935-5		C229C	C35C	C228C		C228C3	300 V	
2N3898	MCR70-6	C229D	C35D	C228D	2N6173	C228D3	400 V	
MCR3935-7		C229E	C35E	C228E		C228E3	500 V	
2N3899 MCR3935-8		C229M	C35M	C228M	2N6174	C228M3	600 V	
MCR3935-9			C35S				700 V	
MCR3935-10			C35N				800 V	
350	850 (1)	300	225	300	350	300	I_{TSM} (Amps) 60 Hz	MAXIMUM ELECTRICAL CHARACTERISTICS
40	30	40					I_{GT} (mA)	
1.6	1.5	2.5	3.0	2.5	1.6	2.5	V_{GT} (V)	
-40 to +100	-40 to +125		-65 to +125	-40 to +125			T_J Operating Range (°C)	

(1) Peak capacitor discharge current for t_w = 1.0 µs. t_w is defined as five time constants of an exponentially decaying current pulse (crowbar applications).

SCRs (continued)

2.2

		On-State (RMS) Current					
		40 AMPS	55 AMPS				
		$T_C = 80°C$	$T_C = 75°C$		$T_C = 70°C$	$T_C = 85°C$	$T_C = 70°C$
					 Isolated		
		Case 221A-02 TO-220AB Style 3	Case 310-02 Style 1	Case 263-04 Style 1	Case 311-02 Style 1	Case 263-04 Style 1	Case 221A-02 TO-220AB Style 3
V_{DRM} V_{RRM}	25 V		MCR63-1	MCR64-1	MCR65-1	MCR71-1	
	50 V	MCR264-2	MCR63-2	MCR64-2	MCR65-2	MCR71-2	MCR265-2
	100 V	MCR264-3	MCR63-3	MCR64-3	MCR65-3	MCR71-3	MCR265-3
	200 V	MCR264-4	MCR63-4	MCR64-4	MCR65-4		MCR265-4
	300 V	MCR264-5	MCR63-5	MCR64-5	MCR65-5		MCR265-5
	400 V	MCR264-6	MCR63-6	MCR64-6	MCR65-6	MCR71-6	MCR265-6
	500 V	MCR264-7	MCR63-7	MCR64-7	MCR65-7		MCR265-7
	600 V	MCR264-8	MCR63-8	MCR64-8	MCR65-8		MCR265-8
	700 V	MCR264-9	MCR63-9	MCR64-9	MCR65-9		MCR265-9
	800 V	MCR264-10	MCR63-10	MCR64-10	MCR65-10		MCR265-10
MAXIMUM ELECTRICAL CHARACTERISTICS	1000 V	MCR264-12					
	I_{TSM} (Amps) 60 Hz	400	550			1700 (1)	550
	I_{GT} (mA)	50	40			30	50
	V_{GT} (V)	1.5	3.0			1.5	1.5
	T_J Operating Range (°C)	-40 to +125					

(1) Peak capacitor discharge current for $t_W = 1.0\ \mu s$. t_W is defined as five time constants of an exponentially decaying current pulse (crowbar applications)

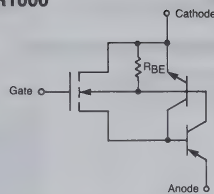
SCRs (continued)

Radar Modulators

On-State (RMS) Current				
100 AMPS		1000 AMPS		
T_C = 85°C		T_C = 65°C		
				
Case 63-03 TO-64 Style 1		Case 263-04 Style 1		
			25 V	
			50 V	
			100 V	
			200 V	
2N4199 2N4199JAN	MCR729-5	MCR1718-5	300 V	V_{DRM}
2N4200 2N4200JAN	MCR729-6	MCR1718-6	400 V	
2N4201 2N4201JAN	MCR729-7	MCR1718-7	500 V	V_{RRM}
2N4202 2N4202JAN	MCR729-8	MCR1718-8	600 V	
2N4203 2N4203JAN	MCR729-9		700 V	
2N4204 2N4204JAN	MCR729-10		800 V	
100*	100*	1000*	I_{TSM} (Amps) 60 Hz	MAXIMUM ELECTRICAL CHARACTERISTICS
50	50	50	I_{GT} (mA)	
1.5	1.5	1.5	V_{GT} (V)	
-65 to +105		-65 to +125	T_J Operating Range (°C)	

*Indicates pulse rating P_W = 3.0 μs duty cycle = 0.6%

TMOS SCR — MCR1000



Two Transistor Equivalent to TMOS SCR

Power FET technology is now extended to include a two-transistor equivalent to latching silicon controlled rectifiers (SCRs). This first-generation TMOS SCR has very fast switching times, high line transient voltage rejection (DV/DT) and asymmetrical blocking.

Possible applications are laser drivers, printers, switching power supplies and inverters, and direct-drive-from-logic robotics. For more details, see Motorola Engineering Bulletin 103.

ON-STATE (RMS) CURRENT					
15 AMPS					
50 V	200 V	400 V	600 V		
MCR1000-2	MCR1000-4	MCR1000-6	MCR1000-8		
90	90	90	90	I_{TSM} (Amps)	MAXIMUM ELECTRICAL CHARACTERISTICS
(see) EB103	(see) EB103	(see) EB103	(see) EB103	I_{GT} (mA)	
2.5 V	2.5 V	2.5 V	2.5 V	V_{GT} (V)	
40	40	40	40	I_H (mA)	

2.2

Thyristors — TRIACs

Metal/Plastic Packages

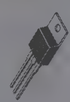
0.6 to 40 Amperes
25 to 800 Volts

2.2

NOTE:
Industry Standards, with a variety of Custom Specifications and Leadforms available.

		On-State (RMS) Current					
		0.6 AMPS			2.5 AMPS		
		T_C = 50°C			T_C = 70°C		
							
		Sensitive Gate					Note: Center Gate Pin Out Allows TO-5 Leadform
		Case 29-02 TO-226AA (TO-92) Style 12			Case 77-04 Style 5		Case 77-04 Style 7
V_{DRM}	50 V	MAC97-2	MAC97A2	MAC97B2	T2322F	T2323F	T2302PF
	100 V	MAC97-3	MAC97A3	MAC97B3	T2322A	T2323A	T2302PA
	200 V	MAC97-4	MAC97A4	MAC97B4	T2322B	T2323B	T2302PB
	300 V	MAC97-5	MAC97A5	MAC97B5	T2322C	T2323C	T2302PC
	400 V	MAC97-6	MAC97A6	MAC97B6	T2322D	T2323D	T2302PD
	500 V	MAC97-7	MAC97A7	MAC97B7	T2322E	T2323E	T2302PE
	600 V	MAC97-8	MAC97A8	MAC97B8	T2322M	T2323M	T2302PM
	700 V						
	800 V						
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps)	8.0	8.0	8.0	25	25	25
	I_{GT} @ 25°C (mA) MT2(+)G(+) MT2(+)G(−) MT2(−)G(−) MT2(−)G(+)	10 10 10 10	5.0 5.0 5.0 7.0	3.0 3.0 3.0 5.0	10 10 10 10	25 40 25 40	10 10 10 10
	V_{GT} @ 25°C (V) MT2(+)G(+) MT2(+)G(−) MT2(−)G(−) MT2(−)G(+)	2.0 2.0 2.0 2.5	2.0 2.0 2.0 2.5	2.0 2.0 2.0 2.5	2.2 2.2 2.2 2.2	2.2 2.2 2.2 2.2	2.2 2.2 2.2 2.2
	T_J Operating Range (°C)	−40 to +110					−40 to +100

TRIACs (continued)

On-State (RMS) Current								
3.0 AMPS	4.0 AMPS			6.0 AMPS				
T_C = 65°C	T_C = 85°C			T_C = 80°C				
		Sensitive Gate						
Case 77-04 Style 7	Case 77-04 Style 5			Case 221A-02 TO-220AB Style 4				
	2N6069	2N6069A	2N6069B				50 V	V_{DRM}
SC136A	2N6070	2N6070A	2N6070B	T2500A	T2801A	SC141A	100 V	
SC136B	2N6071	2N6071A	2N6071B	T2500B	T2801B	SC141B	200 V	
SC136C	2N6072	2N6072A	2N6072B	T2500C	T2801C	SC141C	300 V	
SC136D	2N6073	2N6073A	2N6073B	T2500D	T2801D	SC141D	400 V	
SC136E	2N6074	2N6074A	2N6074B	T2500E	T2801E	SC141E	500 V	
SC136M	2N6075	2N6075A	2N6075B	T2500M	T2801M	SC141M	600 V	
				T2500S	T2801S	SC141S	700 V	
				T2500N	T2801N	SC141N	800 V	
30	30	30	30	60	80	80	I_{TSM} (Amps)	MAXIMUM ELECTRICAL CHARACTERISTICS
							I_{GT} @ 25°C (mA)	
25	30	5.0	3.0	25	80	50	MT2(+)G(+)	
25	—	5.0	3.0	60	80	50	MT2(+)G(-)	
25	30	5.0	3.0	25	80	50	MT2(-)G(-)	
—	—	10	5.0	60	80	—	MT2(-)G(+)	
	@ -40°C	@ -40°C	@ -40°C				V_{GT} @ 25°C (V)	
2.0	2.5	2.5	2.5	2.5	4.0	2.5	MT2(+)G(+)	
2.0	—	2.5	2.5	2.5	4.0	2.5	MT2(+)G(-)	
2.0	2.5	2.5	2.5	2.5	4.0	2.5	MT2(-)G(-)	
—	—	2.5	2.5	2.5	4.0	—	MT2(-)G(+)	
-40 to +110							T_J Operating Range (°C)	

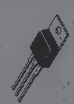
TRIACs (continued)

2.2

		On-State (RMS) Current						
		8.0 AMPS					10 AMPS	
		T_C = 80°C					T_C = 70°C	T_C = 80°C
						Sensitive Gate		
		Case 221A-02 TO-220AB Style 4						
V_{DRM}	50 V			T2800F	T2802F	MAC228-2 MAC228A2		SC146F
	100 V			T2800A	T2802A	MAC228-3 MAC228A3		SC146A
	200 V	MAC218-4 MAC218A4	2N6342 2N6346	T2800B	T2802B	MAC228-4 MAC228A4	MAC210-4 MAC210A4	SC146B
	300 V	MAC218-5 MAC218A5		T2800C	T2802C	MAC228-5 MAC228A5	MAC210-5 MAC210A5	SC146C
	400 V	MAC218-6 MAC218A6	2N6343 2N6347	T2800D	T2802D	MAC228-6 MAC228A6	MAC210-6 MAC210A6	SC146D
	500 V	MAC218-7 MAC218A7		T2800E	T2802E	MAC228-7 MAC228A7	MAC210-7 MAC210A7	SC146E
	600 V	MAC218-8 MAC218A8	2N6344 2N6348	T2800M	T2802M	MAC228-8 MAC228A8	MAC210-8 MAC210A8	SC146M
	700 V	MAC218-9 MAC218A9				MAC228-9 MAC228A9	MAC210-9 MAC210A9	SC146S
	800 V	MAC218-10 MAC218A10	2N6345 2N6349			MAC228-10 MAC228A10	MAC210-10 MAC210A10	SC146N
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps)	100	100	100	100	80	100	120
	I_{GT} @ 25°C (mA)							
	MT2(+)G(+)	50	50	25	50	5.0	50	50
	MT2(+)G(-)	50	75#	60	—	5.0	50	50
	MT2(-)G(-)	50	50	25	50	5.0	50	50
	MT2(-)G(+)	60#	75#	60	—	10#	80*	—
	V_{GT} @ 25°C (V)							
	MT2(+)G(+)	2.0	2.0	2.5	2.5	2.2	2.5	2.5
	MT2(+)G(-)	2.0	2.5#	2.5	—	2.2	2.5	2.5
	MT2(-)G(-)	2.0	2.5	2.5	2.5	2.2	2.5	2.5
	MT2(-)G(+)	3.5#	2.5#	2.5	—	2.5#	3.5*	—
	T_J Operating Range (°C)	-40 to +125		-40 to +100		-40 to +110	-40 to +125	-40 to +100

# Denotes 2N6346-49, MAC218A and MAC228A series only.
* MAC210A series only.

TRIACs (continued)

On-State (RMS) Current								
10 AMPS					12 AMPS			
$T_C = 85°C$	$T_C = 78°C$	$T_C = 85°C$	$T_C = 78°C$	$T_C = 85°C$	$T_C = 80°C$			
				 Isolated				
Case 174-04 TO-203AA Style 3		Case 175-03 Style 3		Case 236-03 Style 2	Case 221A-02 TO-220AB Style 4			
T4101F	SC246F	T4111F	SC245F	T4121F			50 V	V_{DRM}
T4101A	SC246A	T4111A	SC245A	T4121A			100 V	
2N5567	SC246B	2N5569	SC245B	T4121B	2N6342A	2N6346A	200 V	
T4101C	SC246C	T4111C	SC245C	T4121C			300 V	
2N5568	SC246D	2N5570	SC245D	T4121D	2N6343A	2N6347A	400 V	
T4101E	SC246E	T4111E	SC245E	T4121E			500 V	
T4101M	SC246M	T4111M	SC245M	T4121M	2N6344A	2N6348A	600 V	
	SC246S		SC245S	T4121S			700 V	
	SC246N		SC245N	T4121N	2N6345A	2N6349A	800 V	
100	100	100	100	100	120	120	I_{TSM} (Amps)	MAXIMUM ELECTRICAL CHARACTERISTICS
							I_{GT} @ 25°C (mA)	
25	50	25	50	25	50	50	MT2(+)G(+)	
40	50	40	50	40	—	75	MT2(+)G(-)	
25	50	25	50	25	50	50	MT2(-)G(-)	
40	—	40	—	40	—	75	MT2(-)G(+)	
							V_{GT} @ 25°C (V)	
2.5	2.5	2.5	2.5	2.5	2.0	2.0	MT2(+)G(+)	
2.5	2.5	2.5	2.5	2.5	—	2.5	MT2(+)G(-)	
2.5	2.5	2.5	2.5	2.5	2.0	2.0	MT2(-)G(-)	
2.5	—	2.5	—	2.5	—	2.5	MT2(-)G(+)	
-65 to +100	-40 to +100	-65 to +100	-40 to +100	-65 to +100	-40 to +125		T_J Operating Range (°C)	

2.2

TRIACs (continued)

		On-State (RMS) Current						
		15 AMPS						
		$T_C = 85°C$	$T_C = 80°C$	$T_C = 85°C$	$T_C = 80°C$		$T_C = 75°C$	$T_C = 90°C$
						 Isolated	 Isolated	
		Case 174-04 TO-203AA Style 3		Case 175-03 Style 3		Case 311-02 Style 2	Case 235-03 Style 2	Case 221A-02 TO-220AB Style 4
V_{DRM}	50 V	SC251F	T4100F	SC250F	T4110F		T4120F	
	100 V	SC251A	T4100A	SC250A	T4110A		T4120A	
	200 V	SC251B	2N5571	SC250B	2N5573	2N6145	T4120B	MAC15-4 MAC15A4
	300 V	SC251C	T4100C	SC250C	T4110C		T4120C	MAC15-5 MAC15A5
	400 V	SC251D	2N5572	SC250D	2N5574	2N6146	T4120D	MAC15-6 MAC15A6
	500 V	SC251E	T4100E	SC250E	T4110E		T4120E	MAC15-7 MAC15A7
	600 V	SC251M	T4100M	SC250M	T4110M	2N6147	T4120M	MAC15-8 MAC15A8
	700 V	SC251S		SC250S			T4120S	MAC15-9 MAC15A9
	800 V	SC251N		SC250N			T4120N	MAC15-10 MAC15A10
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps)	100	100	100	100	100	100	150
	I_{GT} @ 25°C (mA)							
	MT2(+)G(+)	50	50	50	50	50	50	50
	MT2(+)G(-)	50	80	50	80	80	80	75†
	MT2(-)G(-)	50	50	50	50	50	50	50
	MT2(-)G(+)	—	80	—	80	80	80	75†
	V_{GT} @ 25°C (V)							
	MT2(+)G(+)	2.5	2.5	2.5	2.5	2.5	2.5	2.0
	MT2(+)G(-)	2.5	2.5	2.5	2.5	2.5	2.5	2.5†
	MT2(-)G(-)	2.5	2.5	2.5	2.5	2.5	2.5	2.0
	MT2(-)G(+)	—	2.5	—	2.5	2.5	2.5	2.5†
	T_J Operating Range (°C)	-40 to +115	-65 to +100	-40 to +115	-65 to +100			-40 to +125

†On A Series only.

TRIACs (continued)

TO-220 Overmold Capability

The following two tables show the first products using this solid plastic quick-disconnect/fast-on terminal package based on a preselected TO-220. Its mechanical strength is comparable to steel and aluminum TO-3 packages. Its dimensions and materials are in accordance with UL test requirements. The reliability is also based on TO-220 testing history — very good. Products other than the SCR-TRIAC can be molded, i.e. transistors, darlingtons, voltage regulators, FETs and future products.

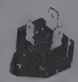
2.2

On-State (RMS) Current								
15 AMPS		25 AMPS						
T_C = 100°C	T_C = 95°C	T_C = 90°C	T_C = 80°C	T_C = 75°C	T_C = 80°C			
*  Hermetic and Isolated	 TO-220 Overmold	*  Hermetic and Isolated		 Isolated				
Case 326-01 Style 2	Case 342-01 Style 1	Case 326-01 Style 2	Case 263-04 Style 2	Case 311-01 Style 2	Case310-02 Style 2	Case 221A-02 TO-220AB Style 4		
			SC260F	SC260F3	SC261F		50 V	V_{DRM}
			SC260A	SC260A3	SC261A	MAC223-3 MAC223A3	100 V	
MAC20-4 MAC20A4	MAC515-4 MAC515A4	MAC25-4 MAC25A4	SC260B	SC260B3	SC261B	MAC223-4 MAC223A4	200 V	
MAC20-5 MAC20A5	MAC515-5 MAC515A5	MAC25-5 MAC25A5	SC260C	SC260C3	SC261C	MAC223-5 MAC223A5	300 V	
MAC20-6 MAC20A6	MAC515-6 MAC515A6	MAC25-6 MAC25A6	SC260D	SC260D3	SC261D	MAC223-6 MAC223A6	400 V	
MAC20-7 MAC20A7	MAC515-7 MAC515A7	MAC25-7 MAC25A7	SC260E	SC260E3	SC261E	MAC223-7 MAC223A7	500 V	
MAC20-8 MAC20A8	MAC515-8 MAC515A8	MAC25-8 MAC25A8	SC260M	SC260M3	SC261M	MAC223-8 MAC223A8	600 V	
MAC20-9 MAC20A9	MAC515-9 MAC515A9	MAC25-9 MAC25A9				MAC223-9 MAC223A9	700 V	
MAC20-10 MAC20A10	MAC515-10 MAC515A10	MAC25-10 MAC25A10				MAC223-10 MAC223A10	800 V	
150	150	250	250	250	250	250	I_{TSM} (Amps)	MAXIMUM ELECTRICAL CHARACTERISTICS
							I_{GT} @ 25°C (mA)	
50	50	70	50	50	50	50	MT2(+)G(+)	
50	75	70	50	50	50	50	MT2(+)G(-)	
50	50	70	50	50	50	50	MT2(-)G(-)	
75†	75†	100†	—	—	—	75†	MT2(-)G(+)	
							V_{GT} @ 25°C (V)	
2.0	2.0	2.0	2.5	2.5	2.5	2.0	MT2(+)G(+)	
2.0	2.5	2.0	2.5	2.5	2.5	2.0	MT2(+)G(-)	
2.0	2.0	2.0	2.5	2.5	2.5	2 0	MT2(-)G(-)	
2.5†	2.5†	2.5†	—	—	—	2.5†	MT2(-)G(+)	
0 to +125	-40 to +125	-0 to +125	-40 to +115			-40 to +125	T_J Operating Range (°C)	

* UL Indicates that device types are UL recognized, file #E69369.
† On A Series only.

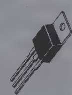
TRIACs (continued)

2.2

		ON-STATE (RMS) CURRENT						
		25 AMPS	30 AMPS					
		T_C = 95°C	T_C = 85°C	T_C = 60°C	T_C = 85°C	T_C = 55°C	T_C = 85°C	T_C = 65°C
		 TO-220 Overmold			 Isolated			
		Case 342-01 Style 1	Case 263-04 Style 2		Case 311-01 Style 2		Case 174-04 TO-203AA Style 3	Case 310-02 TO-203AB Style 2
V_{DRM}	50 V							
	100 V			T6411A		T6421A		T6401A
	200 V	MAC525-4 MAC525A4	2N6160	T6411B	2N6163	T6421B	2N6157	T6401B
	300 V	MAC525-5 MAC525A5		T6411C		T6421C		T6401C
	400 V	MAC525-6 MAC525A6	2N6161	T6411D	2N6164	T6421D	2N6158	T6401D
	500 V	MAC525-7 MAC525A7		T6411E		T6421E		T6401E
	600 V	MAC525-8 MAC525A8	2N6162	T6411M	2N6165	T6421M	2N6159	T6401M
	700 V	MAC525-9 MAC525A9		T6411S		T6421S		T6401S
	800 V	MAC525-10 MAC525A10		T6411N		T6421N		T6401N
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps)	250	250	300	250	300	250	300
	I_{GT} @ 25°C (mA)							
	MT2(+)G(+)	50	60	50	60	50	60	50
	MT2(+)G(-)	50	70	80	70	80	70	80
	MT2(-)G(-)	50	70	50	70	50	70	50
	MT2(-)G(+)	75†	100	80	100	80	100	80
	V_{GT} @ 25°C (V)							
	MT2(+)G(+)	2.0	2.0	2.5	2.0	2.5	2.0	2.5
	MT2(+)G(-)	2.0	2.1	2.5	2.1	2.5	2.1	2.5
	MT2(-)G(-)	2.0	2.1	2.5	2.1	2.5	2.1	2.5
	MT2(-)G(+)	2.5†	2.5	2.5	2.5	2.5	2.5	2.5
	T_J Operating Range (°C)	-40 to +125	-65 to +125	-65 to +100	-40 to +100	-65 to +100	-65 to +125	-65 to +100

†On A Series only.

TRIACs (continued)

ON-STATE (RMS) CURRENT							
40 AMPS							
$T_C = 70°C$		$T_C = 65°C$		$T_C = 60°C$	$T_C = 70°C$	$T_C = 75°C$	
				 Isolated	*  Hermetic and Isolated		
Case 310-02 TO-203AB Style 2		Case 263-04 Style 2		Case 311-02 Style 2	Case 326-01 Style 2	Case 221A-02 TO-220AB Style 4	V_{DRM}
							50 V
	T6400A		T6410A	T6420A			100 V
2N5441	T6400B	2N5444	T6410B	T6420B	MAC50-4 MAC50A4	MAC224-4 MAC224A4	200 V
	T6400C		T6410C	T6420C	MAC50-5 MAC50A5	MAC224-5 MAC224A5	300 V
2N5442	T6400D	2N5445	T6410D	T6420D	MAC50-6 MAC50A6	MAC224-6 MAC224A6	400 V
	T6400E		T6410E	T6420E	MAC50-7 MAC50A7	MAC224-7 MAC224A7	500 V
2N5443	T6400M	2N5446	T6410M	T6420M	MAC50-8 MAC50A8	MAC224-8 MAC224A8	600 V
	T6400S		T6410S	T6420S	MAC50-9 MAC50A9	MAC224-9 MAC224A9	700 V
	T6400N		T6410N	T6420N	MAC50-10 MAC50A10	MAC224-10 MAC224A10	800 V
300	300	300	300	300	300	350	I_{TSM} (Amps) — MAXIMUM ELECTRICAL CHARACTERISTICS
							I_{GT} @ 25°C (mA)
70	50	70	50	50	70	50	MT2(+)G(+)
70	80	70	80	80	70	50	MT2(+)G(-)
70	50	70	50	50	70	50	MT2(-)G(-)
100	80	100	80	80	100†	75†	MT2(-)G(+)
							V_{GT} @ 25°C (V)
2.0	2.5	2.0	2.5	2.5	2.0	2.0	MT2(+)G(+)
2.0	2.5	2.0	2.5	2.5	2.0	2.0	MT2(+)G(-)
2.0	2.5	2.0	2.5	2.5	2.0	2.0	MT2(-)G(-)
2.5	2.5	2.5	2.5	2.5	2.5†	2.5†	MT2(-)G(+)
-65 to +110					0 to +125	-40 to +125	T_J Operating Range (°C)

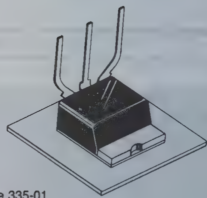
* Indicates that device types are UL recognized, file #E69369.

† On A Series only.

2.2

Chipscretes

A chipscrete is a TO-220 with the tab clipped, leads bent and leadframe flag soldered to a ceramic insulator. With this approach, a tested, isolated die can be designed as a subassembly for relays, controls and power switching applications. The selector guide below shows the popular types only. Any TO-220 can become a chipscrete subassembly.



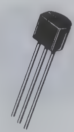
Case 335-01

	Chipscrete SCRs				Chipscrete Triacs			
V_{DRM}/V_{RRM}	8 A	12 A	16 A	25 A	8 A	12 A	15 A	25 A
100	CS122A CS72-3†	CS6395	CS6401	CS6505	CT220-3 CT221-3‡	—	CT15-3 CT15A3‡	CT223-3 CT223A3‡
200	CS122B CS72-4†	CS6396	CS6402	CS6506	CT6342 CT6346‡	CT6342A CT6346A‡	CT15-4 CT15A4‡	CT223-4 CT223A4‡
300	CS122C CS72-5†	CS220-5	CS221-5	—	CT220-5 CT221-5‡	—	CT15-5 CT15A5‡	CT223-5 CT223A5‡
400	CS122D CS72-6†	CS6397	CS6403	CS6507	CT6343 CT6347‡	CT6343A CT6347A‡	CT15-6 CT15A6‡	CT223-6 CT223A6‡
500	CS122E CS72-7†	CS220-7	CS221-7	—	CT220-7 CT221-7‡	—	CT15-7 CT15A7‡	CT223-7 CT223A7‡
600	CS122M CS72-8†	CS6398	CS6404	CS6508	CT6344 CT6348‡	CT6344A CT6348A‡	CT15-8 CT15A8‡	CT223-8 CT223A8‡
700	CS122S —	CS220-9	CS221-9	—	CT220-9 CT221-9‡	—	CT15-9 CT15A9‡	CT223-9 CT223A9‡
800	CS122N —	CS6399	CS6405	CS6509	CT6345 CT6349‡	CT6345A CT6349A‡	CT15-10 CT15A10‡	CT223-10 CT223A10‡

†Sensitive Gate ‡4-mode triggering

Normal delivery — 8 weeks after receiving order. Minimum order size is 100 pieces.

Thyristors — Trigger Devices

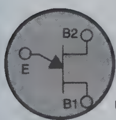


Case 29-02
TO-226AA
TO-92

Case 22A-01
TO-220AB
TO-18

Case 22-03
TO-206AA
TO-18

2.2



UJT

Unijunction Transistors — UJT

Highly stable devices for general-purpose trigger applications and as pulse generators (oscillators) and timing circuits. Useful at frequencies ranging (generally) from 1.0 Hz to 1.0 MHz. Available in low-cost plastic package TO-226AA (TO-92) and in hermetically sealed metal package (Case 22A).

Device Type	η Min	η Max	I_P µA Max	I_{EB20} µA Max	I_V mA Min
Plastic TO-92					
MU10	0.50	0.85	5.0	1.0	1.0
2N4870	0.56	0.75	5.0	1.0	2.0
2N4871	0.70	0.85	5.0	1.0	4.0
MU2646	0.56	0.75	5.0	12	4.0
MU4891	0.55	0.82	5.0	0.01	2.0
MU4892	0.51	0.69	2.0	0.01	2.0
MU4893	0.55	0.82	2.0	0.01	2.0
MU4894	0.74	0.86	1.0	0.01	2.0
Metal TO-18					
MU20	0.50	0.85	5.0	1.0	1.0
2N2646	0.56	0.75	5.0	12	4.0
2N2647	0.68	0.82	2.0	0.2	8.0
2N3980	0.68	0.82	2.0	0.01	1.0
2N4851	0.56	0.75	2.0	0.1	2.0
2N4852	0.70	0.85	2.0	0.1	4.0
2N4853	0.70	0.85	0.4	0.05	6.0
2N4948*	0.55	0.82	2.0	0.01	2.0
2N4949*	0.74	0.86	1.0	0.01	2.0
2N5431*	0.72	0.80	0.4	0.01	2.0

*Also available as JAN and JANTX devices.

PUT

Programmable Unijunction Transistors — PUT

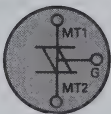
Similar to UJTs, except that I_V, I_P and intrinsic standoff voltage are programmable (adjustable) by means of external voltage divider. This stabilizes circuit performance for variations in device parameters. General operating frequency range is from 0.01 Hz to 10 kHz, making them suitable for long-duration timer circuits. Two-package availability provides cost option.

Device Type	I_P R_G = 10 kΩ	I_P R_G = 1.0 MΩ	I_{GAO} @ 40 V	I_V R_G = 10 kΩ	I_V R_G = 1.0 MΩ
	µA Max		nA Max	µA Min	µA Max
Plastic TO-92					
2N6027	5.0	2.0	10	70	50
2N6028	1.0	0.15	10	25	25
MPU6027	5.0	2.0	10	70	50
MPU6028	1.0	0.15	10	25	25
MPU131	5.0	2.0	5.0	70	50
MPU132	2.0	0.3	5.0	50	50
MPU133	1.0	0.15	5.0	50	25
Metal TO-18					
2N6116*	5.0	2.0	5.0	70	50
2N6117*	2.0	0.3	5.0	50	50
2N6118*	1.0	0.15	5.0	50	25

*Also available as JAN and JANTX devices.

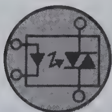
TRIGGER DEVICES (continued)

DIAC

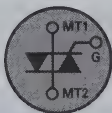


SBS

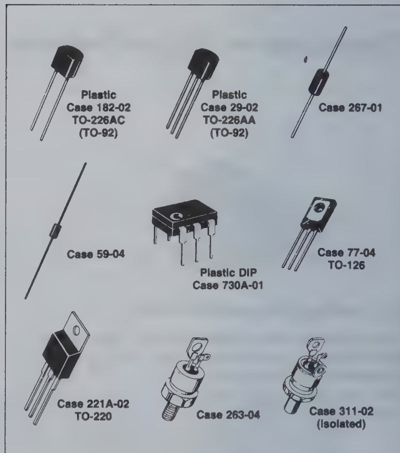
SIDAC



TRIAC DRIVER



TRIAC



Bilateral Triggers — DIACs

Specifically designed as low-cost bidirectional triggers in line-operated Triac control circuits such as light dimmers, motor controls, and temperature controls.

Device Type	V_S Volts	I_S µA Max
Plastic TO-92/TO-226AC		
1N5758 /MPT20	20 ± 4.0	100
1N5760 /MPT28	28 ± 4.0	100
1N5761 /MPT32	32 ± 4.0	100
1N5762	36 ± 4.0	100
1N5758A	20 ± 2.0	25
1N5761A	32 ± 2.0	25

SIDACs

High voltage trigger devices similar in operation to a Triac. Upon reaching the breakover voltage in either direction, the device switches to a low-voltage on-state.

Device Type	I_{TSM} Amps	V_{BO} Volts	
		Min	Max
Case 267-01			
MK1V115	20	104	115
MK1V125	20	110	125
MK1V135	20	120	135
MK1V240	20	220	250
MK1V260	20	240	270
MK1V270	20	250	280
Case 59-04			
MKP9V120	4.0	110	125
MKP9V130	4.0	120	135
MKP9V240	4.0	220	250
MKP9V260	4.0	240	270
MKP9V270	4.0	250	280

Silicon Bidirectional Switch (SBS)

Applications similar to DIAC, but has gate electrode that permits synchronization.

Device Type	V_S Volts		I_S µA Max	I_H mA Max
	Min	Max		
Plastic TO-92/TO-226AA				
MBS4991	6.0	10	500	1.5
MBS4992	7.5	9.0	120	0.5

Optically Isolated Triac Driver

An infrared LED and a bidirectional photodetector in one 7500 V isolated plastic DIP allows safe, economical triggering of Triacs and SCRs from logic sources as low as 3 Volts, 15 mA.

Device Type	Isolation Voltage Volts Min	Typ LED Trigger Current I_{FT} mA	Peak Blocking Voltage Volts
Plastic — DIP Case 730A-01			
MOC3009	7500	30	250
MOC3010	7500	15	250
MOC3011	7500	10	250
MOC3020	7500	30	400
MOC3021	7500	15	400
MOC3030*†	7500	30	250
MOC3031*†	7500	15	250
MOC3040†	7500	30	400
MOC3041†	7500	15	400

*Underwriters' Laboratories Recognition, File No. E54915.
†With zero crossing detector.

TRIGGER DEVICES (continued)

TRIACs

Compatible MOC3030/31 & 3040/41

For applications requiring zero crossover firing, the MAC3030 series triacs and MOC3030/31 couplers offer full-wave 110 Vac control, 7500 V isolation and load independence. For 220 Vac control, use MAC3040 series triacs and MOC3040/41 couplers.

Package	Device Type		RMS Current A Max
	250 V	400 V	
TO-126/Case 77-04	MAC3030-4	MAC3040-4	4.0
TO-220/Case 221A-02	MAC3030-8 MAC3030-15 MAC3030-25	MAC3040-8 MAC3040-15 MAC3040-25	8.0 15 25
Case 263-04	MAC3030-40	MAC3040-40	40
Case 311-02 (Isolated)	MAC3030-40I	MAC3040-40I	40

Compatible MOC3009/10/11 & 3020/21

For applications requiring 110 Vac control, the MAC3010 series triacs and MOC3009/10/11 couplers offer 7500 V isolation and load independence in either the hot or the ground line. For 220 Vac control, use MAC3020 series triacs and MOC3020/21 couplers.

TO-126/Case 77-04	MAC3010-4	MAC3020-4	4.0
TO-220/Case 221A-02	MAC3010-8 MAC3010-15 MAC3010-25	MAC3020-8 MAC3020-15 MAC3020-25	8.0 15 25
Case 263-04	MAC3010-40	MAC3020-40	40
Case 311-02 (Isolated)	MAC3010-40I	MAC3020-40I	40

2.2

Thyristors

Data Sheets

2.3

The following thyristor data sheets are arranged in alphanumeric sequence except in such instances where a particular data sheet may contain information applying to more than one SCR — e.g. 2N6504, 2N6506, 2N6508. To determine if a particular device type is covered by a data sheet in this section, please refer to the alphanumeric listing of the Index and Cross Reference on page 2-1.

1N5758,A
thru
1N5761,A

MOTOROLA

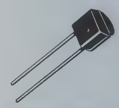
DIACS

BIDIRECTIONAL DIODE THYRISTORS

. . . two-terminal 3-layer devices that exhibit bidirectional negative resistance switching characteristics. These economical, durable devices have been developed for use in thyristor triggering circuits for lamp drivers and universal motor speed controls.

- Switching Voltage Range — 20 to 36 Volts Nominal
- Symmetrical Characteristics
- Passivated Surface for Reliability and Uniformity

2.3



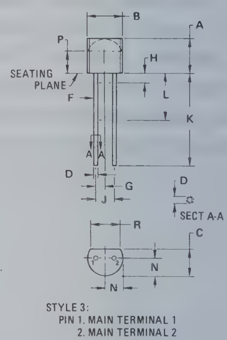
*MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Pulse Current (30 µs duration, 120 Hz repetition rate)	I_{pulse}	2.0	Amp
Power Dissipation @ T_A = −40 to +25°C Derate above 25°C	P_D	300 4.0	mW mW/°C
Operating Junction Temperature Range	T_J	−40 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Switching Voltage (Both Directions)	V_S			Volts
1N5758		16	24	
1N5759		20	28	
1N5760		24	32	
1N5761		28	36	
1N5758A		18	22	
1N5759A		22	26	
1N5761A		30	34	
Switching Current (Both Directions) (T_A = −40 to +75°C) 1N5758/5761	I_S	–	100	µA
1N5758A/5761A		–	25	
Switching Voltage Change (Both Directions) ($\Delta I = I_S$ to I = 10 mA) 1N5758,A,1N5759,A	ΔV	5.0	–	Volts
1N5760,61,A		7.0	–	
Leakage Current (Both Directions), (Applied Voltage = 14 Volts)	I_B	–	10	µA
Switching Voltage Symmetry 1N5758	$(V_S+)-(V_S-)$	–	±4.0	Volts
1N5758A		–	±2.0	
Peak Pulse Amplitude (Figure 1) (Both Polarities) 1N5758,A,1N5759,A		3.0	–	Volts
1N5760,61,A		5.0	–	

*Indicates JEDEC Registered Data.



STYLE 3:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

All JEDEC dimensions and notes apply

CASE 182-02
TO-92

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — PEAK PULSE AMPLITUDE TEST CIRCUIT

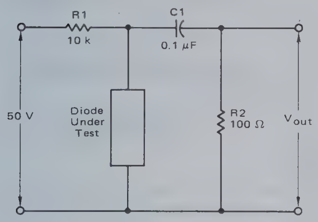
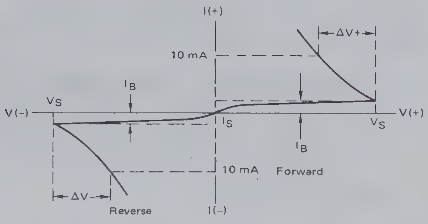


FIGURE 2 — VOLT-AMPERE CHARACTERISTICS



2.3

FIGURE 3 — BREAKOVER VOLTAGE BEHAVIOR

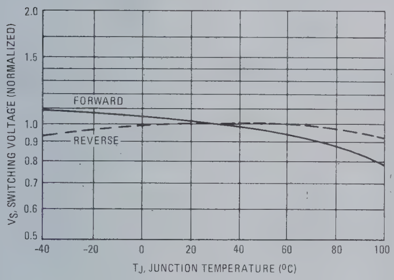


FIGURE 4 — NORMALIZED OUTPUT VOLTAGE BEHAVIOR

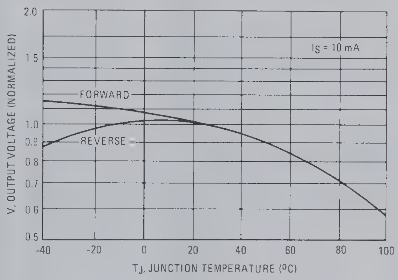


FIGURE 5 — SWITCHING TIMES

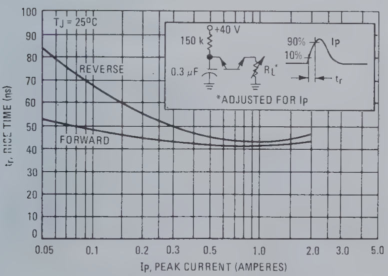
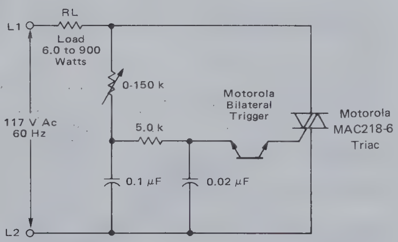


FIGURE 6 — CONTROL CIRCUIT



2N681
thru
2N692

MOTOROLA

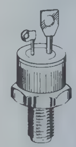
REVERSE BLOCKING TRIODE THYRISTORS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Blocking Voltage to 800 Volts

SILICON CONTROLLED RECTIFIER

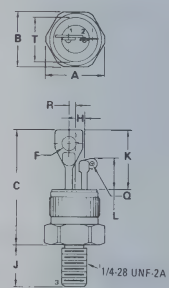
25 AMPERES RMS
25-800 VOLTS



2.3

MAXIMUM RATINGS ($T_J = 125^oC$ unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Blocking Voltage (1)	V_{RRM} or V_{DRM}		Volts
2N681		25	
2N682		50	
2N683		100	
2N684		150	
2N685		200	
2N686		250	
2N687		300	
2N688		400	
2N689		500	
2N690		600	
2N691		700	
2N692		800	
*Peak Non-Repetitive Reverse Voltage	V_{RSM}		Volts
2N681		35	
2N682		75	
2N683		150	
2N684		225	
2N685		300	
2N686		350	
2N687		400	
2N688		500	
2N689		600	
2N690		720	
2N691		840	
2N692		960	
*RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	25	Amp
*Average On-State Current ($T_C = 65^oC$)	$I_{T(AV)}$	16	Amp
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, preceded and followed by rated current and voltage)	I_{TSM}	150	Amp
Circuit Fusing Considerations (T_J = -40 to +125^oC, t = 1.0 to 8.3 ms)	I^2t	93	A^2s
*Peak Gate Power	P_{GM}	5.0	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current 2N681-2N689	I_{GM}	2.0	Amp
2N690-2N692		1.2	
*Peak Gate Voltage — Forward	V_{FGM}	10	Volts
Reverse	V_{RGM}	5.0	
*Operating Junction Temperature Range	T_J	-65 to +125	^oC
*Storage Temperature Range	T_{stg}	-65 to +150	^oC
Stud Torque	—	30	in. lb.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

CASE 263-03

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Average Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open, $T_J = 125°C$)		$I_{D(AV)}, I_{R(AV)}$				mA
	2N681-2N684		–		6.5	
	2N685		–	–	6.0	
	2N686		–	–	5.5	
	2N687		–	–	5.0	
	2N688		–	–	4.0	
	2N689		–	–	3.0	
	2N690		–	–	2.5	
	2N691		–		2.25	
	2N692		–	–	2.0	
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open, $T_J = 125°C$)		I_{DRM}, I_{RRM}	–	–	2.0	mA
*Peak On-State Voltage (I_{TM} = 50.3 A peak, Pulse Width ≤ 1.0 ms, Duty Cycle ≤ 2.0%)		V_{TM}		–	2.0	Volts
Gate Trigger Current, Continuous dc		I_{GT}				mA
(V_{AK} = 12 Vdc, R_L = 50 Ω)			–	–	40	
*(V_{AK} = 12 Vdc, R_L = 50 Ω, T_C = -65°C)			–	–	80	
Gate Trigger Voltage, Continuous dc		V_{GT}				Volts
(V_{AK} = 12 Vdc, R_L = 50 Ω)			–	0.65	2.0	
*(V_{AK} = 12 Vdc, R_L = 50 Ω, T_J = -65°C)			–	–	3.0	
*Gate Non-Trigger Voltage (Rated V_{DRM}, R_L = 50 Ω, T_J = 125°C)		V_{GD}	0.25	–	–	Volts
Holding Current (V_{AK} = 12 Vdc, Gate Open)		I_H	–	7.3	50	mA
Critical Rate of Rise of Off-State Voltage (Rated V_{DRM}, Exponential Waveform, T_J = 125°C, Gate Open)		dv/dt	–	30	–	V/µs

*Indicates JEDEC Registered Data.

2.3

FIGURE 1 – AVERAGE CURRENT DERATING

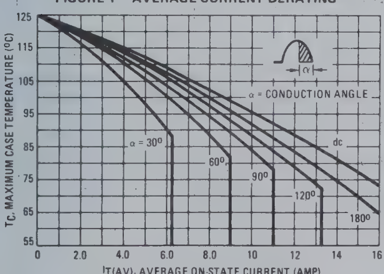


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

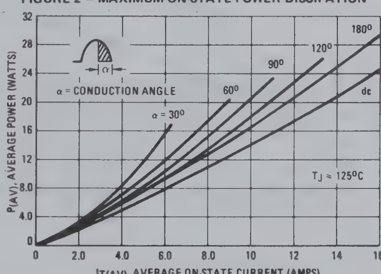


FIGURE 3 – ON-STATE CHARACTERISTICS

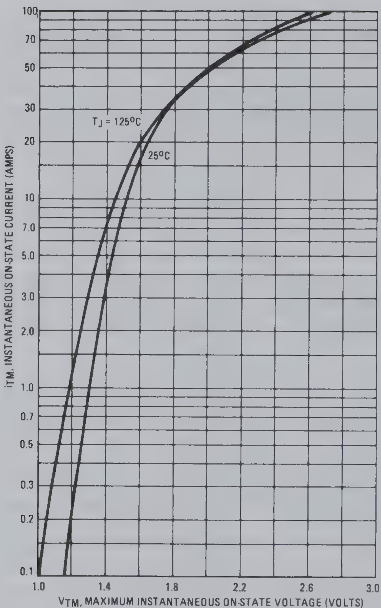
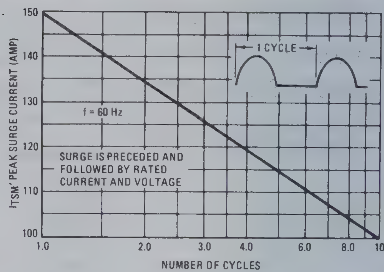
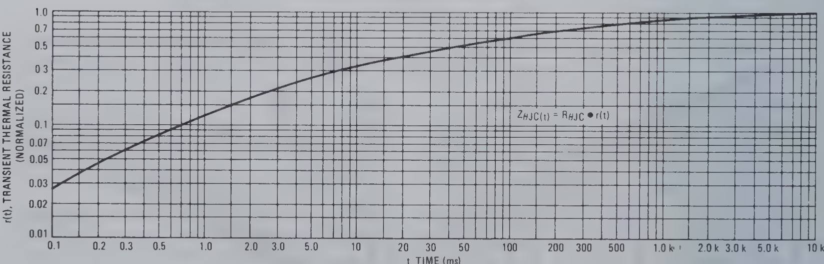


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT



2.3

FIGURE 5 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 6 — PULSE TRIGGER CURRENT

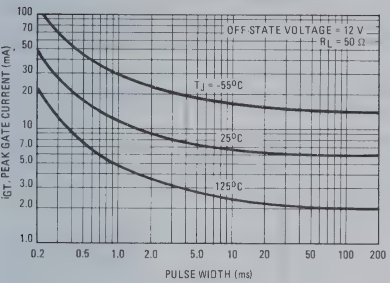


FIGURE 7 — GATE TRIGGER CURRENT

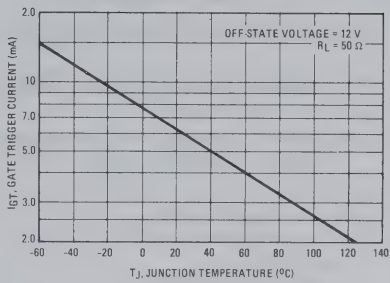


FIGURE 8 — GATE TRIGGER VOLTAGE

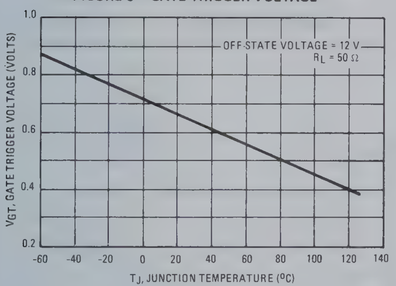
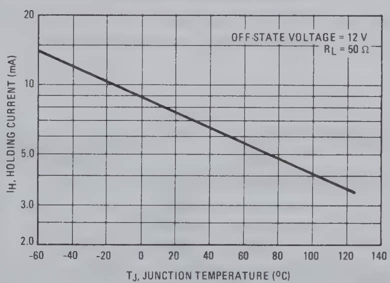


FIGURE 9 — HOLDING CURRENT



2.3

2N1595 thru 2N1599

MOTOROLA

2.3

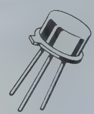
REVERSE BLOCKING TRIODE THYRISTORS

These devices are glassivated planar construction designed for gating operation in mA/μA signal or detection circuits.

- Low-Level Gate Characteristics —
  I_{GT} = 10 mA (Max) @ 25°C
- Low Holding Current —
  I_H = 5.0 mA (Typ) @ 25°C
- Glass-to-Metal Bond for Maximum Hermetic Seal

SILICON CONTROLLED RECTIFIERS

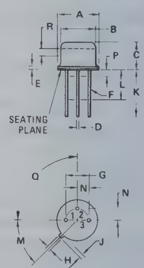
1.6 AMPERE RMS
50 thru 400 VOLTS



***MAXIMUM RATINGS** (T_J = 125°C unless otherwise noted, R_{GC} = 1 kΩ)

Rating	Symbol	Value	Unit
Repetitive Peak Reverse Blocking Voltage (1)	V_{RRM}		Volts
2N1595		50	
2N1596		100	
2N1597		200	
2N1598		300	
2N1599		400	
Repetitive Peak Forward Blocking Voltage (1)	V_{DRM}		Volts
2N1595		50	
2N1596		100	
2N1597		200	
2N1598		300	
2N1599		400	
RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	1.6	Amps
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz, T_J = -65 to +125°C)	I_{TSM}	15	Amps
Peak Gate Power	P_{GM}	0.1	Watt
Average Gate Power	$P_{G(AV)}$	0.01	Watt
Peak Gate Current	I_{GM}	0.1	Amp
Peak Gate Voltage — Forward	V_{GFM}	10	Volts
Reverse	V_{GRM}	10	
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Indicates JEDEC Registered Data.
(1) V_{DRM} or V_{RRM} for all types can be applied on a continuous DC basis without incurring damage.



STYLE 3
PIN 1. CATHODE
2. GATE
3. ANODE (CONNECTED TO CASE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Reverse Blocking Current (V_R = Rated V_{RRM}, T_J = 125°C)	I_{RRM}	–	–	1.0	mA
*Peak Forward Blocking Current (V_D = Rated V_{DRM}, T_J = 125°C)	I_{DRM}	–	–	1.0	mA
*Peak On-State Voltage (I_F = 1.0 Adc, Pulsed, 1.0 ms (Max), Duty Cycle ≤ 1%)	V_{TM}	–	1.1	2.0	Volts
*Gate Trigger Current (V_D = 7 V, R_L = 12 Ohms)	I_{GT}	–	2.0	10	mA
*Gate Trigger Voltage	V_{GT}				Volts
(V_D = 7.0 V, R_L = 12 Ohms)		–	0.7	3.0	
(V_D = 7.0 V, R_L = 12 Ohms, T_J = 125°C)		0.2	–	–	
Reverse Gate Current (V_{GK} = 10 V)	I_{GR}	–	17	–	mA
Holding Current (V_D = 7.0 V)	I_H	–	5.0	–	mA
Turn-On Time	t_{gt}				μs
(I_{GT} = 10 mA, I_F = 1.0 A)		–	0.8	–	
(I_{GT} = 20 mA, I_F = 1.0 A)		–	0.6	–	
Turn-Off Time (I_F = 1.0 A, I_R = 1.0 A, dv/dt = 20 V/μs, T_J = 125°C)	t_q	–	10	–	μs

*Indicates JEDEC Registered Data.

2.3

CURRENT DERATING

FIGURE 1 – CASE TEMPERATURE REFERENCE

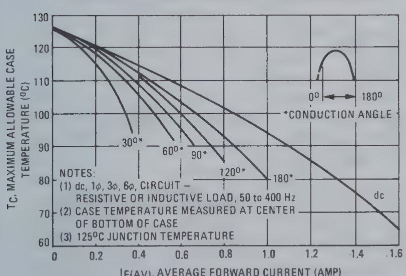
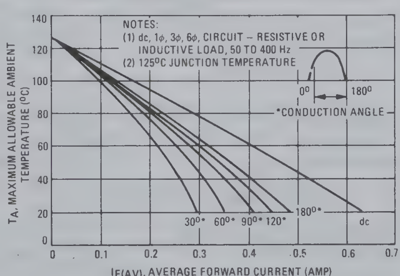


FIGURE 2 – AMBIENT TEMPERATURE REFERENCE



2N1842
thru
2N1850

MOTOROLA

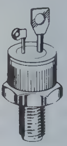
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Blocking Voltage to 500 Volts

SILICON CONTROLLED RECTIFIERS

16 AMPERE RMS
25–500 VOLTS



2.3

MAXIMUM RATINGS ($T_J = 100^oC$ unless otherwise noted.)

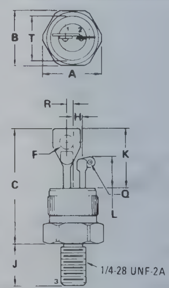
Rating	Symbol	Value	Unit
*Peak Repetitive Forward or Reverse Blocking Voltage (1)	V_{DRM} or V_{RRM}		Volts
2N1842		25	
2N1843		50	
2N1844		100	
2N1845		150	
2N1846		200	
2N1847		250	
2N1848		300	
2N1849		400	
2N1850		500	
*Non-Repetitive Peak Reverse Voltage	V_{RSM}		Volts
2N1842		35	
2N1843		75	
2N1844		150	
2N1845		225	
2N1846		300	
2N1847		350	
2N1848		400	
2N1849		500	
2N1850		600	
*Average On-State Current ($T_C = 35^oC$)	$I_{T(AV)}$	10	Amp
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, preceded and followed by rated current and voltage)	I_{TSM}	125	Amp
Circuit Fusing (T_J = –40 to +100°C, t = 1.0 to 8.3 ms)	I^2t	60	A^2s
*Peak Gate Power	P_{GM}	5.0	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GM}	2.0	Amp
*Peak Gate Voltage — Forward	V_{FGM}	10	Volts
Reverse	V_{RGM}	5.0	
*Operating Junction Temperature Range	T_J	–40 to +100	°C
*Storage Temperature Range	T_{stg}	–40 to +125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

CASE 263-03

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Average Forward or Reverse Blocking Current (V_D = Rated V_{DRM}, V_R = Rated V_{RRM}, T_C = 35°C)	$I_{D(AV)}, I_{R(AV)}$				mA
2N1842		–	–	22.5	
2N1843		–	–	19	
2N1844		–	–	12.5	
2N1845		–	–	6.5	
2N1846		–	–	6.0	
2N1847		–	–	5.5	
2N1848		–	–	5.0	
2N1849		–	–	4.0	
2N1850		–	–	3.0	
Peak Forward or Reverse Blocking Current (V_D Rated V_{DRM}, V_D = Rated V_{RRM}, gate open, T_C = 100°C)	I_{DRM}, I_{RRM}	–	–	6.0	mA
*Peak On-State Voltage (I_{TM} = 31.4 A peak, Pulse Width ≤ 1.0 ms, Duty Cycle ≤ 2.0%)	V_{TM}	–	–	2.5	Volts
Gate Trigger Current, Continuous dc	I_{GT}				mA
(V_D = 12 Vdc, R_L = 50 Ω)		–	6.0	80	
*(V_D = 12 Vdc, R_L = 50 Ω, T_C = −40°C)		–	–	150	
Gate Trigger Voltage, Continuous dc	V_{GT}				Volts
(V_D = 12 Vdc, R_L = 50 Ω)		–	0.65	–	
*(V_D = 12 Vdc, R_L = 50 Ω, T_C = −40°C)		–	–	3.5	
*(V_D Rated V_{DRM}, R_L = 50 Ω, T_C = 100°C)		0.3	–	–	
Holding Current (V_D = 12 Vdc, Gate Open)	I_H	–	7.0	–	mA
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 100°C, Gate Open)	dv/dt	–	30	–	V/µS

*Indicates JEDEC Registered Data.

FIGURE 1 — AVERAGE CURRENT DERATING

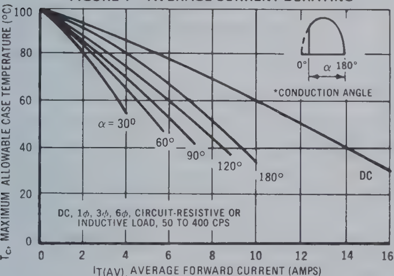


FIGURE 2 — GATE TRIGGER CURRENT

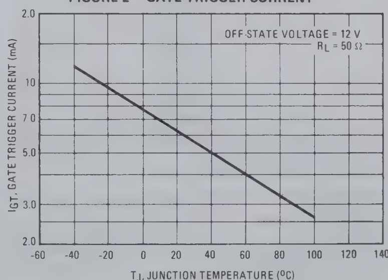


FIGURE 3 — GATE TRIGGER VOLTAGE

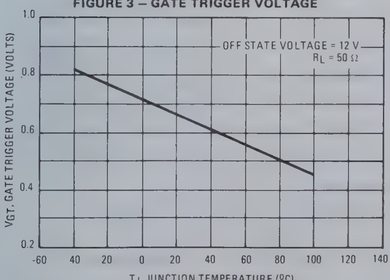
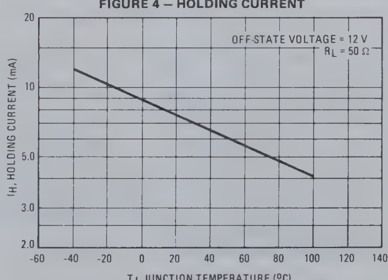


FIGURE 4 — HOLDING CURRENT



2N1842A
thru
2N1850A

MOTOROLA

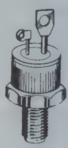
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Blocking Voltage to 500 Volts
- Junction Temperature Rated @ 125°C

SILICON CONTROLLED RECTIFIERS

16 AMPERE RMS
25 – 500 VOLTS



2.3

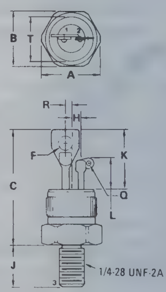
MAXIMUM RATINGS (T_C = 125°C unless otherwise noted.)

Rating		Symbol	Value	Unit
*Peak Repetitive Forward or Reverse Blocking Voltage (1)	2N1842A	V_{DRM} or V_{RRM}	25	Volts
	2N1843A		50	
	2N1844A		100	
	2N1845A		150	
	2N1846A		200	
	2N1847A		250	
	2N1848A		300	
	2N1849A		400	
	2N1850A		500	
*Non-Repetitive Peak Reverse Voltage	2N1842A	V_{RSM}	35	Volts
	2N1843A		75	
	2N1844A		150	
	2N1845A		225	
	2N1846A		300	
	2N1847A		350	
	2N1848A		400	
	2N1849A		500	
	2N1850A		600	
*Average On-State Current (T_C = 80°C)		$I_{T(AV)}$	10	Amp
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, preceded and followed by rated current and voltage)		I_{TSM}	125	Amp
Circuit Fusing (T_J = –65 to +125°C, t = 1.0 to 8.3 ms)		I^2t	60	A^2s
*Peak Gate Power		P_{GM}	5.0	Watts
*Average Gate Power		$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current		I_{GM}	2.0	Amp
*Peak Gate Voltage — Forward		V_{FGM}	10	Volts
Reverse		V_{RGM}	5.0	
*Operating Junction Temperature Range		T_J	-65 to +125	°C
*Storage Temperature Range		T_{stg}	-65 to +125	°C

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.
*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

CASE 263-03

ELECTRICAL CHARACTERISTICS (T_C = 125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Average Forward or Reverse Blocking Current (V_D = Rated V_{DRM} or V_R = Rated V_{RRM}, gate open, T_C = 125°C)	$I_{D(AV)}, I_{R(AV)}$				mA
2N1842A		–	–	22.5	
2N1843A		–	–	19	
2N1844A		–	–	12.5	
2N1845A		–	–	6.5	
2N1846A		–	–	6.0	
2N1847A		–	–	5.5	
2N1848A		–	–	5.0	
2N1849A		–	–	4.0	
2N1850A		–	–	3.0	
Peak Forward or Reverse Blocking Current (V_D = Rated V_{DRM} or V_R = Rated V_{RRM}, gate open, T_C = 125°C)	I_{DRM} I_{RRM}	–	–	6.0	mA
*Peak On-State Voltage (I_{TM} = 31.4 A peak, Pulse Width ≤ 1.0 ms, Duty Cycle ≤ 2.0%)	V_{TM}	–	–	2.5	Volts
Gate Trigger Current, Continuous dc	I_{GT}				mA
(V_D = 12 Vdc, R_L = 50 Ω)		–	6.0	80	
*V_D = 12 Vdc, R_L = 50 Ω, T_C = −65°C)		–	–	150	
Gate Trigger Voltage, Continuous dc	V_{GT}				Volts
(V_D = 12 Vdc, R_L = 50 Ω)		–	0.65	–	
*(V_D = 12 Vdc, R_L = 50 Ω, T_C = −40°C)		–	–	3.5	
*(V_D = 12 Vdc, R_L = 50 Ω, T_C = −65°C)		–	–	3.7	
*(V_D = Rated V_{DRM}, R_L = 50 Ω, T_C = 125°C)		0.25	–	–	
Holding Current (V_D = 12 Vdc, Gate Open)	I_H	–	7.0	–	mA
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 125°C, Gate Open)	dv/dt	–	30	–	V/μS

*Indicates JEDEC Registered Data.

FIGURE 1 — AVERAGE CURRENT DERATING

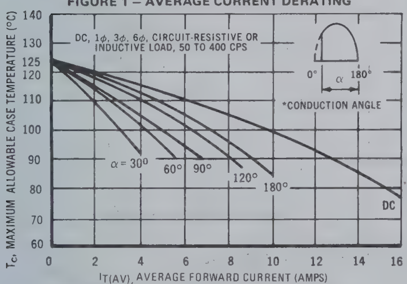


FIGURE 2 — GATE TRIGGER CURRENT

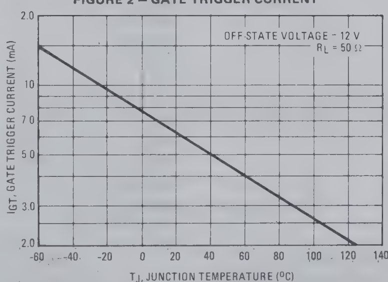


FIGURE 3 — GATE TRIGGER VOLTAGE

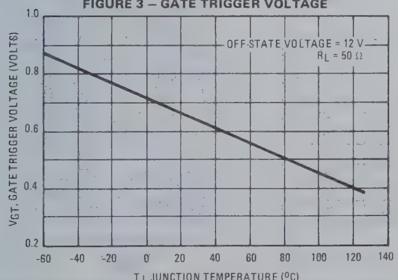
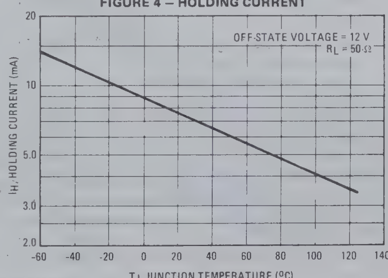


FIGURE 4 — HOLDING CURRENT



2.3

2N2322
thru
2N2329

MOTOROLA

REVERSE BLOCKING TRIODE THYRISTOR

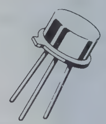
. . . all-diffused PNP devices designed for gating operation in mA/ μA signal or detection circuits.

- Low-Level Gate Characteristics
  I_{GT} = 200 μA (Max) @ 25°C
- Low Holding Current — I_H = 2.0 mA (Max) @ 25°C
- Anode Common to Case
- Glass-to-Metal Bond for Maximum Hermetic Seal

2.3

SILICON CONTROLLED RECTIFIER

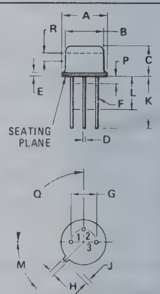
1.6 AMPERE RMS
25 thru 400 VOLTS



***MAXIMUM RATINGS** (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms)

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (Notes 2 and 3)	2N2322	V_{DRM} or V_{RRM}	25	Volts
	2N2323		50	
	2N2324		100	
	2N2325		150	
	2N2326		200	
	2N2327		250	
	2N2328		300	
	2N2329		400	
Non-Repetitive Peak Reverse Blocking Voltage ($t \leq$ 5.0 ms, Notes 2 and 3)	2N2322	V_{RSM}	40	Volts
	2N2323		75	
	2N2324		150	
	2N2325		225	
	2N2326		300	
	2N2327		350	
	2N2328		400	
	2N2329		500	
RMS On-State Current (All Conduction Angles)		$I_{T(RMS)}$	1.6	Amp
Average On-State Current	T_C = 85°C	$I_{T(AV)}$	1.0	Amp
	T_A = 30°C		0.45	
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz, T_C = 80°C) Preceded and followed by rated current and voltage		I_{TSM}	15	Amp
Peak Gate Power		P_{GM}	0.1	Watt
Average Gate Power		$P_{G(AV)}$	0.01	Watt
Peak Gate Current		I_{GM}	0.1	Amp
Peak Gate Voltage		V_{GM}	6.0	Volts
Operating Junction Temperature Range		T_J	-65 to +125	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Lead Solder Temperature (>1/16" from case, 10 s max)		—	+230	°C

*Indicates JEDEC Registered Data.



STYLE 3:
PIN 1. CATHODE
2. GATE
3. ANODE (CONNECTED TO CASE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted, R_{GK} = 1000 ohms)

Characteristic	Symbol	Min	Max	Unit
*Peak Reverse Blocking Current (Rated V_{RRM}, $T_J = 125^oC$)	I_{RRM}	–	100	μA
*Peak Forward Blocking Current (Rated V_{DRM}, $T_J = 125^oC$)	I_{DRM}	–	100	μA
Peak On-State Voltage	V_{TM}			Volts
(I_{TM} = 1.0 A Peak)		–	1.5	
(I_{TM} = 3.14 A Peak, $T_C = 85^oC$)*		–	2.0	
Gate Trigger Current (Note 1)	I_{GT}			μA
(V_D = 6.0 Vdc, R_L = 100 ohms)		–	200	
(V_D = 6.0 Vdc, R_L = 100 ohms, $T_C = -65^oC$)		–	350*	
Gate Trigger Voltage	V_{GT}			Volts
(V_D = 6.0 Vdc, R_L = 100 ohms)		–	0.8	
(V_D = 6.0 Vdc, R_L = 100 ohms, $T_C = -65^oC$)*		–	1.0	
(V_D = Rated V_{DRM}, R_L = 100 ohms, $T_J = 125^oC$)*		0.1	–	
Holding Current	I_H			mA
(V_D = 6.0 Vdc)		–	2.0	
(V_D = 6.0 Vdc, $T_C = -65^oC$)*		–	3.0	
(V_D = 6.0 Vdc, $T_C = 125^oC$)*		0.15	–	

*Indicates JEDEC Registered Data.

Notes: 1. R_{GK} current is not included in measurement.

2. Thyristor devices shall not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

3. Thyristor devices shall not have a positive bias applied to the gate concurrently with a negative potential applied to the anode.

2.3

CURRENT DERATING

FIGURE 1 – CASE TEMPERATURE

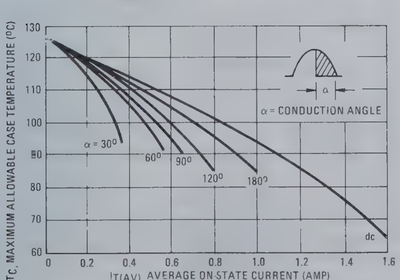
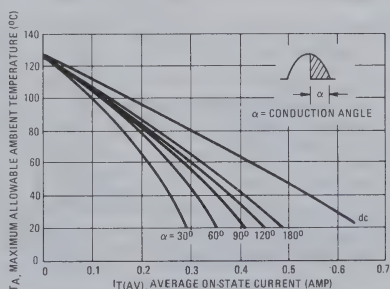


FIGURE 2 – AMBIENT TEMPERATURE



2N2573 thru 2N2579
MCR649AP-1 thru -10

MOTOROLA

REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for industrial applications such as motor controls, heater controls, and power supplies, wherever half-wave or dc silicon gate controlled devices are needed.

- Glass Passivated Junctions for Maximum Reliability
- Center Gate Geometry for Parameter Uniformity
- High Surge Current, I_{TSM} = 260 A, for Crowbar Service

SILICON CONTROLLED RECTIFIER

20 - 25 AMPERES RMS

25-500 VOLTS

CASE 61-03 CASE 54-05

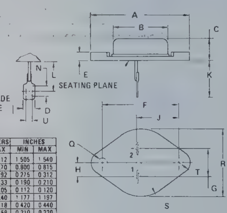
2.3

MAXIMUM RATINGS (T_J = 125°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (1)	V_{DRM} or V_{RRM}		Volts
2N2573, MCR649AP-1		25	
2N2574, MCR649AP-2		50	
2N2575, MCR649AP-3		100	
2N2576, MCR649AP-4		200	
2N2577, MCR649AP-5		300	
2N2578, MCR649AP-6		400	
2N2579, MCR649AP-7		500	
MCR649AP-8		600	
MCR649AP-9		700	
MCR649AP-10		800	
On-State Current 2N Series	$I_{T(RMS)}$	25	Amp
MCR Series		20	
Circuit Fusing (T_J = −65°C to +125°C, t ≤ 8.3 ms) 2N Series	I^2t	275	A^2sec.
MCR Series		235	
Peak Surge Current (Half Cycle, 60 Hz, T_J = −65° to +125°C)	I_{TSM}	260	Amp
Peak Gate Power — Forward	P_{GM}	5.0	Watts
Average Gate Power — Forward	$P_{G(AVG)}$	0.5	Watts
Peak Gate Current — Forward	I_{GM}	2.0	Amp
Peak Gate Voltage — Forward	V_{GFM}	10	Volts
Reverse	V_{GRM}	5.0	
Operating Junction Temperature	T_J	−65 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis without incurring damage. Ratings apply for zero or negative gate voltage.

2N2573 thru 2N2579

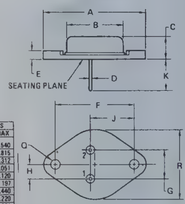


STYLE 1:
PIN 1. GATE
2. CATHODE
CASE: ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38 23	39 12	1 505	1 540
B	20.32	20.70	0.800	0 815
C	6 99	7 92	0 275	0 312
D	4.83	5 33	0 190	0 210
E	2.84	3.05	0 112	0 120
F	29 90	30.40	1 177	1 197
G	10.67	11 18	0 420	0 440
H	5 33	5 59	0 210	0.220
J	16 54	16.79	0 651	0.661
K	16 51	17 27	0.650	0 680
N	3 30	4.32	0 130	0 170
Q	3 84	4 09	0 151	0.161
R	24 64	26.16	0.970	1.030
U	2 29	2.79	0.090	0 110

CASE 61-03

MCR649AP-1 thru MCR649AP-10



STYLE 2:
PIN 1. GATE
2. CATHODE
CASE: ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.12	–	1.540
B	–	20.70	–	0.815
C	–	7 92	–	0.312
D	1.22	1 30	0.048	0.051
E	2.84	3.05	0.112	0.120
F	29 90	30 40	1 177	1 197
G	10.67	11 18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.54	16.79	0.651	0.661
K	8.13	10.67	0.320	0.420
Q	3.84	4.09	0.151	0.161
R		26 16	–	1.030

CASE 54-05

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Units
Peak Forward Blocking Current (V_D = Rated V_{DRM} with gate open, $T_J = 125^oC$)	I_{DRM}	–	0.6	5.0	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}, $T_J = 125^oC$)	I_{RRM}	–	0.6	5.0	mA
Gate Trigger Current (Continuous dc) (V_D = 7 Vdc, $R_L = 100\ \Omega$)	I_{GT}	–	–	40	mA
Gate Trigger Voltage (Continuous dc) (V_D = 7 Vdc, $R_L = 100\ \Omega$)	V_{GT}	–	0.7	3.5	Volts
(V_D = Rated V_{DRM}, $R_L = 100\ \Omega$, $T_J = 125^oC$)		0.3	–	–	
Forward On Voltage (I_{TM} = 20 Adc)	V_{TM}	–	1.1	1.4	Volts
Holding Current (V_D = 7 Vdc, Gate Open)	I_H	–	10	–	mA
Turn-On Time ($t_d + t_r$) (I_{GT} = 50 mA, I_T = 10A, V_D = Rated V_{DRM})	t_{gt}	–	1.0	–	µs
Turn-Off Time (I_T = 10 A, I_R = 10 A, dv/dt = 20 V/µs, $T_J = 125^oC$) (V_D = Rated Voltage V_{DRM})	t_q	–	30	–	µs
Forward Voltage Application Rate (Exponential) (Gate Open, $T_J = 125^oC$, V_D = Rated V_{DRM})	dv/dt	–	30	–	V/µs

2.3

FIGURE 1 – CURRENT DERATING

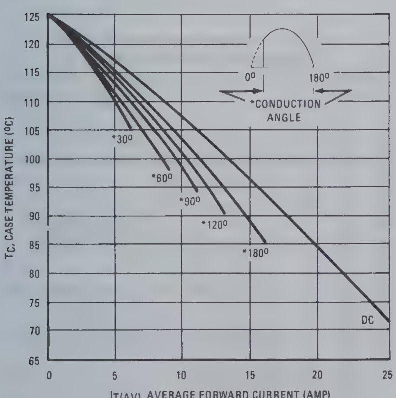


FIGURE 2 – GATE TRIGGER CHARACTERISTICS

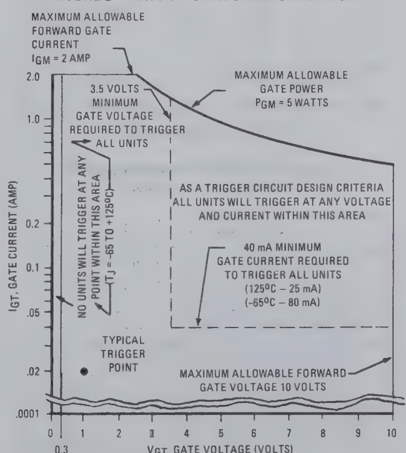


FIGURE 3 — ON-STATE CHARACTERISTICS

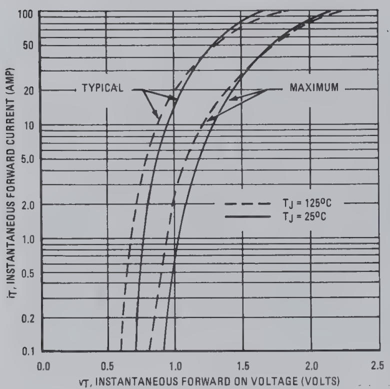


FIGURE 4 — MAXIMUM ALLOWABLE NON-RECURRENT SURGE CURRENT

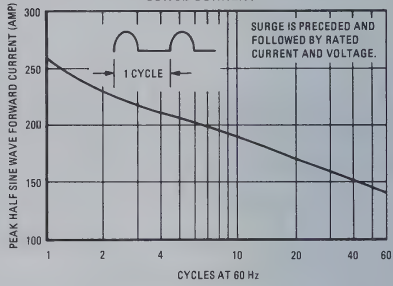


FIGURE 5 — EFFECT OF TEMPERATURE ON TYPICAL HOLDING CURRENT

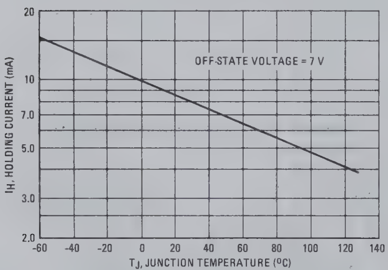


FIGURE 6 — EFFECT OF TEMPERATURE ON TYPICAL GATE CURRENT

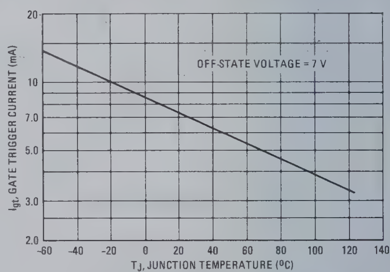


FIGURE 7 — EFFECT OF TEMPERATURE ON TYPICAL GATE VOLTAGE

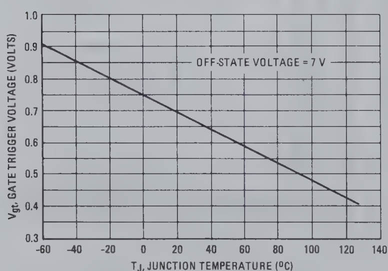
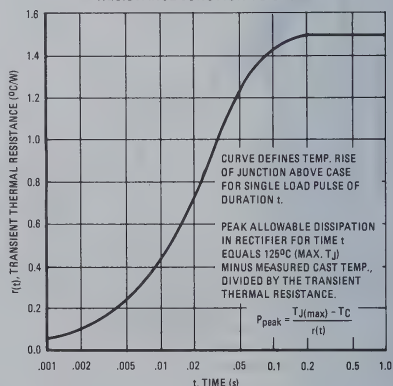
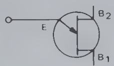


FIGURE 8 — MAXIMUM TRANSIENT THERMAL RESISTANCE JUNCTION TO CASE



MOTOROLA

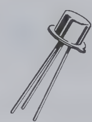


SILICON PN UNIJUNCTION TRANSISTORS

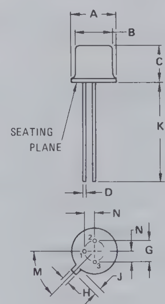
. . . designed for use in pulse and timing circuits, sensing circuits and thyristor trigger circuits. These devices feature:

- Low Peak Point Current — 2.0 μA (Max)
- Low Emitter Reverse Current — 200 nA (Max)
- Passivated Surface for Reliability and Uniformity

PN UNIJUNCTION TRANSISTORS



2.3



STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2

Pin 3 Connected to Case.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A-01

(TO-18 Except for Lead Position)

***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Dissipation (1)	P_D	300	mW
RMS Emitter Current	$I_{E(RMS)}$	50	mA
Peak Pulse Emitter Current (2)	i_E	2.0	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Indicates JEDEC Registered Data.

(1) Derate 3.0 mW/°C increase in ambient temperature. The total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry.

(2) Capacitor discharge — 10 μF or less, 30 volts or less.

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) (Note 1)	2N2646 2N2647	η	0.56 0.68	– –	0.75 0.82	–
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)		r_{BB}	4.7	7.0	9.1	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -55°C to +125°C)		$\alpha_{r_{BB}}$	0.1	–	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) (Note 2)		$V_{EB1(sat)}$	–	3.5	–	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	–	15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	2N2646 2N2647	I_{EB2O}	– –	0.005 0.005	12 0.2	µA
Peak Point Emitter Current (V_{B2B1} = 25 V)	2N2646 2N2647	I_P	– –	1.0 1.0	5.0 2.0	µA
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) (Note 2)	2N2646 2N2647	I_V	4.0 8.0	6.0 10	– 18	mA
Base-One Peak Pulse Voltage (Note 3, Figure 3)	2N2646 2N2647	V_{OB1}	3.0 6.0	5.0 7.0	– –	Volts

*Indicates JEDEC Registered Data.

Notes:

(1) Intrinsic standoff ratio, η, is defined by equation:

$$\eta = \frac{V_P - V_F}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
V_F = Emitter to Base-One Junction Diode Drop ($\approx$ 0.45 V @ 10 µA)

(2) Use pulse techniques: PW $\approx$ 300 µs, duty cycle $\leqslant$ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

(3) Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1
UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

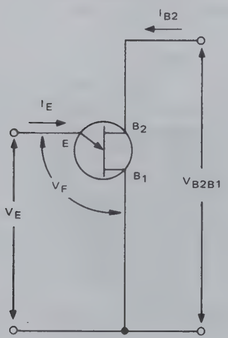


FIGURE 2
STATIC EMITTER CHARACTERISTIC CURVES
(Exaggerated to Show Details)

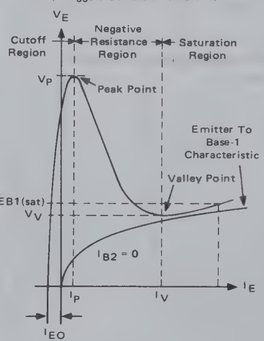
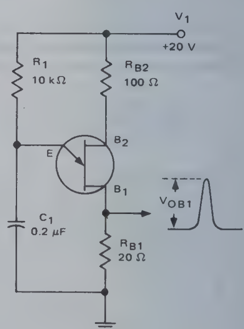
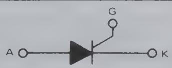


FIGURE 3 – V_{OB1} TEST CIRCUIT
(Typical Relaxation Oscillator)



2N3668 thru 2N3670
2N4103

MOTOROLA



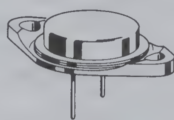
SILICON CONTROLLED RECTIFIER

12.5 AMPERES RMS
100–600 VOLTS

REVERSE BLOCKING TRIODE THYRISTOR

These devices are designed for 12.5 Ampere RMS, 100 through 600 Volt power supply and computer control applications to 100°C maximum Junction Temperature.

- Low Forward "On" Voltage – V_{TM} = 1.8 Volts (Max) @ T_J = 25°C
- All Diffused Junctions for Greater Parameter Uniformity
- Glass Passivated for Greater Stability



2.3

***MAXIMUM RATINGS**

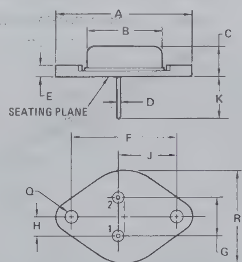
Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (1)	V_{DRM} or V_{RRM}		Volts
2N3668		100	
2N3669		200	
2N3670		400	
2N4103		600	
Forward Current RMS (T_C = 80°C) (All Conduction Angles)	$I_{T(RMS)}$	12.5	Amps
Peak Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz, T_J = –40 to 100°C)	I_{TSM}	200	Amps
Circuit Fusing (T_J = –40 to +100°C, t = 1.0 to 8.3 ms)	I^2t	170	A^2s
Forward Peak Gate Power	P_{GM}	5.0	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2.0	Amps
Peak Forward Gate Voltage	V_{GF}	10	Volts
Peak Reverse Gate Voltage	V_{GR}	5.0	Volts
Operating Junction Temperature Range	T_J	–40 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.7	°C/W

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurrent damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

*Indicates JEDEC Registered Data.



STYLE 2: (THY)
PIN 1. GATE
2. CATHODE
CASE: ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.12	–	1.540
B	–	20.70	–	0.815
C	–	7.92	–	0.312
D	1.22	1.30	0.048	0.051
E	2.84	3.05	0.112	0.120
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.54	16.79	0.651	0.661
K	8.13	10.67	0.320	0.420
Q	3.84	4.09	0.151	0.161
R	–	26.16	–	1.030

CASE 54-05

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM} @ $T_J = 100^oC$)		I_{DRM}				mA
	2N3668		–	–	2.0	
	2N3669		–	–	2.5	
	2N3670		–	–	3.0	
	2N4103		–	–	4.0	
*Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ $T_J = 100^oC$)		I_{RRM}				mA
	2N3668		–	–	1.0	
	2N3669		–	–	1.25	
	2N3670		–	–	1.5	
	2N4103		–	–	2.0	
*Forward "On" Voltage (1) (I_{TM} = 25 A peak)		V_{TM}	–	1.1	1.8	Volts
*Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 24 Ohms)	($T_J = 25^oC$)	I_{GT}	–	7.0	40	mA
	($T_J = -40^oC$)*		–	–	80	
*Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 24 Ohms)		V_{GT}				Volts
	($T_J = -40^oC$)*		–	1.0	3.0	
	($T_J = +25^oC$)		–	0.68	2.0	
	($T_J = +100^oC$)		0.3	–	–	
Holding Current (V_D = 12 Vdc, I_T = 0.5A)		I_H	–	20	50	mA
Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 8A, I_G = 0.2A, t_r = 100ns)		t_{gt}	–	0.5	–	μs
Turn-Off Time (V_D = Rated V_{DRM}, I_{TM} = 8A, I_G = 200 mA, Pulse Width ≤ 50μs, dv/dt = 20V/μs, di/dt = 30A/μs, $T_C = 80^oC$)		t_q	–	20	–	μs
Forward Voltage Application Rate Exponential (V_D = Rated V_{DRM}, $T_C = 100^oC$)		dv/dt	10	100	–	V/μs

* Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 1 ms, Duty Cycle ≤ 1%

2.3

FIGURE 1 – TYPICAL GATE TRIGGER CURRENT

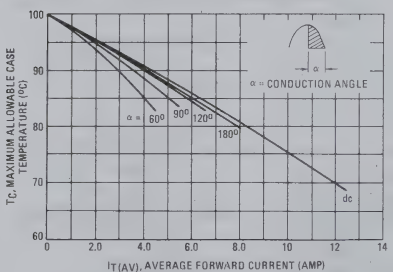


FIGURE 2 – TYPICAL GATE TRIGGER VOLTAGE

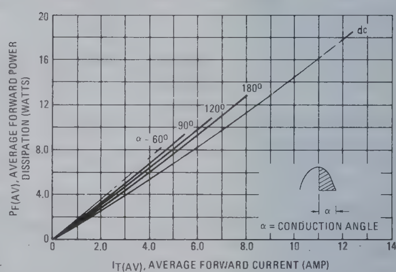


FIGURE 3 – TYPICAL GATE TRIGGER CURRENT

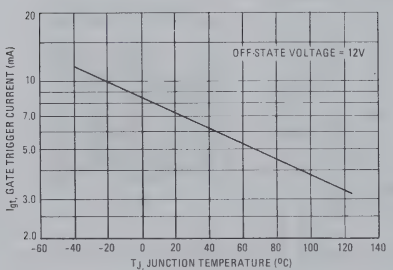
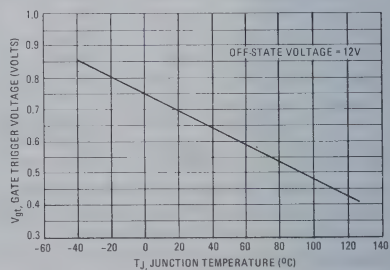


FIGURE 4 – TYPICAL GATE TRIGGER VOLTAGE



![MOTOROLA]

MOTOROLA

2N3870 thru 2N3873
2N3896 thru 2N3899
2N6171 thru 2N6174

REVERSE BLOCKING TRIODE THYRISTORS

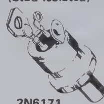
. . . designed for industrial and consumer applications such as power supplies; battery chargers; temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 350 Amp
- Practical Level Triggering and Holding Characteristics — 4.0 and 5.2 mA (Typ) @ $T_C = 25^oC$
- Rugged Construction in Either Pressfit, Stud or Isolated Stud Package

SILICON CONTROLLED RECTIFIERS

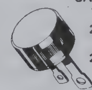
35 AMPERES RMS
100-800 VOLTS

CASE 311-01
(Stud Isolated)

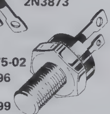


2N6171
thru
2N6174

CASE 174-03
TO-203
2N3870
thru
2N3873



CASE 175-02
2N3896
thru
2N3899



MAXIMUM RATINGS (T_C - 100°C unless otherwise noted)

Rating	Symbol	Value	Unit
*Peak Repetitive Forward or Reverse Blocking Voltage (1) (T_J = −40 to +100°C, 1/2 Sine Wave, 50 to 400 Hz, Gate Open)	V_{RRM} or V_{DRM}		Volts
2N3870, 2N3896, 2N6171		100	
2N3871, 2N3897, 2N6172		200	
2N3872, 2N3898, 2N6173		400	
2N3873, 2N3899, 2N6174		600	
*Peak Non-Repetitive Forward or Reverse Blocking Voltage (t ≤ 5.0 ms)	V_{RSM} or V_{DSM}		Volts
2N3870, 2N3896, 2N6171		150	
2N3871, 2N3897, 2N6172		330	
2N3872, 2N3898, 2N6173		660	
2N3873, 2N3899, 2N6174		700	
*Average On-State Current (2)	$I_{T(AV)}$		Amp
(T_C = −40 to +65°C)		22	
(T_C = +85°C)		11	
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz) (T_C = +65°C)	I_{TSM}	350	Amp
Circuit Fusing (T_C = −40 to +100°C) (t = 1.0 to 8.3 ms)	I^2t	510	A^2s
*Peak Gate Power	P_{GM}	20	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GM}	2.0	Amp
Peak Gate Voltage	V_{GM}	10	Volts
*Operating Junction Temperature Range	T_J	−40 to +100	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C
Stud Torque		30	in. lb.

*THERMAL CHARACTERISTICS

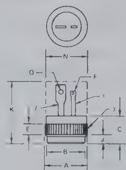
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
2N3870 thru 2N3873, 2N3896 thru 2N3899		0.9	
2N6171 thru 2N6174		1.0	

*Indicates JEDEC Registered Data

(1) Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

(2) Isolated stud devices must be derated an additional 10 percent.

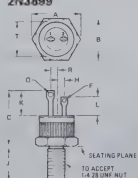
2N3870 thru 2N3873 — **CASE 174-03 TO-203**



STYLE 1
TERM 1 GATE
2 CATHODE
3 ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54		0.100	
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32		0.800
N		12.95		0.510
Q	1.65	4.06	0.065	0.160

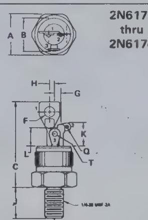
2N3896 thru 2N3899 — **CASE 175-02**



STYLE 1
TERM 1 CATHODE
2 GATE
STUD ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

2N6171 thru 2N6174 — **CASE 311-01 (Stud Isolated)**



STYLE 1
1 CATHODE
2 GATE
3 ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51		1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

2.3

2.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM}, with gate open, $T_C = 100^oC$)	I_{DRM}				mA
2N3870, 2N3896, 2N6171		–	1.0	2.0	
2N3871, 2N3897, 2N6172		–	1.0	2.5	
2N3872, 2N3898, 2N6173		–	1.0	3.0	
2N3873, 2N3899, 2N6174		–	1.0	4.0	
*Peak Reverse Blocking Current (V_R = Rated V_{RRM}, with gate open, $T_C = 100^oC$)	I_{RRM}				mA
2N3870, 2N3896, 2N6171		–	1.0	2.0	
2N3871, 2N3897, 2N6172		–	1.0	2.5	
2N3872, 2N3898, 2N6173		–	1.0	3.0	
2N3873, 2N3899, 2N6174		–	1.0	4.0	
*Peak On-State Voltage (I_{TM} = 69 A Peak)	V_{TM}	–	1.5	1.85	Volts
*Gate Trigger Current, Continuous dc (V_D = 12 V, R_L = 24 ohms) *$T_C = -40^oC$	I_{GT}	–	9.0	80	mA
$T_C = 25^oC$		–	4.0	40	
*Gate Trigger Voltage Continuous dc (V_D = 12 V, R_L = 24 ohms) *$T_C = -40^oC$	V_{GT}	–	0.9	3.0	Volts
$T_C = 25^oC$		–	0.69	1.6	
*Holding Current (Gate Open) (V_D = 12 V, I_{TM} = 200 mA) *$T_C = -40^oC$	I_H	–	14	90	mA
$T_C = 25^oC$		–	5.2	50	
*Gate Controlled Turn-On Time ($t_d + t_r$) (I_{TM} = 41 Adc, V_D = rated V_{DRM}, I_{GT} = 40 mAdc, Rise Time ≤ 0.05 μs, Pulse Width = 10 μs)	t_{gt}	–	–	1.5	μs
Circuit Commutated Turn-Off Time	t_q				μs
(I_{TM} = 10 A, I_R = 10 A)		–	25	–	
(I_{TM} = 10 A, I_R = 10 A, $T_C = 100^oC$)		–	35	–	
Forward Voltage Application Rate ($T_C = 100^oC$, V_D = Rated V_{DRM})	dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 — AVERAGE CURRENT DERATING

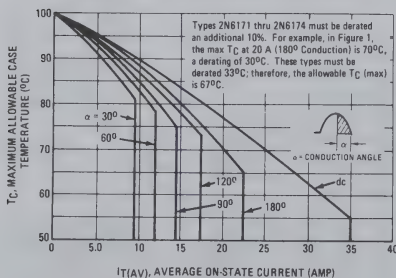


FIGURE 2 — ON-STATE POWER DISSIPATION

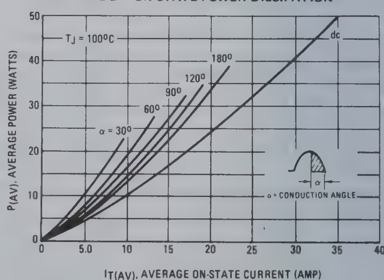


FIGURE 3 – ON-STATE CHARACTERISTICS

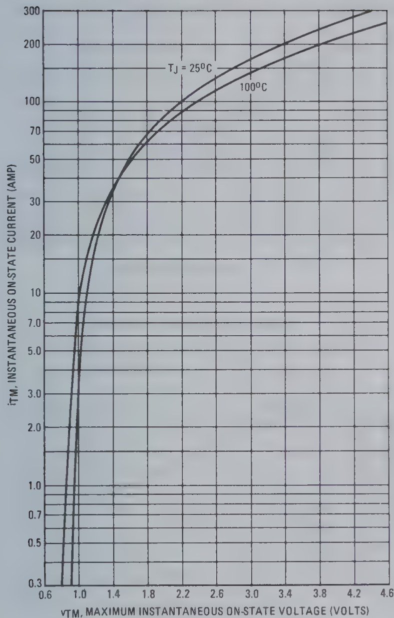


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

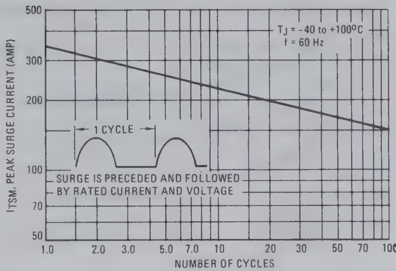


FIGURE 5 – TYPICAL THERMAL RESPONSE

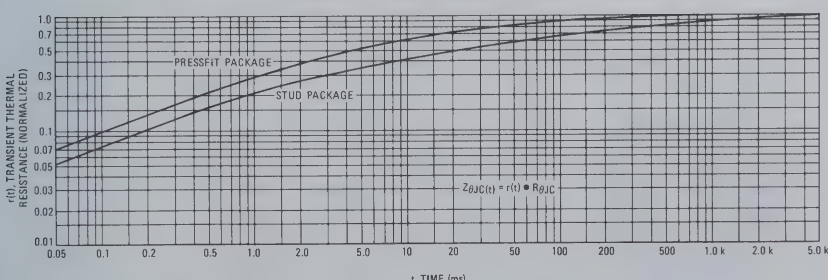


FIGURE 6 – PULSE TRIGGER CURRENT

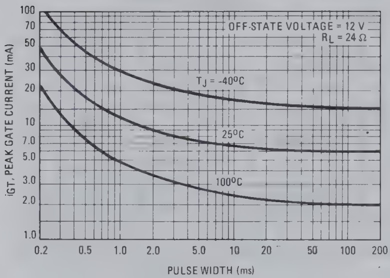


FIGURE 7 – GATE TRIGGER CURRENT

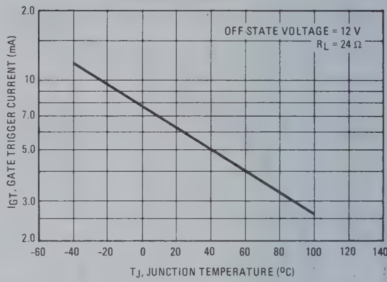


FIGURE 8 – GATE TRIGGER VOLTAGE

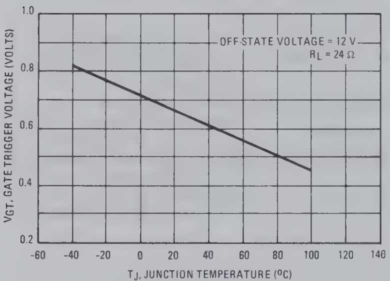
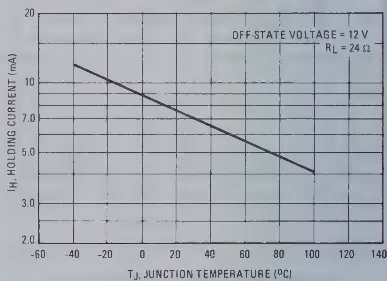


FIGURE 9 – HOLDING CURRENT



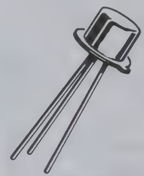
MOTOROLA

SILICON ANNULAR PN UNIJUNCTION TRANSISTOR

. . . designed for military and industrial use in pulse, timing, sensing, and oscillator circuits. These devices feature:

- Low Peak Point Current — 2.0 μA max
- Fast Switching — to 1.0 MHz
- Low Emitter Reverse Current — 10 nA max
- Passivated Surface for Reliability and Uniformity

PN UNIJUNCTION TRANSISTOR

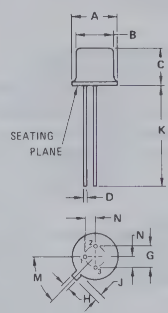


MAXIMUM RATINGS ($T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
RMS Power Dissipation (1)	P_D	360	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current (2)	i_e	1.0	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
Storage Temperature Range	T_{stg}	-65 to +200	$^{\circ}C$

(1) Derate 2.4 mW/$^{\circ}$C increase in ambient temperature. Total power dissipation (available power to Emitter and Base-Two) must be limited by external circuitry.

(2) Capacitance discharge current must fall to 0.37 Amp within 3.0 ms and PRR $\leqslant$ 10 PPS.



STYLE 1
PIN 1. EMITTER
2. BASE 1
3. BASE 2 CONNECTED TO CASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

TO-18 except for lead position

CASE 22A-01
(TO-18 Type)

2.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) Note 1	η	0.68	–	0.82	–
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)	R_{BB}	4.0	6.0	8.0	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -65°C to +100°C)	αR_{BB}	0.4	–	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) Note 2	$V_{EB1(sat)}$	–	2.5	3.0	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)	$I_{B2(mod)}$	12	15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	I_{EB20}	–	5.0	10	nA
(V_{B2E} = 30 V, I_{B1} = 0, T_A = 125°C)		–	–	1.0	µA
Peak Point Emitter Current (V_{B2B1} = 25V)	I_P	–	0.6	2.0	µA
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) Note 2	I_V	1.0	4.0	10	mA
Base-One Peak Pulse Voltage (Note 3, Figure 3)	V_{OB1}	6.0	8.0	–	Volts
Maximum Oscillation Frequency (Figure 4)	f(max)	1.0	1.25	–	MHz

NOTES

1. Intrinsic standoff ratio, η, is defined by equation:

$$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
$V_{(EB1)}$ = Emitter to Base-One Junction Diode Drop (0.45V @ 10 µA)

2. Use pulse techniques: PW ≈ 300 µs duty cycle ≤2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

3. Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in ACR firing circuits and other types of pulse circuits.

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

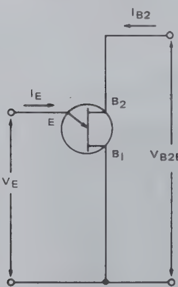


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES (Exaggerated to Show Details)

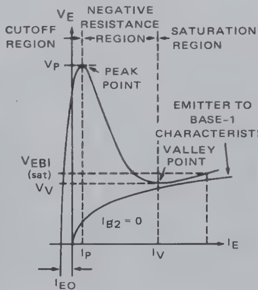


FIGURE 3 – V_{OB1} TEST CIRCUIT (Typical Relaxation Oscillator)

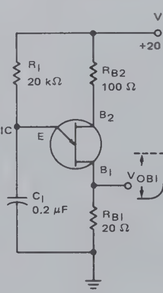
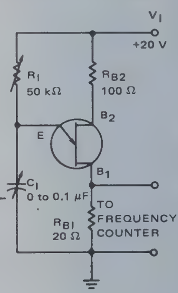


FIGURE 4 – f(max) MAXIMUM FREQUENCY TEST CIRCUIT



MOTOROLA

2N4167 thru 2N4174
2N4183 thru 2N4190

SILICON CONTROLLED RECTIFIERS

8-AMPERE RMS
25 thru 600 VOLTS

REVERSE BLOCKING TRIODE THYRISTOR

. . . multi-purpose PNPN silicon controlled rectifiers suited for industrial, consumer, and mulitary applications. Offered in a choice of space-saving, economical packages for mounting versatility.

- Uniform Low-Level Noise-Immune Gate Triggering — I_{GT} = 10 mA (Typ) @ T_C = 25°C
- Low Forward "On" Voltage — v_T = 1.0 V (Typ) @ 5.0 Amp @ 25°C
- High Surge-Current Capability — I_{TSM} = 100 Amp Peak
- Shorted Emitter Construction

MAXIMUM RATINGS

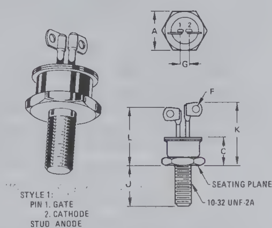
(Apply over operating temperature range and for all case types unless otherwise noted)

Rating	Symbol	Value	Unit
*Peak Repetitive Forward and Reverse Blocking Voltage (1)	V_{DRM} or V_{RRM}		Volts
2N4167, 83,		25	
2N4168, 84,		50	
2N4169, 85,		100	
2N4170, 86,		200	
2N4171, 87,		300	
2N4172, 88,		400	
2N4173, 89,		500	
2N4174, 90,		600	
Forward Current RMS	$I_{T(RMS)}$	8.0	Amp
*Peak Forward Surge Current (One cycle, 60 Hz, T_J = −40 to +100°C)	I_{TSM}	100	Amp
Circuit Fusing (T_J = −40 to +100°C; $t \leq 8.3$ ms)	I^2t	40	A^2s
*Peak Gate Power	P_{GM}	5.0	Watt
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
Peak Gate Voltage (2)	V_{GM}	10	Volts
*Operating Temperature Range	T_J	−40 to +100	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C
Stud Torque		15	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	1.5	2.5*	°C/W
Thermal Resistance, Case to Ambient (See Fig. 11) 2N4183-98	$R\theta_{CA}$	50	—	°C/W

(1) Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.
(2) Devices should not be operated with a positive bias applied to the gate concurrently with a negative potential applied to the anode.
*Indicates JEDEC Registered Data

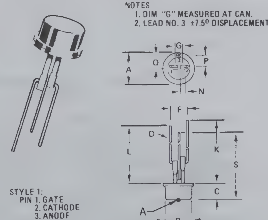


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	11.10	–	0.437
C	–	7.87	–	0.310
F	1.78 TYP		0.070 TYP	
G	2.29	2.79	0.090	0.110
J	10.72	11.48	0.422	0.452
K	–	16.76	–	0.660
L	–	15.49	–	0.610

NOTE:
1. DIM "G" MEASURED AT CAN.

2N4167—74
CASE 86-01

NOTES
1. DIM "G" MEASURED AT CAN.
2. LEAD NO. 3 ±7.5° DISPLACEMENT.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		10.92	-	0.430
B	–	8.89	-	0.350
C		5.97	-	0.235
D	0 76	0.86	0.030	0.034
F	4 83	5.33	0.190	0.210
G	2 29	2 79	0.090	0.110
K	33 53		1 320	
L	31 50 TYP		1.240 TYP	
N	1 65	1.91	0.065	0.075
P	3 43	3.68	0.135	0.145
Q	4 57	5.08	0.180	0.200
S	30 48	-	1.20	-

2N4183—90
CASE 87L-01

2.3

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM} @ T_J = 100°C, gate open)	I_{DRM}	–	–	2.0	mA
*Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ T_J = 100°C, gate open)	I_{RRM}	–	–	2.0	mA
Gate Trigger Current (Continuous dc) (1)	I_{GT}				mA
(V_D = 7.0 Vdc, R_L = 100 Ω)		–	10	30	
*(V_D = 7.0 Vdc, R_L = 100 Ω, T_C = –40°C)		–		60	
Gate Trigger Voltage (Continuous dc)	V_{GT}				Volts
(V_D = 7.0 Vdc, R_L = 100 Ω)		–	0.75	1.5	
*(V_D = 7.0 Vdc, R_L = 100 Ω, T_C = –40°C)		–	–	2.5	
*(V_D = 7.0 Vdc, R_L = 100 Ω, T_J = 100°C)		0.2	–	–	
*Forward "On" Voltage (pulsed, 1.0 ms max, duty cycle ≤ 1%) (I_{TM} = 15.7 A)	V_{TM}	–	1.4	2.0	Volts
Holding Current	I_H				mA
(V_D = 7.0 Vdc, gate open)		–	10	30	
*(V_D = 7.0 Vdc, gate open, T_C = –40°C)		–	–	60	
Turn-On Time (t_d + t_r) (I_G = 20 mAdc, I_F = 5.0 Adc, V_D = Rated V_{DRM})	t_{on}	–	1.0	·	μs
Turn-Off Time	t_{off}				μs
(I_F = 5.0 Adc, I_R = 5.0 Adc)		–	15	–	
(I_F = 5.0 Adc, I_R = 5.0 Adc, T_J = 100°C, V_D = Rated V_{DRM}) (dv/dt = 30 V/μs)		–	25	–	
Forward Voltage Application Rate (Exponential) (Gate open, T_J = 100°C, V_D = Rated V_{DRM})	dv/dt	–	50	–	V/μs

(1) For optimum operation, i.e. faster turn-on, lower switching losses, best di/dt capability, recommended I_{GT} = 200 mA minimum.

*Indicates JEDEC Registered Data

TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 – PULSE CURRENT TRIGGERING

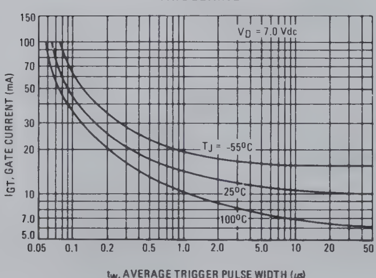
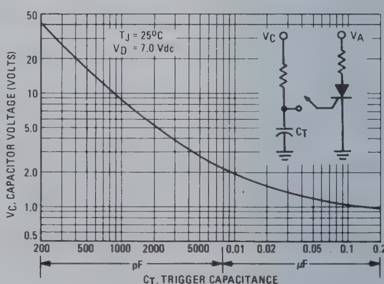


FIGURE 2 – CAPACITIVE DISCHARGE TRIGGERING



CURRENT DERATING

FIGURE 3 – MAXIMUM CASE TEMPERATURE

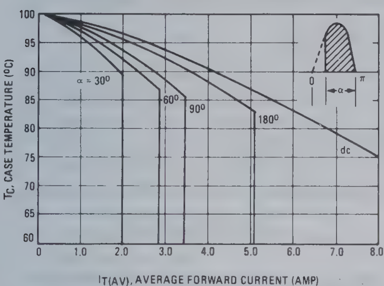


FIGURE 4 – MAXIMUM AMBIENT TEMPERATURE

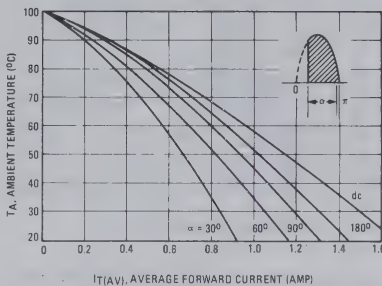


FIGURE 5 – POWER DISSIPATION

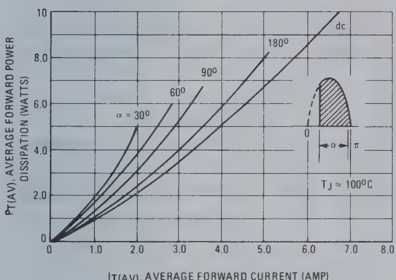


FIGURE 6 – MAXIMUM SURGE CAPABILITY

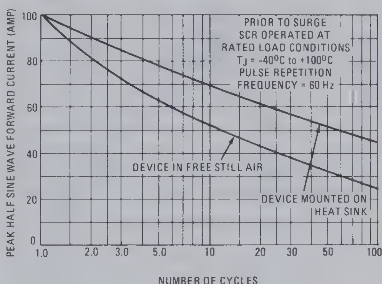
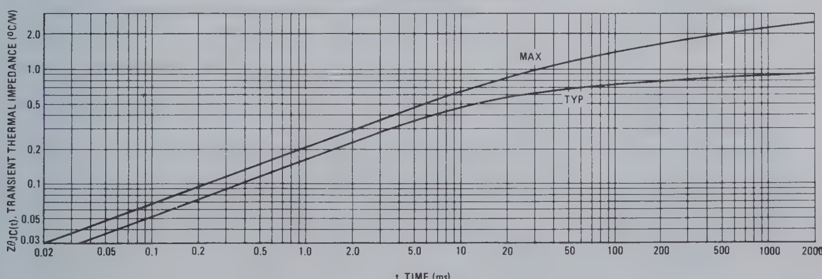


FIGURE 7 – THERMAL RESPONSE



2.3

FIGURE 8 – FORWARD VOLTAGE

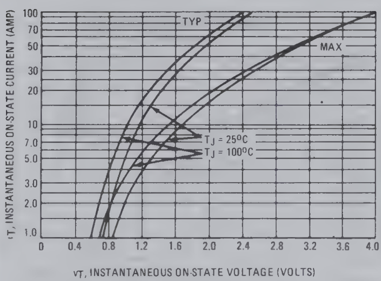


FIGURE 9 – HOLDING CURRENT

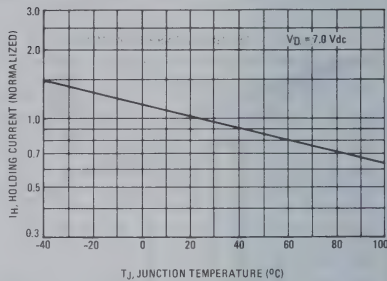


FIGURE 10 – TYPICAL THERMAL RESISTANCE OF PLATES

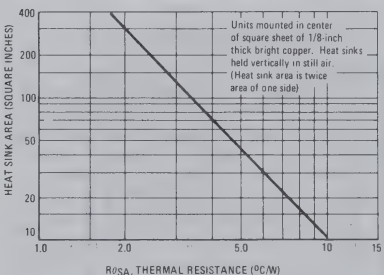
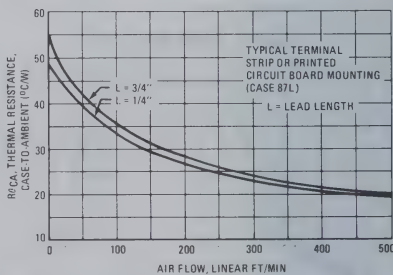


FIGURE 11 – CASE-TO-AMBIENT THERMAL RESISTANCE



2N4199
thru
2N4204

MOTOROLA

Designers Data Sheet

REVERSE BLOCKING TRIODE THYRISTOR

. . . fast switching, high-voltage Thyristors especially designed for pulse modulator applications in radar and other similar equipment.

- Guaranteed Limits on All Critical Parameters
- High-Voltage: V_{DRM} = 300 to 800 Volts
- Maximum Turn-On Times Specified – 300 to 400 ns
- Repetitive Pulse Current to 100 Amperes
- Stable Switching Characteristics Over an Operating Temperature Range From –65 to +105°C
- Pulse Repetition Rates as High as 20,000 pps
- Jan Versions Available

SILICON
CONTROLLED
RECTIFIERS

100 AMPERE PULSE
300 thru 800 VOLTS

Designers Data for "Worst Case" Conditions

The Designers Data Sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

2.3

MAXIMUM RATINGS

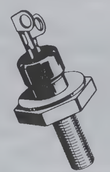
Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (1) (T_J = 105°C)	V_{RRM}	50	Volts
*Peak Forward Blocking Voltage (1) (T_C = 105°C) 2N4199	V_{DRM}	300	Volts
2N4200		400	
2N4201		500	
2N4202		600	
2N4203		700	
2N4204		800	
Repetitive Peak On-State Current (PW = 3.0 μs, Duty Cycle = 0.6%, T_C = 85°C)	I_{TRM}	100	Amp
Continuous On-State Current (T_C = 65°C)	I_T	5.0	Amp
Current Application Rate (2)	di/dt	5000	A/μs
Peak Forward Gate Power	P_{GFM}	20	Watts
Average Forward Gate Power	$P_{GF(AV)}$	1	Watt
Peak Forward Gate Current	I_{GFM}	5.0	Amp
Peak Gate Voltage – Forward	V_{GFM}	10	Volts
Reverse (3)	V_{GRM}	10	
Operating Junction Temperature Range	T_J		°C
Blocking State		–65 to +105	
Conducting State		–65 to +200	
Storage Temperature Range	T_{stg}	–65 to +200	°C
Stud Torque	–	15	in. lb.

THERMAL CHARACTERISTICS

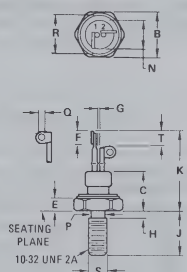
Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.0	°C/W

(1) Characterized for unilateral applications where reverse blocking capability is not important. Higher voltage units available upon request. V_{DRM} and V_{RRM} may be applied as a continuous dc voltage for zero or negative gate voltage but positive gate voltage must not be applied concurrently with a negative potential on the anode. When checking blocking capability, do not permit the applied voltage to exceed the rated voltage.
(2) Minimum Gate Trigger Pulse: i_G = 200 mA, PW = 1 μs, t_r = 20 ns.
(3) Do not reverse bias gate during forward conduction if anode current exceeds 10 amperes.

*JEDEC Registered Data



STYLE 1.
PIN 1. CATHODE
2. GATE
STUD – ANODE



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.57	12.83	0.495	0.505
B	10.77	11.10	0.424	0.437
C	–	10.80	–	0.425
D	3.94	4.70	0.155	0.185
E	–	3.56		0.140
J	10.16	11.51	0.400	0.453
K	–	21.72	–	0.855
L	–	17.78	–	0.700
N	–	7.11	–	0.280
Q	1.02	1.91	0.040	0.075

CASE 63-03

2.3

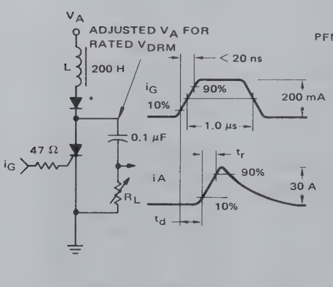
ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
*Peak Forward and Reverse Blocking Current (Rated V_{DRM} and V_{RRM}, $T_C = 105^oC$, gate open)	17	I_{DRM} I_{RRM}	– –	2.0 2.0	mA
Gate Trigger Current (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 ohms, $T_C = 25^oC$) * (Anode Voltage = 7.0 Vdc, R_L = 100 ohms, $T_C = -65^oC$)	14	I_{GT}	 – –	 50 100	mA
Gate Trigger Voltage (Continuous dc) * (Anode Voltage = rated V_{DRM}, R_L = 100 ohms, $T_C = 105^oC$) (Anode Voltage = 7.0 Vdc, R_L = 100 ohms, $T_C = 25^oC$) * (Anode Voltage = 7.0 Vdc, R_L = 100 ohms, $T_C = -65^oC$)	12	V_{GT}	 0.2 – –	 – 1.5 2.0	Volts
*Holding Current (Anode Voltage = 7.0 Vdc, gate open, $T_C = 105^oC$)	18	I_H	 3.0	 –	mA
*Forward "On" Voltage (I_{TM} = 5 Adc, PW = 1.0 ms max, Duty cycle ≤ 1%)	8	V_{TM}	 2.6		Volts
*Dynamic Forward "On" Voltage (0.5 μs after 50% decay point on dynamic forward voltage waveform.) Forward Current: 30 A pulse Gate Pulse: at 200 mA, PW = 1.0 μs, t_r = 20 ns	7	v_{TM}	 –	 25	Volts
*Turn-On Time (2) I_{TM} = 30A Delay Time — All types Rise Time — 2N4199 and 2N4200 2N4201 2N4202 2N4203 and 2N4204	 1, 9 1, 11	 t_d t_r	 – – – – –	 200 200 150 130 100	ns
*Pulse Turn-Off Time Test Conditions: PFN discharge; Forward Current = 30 A pulse; Reverse Current = 5.0 A, $T_C = 85^oC$, dv/dt = 250 V/μs to Rated V_{DRM}; Reverse anode voltage during turn-off interval = 0 V; Reverse gate bias during turn-off interval = 6.0 V.	2, 13	t_q	 –	 20	μs
*Forward Voltage Application Rate (Linear Rise of Voltage) ($T_C = 105^oC$, gate open, V_D = Rated V_{DRM})	16	dv/dt	 250	 –	V/μs

*V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. When checking forward or reverse blocking capability, these devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage. Other voltage units available upon request.

TEST CIRCUITS

FIGURE 1 — TURN-ON TIME



*Two 1N4937 fast-recovery diodes in series each shunted by a 180 kΩ resistor.

FIGURE 2 — TURN-OFF TIME

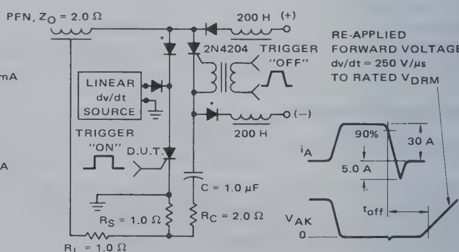


FIGURE 3 – MAXIMUM ALLOWABLE FORWARD PULSE CURRENT

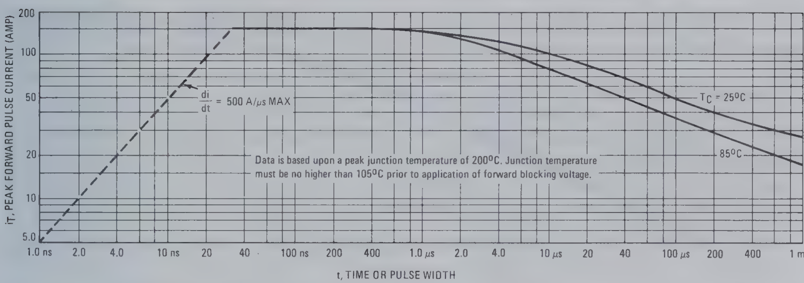


FIGURE 4 – DERATING USING NO SWITCHING LOSSES

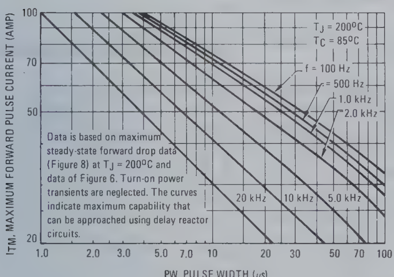
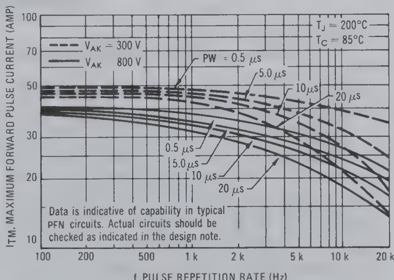


FIGURE 5 – DERATING USING TYPICAL SWITCHING LOSSES



DESIGN NOTE

Use of Transient Thermal Resistance Data

A train of periodical power pulses can be represented by the model shown in Fig. A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Fig. 6 was calculated for various duty cycles from:

$$r(t) = D + (1 - D) \cdot r(t_A + t_p) + r(t_A) - r(t_p)$$

To find $\theta_{JC}(t)$ multiply the value obtained from Fig. 6 by the steady-state value $\theta_{JC}(\infty)$. Use 3°C/W for worst-case results; use 2°C/W for typical information.

DESIGN EXAMPLE

A 2N4199 discharging a PFN, transient power pulse shown in Fig. C.

Conditions: V_{AK} = 150 V., I_{PK} = 44 A., f = 5000 Hz.

Determine: ΔT

Method 1: (See Fig. A) $P_A t_A$ is chosen to have the same energy as the actual power pulse, i.e.: the area under the curves are equal. P_A equals the peak of the actual power pulse. At a pulse repetition frequency of 5000 Hz and T_A = 2.14 μs (D = 0.0107); the reading on Fig. 6 is 0.039.

$\therefore \Delta T = r(t)\, R_{\theta JC}(\infty)\, P_A = (0.039)\,(3)\,(1000) = 120°C.$

Method 2: For a power waveform where the time of the peak power is short compared to the total transient, the foregoing method results in an overly large safety factor. A pulse model closer to the real case is shown in Fig. B. Using the transient thermal resistance information for D = 0 in Fig. 6, $\Delta T(t_4)$ and $\Delta T(t_5)$ can be evaluated from

$$\Delta T(t_4) = \left[P_1\,[r(T_1) + (1 - D_1) \cdot r(T + T_1) + D - r(T)] + P_2[(1 - D_2) \cdot r(T) + D_2 - r(T - T_2)]\right] R_{\theta JC}(\infty)$$

$$\Delta T(t_5) = \left[P_1\,[r(T_1 + T_2) + (1 - D_1) \cdot r(T + T_1 + T_2) - r(T + T_2) - r(T_2)] + P_2\,[r(T_2) + (1 - D_2) \cdot r(T + T_2) + D_2 - r(T)]\right] R_{\theta JC}(\infty)$$

The two results are compared; the one with higher value is taken for worst-case design. For the problem, values for the equivalent pulses of Fig. B are P_1 = 1000 W, P_2 = 700 W, T_1 = 1.05 μs, T_2 = 1.55 μs, $D_1 = 5.25(10^{-3})$, $D_2 = 7.75(10^{-3})$.

(CONTINUED)

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
*Peak Forward and Reverse Blocking Current	17	I_{DRM}	–	2.0	mA
(Rated V_{DRM} and V_{RRM}, $T_C = 105^oC$, gate open)		I_{RRM}	–	2.0	
Gate Trigger Current (Continuous dc)	14	I_{GT}			mA
(Anode Voltage = 7.0 Vdc, R_L = 100 ohms, $T_C = 25^oC$)			–	50	
* (Anode Voltage = 7.0 Vdc, R_L = 100 ohms, $T_C = -65^oC$)			–	100	
Gate Trigger Voltage (Continuous dc)	12	V_{GT}			Volts
* (Anode Voltage = rated V_{DRM}, R_L = 100 ohms, $T_C = 105^oC$)			0.2	–	
(Anode Voltage = 7.0 Vdc, R_L = 100 ohms, $T_C = 25^oC$)			–	1.5	
* (Anode Voltage = 7.0 Vdc, R_L = 100 ohms, $T_C = -65^oC$)			–	2.0	
*Holding Current	18	I_H			mA
(Anode Voltage = 7.0 Vdc, gate open, $T_C = 105^oC$)			3.0	–	
*Forward "On" Voltage	8	V_{TM}			Volts
(I_{TM} = 5 Adc, PW = 1.0 ms max, Duty cycle ≤ 1%)			2.6		
*Dynamic Forward "On" Voltage	7	v_{TM}			Volts
(0.5 μs after 50% decay point on dynamic forward voltage waveform.)					
Forward Current: 30 A pulse			–	25	
Gate Pulse: at 200 mA, PW = 1.0 μs, t_r = 20 ns					
*Turn-On Time (2) I_{TM} = 30A					ns
Delay Time — All types	1, 9	t_d	–	200	
Rise Time — 2N4199 and 2N4200	1, 11	t_r	–	200	
2N4201			–	150	
2N4202			–	130	
2N4203 and 2N4204			–	100	
*Pulse Turn-Off Time	2, 13	t_q			μs
Test Conditions: PFN discharge; Forward Current = 30 A pulse;			–	20	
Reverse Current = 5.0 A, $T_C = 85^oC$, dv/dt = 250 V/μs to Rated V_{DRM};					
Reverse anode voltage during turn-off interval = 0 V;					
Reverse gate bias during turn-off interval = 6.0 V.					
*Forward Voltage Application Rate (Linear Rise of Voltage)	16	dv/dt			V/μs
($T_C = 105^oC$, gate open, V_D = Rated V_{DRM})			250	–	

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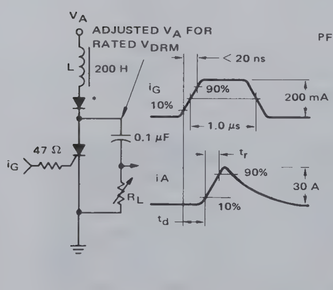
TEST CIRCUITS

FIGURE 1 — TURN-ON TIME



*Two 1N4937 fast-recovery diodes in series each shunted by a 180 kΩ resistor.

FIGURE 2 — TURN-OFF TIME

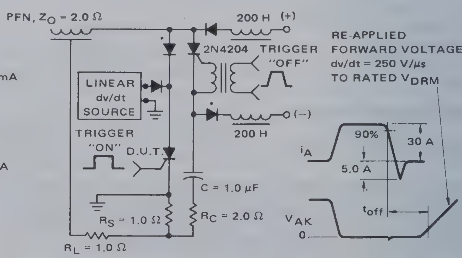


FIGURE 3 – MAXIMUM ALLOWABLE FORWARD PULSE CURRENT

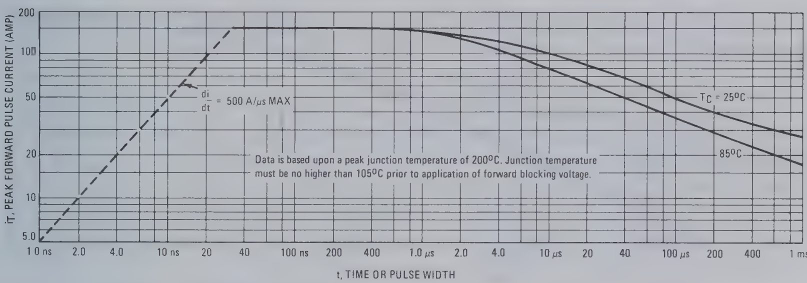


FIGURE 4 – DERATING USING NO SWITCHING LOSSES

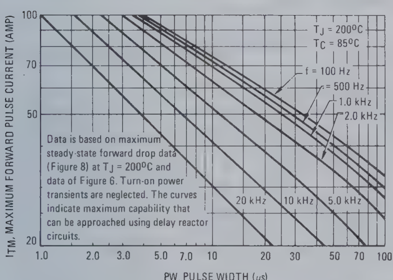
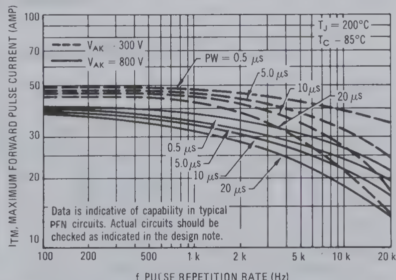


FIGURE 5 – DERATING USING TYPICAL SWITCHING LOSSES



DESIGN NOTE

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$$r(t) = D + (1 - D) \cdot r(t_A + t_p) + r(t_A) - r(t_p)$$

To find $\theta_{JC}(t)$ multiply the value obtained from Fig. 6 by the steady-state value $\theta_{JC}(\infty)$. Use 3°C/W for worst-case results; use 2°C/W for typical information.

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Conditions: V_{AK} = 150 V., I_{PK} = 44 A., f = 5000 Hz.

Determine: ΔT

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$\therefore \Delta T = r(t)\, R_{\theta JC}(\infty)\, P_A = (0.039)\,(3)\,(1000) = 120°C.$

Method 2: For a power waveform where the time of the peak power is short compared to the total transient, the foregoing method results in an overly large safety factor. A pulse model closer to the real case is shown in Fig. B. Using the transient thermal resistance information for D = 0 in Fig. 6, $\Delta T(t_4)$ and $\Delta T(t_5)$ can be evaluated from

$$\Delta T(t_4) = \left[P_1 \left[r(T_1) + (1 - D_1) \cdot r(T + T_1) + D - r(T)\right] + P_2\left[(1 - D_2) \cdot r(T) + D_2 - r(T - T_2)\right]\right] R_{\theta JC}(\infty)$$

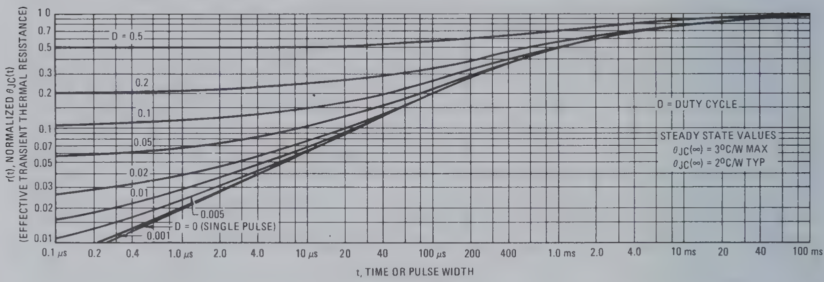
$$\Delta T(t_5) = \left[P_1 \left[r(T_1 + T_2) + (1 - D_1) \cdot r(T + T_1 + T_2) - r(T + T_2) - r(T_2)\right] + P_2 \left[r(T_2) + (1 - D_2) \cdot r(T + T_2) + D_2 - r(T)\right]\right] R_{\theta JC}(\infty)$$

The two results are compared; the one with higher value is taken for worst-case design. For the problem, values for the equivalent pulses of Fig. B are P_1 = 1000 W, P_2 = 700 W, T_1 = 1.05 μs, T_2 = 1.55 μs, $D_1 = 5.25(10^{-3})$, $D_2 = 7.75(10^{-3})$.

(CONTINUED)

2.3

FIGURE 6 – NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE



FORWARD "ON" VOLTAGE DATA

FIGURE 7 – TYPICAL DYNAMIC FORWARD "ON" VOLTAGE

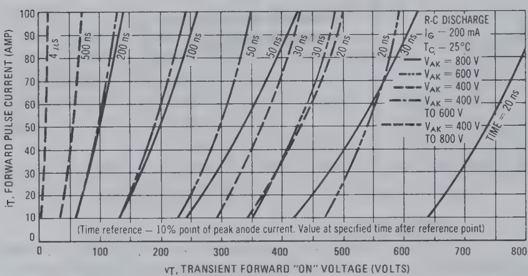
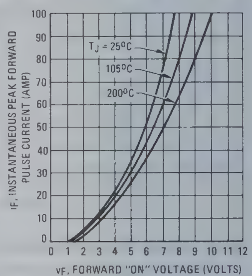


FIGURE 8 – MAXIMUM STEADY-STATE



DESIGN NOTE CONTINUED

$$\Delta T(t_4) = [\ 1000\ [0.0205 + (1 - 5.25 \cdot 10^{-3})\ 0.27 + 5.25 \cdot 10^{-3} - 0.27] + 700\ [(1 - 7.75 \cdot 10^{-3})\ 0.27 + 7.75 \cdot 10^{-3} - 0.27]\ ]\ 3 = 93.51^{\circ}C$$

$$\Delta T(t_5) = [\ 1000\ [0.032 + (1 - 5.25 \cdot 10^{-3})\ 0.27 + 5.25 \cdot 10^{-3} - 0.27 - 0.0205] + 700\ [0.025 + (1 - 7.75 \cdot 10^{-3})\ 0.27 + 7.75 \cdot 10^{-3} - 0.27]\ ]\ 3 = 105.6^{\circ}C$$

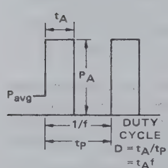


FIGURE A – SIMPLE MODEL

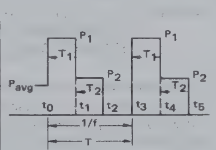


FIGURE B – MORE ACCURATE MODEL

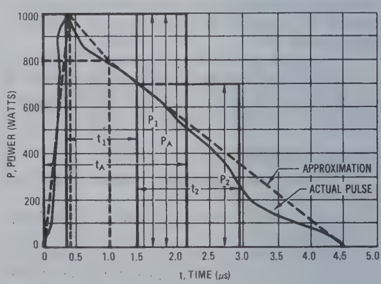
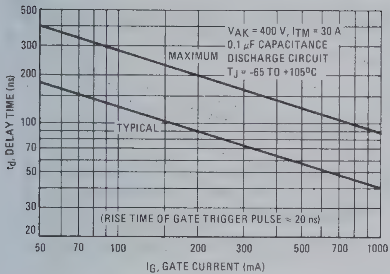


FIGURE C – AN ACTUAL TRANSIENT POWER PULSE

SWITCHING CHARACTERISTICS

FIGURE 9 – DELAY TIME



TRIGGERING CHARACTERISTICS

FIGURE 10 – TYPICAL PULSE TRIGGER CHARGE/CURRENT

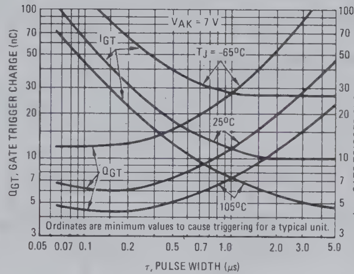


FIGURE 11 – CURRENT RISE TIME

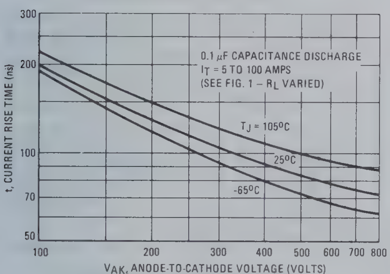


FIGURE 12 – DC GATE TRIGGER VOLTAGE

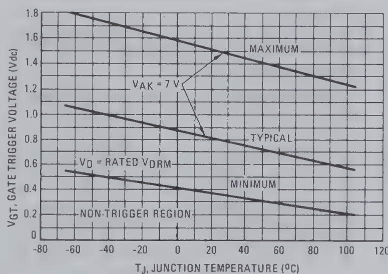


FIGURE 13 – TYPICAL TURN-OFF TIME

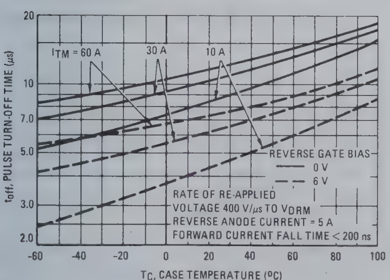
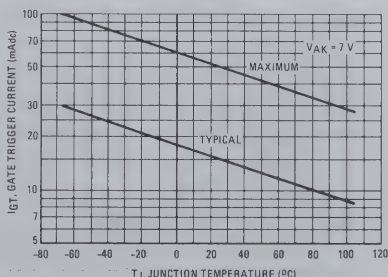


FIGURE 14 – DC GATE TRIGGER CURRENT



2.3

2.3

FIGURE 15 — TYPICAL BLOCKING VOLTAGE DERATING

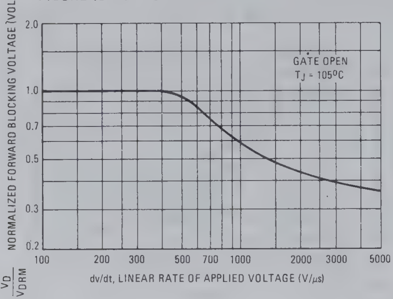


FIGURE 16 — TYPICAL LINEAR dv/dt CAPABILITY

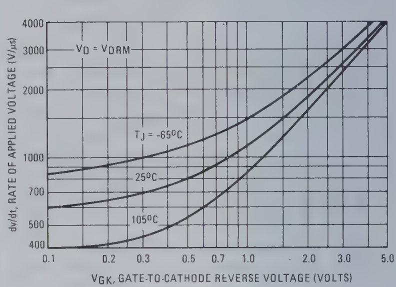


FIGURE 17 — FORWARD BLOCKING CURRENT

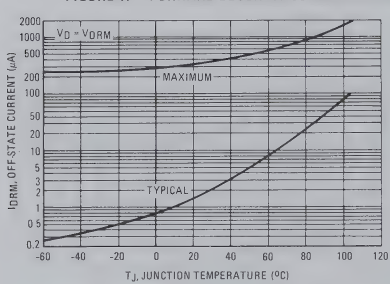


FIGURE 18 — HOLDING CURRENT

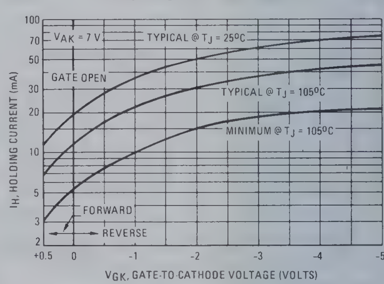


FIGURE 19 — TYPICAL ANODE-TO-CATHODE CAPACITANCE

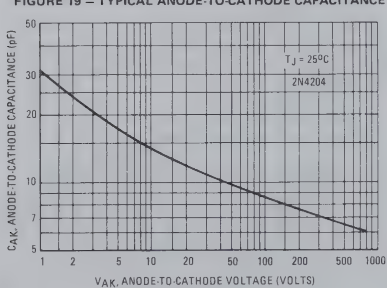
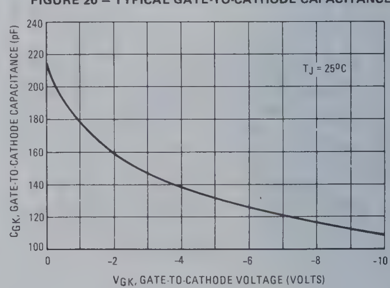


FIGURE 20 — TYPICAL GATE-TO-CATHODE CAPACITANCE



2N4212 thru 2N4216

MOTOROLA

REVERSE BLOCKING TRIODE THYRISTOR

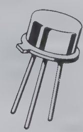
. . . all-diffused PNPN devices designed for operation in mA/μA signal or detection circuits.

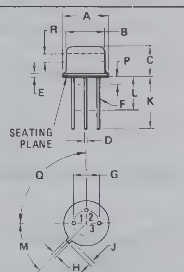
- Low-Level Gate Characteristics — I_{GT} = 100 μA Max @ 25°C
- Low Holding Current — I_{HX} = 3.0 mA Max @ 25°C
- Anode Common To Case
- Glass-to-Metal Bond for Maximum Hermetic Seal

SILICON CONTROLLED RECTIFIERS

PNPN

1.6 AMPERES RMS
25–200 VOLTS





STYLE 3:
PIN 1. CATHODE
2. GATE
3. ANODE (CONNECTED TO CASE)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO -39

***MAXIMUM RATINGS** (T_J = 125°C unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Peak Repetitive Forward and Reverse Blocking Voltage	V_{DRM} or V_{RRM}		Volt
2N4212		25	
2N4213		50	
2N4214		100	
2N4215		150	
2N4216		200	
Forward Current RMS (All Conduction Angles)	$I_{T(RMS)}$	1.6	Amp
Peak Surge Current (One Cycle, 60 Hz) No Repetition until Thermal Equilibrium is Restored	I_{TSM}	15	Amp
Peak Gate Power — Forward	P_{GFM}	0.1	Watt
Average Gate Power — Forward	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current — Forward	I_{GFM}	0.1	Amp
Peak Gate Voltage — Forward	V_{GFM}	6.0	Volt
Reverse	V_{GRM}	6.0	
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Solder Temperature (> 1/16.. from case, 10 sec. max)	—	+230	°C

*JEDEC Registered Values.

2.3

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms)

Characteristics	Symbol	Min	Max	Unit
*Peak Forward and Reverse Blocking Current (Rated V_{DRM} and V_{RRM}, T_J = 125°C)	I_{DRM} or I_{RRM}	–	200	µA
*Forward "On" Voltage (I_{TM} = 1.0 Adc peak)	V_{TM}	–	1.5	Volt
Gate Trigger Current (Note 2) (V_D = 7.0 V, R_L = 100 ohms)	I_{GT}			µAdc
(T_C = 25°C)		–	100	
(T_C = –65°C)		–	300	
Gate Trigger Voltage	V_{GT}			Volt
(V_D = 7.0 V, R_L = 100 ohms, T_C = 25°C)		–	0.8	
*(V_D = 7.0 V, R_L = 100 ohms, T_C = –65°C)		–	1.0	
*(V_D = Rated V_{DRM}, R_L = 100 ohms, T_J = 125°C)		0.1	–	
Holding Current (V_D = 7.0 V) T_C = 25°C	I_{HX}		3.0	mA
*T_C = –65°C			7.0	
Turn-On Time	t_{on}	Circuit dependent,		
Turn-Off Time	t_{off}	consult manufacturer		

* JEDEC Registered Values

Notes: 1. V_{DRM} and V_{RRM} can be applied for all types on a continuous dc basis without incurring damage.

2. R_{GK} current is not included in measurement.

Thyristor devices shall not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

Thyristor devices shall not have a positive bias applied to the gate concurrently with a negative potential applied to the anode.

FIGURE 1 — CASE TEMPERATURE vs CURRENT

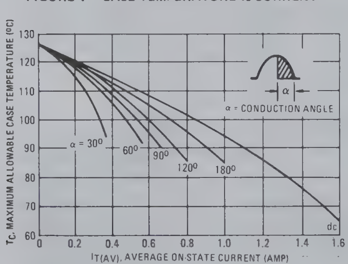
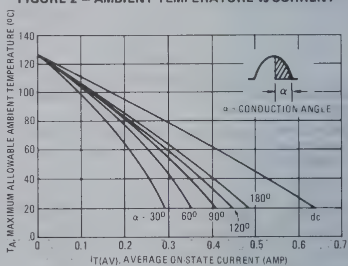


FIGURE 2 — AMBIENT TEMPERATURE vs CURRENT



MOTOROLA

2N4441 thru 2N4444

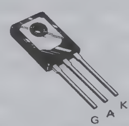
SILICON CONTROLLED RECTIFIERS

8.0 AMPERES RMS
50 thru 600 VOLTS

REVERSE BLOCKING TRIODE THYRISTORS

. . . designed for high-volume consumer phase-control applications such as motor speed, temperature, and light controls and for switching applications in ignition and starting systems, voltage regulators, vending machines, and lamp drivers requiring:

- Small, Rugged, Thermopad Construction — for Low Thermal Resistance, High Heat Dissipation, and Durability.
- Practical Level Triggering and Holding Characteristics @ 25°C
  I_{GT} = 7.0 mA (Typ)
  I_H = 6.0 mA (Typ)
- Low "On" Voltage — V_{TM} = 1.0 Volt (Typ) @ 5.0 Amp @ 25°C
- High Surge Current Rating — I_{TSM} = 80 Amp



MAXIMUM RATING (T_J = 100°C unless otherwise noted.)

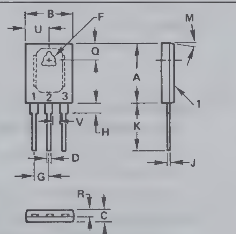
Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (Note1) 2N4441 2N4442 2N4443 2N4444	V_{DRM} V_{RRM}	 50 200 400 600	Volts
*Non-Repetitive Peak Reverse Blocking Voltage (t = 5.0 ms (max) duration) 2N4441 2N4442 2N4443 2N4444	V_{RSM}	 75 300 500 700	Volts
*RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	8.0	Amp
Average On-State Current, T_C = 73°C	$I_{T(AV)}$	5.1	Amp
*Peak Non-Repetitive Surge Current (1/2 cycle, 60 Hz preceded and followed by rated current and voltage)	I_{TSM}	80	Amp
Circuit Fusing (T_J = −40 to +100°C; t = 1.0 to 8.3 ms)	I^2t	25	A^2s
*Peak Gate Power	P_{GM}	5.0	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GM}	2.0	Amp
*Peak Reverse Gate Voltage	V_{RGM}	10	Volts
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Mounting Torque (6-32 screw) (Note 2)	–	8.0	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	–	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	–	°C/W

*Indicates JEDEC Registered Data.

Notes 1, 2, See page 2



STYLE 1:
PIN 1. CATHODE
2. ANODE
3. GATE

NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05

2.3

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}, T_J = 100°C, gate open)	I_{DRM}	–	–	2.0	mA
Peak Reverse Blocking Current (V_D = Rated V_{RRM}, T_J = 100°C, gate open)	I_{RRM}	–	–	2.0	mA
Gate Trigger Current (Continuous dc) (V_D = 7.0 Vdc, R_L = 100 Ohms) T_C = 25°C * T_C = –40°C	I_{GT}	– 	7.0 	30 60	mA
Gate Trigger Voltage (Continuous dc) (V_D = 7.0 Vdc, R_L = 100 Ohms) T_C = 25°C (V_D = 7.0 Vdc, R_L = 100 Ohms) T_C = -40°C (V_D = Rated V_{DRM}, R_L = 100 Ohms) T_J = 100°C	V_{GT}	– – 0.2	0.75 – –	1.5 2.5 –	Volts
Peak On-State Voltage (Pulse Width = 1.0 to 2.0 ms, Duty Cycle ⩽ 2.0%) (I_{TM} = 5.0 A peak) * (I_{TM} = 15.7 A peak)	V_{TM}	– –	1.0 –	1.5 2.0	Volts
Holding Current (V_D = 7.0 Vdc, gate open) T_C = 25°C * T_C = -40°C	I_H	– –	6.0 –	40 70	mA
Gate Controlled Turn-On Time (I_{TM} = 5.0 A, I_{GT} = 20 mA, V_D = Rated V_{DRM})	t_{gt}	–	1.0	–	μs
Circuit Commutated Turn-Off Time (I_{TM} = 5.0 A, I_R = 5.0 A) (I_{TM} = 5.0 A, I_R = 5.0 A, T_J = 100°C)	t_q	– –	15 20	– –	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_J = 100°C, Gate Open)	dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data

Note 1. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.

Note 2. Torque rating applies with use of torque washer (Shakeproof WD19522 #6 or equivalent). Mounting torque in excess of 8 in. lbs. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common.

For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C.

FIGURE 1 — ON-STATE CHARACTERISTICS

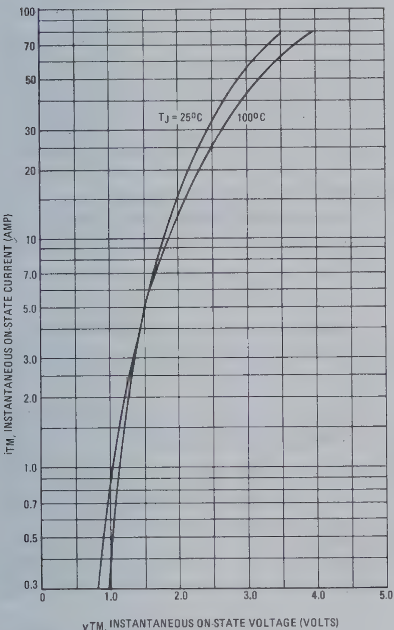


FIGURE 2 — MAXIMUM ON-STATE POWER DISSIPATION

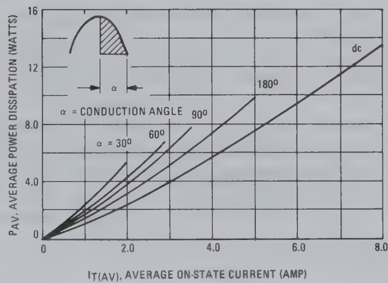


FIGURE 3 — AVERAGE CURRENT DERATING

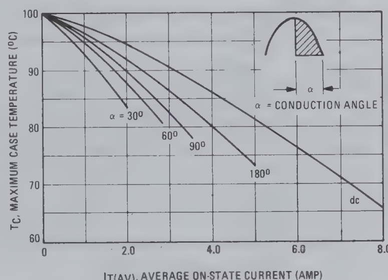


FIGURE 4 — THERMAL RESPONSE

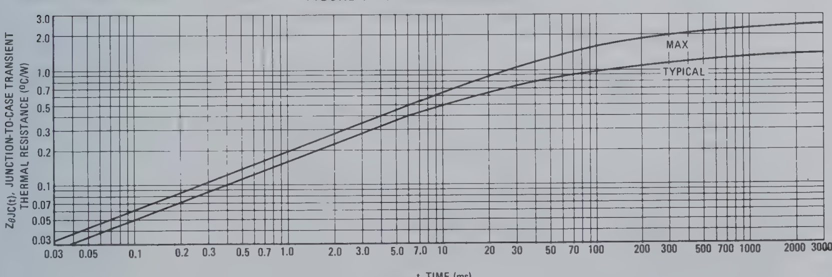


FIGURE 5 — MAXIMUM NON-REPETITIVE SURGE CURRENT

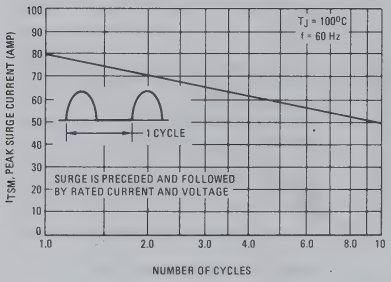
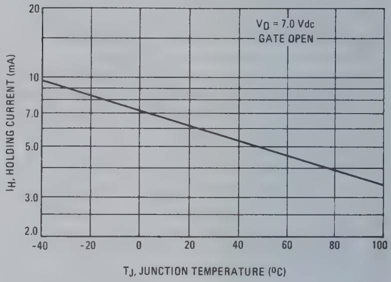


FIGURE 6 — TYPICAL HOLDING CURRENT



2.3

FIGURE 7 — TYPICAL GATE TRIGGER CURRENT

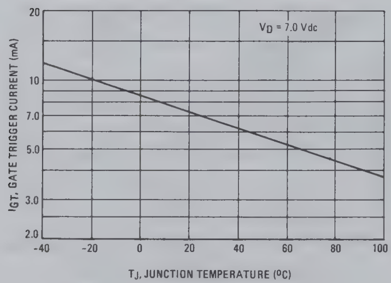
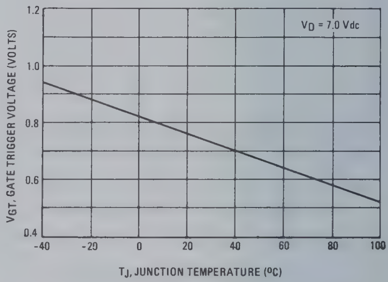
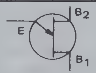


FIGURE 8 — TYPICAL GATE TRIGGER VOLTAGE



MOTOROLA

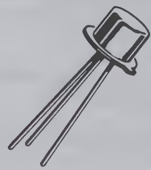


SILICON UNIJUNCTION TRANSISTOR

. . . designed for pulse and timing circuits, sensing circuits, and thyristor trigger circuits.

- Low Peak-Point Current — I_P = 0.4 μA Max
- Low Emitter Reverse Current — I_{EO} = 50 nA Max
- Fast Switching

PN UNIJUNCTION TRANSISTORS

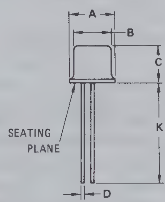


2.3

***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted)

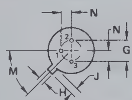
Rating	Symbol	Value	Unit
RMS Power Dissipation (1)	P_D	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current (2)	i_e	1.5	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage (3)	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	−65 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

*Indicates JEDEC Registered Data
(1) Derate 3.0 mW/°C increase in ambient temperature
(2) Duty cycle ≤ 1%, PRR = (see figure 6)
(3) Based upon power dissipation at T_A = 25°C



NOTE:
1. PIN 3 CONNECTED TO CASE.

STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	—	0.500	—
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A - 01
(TO-18 Except for Lead Position)

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

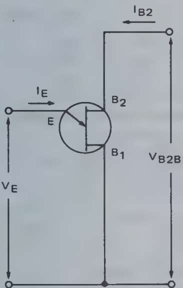
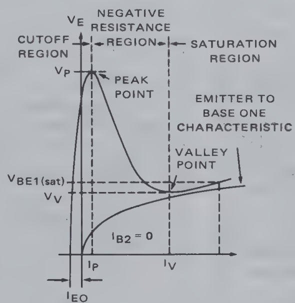


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES



2.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Rating		Figure No.	Symbol	Min	Typ	Max	Unit
*Intrinsic Standoff Ratio (1)		4, 8	η				–
(V_{B2B1} = 10 V)	2N4851			0.56	–	0.75	
	2N4852, 2N4853			0.70	–	0.85	
*Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)		11, 12	r_{BB}	4.7	–	9.1	k ohms
*Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = –65 to +125°C)		12	α_{BB}	0.2	–	0.8	%/°C
Emitter Saturation Voltage (2) (V_{B2B1} = 10 V, I_E = 50 mA)			$V_{EB1(sat)}$	–	2.5	–	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)			$I_{B2(mod)}$	–	15	–	mA
*Emitter Reverse Current		7	I_{EB2O}				µA
(V_{B2E} = 30 V, I_{B1} = 0)	2N4851, 2N4852			–	–	0.1	
	2N4853			–	–	0.05	
*Peak-Point Emitter Current		9, 10	I_P				µA
(V_{B2B1} = 25 V)	2N4851, 2N4852			–	–	2.0	
	2N4853			–	–	0.4	
*Valley-Point Current (2)		13, 14	I_V				mA
(V_{B2B1} = 20 V, R_{B2} = 100 ohms)	2N4851			2.0	–	–	
	2N4852			4.0	–	–	
	2N4853			6.0	–	–	
*Base-One Peak Pulse Voltage	2N4851	3, 17	V_{OB1}	3.0	–	–	Volts
	2N4852			5.0	–	–	
	2N4853			6.0	–	–	
*Maximum Frequency of Oscillation		5	$f_{(max)}$	–	1.25	–	MHz

*Indicates JEDEC Registered Data.

(1) η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.49 volt at 25°C @ I_F = 10 µA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

(2) Use pulse techniques: PW ≈ 300 µs, duty cycle ⩽ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 3 – V_{OB1} TEST CIRCUIT

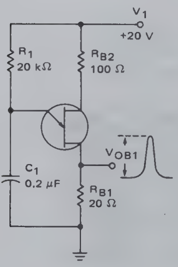
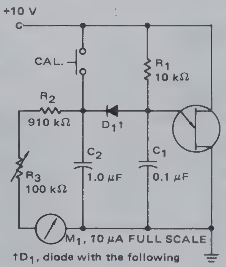


FIGURE 4 – η TEST CIRCUIT



†D_1, diode with the following characteristics:

V_F = 0.49 V @ I_F = 10 µA
I_R ⩽ 2.0 µA @ V_R = 20 V

FIGURE 5 – $f_{(max)}$ TEST CIRCUIT

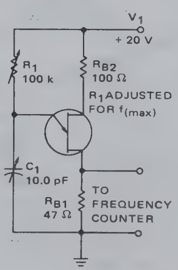
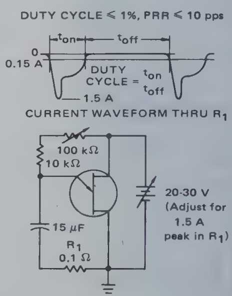


FIGURE 6 – PRR TEST CIRCUIT AND WAVEFORM



TYPICAL CHARACTERISTICS

FIGURE 7 — EMITTER REVERSE CURRENT

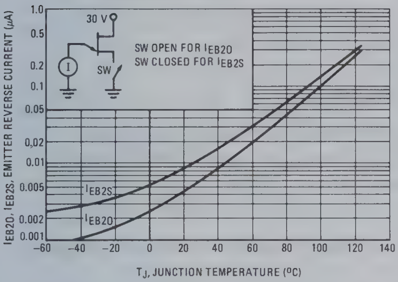
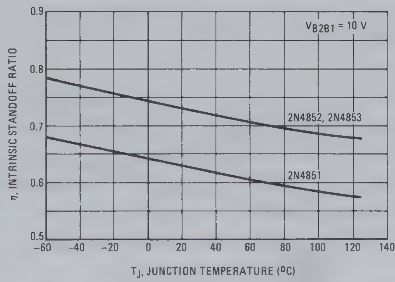


FIGURE 8 — INTRINSIC STANDOFF RATIO



PEAK POINT CURRENT

FIGURE 9 — EFFECT OF VOLTAGE

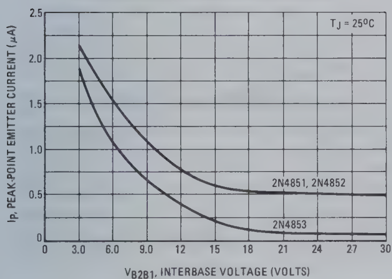
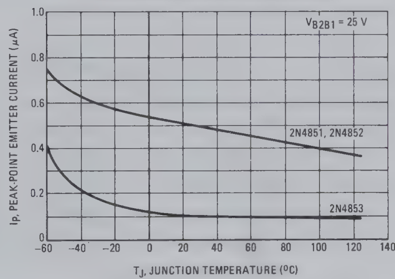


FIGURE 10 — EFFECT OF TEMPERATURE



INTERBASE RESISTANCE

FIGURE 11 — EFFECT OF VOLTAGE

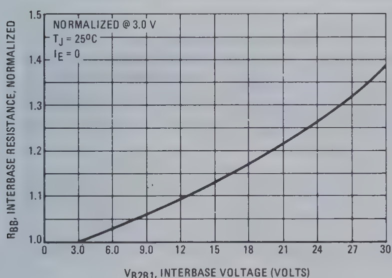
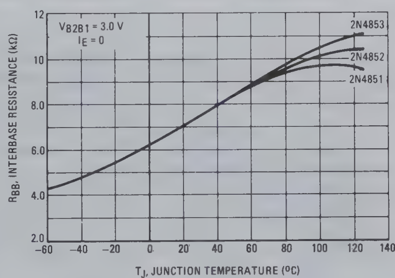


FIGURE 12 — EFFECT OF TEMPERATURE



2.3

TYPICAL CHARACTERISTICS

VALLEY CURRENT

FIGURE 13 — EFFECT OF VOLTAGE

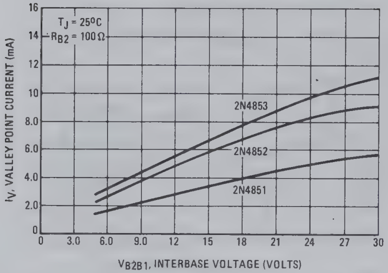
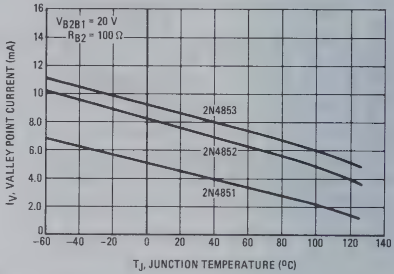


FIGURE 14 — EFFECT OF TEMPERATURE



2.3

VALLEY VOLTAGE

FIGURE 15 — EFFECT OF VOLTAGE

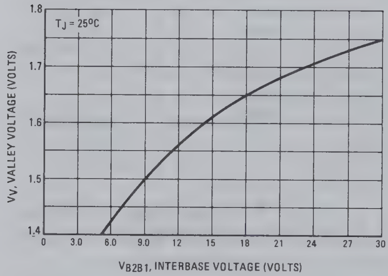


FIGURE 16 — EFFECT OF TEMPERATURE

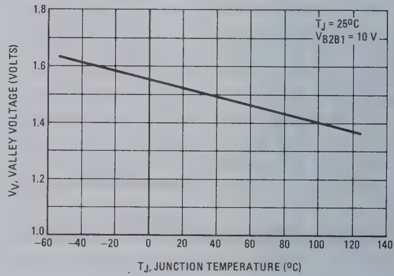
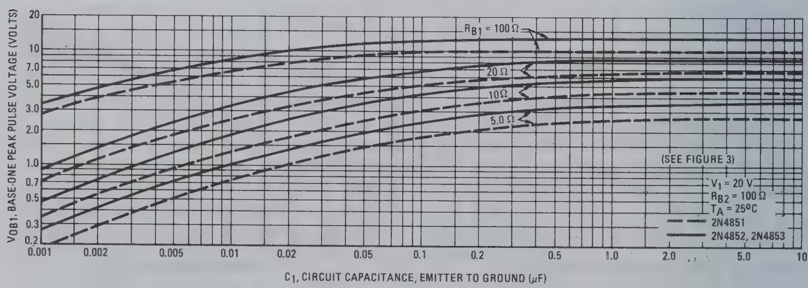
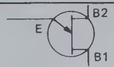


FIGURE 17 — OUTPUT VOLTAGE



2N4870
2N4871

MOTOROLA

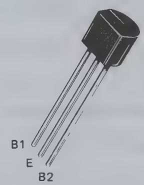


SILICON UNIJUNCTION TRANSISTORS

. . .designed for pulse and timing circuits, sensing circuits, and thyristor trigger circuits. These devices feature:

- Low Peak Point Current — 1.0 μA Typical
- Low Emitter Reverse Current — 5.0 nA Typical
- Passivated Surface for Reliability and Uniformity
- One-Piece Injection-Molded Unibloc‡ Plastic Package for Economy and Reliability
- High η for greater bandwith.

PN UNIJUNCTION TRANSISTORS

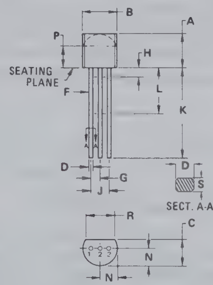


2.3

MAXIMUM RATINGS (T_A = 25° unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D*	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current**	i_e**	1.5	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage†	V_{B2B1}†	35	Volts
Operating Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

*Derate 3.0 mW/°C increase in ambient temperature.
**Duty cycle ≤ 1%, PRR = 10 PPS (see Figure 5).
†Based upon power dissipation at T_A = 25°C.



STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

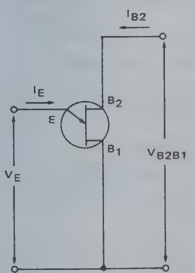
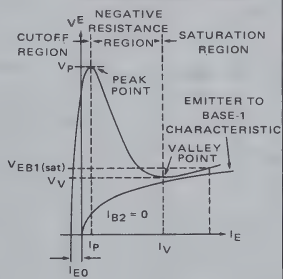


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES



2.3

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio* (V_{B2B1} = 10 V)	4, 7	η*				–
2N4870			0.56	–	0.75	
2N4871			0.70	–	0.85	
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)	10,11	R_{BB}	4.0	6.0	9.1	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = –65 to +125°C)	11	αR_{BB}	0.10	–	0.90	%/°C
Emitter Saturation Voltage** (V_{B2B1} = 10 V, I_E = 50 mA)		$V_{EB1(sat)}$**	–	2.5	–	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	–	15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	6	I_{EB2O}	–	0.005	1.0	μA
Peak-Point Emitter Current (V_{B2B1} = 25 V)	8, 9	I_P	–	1.0	5.0	μA
Valley-Point Current** (V_{B2B1} = 20 V, R_{B2} = 100 ohms)	12, 13	I_V**				mA
2N4870			2.0	5.0	–	
2N4871			4.0	7.0	–	
Base-One Peak Pulse Voltage 2N4870	3, 16	V_{OB1}	3.0	6.0	–	Volts
2N4871			5.0	8.0	–	

* η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.49 volt at 25°C @ I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_R. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

** Use pulse techniques: PW ≈ 300 μs, duty cycle ≤ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 3 – V_{OB1} TEST CIRCUIT

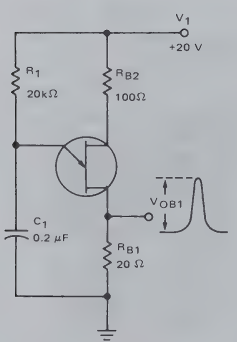
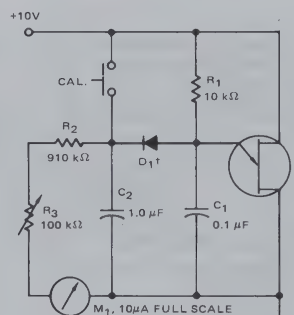


FIGURE 4 – η TEST CIRCUIT

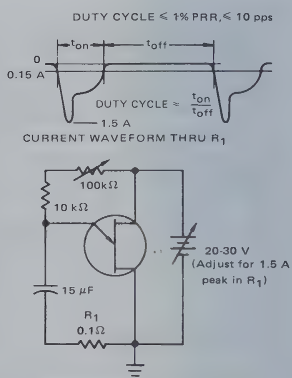


†D_1, diode with the following characteristics:

V_F = 0.49 V @ I_F = 10 μA

I_R ≤ 2.0 μA @ V_R = 20 V

FIGURE 5 – PRR TEST CIRCUIT AND WAVEFORM



TYPICAL CHARACTERISTICS

FIGURE 6 – EMITTER REVERSE CURRENT

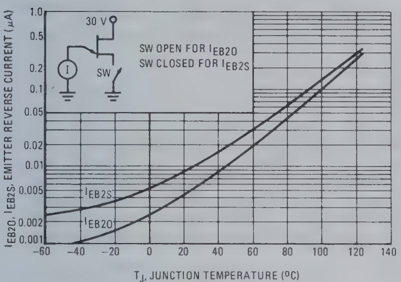
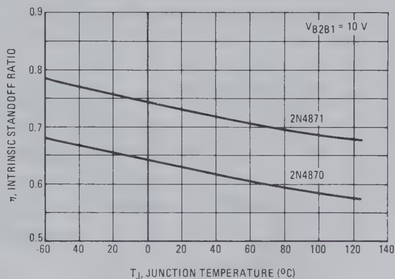


FIGURE 7 – INTRINSIC STANDOFF RATIO



PEAK POINT CURRENT

FIGURE 8 – EFFECT OF VOLTAGE

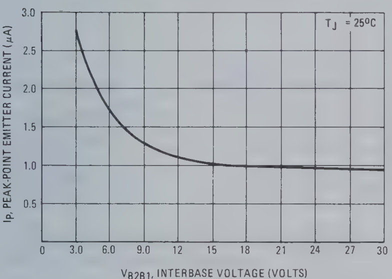
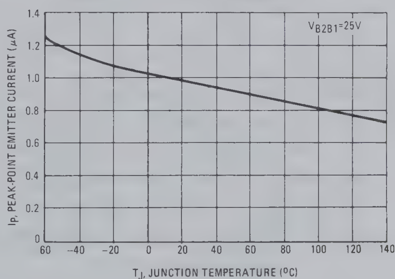


FIGURE 9 – EFFECT OF TEMPERATURE



INTERBASE RESISTANCE

FIGURE 10 – EFFECT OF VOLTAGE

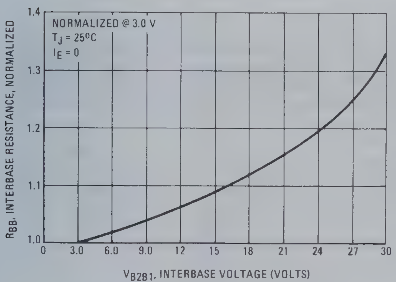
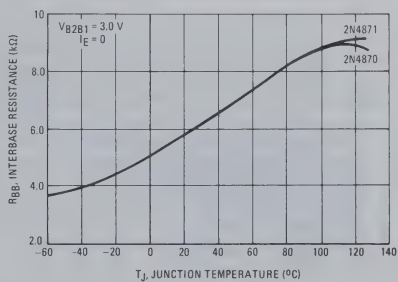


FIGURE 11 – EFFECT OF TEMPERATURE



2.3

TYPICAL CHARACTERISTICS

VALLEY CURRENT

FIGURE 12 — EFFECT OF VOLTAGE

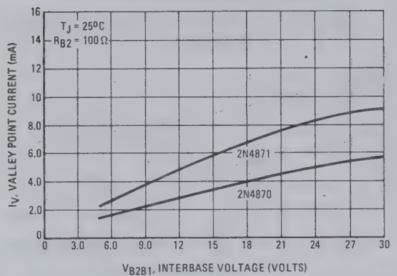
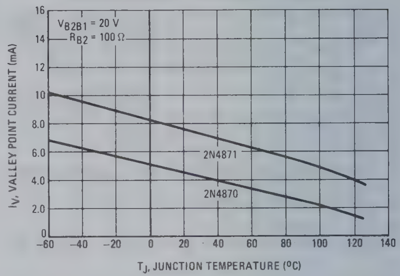


FIGURE 13 — EFFECT OF TEMPERATURE



2.3

VALLEY VOLTAGE

FIGURE 14 — EFFECT OF VOLTAGE

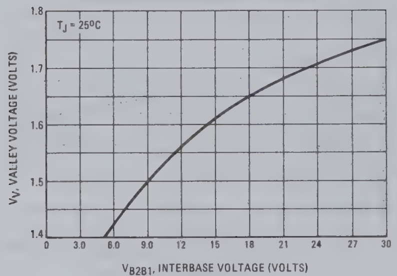


FIGURE 15 — EFFECT OF TEMPERATURE

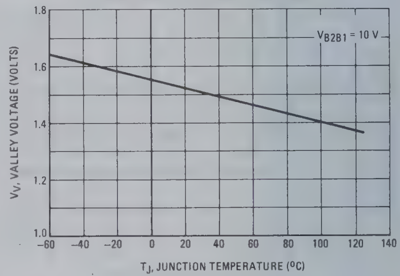
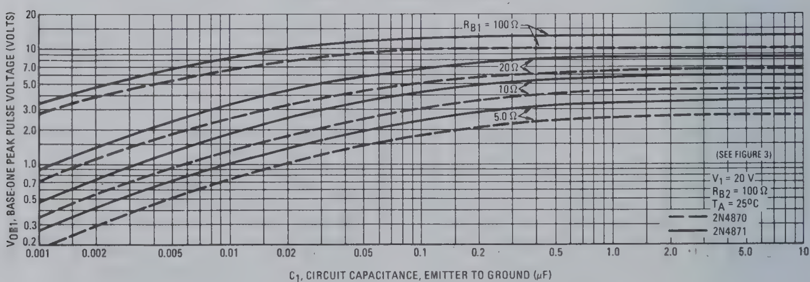
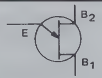


FIGURE 16 — OUTPUT VOLTAGE



MOTOROLA



SILICON UNIJUNCTION TRANSISTORS

. . . designed for military and industrial use in pulse, timing, triggering, sensing, and oscillator circuits. The annular process provides low leakage current, fast switching and low peak-point currents as well as outstanding reliability and uniformity. Recommended usage includes:

- Silicon Controlled Rectifier Triggering Circuits — 2N4948
- Long-time Delay Circuits — 2N4949

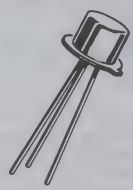
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D	360*	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current**	i_e	1.0**	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Storage Temperature Range	T_{stg}	-65 to +200	°C

* Derate 2.4 mW/°C increase in ambient temperature. Total power dissipation (available power to Emitter and Base-Two) must be limited by external circuitry. Interbase voltage (V_{B2B1}) limited by power dissipation, $V_{B2B1} = \sqrt{R_{BB} \cdot P_D}$.

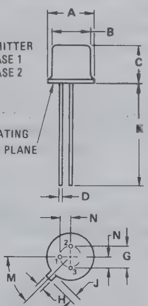
** Capacitance discharge current must fall to 0.37 Amp within 3.0 ms and PRR ≤ 10 PPS.

PN UNIJUNCTION TRANSISTORS



NOTE:
1. PIN 3 CONNECTED TO CASE.

STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A-01

TO-18 PACKAGE
(Except for lead position)

2.3

2.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) Note 1	2N4948	η	0.55	–	0.82	–
	2N4949		0.74	–	0.86	
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)	2N4948, 2N4949	R_{BB}	4.0	7.0	12.0	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = –65°C to +100°C)		αR_{BB}	0.1	–	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) Note 2		$V_{EB1(sat)}$	–	2.5	3.0	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	12	15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)		I_{EB2O}	–	5.0	10	nA
(V_{B2E} = 30 V, I_{B1} = 0, T_A = 125°C)			–	–	1.0	µA
Peak Point Emitter Current (V_{B2B1} = 25 V)	2N4948	I_P	–	0.6	2.0	µA
	2N4949		–	0.6	1.0	
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) Note 2	2N4948, 2N4949	I_V	2.0	4.0	–	mA
Base-One Peak Pulse Voltage (Note 3, Figure 3)	2N4949	V_{OB1}	3.0	5.0	–	Volts
	2N4948		6.0	8.0	–	
Maximum Oscillation Frequency (Figure 4)		$f_{(max)}$	–	1.25	–	MHz

NOTES

1. Intrinsic standoff ratio.
η, is defined by equation:

$$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
$V_{(EB1)}$ = Emitter to Base-One Junction Diode Drop
(≈ 0.45 V @ 10 µA)

2. Use pulse techniques: PW ≈ 300 µs duty cycle ≤ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

3. Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

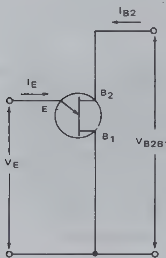


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES
(Exaggerated to Show Details)

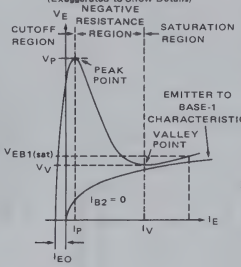


FIGURE 3 – V_{OB1} TEST CIRCUIT
(Typical Relaxation Oscillator)

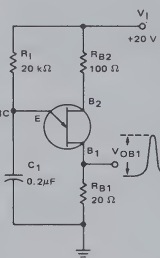
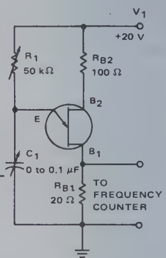


FIGURE 4 – F(max) MAXIMUM FREQUENCY TEST CIRCUIT



2N5060 thru 2N5064

MOTOROLA

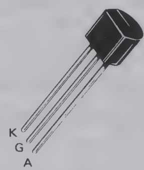
REVERSE BLOCKING TRIODE THYRISTORS

. . . Annular PNPN devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current — 200 μA Maximum
- Low Reverse and Forward Blocking Current — 50 μA Maximum, T_C = 125°C
- Low Holding Current — 5.0 mA Maximum
- Passivated Surface for Reliability and Uniformity
- Also Available with TO-5 or TO-18 Lead Form

SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
30 thru 200 VOLTS



2.3

MAXIMUM RATINGS(1)

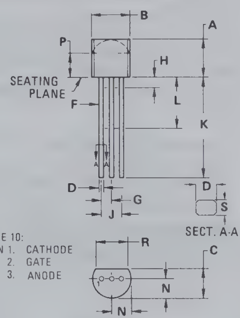
Rating	Symbol	Value	Unit
*Peak Repetitive Reverse Blocking Voltage (1) (R_{GK} = 1000 ohms, T_C = +125°C)	V_{DRM} V_{RRM}		Volts
2N5060		30	
2N5061		60	
2N5062		100	
2N5063		150	
2N5064		200	
On-State Current RMS (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
*Average On-State Current (T_C = 67°C) (T_C = 102°C)	$I_{T(AV)}$	0.51 0.255	Amp
*Peak Non-Repetitive Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.15	A^2s
*Peak Gate Power, T_A = 25°C	P_{GM}	0.1	Watt
*Average Gate Power, T_A = 25°C	$P_{G(AV)}$	0.01	Watt
*Peak Forward Gate Current, T_A = 25°C (300 μs, 120 PPS)	I_{FGM}	1.0	Amp
*Peak Reverse Gate Voltage	V_{RGM}	5.0	Volts
*Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-65 to +125	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
*Lead Solder Temperature (Lead Length ⩾ 1/16″ from case, 10 s Max)	—	+230*	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

(1) Ratings apply for zero or negative gate voltage. Device ratings exclude having a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
(2) This measurement is made with the case mounted "flat side down" on a heat sink and held in position by means of a metal clamp over the curved surface.

*Indicates JEDEC Registered Data.



STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (4) (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage (Note 1) (T_C = 125°C, R_{GK} = 1000 Ohms)	2N5060 2N5061 2N5062 2N5063 2N5064	V_{DRM}	30 60 100 150 200	– – – – –	– – – – –	Volts
*Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C, R_{GK} = 1000 Ohms)		I_{DRM}	–	–	50	μA
*Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C, R_{GK} = 1000 Ohms)		I_{RRM}	–	–	50	μA
*Forward "On" Voltage (Note 2) (I_{TM} = 1.2 A peak @ T_A = 25°C)		V_{TM}	–	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 3) *(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms, R_{GK} = 1000 Ohms)	T_C = 25°C T_C = -65°C	I_{GT}	– –	– –	200 350	μA
Gate Trigger Voltage (Continuous dc) *(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms) (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 25°C T_C = -65°C T_C = 125°C	V_{GT} V_{GD}	– – 0.1		0.8 1.2 –	Volts
Holding Current *(Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = 25°C T_C = -65°C	I_H	– –	– –	5.0 10	mA
Turn-On Time Delay Time Rise Time (I_{GT} = 1.0 mA, R_{GK} = 1.0 Ohm, V_D = Rated V_{DRM}, Forward Current = 1.0 A, di/dt = 6.0 A/μs)		t_d t_r	– –	3.0 0.2	– –	μs
Turn-Off Time (Forward Current = 1.0 A pulse, Pulse Width = 50 μs, 0.1% Duty Cycle, di/dt = 6.0 A/μs, dv/dt = 20 V/μs, I_{GT} = 1.0 mA, R_{GK} = 1.0 k Ohm)	2N5060,2N5061 2N5062,5063,5064	tq	– –	10 30	– –	μs
Forward Voltage Application Rate (Rated V_{DRM}, R_{GK} = 1.0 k, Exponential)		dv/dt	–	30	–	V/μs

*Indicates JEDEC Registered Data.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
3. R_{GK} current is not included in measurement.
4. For electrical characteristics for Gate-to-cathode resistance other than 1000 ohms see Motorola Bulletin EB-30.

2.3

CURRENT DERATING

FIGURE 1 — MAXIMUM CASE TEMPERATURE

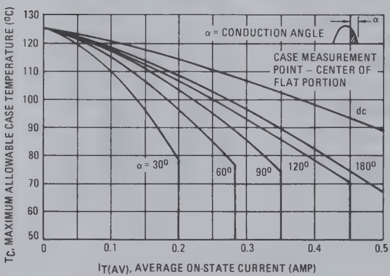


FIGURE 2 — MAXIMUM AMBIENT TEMPERATURE

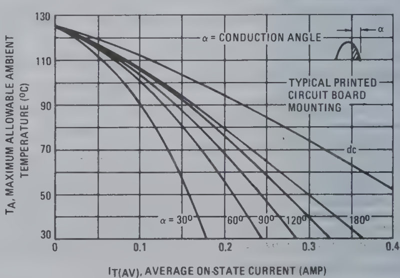


FIGURE 3 — TYPICAL FORWARD VOLTAGE

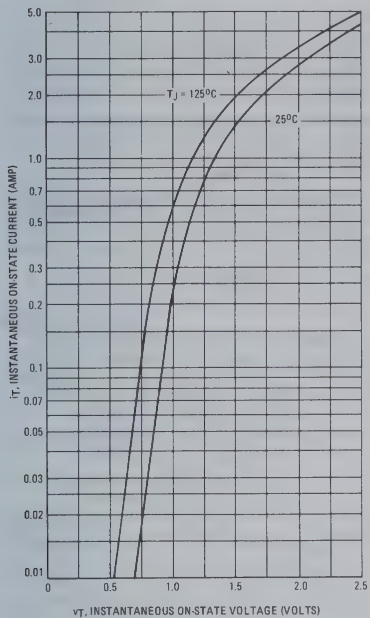


FIGURE 4 — MAXIMUM NON-REPETITIVE SURGE CURRENT

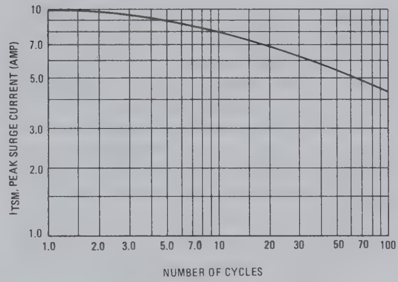


FIGURE 5 — POWER DISSIPATION

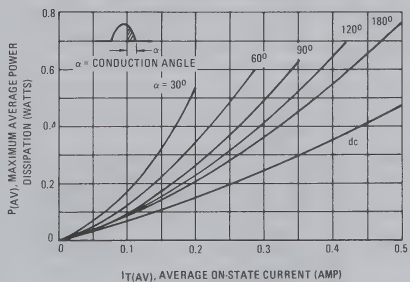
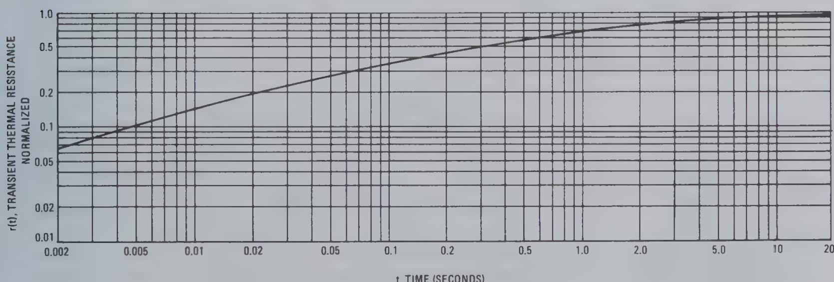


FIGURE 6 — THERMAL RESPONSE



2.3

2.3

TYPICAL CHARACTERISTICS

FIGURE 7 – GATE TRIGGER VOLTAGE

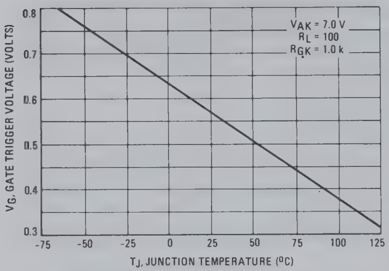


FIGURE 8 – GATE TRIGGER CURRENT

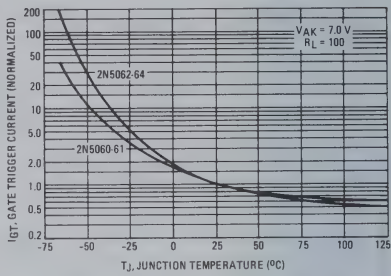


FIGURE 9 – HOLDING CURRENT

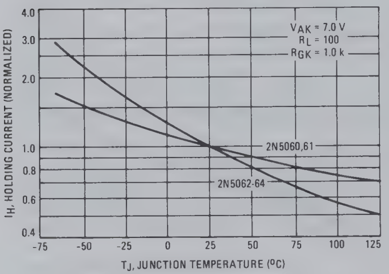
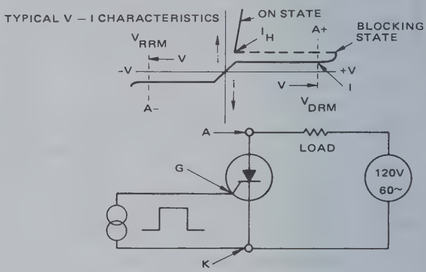


FIGURE 10 – CHARACTERISTICS AND SYMBOLS

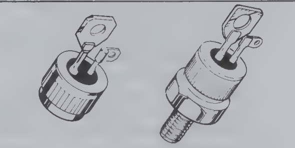


MOTOROLA

2N5164 thru 2N5171

SILICON CONTROLLED RECITIFIER

20 AMPERES RMS
50-600 VOLTS



REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Supplied in Either Pressfit or Stud Package
- High Surge Current Rating — I_{TSM} = 240 Amp
- Low On-State Voltage — 1.2 V (Typ) @ I_{TM} = 20 Amp
- Practical Level Triggering and Holding Characteristics — 40 mA (Max) and 50 mA (Max) @ T_C = 25°C

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Forward and *Repetitive Reverse Blocking Voltage (1), (2) 2N5164, 2N5168	V_{DRM} or V_{RRM}	50	Volts
2N5165, 2N5169		200	
2N5166, 2N5170		400	
2N5167, 2N5171		600	
*Non-repetitive Peak Reverse Blocking Voltage 2N5164, 2N5168	V_{RSM}	75	Volts
2N5165, 2N5169		300	
2N5166, 2N5170		500	
2N5167, 2N5171		700	
On-State Current RMS	$I_{T(RMS)}$	20	Amp
Average On-State Current (T_C = 67°C)	$I_{T(AV)}$	13	Amp
Circuit Fusing (T_J = -40 to +100°C, t ⩽ 8.3 ms)	I^2t	235	A^2s
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, T_J = -40 to +100°C) Preceded and followed by rated current and voltage.	I_{TSM}	240	Amp
*Peak Gate Power (Maximum Pulse Width = 10 μs)	P_{GM}	5.0	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current (Maximum Pulse Width = 10 μs)	I_{GM}	2.0	Amp
Peak Gate Voltage	V_{GM}	10	Volts
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque 2N5168-2N5171		30	in. lb.

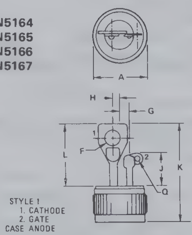
THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
*Thermal Resistance, Junction to Case 2N5164, 65, 66, 67	$R_{\theta JC}$	1.0	1.5	°C/W
2N5168, 69, 70, 71		1.1	1.6	

(1) V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.

(2) Devices should not be operated with a positive bias applied to the gate concurrent with a negative potential applied to the anode.

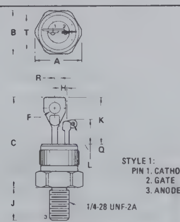
2N5164
2N5165
2N5166
2N5167



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
F	–	4 06		0.160
G	2 16	2 41	0.085	0.095
H	1.52	1.78	0.060	0.070
J	7.62	8 89	0.300	0.350
K		26 67	–	1.050
L		17.02	–	0.670
Q	1.40	2.16	0.055	0.085

CASE 310-01

2N5168
2N5169
2N5170
2N5171



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0 090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

2.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM} @ $T_J = 100^oC$, gate open)	I_{DRM}	–	5.0	mA
*Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ $T_J = 100^oC$, gate open)	I_{RRM}	–	5.0	mA
Gate Trigger Current (Continuous dc) (2)	I_{GT}			mA
(V_D = 7.0 Vdc, R_L = 100 Ω)		–	40	
*(V_D = 7.0 Vdc, R_L = 100 Ω, $T_C = -40^oC$)		–	75	
Gate Trigger Voltage (Continuous dc)	V_{GT}			Volts
(V_D = 7.0 Vdc, gate open)		–	1.5	
*(V_D = 7.0 Vdc, R_L = 100 Ω, $T_C = -40^oC$)		–	2.5	
*(V_D = Rated V_{DRM}, R_L = 100 Ω, $T_J = 100^oC$)		0.2	–	
Peak On-State Voltage (Pulse Width = 1.0 ms max, duty cycle ≤ 1%)	V_{TM}			Volts
(I_{TM} = 20 A)		–	1.5	
*(I_{TM} = 41 A)		–	1.7	
Holding Current	I_H			mA
(V_D = 7.0 Vdc, gate open)		–	50	
*(V_D = 7.0 Vdc, gate open, $T_C = -40^oC$)		–	90	
		Typical		
Gate Controlled Turn-On Time ($t_d + t_r$) (I_{TM} = 20 A, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})	t_{gt}	1.0		μs
Circuit Commutated Turn-Off Time	t_q			μs
(I_{TM} = 10 A, I_R = 10 A)		20		
(I_{TM} = 10 A, I_R = 10 A, $T_J = 100^oC$) ($V_D = V_{DRM}$ = rated voltage) (dv/dt = 30 V/μs)		30		
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Wave Form, Gate open, $T_J = 100^oC$)	dv/dt	50		V/μs

*Indicates JEDEC registered data.

EFFECT OF TEMPERATURE UPON TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 — GATE TRIGGER CURRENT

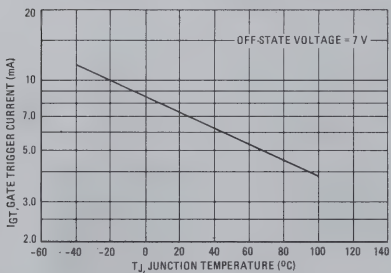
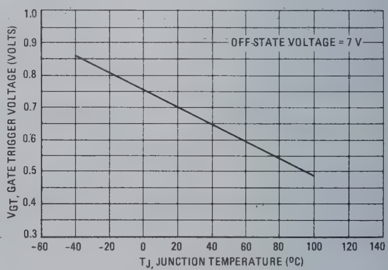


FIGURE 2 — GATE TRIGGER VOLTAGE



MAXIMUM ALLOWABLE NON-REPETITIVE SURGE CURRENT

FIGURE 3 — 60 Hz SURGES

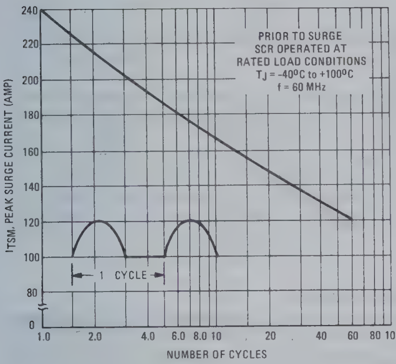
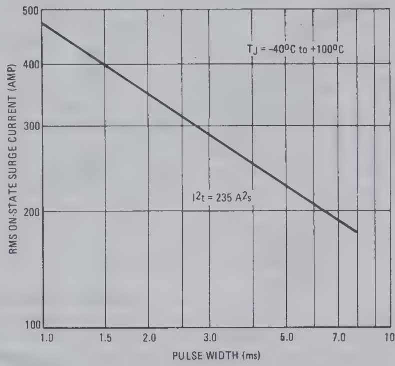


FIGURE 4 — SUB-CYCLE SURGES



2.3

FIGURE 5 — GATE TRIGGER CHARACTERISTICS

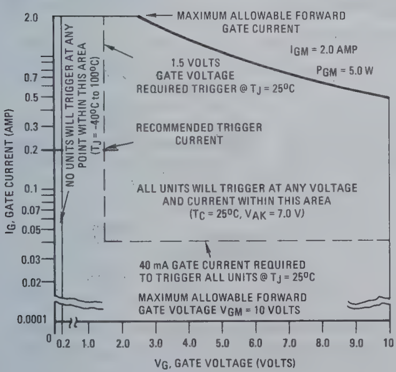
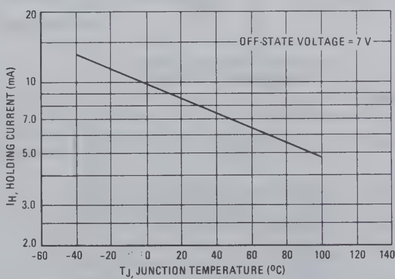


FIGURE 6 — EFFECT OF TEMPERATURE ON TYPICAL HOLDING CURRENT



DERATING AND DISSIPATION FOR RESISTIVE AND INDUCTIVE LOADS (f = 60 to 400 Hz, SINE WAVE)

FIGURE 7 – AVERAGE CURRENT DERATING

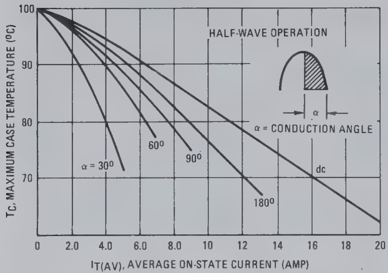
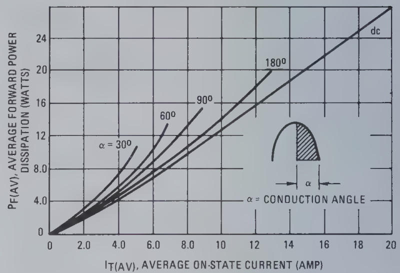


FIGURE 8 – ON-STATE POWER DISSIPATION



2.3

FIGURE 9 – ON-STATE CHARACTERISTICS

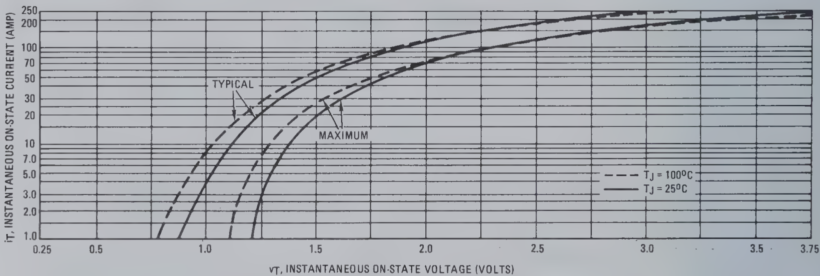


FIGURE 10 – TYPICAL THERMAL RESISTANCE OF PLATES

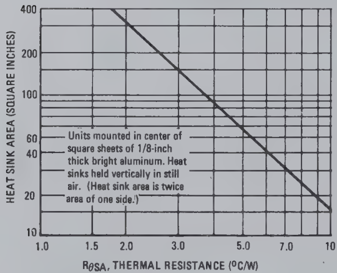
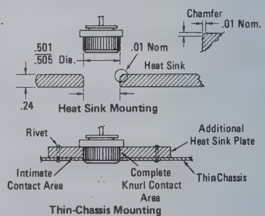


FIGURE 11 – MOUNTING DETAILS FOR PRESSFIT THYRISTORS



The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the rectifier during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the rectifier case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heat sink material. Recommended hardnesses are: copper – less than 50 on the Rockwell F scale; aluminum – less than 65 on the Brinell scale. A heat sink as thin as 1/8" may be used, but the interface thermal resistance will increase in proportion to the reduction of contact area. A thin chassis requires the addition of a back-up plate.

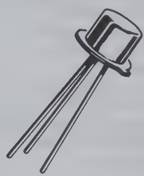
MOTOROLA

SILICON ANNULAR UNIJUNCTION TRANSISTORS

. . . characterized primarily for low interbase-voltage operation in sensing, pulse triggering, and timing circuits.

- Low R_{BB} Spread — 6.0 to 8.5 kΩ
- Low Peak-Point Current — I_P = 4.0 μA (Max) @ V_{B2B1} = 4.0 V
- Low Emitter Saturation Voltage — $V_{EB1(sat)}$ = 3.0 V (Max)
- Narrow Intrinsic Standoff Ratio — η = 0.72 to 0.80

PN UNIJUNCTION TRANSISTORS

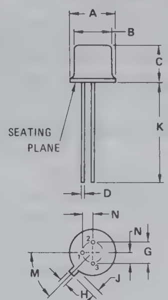


2.3

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D*	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current**	i_e**	1.5	A
Emitter Reverse Voltage	V_{B2E}	30	V
Interbase Voltage‡	V_{B2B1}‡	35	V
Operating Junction Temperature Range	T_J	–65 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +200	°C

*Derate 3.0 mW/°C increase in ambient temperature.
**Duty Cycle ≤ 1.0%, PRR = 10 PPS (see figure 5).
‡Based upon power dissipation at T_A = 25°C.



NOTE:
1. PIN 3 CONNECTED TO CASE.

STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A
(TO-18 Outline
Except for Lead Position)

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

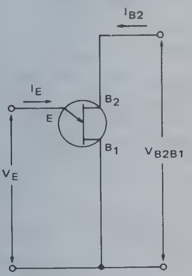
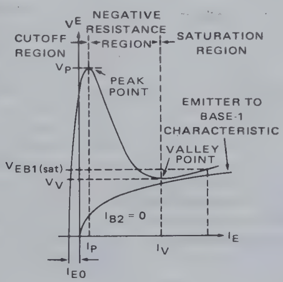


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES



ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
Intrinsic Standoff Ratio [1] ($V_{B2B1} = 10$ V)	4	η	0.72	0.80	–
Interbase Resistance ($V_{B2B1} = 3.0$ V, $I_E = 0$)		R_{BB}	6.0	8.5	kΩ
Interbase Resistance Temperature Coefficient ($V_{B2B1} = 3.0$ V, $I_E = 0$, $T_A = 0$ to 100^oC)		αR_{BB}	0.4	0.8	%/^oC
Emitter Saturation Voltage [2] ($V_{B2B1} = 10$ V, $I_E = 50$ mA)		$V_{EB1(sat)}$	–	3.0	V
Modulated Interbase Current ($V_{B2B1} = 10$ V, $I_E = 50$ mA)		$I_{B2(mod)}$	5.0	30	mA
Emitter Reverse Current ($V_{B2E} = 30$ V, $I_{B1} = 0$)		I_{EB2O}	–	10	nA
Peak-Point Emitter Current ($V_{B2B1} = 25$ V) ($V_{B2B1} = 4.0$ V)		I_P	– –	0.4 4.0	µA
Valley-Point Current [2] ($V_{B2B1} = 20$ V, $R_{B2} = 100$ ohms)		I_V	2.0	–	mA
Base-One Peak Pulse Voltage ($V_{BB} = 4.0$ volts)	3	V_{OB1}	1.0	–	V

[1] η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.45 volt at 25^oC @$I_F = 10\ \mu A$ and decreases with temperature at about 2.5 mV/^oC. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

[2] Use pulse techniques: PW ≈ 300 µs, Duty Cycle ≤ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 3 – V_{OB1} TEST CIRCUIT

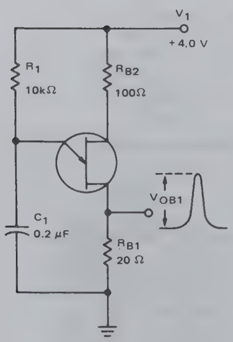
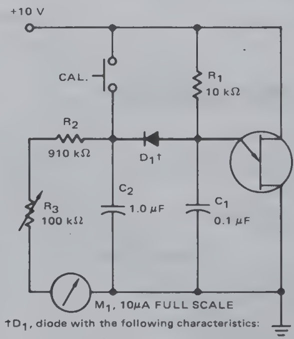


FIGURE 4 – η TEST CIRCUIT

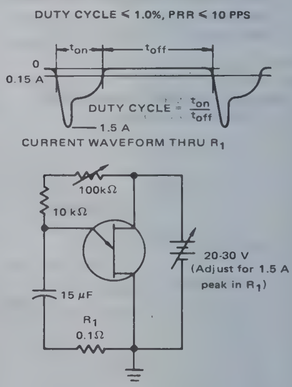


†D_1, diode with the following characteristics:

$V_F = 0.49$ V @ $I_F = 10\ \mu A$

$I_R \leq 2.0\ \mu A$ @ $V_R = 20$ V

FIGURE 5 – PRR TEST CIRCUIT AND WAVEFORM



2N5441 thru 2N5446

MOTOROLA

TRIACS

40 AMPERES RMS
200–600 VOLTS

2.3

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Isolated Stud for Ease of Assembly
- Gate Triggering Guaranteed In All 4 Quadrants

MAXIMUM RATINGS

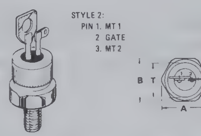
Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = –65 to +110°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
*Peak Principal Voltage 2N5441, 2N5444 2N5442, 2N5445 2N5443, 2N5446		 200 400 600	
*RMS On-State Current (T_C per Fig. 2) (T_C = +100°C) Full Sine Wave, 50 to 60 Hz	$I_{T(RMS)}$	 40 20	Amp
*Peak Non-Repetitive Surge Current (One Full Cycle of surge current at 60 Hz, preceeded and followed by a 40 A RMS current, T_J = +110°C)	I_{TSM}	300	Amp
*Peak Gate Power (Pulse Width = 10 μs Max)	P_{GM}	40	Watts
*Average Gate Power	$P_{G(AV)}$	0.75	Watt
*Peak Gate Current (10 μs Max)	I_{GM}	4.0	Amp
*Peak Gate Voltage	V_{GM}	30	Volts
*Operating Junction Temperature Range	T_J	–65 to +110	°C
*Storage Temperature Range	T_{stg}	–65 to +150	°C
*Stud Torque	–	30	in. lb.

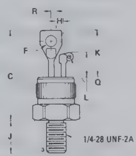
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case 2N5441, 2N5442, 2N5443 2N5444, 2N5445, 2N5446	$R_{\theta JC}$	 0.8 0.9 1.0	°C/W

*Indicates JEDEC Registered Data for 2N5441 thru 2N5446.

2N5444 thru 2N5446

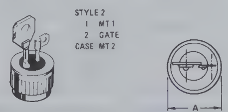


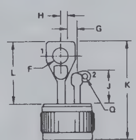


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.34	15.60	0.604	0.614
B	14 00	14.20	0.551	0 559
C	26.67	30.23	1.050	1 190
F	3.43	4 06	0.135	0 160
H	2.29 REF		0 090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7 62	8.89	0.300	0.350
Q	1.40	2 16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

2N5441 thru 2N5443





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.73	12.83	0.501	0.505
F	–	4.08	–	0 160
G	2.16	2.41	0.085	0.095
H	1.52	1.78	0.060	0.070
J	7.62	8.89	0.300	0.350
K	–	26.67	–	1.050
L	–	17.02	–	0.670
Q	1.40	2.16	0.055	0.085

CASE 310-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and either polarity of MT2 to MT1 voltage, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak On-State Voltage Rated V_{DRM} @ T_J = 110°C	I_{DRM}	–	0.5	4.0	mA
*Peak On-State Voltage I_{TM} = 56 A Peak, Pulse Width ≤ 1.0 ms, Duty Cycle ≤ 2.0%	V_{TM}	–	1.65	1.85	Volts
Gate Trigger Current (1) Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms	I_{GT}				mA
MT2 (+), G(+)		–	–	70	
MT2 (+), G(–)		–	–	70	
MT2 (–), G(–)		–	–	70	
MT2 (–), G(+)		–	–	100	
*MT2 (+), G(+); MT2 (–), G (–) T_C = –65°C		–	–	125	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –65°C		–	–	240	
*Gate Trigger Voltage Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms	V_{GT}				Volts
MT2 (+), G(+)		–	–	2.0	
MT2 (+), G(–)		–	–	2.0	
MT2 (–), G(–)		–	–	2.0	
MT2 (–), G(+)		–	–	2.5	
*All Quadrants, T_C = –65°C		–	–	3.4	
*Main Terminal Voltage = Rated V_{DRM} = R_L = 10 k ohms, T_J = +110°C		0.2	–	–	
*Holding Current Main Terminal Voltage = 12 Vdc, Gate Open Initiating Current = 150 mA	I_H				mA
T_C = 25°C		–	–	70	
*T_C = –65°C		–	–	100	
*Turn-On Time Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 56 A, Gate Source Voltage = 12 V, R_S = 12 Ohms, Rise Time = 0.1 µs, Pulse Width = 2.0 µs	t_{gt}	–	1.0	2.0	µs
*Critical Rate-of -Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 40 A, Commutating di/dt = 22 A/ms, gate energized	dv/dt(c)				V/µs
T_C = 70°C 2N5441, 2N5442, 2N5443		5.0	30	–	
= 65°C 2N5444, 2N5445, 2N5446		5.0	30	–	
		5.0	30	–	
Critical Rate of Rise of Off State Voltage Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 110°C	dv/dt				V/µs
2N5441, 2N5444		50			
2N5442, 2N5445		30			
2N5443, 2N5446		20			

*Indicates JEDEC Registered Data for 2N5441 thru 2N5446.

FIGURE 1 — ON-STATE POWER DISSIPATION

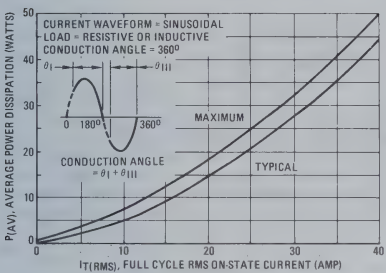


FIGURE 2 — RMS CURRENT DERATING

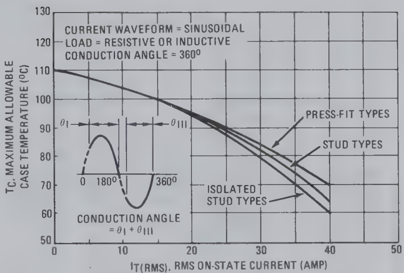


FIGURE 3 — TYPICAL GATE TRIGGER VOLTAGE

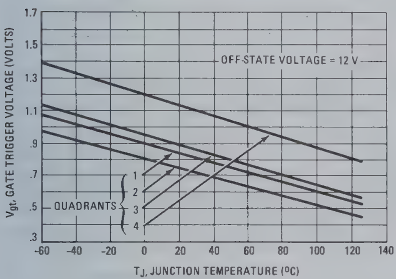


FIGURE 4 — TYPICAL GATE TRIGGER CURRENT

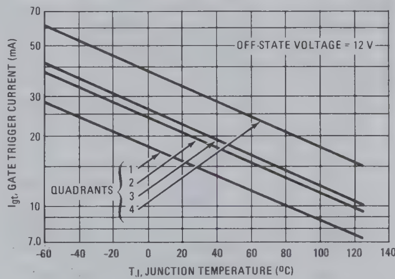
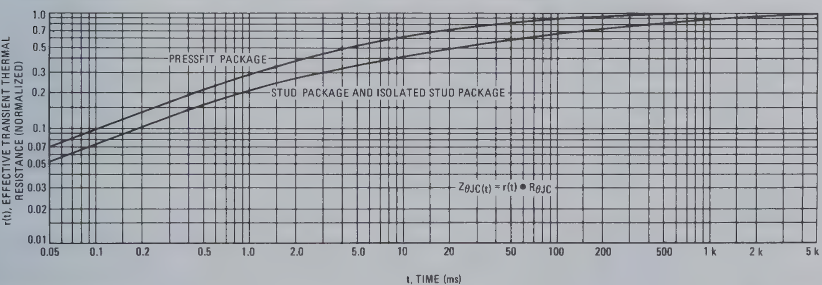


FIGURE 5 — TYPICAL THERMAL RESPONSE



2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current V_D = Rated V_{DRM} @ T_C = 100°C	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage I_{TM} = 14.2 A Peak, Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0%	V_{TM}	–	1.3	1.65	Volts
Gate Trigger Current, Pulse Width ≥ 50 μs (1) V_D = 12 Vdc, R_L = 12 Ohms MT2 (+), G (+); MT2 (–), G (–) MT2 (+), G (–); MT2 (–), G (+) *MT2 (+), G (+); MT2 (–), G (–), T_C = –65°C *MT2 (+), G (–); MT2 (–), G (+), T_C = –65°C	I_{GT}	 – – – –	 – – – –	 25 40 100 150	mA
Gate Trigger Voltage, Continuous dc (All Quadrants) V_D = 12 Vdc, R_L = 12 Ohms T_C = 25°C *T_C = –65°C V_D = Rated V_{DRM}, R_L = 125 Ω T_C = 100°C	V_{GT}	 – – 0.2	 – – –	 2.5 4.0 –	Volts
Holding Current V_D - 12 Vdc, Gate Open T_C = 25°C *T_C = –65°C	I_H	 – –	 – –	 30 200	mA
Gate Controlled Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 15 A Peak, I_{GT} = 160 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs MT2 (+), G (+); MT2 (–), G (–)	t_{gt}	–	1.0	2.5	μs
*Critical Rate-of-Rise of Commutation Voltage V_D = Rated V_{DRM}, I_{TM} = 14.2 A Peak, Commutating di/dt = 5.4 A/ms, gate unenergized T_C = 85°C	dv/dt(c)	 2.0	 10	 –	V/μs
Critical Rate-of-Rise of Off-State Voltage V_D = Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C: *2N5567, *2N5569, T4121B *2N5568, *2N5570, T4121D T4101M, T4111M, T4121M	dv/dt	 30 20 10	 150 100 75	 – – –	V/μs

*Indicates JEDEC Registered Data.
(1) All Voltage polarity reference to main terminal 1.

FIGURE 1 — RMS CURRENT DERATING (Isolated Stud)

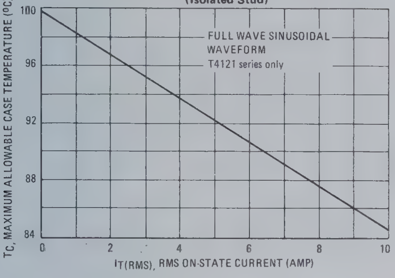


FIGURE 2 — RMS CURRENT DERATING (Pressfit and Stud)

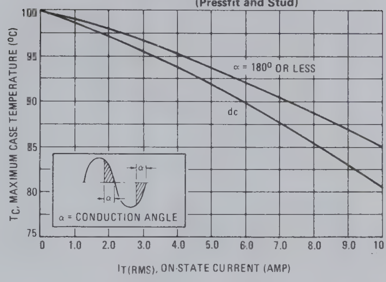


FIGURE 3 — POWER DISSIPATION (Isolated Stud)

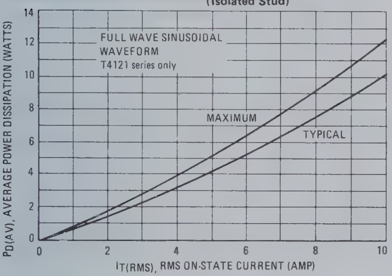


FIGURE 4 — POWER DISSIPATION (Pressfit and Stud)

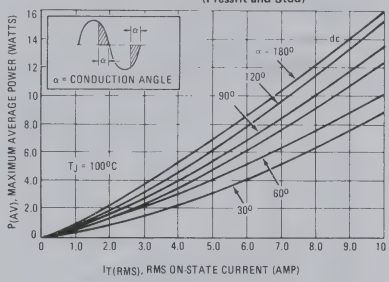


FIGURE 5 — TYPICAL GATE TRIGGER VOLTAGE

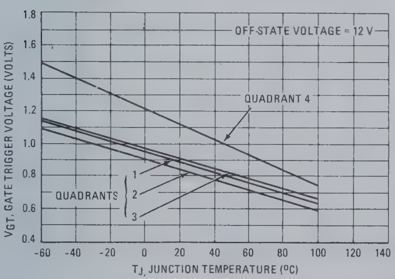
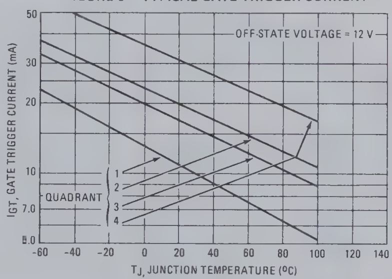


FIGURE 6 — TYPICAL GATE TRIGGER CURRENT



2.3

2.3

FIGURE 7 – ON-STATE CHARACTERISTICS

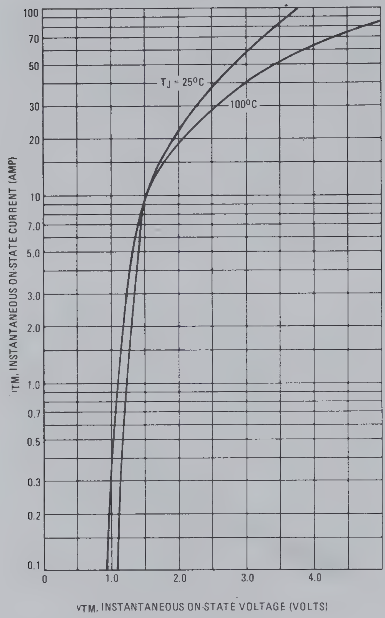


FIGURE 8 – TYPICAL HOLDING CURRENT

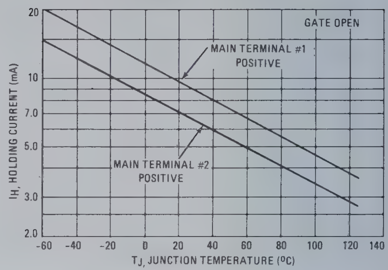


FIGURE 9 – MAXIMUM NON-REPETITIVE SURGE CURRENT

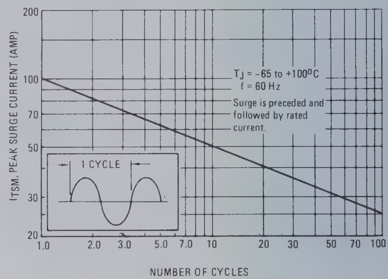
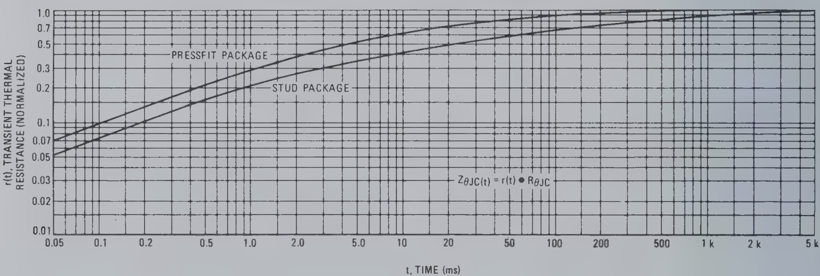


FIGURE 10 – TYPICAL THERMAL RESPONSE



2N5571 thru 2N5574
2N6145 thru 2N6147
T4100M, T4110M

MOTOROLA

TRIACS

15 AMPERES RMS
200–600 VOLTS

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 4 Quadrants

MAXIMUM RATINGS

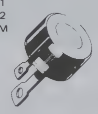
Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = −65 to +100°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
2N5571, 2N5573, 2N6145		200	
2N5572, 2N5574, 2N6146		400	
T4100M, T4110M, 2N6147		600	
*Peak Gate Voltage	V_{GM}	20	Volts
*RMS On-State Current	$I_{T(RMS)}$		Amp
(T_C = −65 to +80°C)		15	
(T_C = +85°C)		10	
*Peak Non-Repetitive Surge Current (One Full cycle of surge current at 60 Hz, preceeded and followed by rated current, T_C = +80°C)	I_{TSM}	100	Amp
Circuit Fusing (T_C = −65 to +80°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
Peak Gate Power	P_{GM}		Watts
*(T_C = 80°C, Pulse Width = 1.0 μs) 2N5571 thru 2N5574		16	
T4100M, T4110M		16	
*(T_C = 80°C, Pulse Width = 2.0 μs) 2N6145 thru 2N6147		20	
*Average Gate Power (T_C = +80°C, Pulse Width = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-65 to +100	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
Stud Torque	—		in. lb.
*2N5573, 2N5574, T4110M		30	
*2N6145, 2N6146, 2N6147			

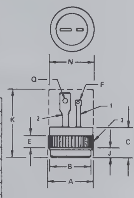
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

*Indicates JEDEC Registered Data.

2N5571
2N5572
T4100M



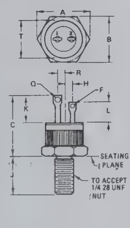


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54		0.100	–
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160

STYLE 3:
TERM. 1. GATE
2. MAIN TERMINAL 1
3. MAIN TERMINAL 2

CASE 174-03

2N5573
2N5574
T4110M

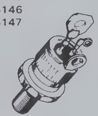


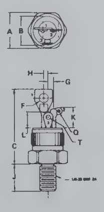
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

STYLE 3
TERM. 1. MAIN TERMINAL 1
2. GATE
STUD MAIN TERMINAL 2

CASE 175-02

2N6145
2N6146
2N6147





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

STYLE 2.
1. MT 1
2. GATE
3. MT 2

CASE 311-01

2.3

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and either polarity of MT2 to MT1 voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current V_D = Rated V_{DRM} @ T_C = 100°C	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage I_{TM} = 21 A Peak, Pulse Width = 1.0 to 2.0 ms, Duty Cycle ⩽ 2.0%	V_{TM}	–	1.3	1.8	Volts
Gate Trigger Current, Continuous dc (1) V_D = 12 Vdc, R_L = 30 ohms MT2 (+), G(+); MT2(-), G(-) MT2 (+), G(-); MT2(-), G(+) *MT2 (+), G(+); MT2(-), G(-), T_C = -65°C *MT2 (+), G(-); MT2(-), G(+), T_C = -65°C	I_{GT}	 – – – 	 – – – 	 50 80 150 200	mA
Gate Trigger Voltage, Continuous dc (All Quadrants) V_D = 12 Vdc, R_L = 30 ohms T_C = 25°C *T_C = -65°C *V_D = Rated V_{DRM}, R_L = 10 k ohms, T_C = +100°C	V_{GT}	 – 0.2		 2.5 4.0 –	Volts
Holding Current V_D = 12 Vdc, Gate Open Initiating Current = 500 mA T_C = 25°C *T_C = -65°C	I_H	 – –	 – –	 75 300	mA
Gate Controlled Turn-On Time Rated V_{DRM}, I_{TM} = 21 A Peak, I_{GT} = 160 mA, Rise Time ⩽ 0.1 μs, Pulse Width = 2.0 μs	t_{gt}		1.0	2.0	μs
*Critical Rate-of-Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 21 A Peak, Commutating di/dt = 8.0 A/ms, gate unenergized T_C = 80°C 2N5571 thru 2N5574, T4100M, T4110M T_C = 75°C 2N6145 thru 2N6147	dv/dt(c)	 2.0 2.0	 10 10	 – –	V/μs
Critical Rate-of-Rise of Off-State Voltage Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C: *2N5571, 2N5573, 2N6145 *2N5572, 2N5574, 2N6146 T4100M, T4110M, 2N6147	dv/dt	 30 20 10	 150 100 75	 – – –	V/μs

*Indicates JEDEC Registered Data.
(1) All Voltage polarity reference to main terminal 1.

FIGURE 1 — RMS CURRENT DERATING

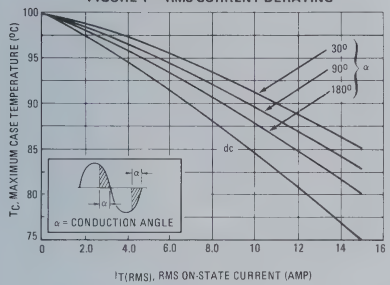


FIGURE 2 — ON-STATE POWER DISSIPATION

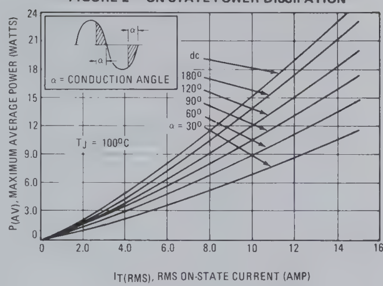


FIGURE 3 — TYPICAL GATE TRIGGER VOLTAGE

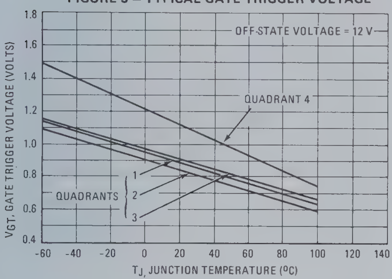
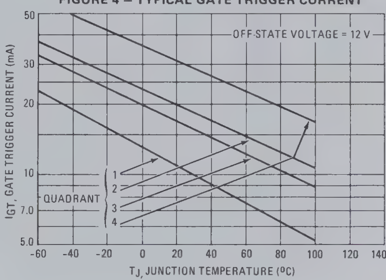


FIGURE 4 — TYPICAL GATE TRIGGER CURRENT



2.3

FIGURE 5 – MAXIMUM ON-STATE CHARACTERISTICS

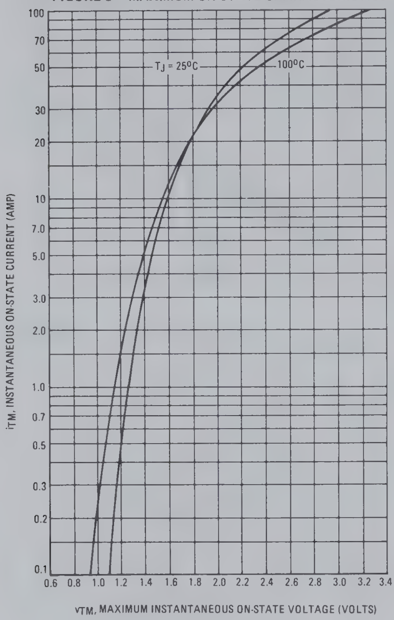


FIGURE 6 – TYPICAL HOLDING CURRENT

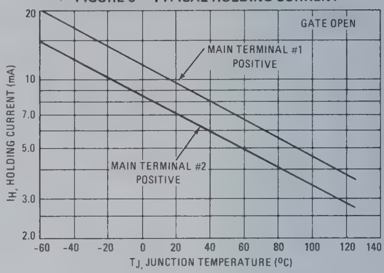


FIGURE 7 – MAXIMUM NON-REPETITIVE SURGE CURRENT

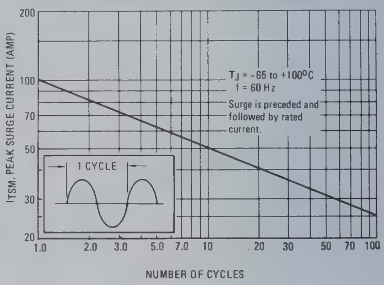
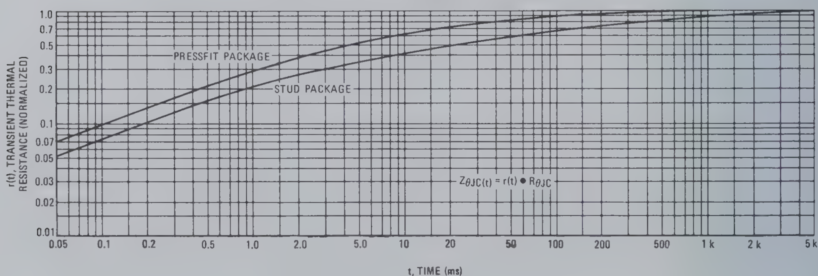


FIGURE 8 – TYPICAL THERMAL RESPONSE



MOTOROLA

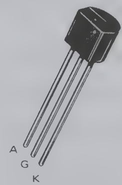
SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

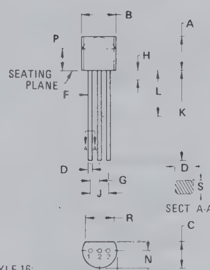
. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-trigger, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO-92 plastic package for high-volume requirements, this package is readily adaptable for use in automatic insertion equipment.

- Programmable – R_{BB}, η, I_V and I_P.
- Low On-State Voltage – 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current – 10 nA Maximum
- High Peak Output Voltage – 11 Volts Typical
- Low Offset Voltage – 0.35 Volt Typical (R_G = 10 k ohms)

PROGRAMMABLE UNIJUNCTION TRANSISTORS

40 VOLTS
375 mW





STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70		0.500	–
L	6.35	–	0.250	
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-92
PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Power Dissipation Derate Above 25°C	P_F $1/\theta_{JA}$	300 4.0	mW mW/°C
*DC Forward Anode Current Derate Above 25°C	I_T	150 2.67	mA mA/°C
*DC Gate Current	I_G	±50	mA
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle *20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
*Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
*Gate to Cathode Reverse Voltage	V_{GKR}	-5.0	Volt
*Gate to Anode Reverse Voltage	V_{GAR}	40	Volt
*Anode to Cathode Voltage (1)	V_{AK}	±40	Volt
Operating Junction Temperature Range	T_J	-50 to +100	°C
*Storage Temperature Range	T_{stg}	-55 to +150	°C

*Indicates JEDEC Registered Data
(1) Anode positive, R_{GA} = 1000 ohms
Anode negative, R_{GA} = open

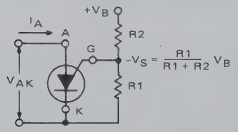
2.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

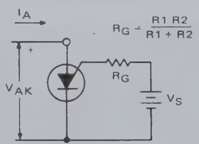
Characteristic		Figure	Symbol	Min	Typ	Max	Unit
*Peak Current		2,9,11	I_P				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			–	1.25	2.0	
	2N6028			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6027			–	4.0	5.0	
	2N6028			–	0.70	1.0	
*Offset Voltage		1	V_T				Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			0.2	0.70	1.6	
	2N6028			0.2	0.50	0.6	
(V_S - 10 Vdc, R_G = 10 k ohms)	(Both Types)			0.2	0.35	0.6	
*Valley Current		1,4,5,	I_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			–	18	50	
	2N6028			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6027			70	270	–	
	2N6028			25	270	–	
(V_S = 10 Vdc, R_G = 200 Ohms)	2N6027			1.5		–	mA
	2N6028			1.0	–	–	
* Gate to Anode Leakage Current			I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1 0	10	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				-	3.0	–	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}	–	5.0	50	nAdc
*Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	–	0 8	1.5	Volts
*Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	11	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

*Indicates JEDEC Registered Data

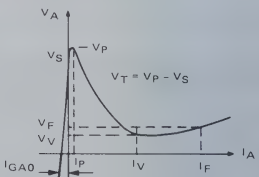
FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – Programmable Unijunction with "Program" Resistors R1 and R2



1B – Equivalent Test Circuit for Figure 1A used for electrical characteristics testing (also see Figure 2)



IC – Electrical Characteristics

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

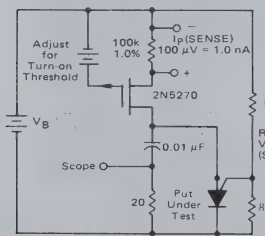
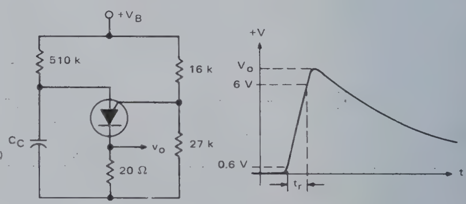


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

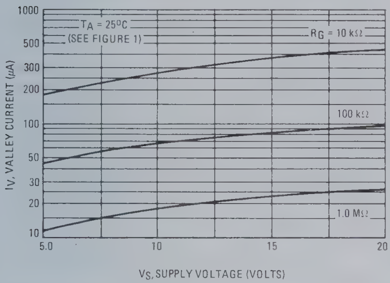
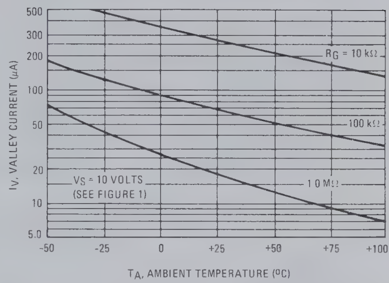


FIGURE 5 – EFFECT OF TEMPERATURE



2.3

FIGURE 6 – FORWARD VOLTAGE

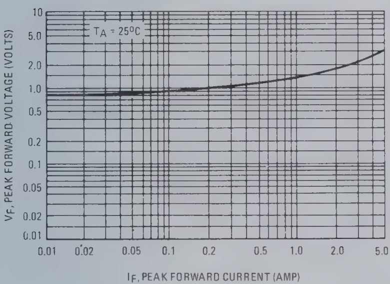


FIGURE 7 – PEAK OUTPUT VOLTAGE

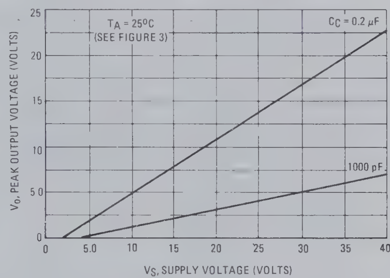
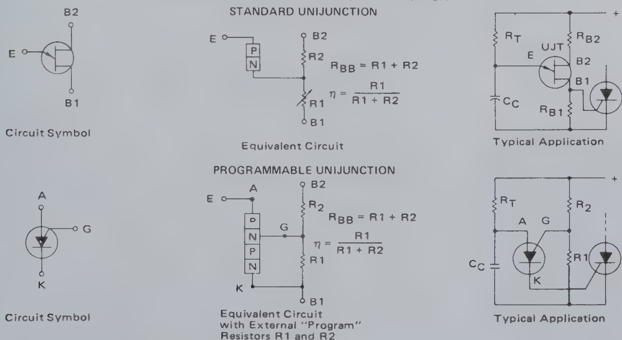


FIGURE 8 – STANDARD UNIJUNCTION COMPARED TO PROGRAMMABLE UNIJUNCTION



*TYPICAL PEAK CURRENT BEHAVIOR

2N6027

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

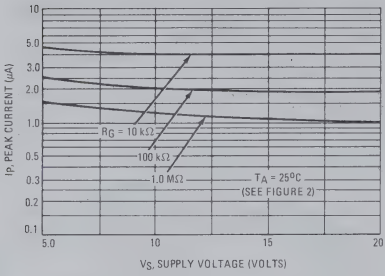
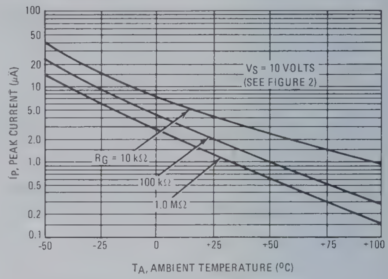


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



2N6028

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

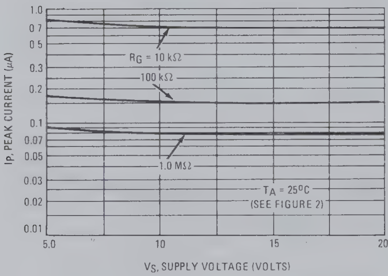
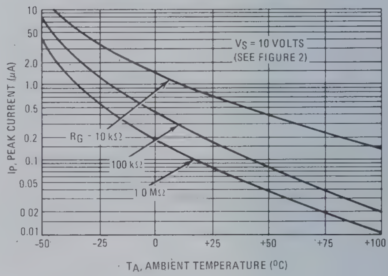


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



2.3

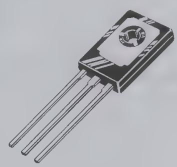
MOTOROLA

2N6068, A, B thru 2N6075, A, B

SENSITIVE GATE

TRIACS
(THYRISTORS)
4 AMPERES RMS
25 THRU 600 VOLTS

2.3



SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Sensitive Gate Triggering (A and B versions) Uniquely Compatible for Direct Coupling to TTL, HTL, CMOS and Operational Amplifier Integrated Circuit Logic Functions.
- Gate Triggering 2 Mode – 2N6068 thru 2N6075
  4 Mode – 2N6068A,B thru 2N6075A,B
- Blocking Voltages to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Repetitive Peak Off-State Voltage, Note 1 (T_J = 110°C)	V_{DRM}		Volts
2N6068,A,B		25	
2N6069,A,B		50	
2N6070,A,B		100	
2N6071,A,B		200	
2N6072,A,B		300	
2N6073,A,B		400	
2N6074,A,B		500	
2N6075,A,B		600	
*On-State Current RMS (T_C = 85°C)	$I_{T(RMS)}$	4.0	Amp
*Peak Surge Current (One Full cycle, 60 Hz, T_J = -40 to +110°C)	I_{TSM}	30	Amp
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	3.6	A^2s
*Peak Gate Power	P_{GM}	10	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Gate Voltage	V_{GM}	5.0	Volts
*Operating Junction Temperature Range	T_J	-40 to +110	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Mounting Torque (6-32 Screw), Note 2	–	8.0	in. lb.

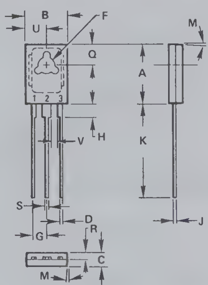
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Case to Ambient	$R_{\theta JA}$	75	°C/W

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of compression washer (B52200F006). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heatsink contact pad are common.
   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C, for 10 seconds. Consult factory for lead bending options.



STYLE 5
PIN 1. MT1
2. MT2
3. GATE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

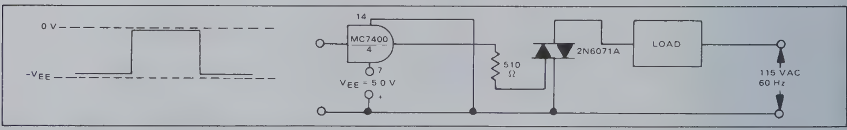
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C, Gate Open	I_{DRM}	–	–	2.0	mA
*On-State Voltage (Either Direction) I_{TM} = 6.0 A Peak	V_{TM}	–	–	2.0	Volts
*Peak Gate Trigger Voltage Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms, T_J = –40°C	V_{GTM}				Volts
MT2 (+), G(+); MT2 (–), G(–) All Types		–	1.4	2.5	
MT2 (+), G(–); MT2 (–), G(+) 2N6068A,B thru 2N6075A,B		–	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C					
MT2 (+), G(+); MT2 (–), G(–) All Types		0.2	–	–	
MT2 (+), G(–); MT2 (–), G(+) 2N6068A,B thru 2N6075A,B		0.2	–	–	
*Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, T_J = –40°C Initiating Current = 1.0 Adc	I_H				mA
2N6068 thru 2N6075		–	–	70	
2N6068A,B thru 2N6075A,B		–	–	30	
T_J = 25°C 2N6068 thru 2N6075		–	–	30	
2N6068A,B thru 2N6075A,B		–	–	15	
Turn-On Time (Either Direction) I_{TM} = 14 Adc, I_{GT} = 100 mAdc	t_{on}	–	1.5	–	μs
Blocking Voltage Application Rate at Commutation @ V_{DRM}, T_J = 85°C, Gate Open	dv/dt	–	5.0	–	V/μs

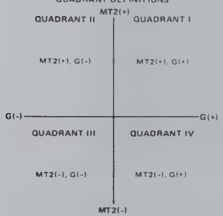
	Type	I_{GTM} @ T_J	QUADRANT (See Definition Below) I mA	II mA	III mA	IV mA
*Peak Gate Trigger Current Main Terminal Voltage = 12 Vdc, R_L = 100 ohms	2N6068 thru 2N6075	+25°C	30	–	30	–
		–40°C	60	–	60	–
Maximum Value	2N6068A thru 2N6075A	+25°C	5.0	5.0	5.0	10
		–40°C	20	20	20	30
	2N6068B thru 2N6075B	+25°C	3.0	3.0	3.0	5.0
		–40°C	15	15	15	20

*Indicates JEDEC Registered Data.

SAMPLE APPLICATION:
TTL-SENSITIVE GATE 4 AMPERE TRIAC TRIGGERS IN MODES II AND III



QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide

1. Consistent predictable turn-on points.
2. Simplified circuitry
3. Fast turn-on time for cooler, more efficient and reliable operation.

For 2N6068 Thru 2N6075

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General		Lamp Dimmer
PART NUMBER	MBS4991	MBS4992	MBS100
V_S	6.0 - 10 V	7.5 - 9.0 V	3.0 – 5.0 V
I_S	350 μA Max	120 μA Max	100 - 400 μA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient	0.02%/°C Typ		

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches

SENSITIVE GATE LOGIC REFERENCE

IC LOGIC FUNCTIONS	FIRING QUADRANT I	II	III	IV
TTL		2N6068A Series	2N6068A Series	
HTL		2N6068A Series	2N6068A Series	
CMOS(NAND)	2N6068B Series			2N6068B Series
CMOS(Buffer)		2N6068B Series	2N6068B Series	
Operational Amplifier	2N6068A Series			2N6068A Series
Zero Voltage Switch		2N6068A Series	2N6068A Series	

FIGURE 1 — AVERAGE CURRENT DERATING

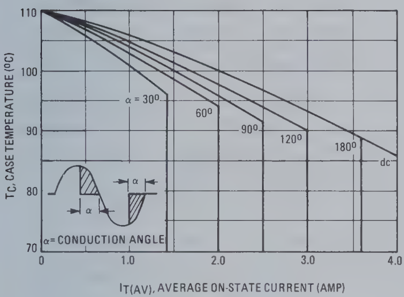


FIGURE 2 — RMS CURRENT DERATING

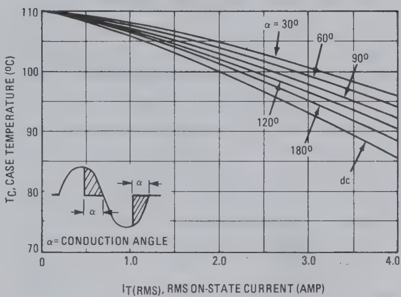


FIGURE 3 — POWER DISSIPATION

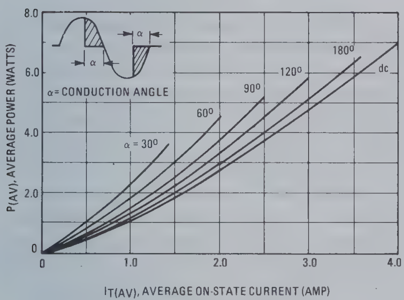


FIGURE 4 — POWER DISSIPATION

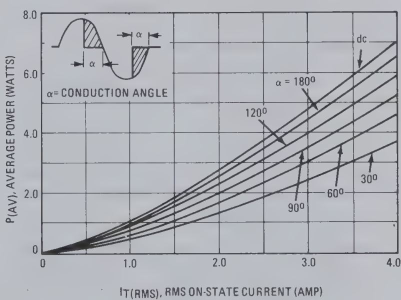


FIGURE 5 — TYPICAL GATE-TRIGGER VOLTAGE

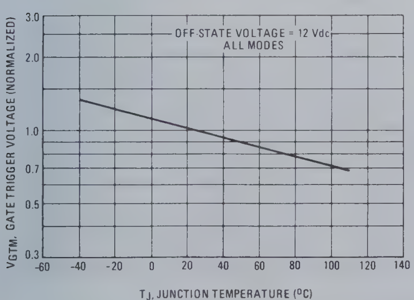


FIGURE 6 — TYPICAL GATE-TRIGGER CURRENT

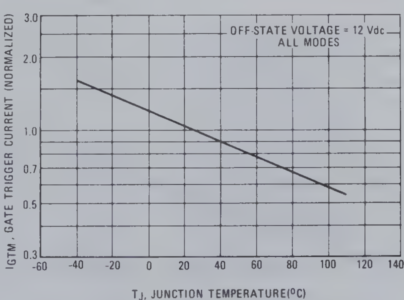


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

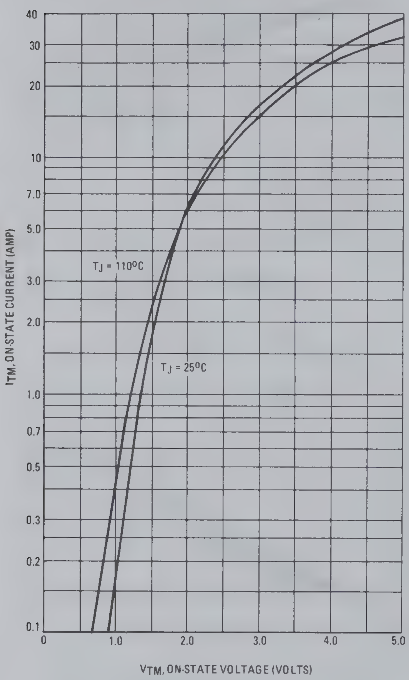


FIGURE 8 – TYPICAL HOLDING CURRENT

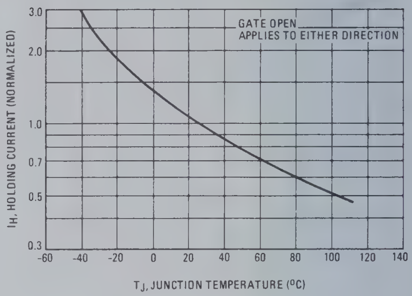


FIGURE 9 – MAXIMUM ALLOWABLE SURGE CURRENT

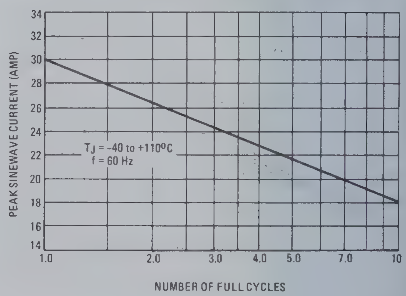
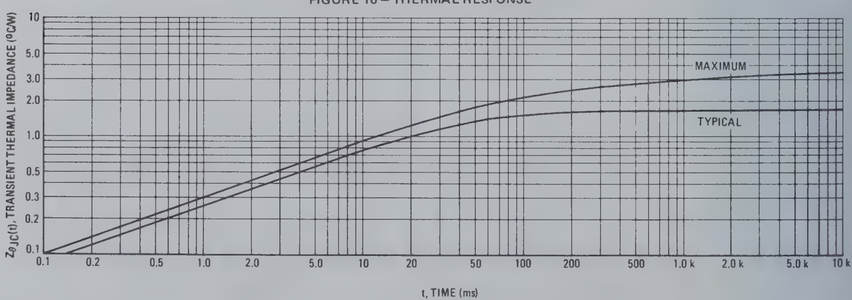


FIGURE 10 – THERMAL RESPONSE



2N6116 2N6117 2N6118

(FORMERLY MPU231, MPU232, MPU233)

MOTOROLA

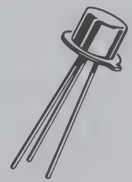
SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS
40 VOLTS
250 mW

2.3

SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-triggor, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate.

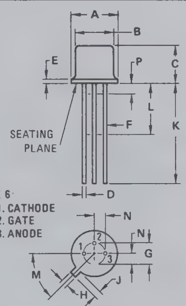
- Programmable — R_{BB}, η, I_V and I_P
- Hermetic TO-18 Package
- Low On-State Voltage — 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current — 5.0 nA Maximum
- High Peak Output Voltage — 16 Volts Typical
- Low Offset Voltage — 0.35 Volt Typical (R_G = 10 k ohms)



*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle 20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
DC Forward Anode Current Derate Above 25°C	I_T	200 2.0	mA mA/°C
DC Gate Current	I_G	±20	mA
Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
Gate to Cathode Reverse Voltage	V_{GKR}	5.0	Volt
Gate to Anode Reverse Voltage	V_{GAR}	40	Volt
Anode to Cathode Voltage	V_{AK}	±40	Volt
Forward Power Dissipation @ T_A = 25°C Derate Above 25°C	P_F $1/\theta_{JA}$	250 2.5	mW mW/°C
Operating Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data



STYLE 6
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E	–	0.762	–	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC notes and dimensions apply.

CASE 22-03
(TO-18)

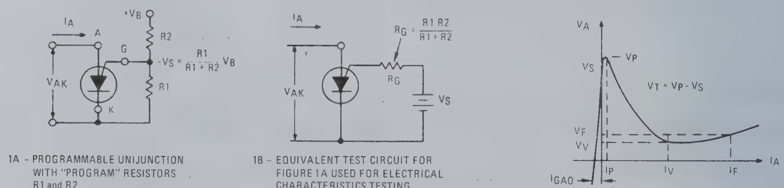
2.3

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Offset Voltage	2N6116	1	V_F	0.2	0.70	1.6	Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6117			0.2	0.50	0.6	
	2N6118			0.2	0.40	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms)	All Types			0.2	0.35	0.6	
Gate to Anode Leakage Current		–	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1.0	5.0	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	30	75	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}	–	5.0	50	nAdc
Peak Current	2N6116	2,9-14	I_P	–	1.25	2.0	μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6117			–	0.19	0.3	
	2N6118			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6116			–	4.0	5.0	
	2N6117			–	1.20	2.0	
	2N6118			–	0.70	1.0	
Valley Current		1,4,5	I_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6116, 2N6117			–	18	50	
	2N6118			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6116			70	270	–	
	2N6117, 2N6118			50	270	–	
Forward Voltage (I_F = 50 mA Peak)		1,6	V_T	–	0.8	1.5	Volts
Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	16	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

*Indicates JEDEC Registered Data

FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – PROGRAMMABLE UNIJUNCTION WITH "PROGRAM" RESISTORS R1 and R2

1B – EQUIVALENT TEST CIRCUIT FOR FIGURE 1A USED FOR ELECTRICAL CHARACTERISTICS TESTING (ALSO SEE FIGURE 2)

1C – ELECTRICAL CHARACTERISTICS

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

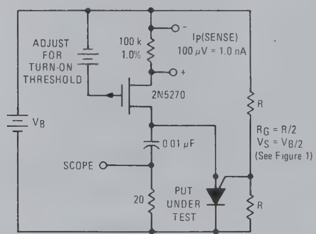
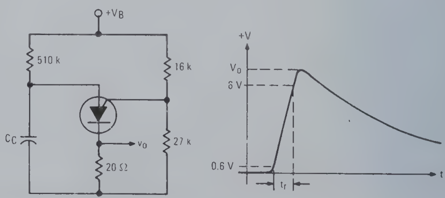


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

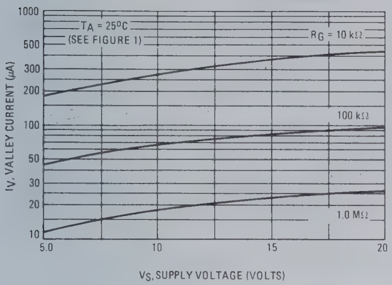
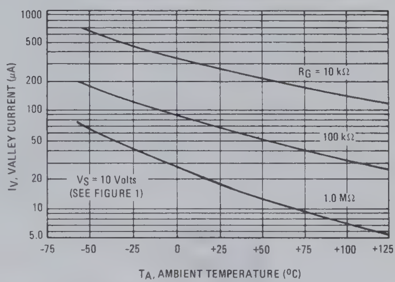


FIGURE 5 – EFFECT OF TEMPERATURE



2.3

FIGURE 6 – FORWARD VOLTAGE

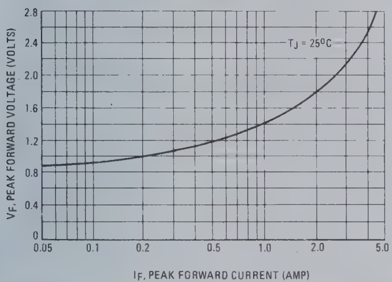


FIGURE 7 – PEAK OUTPUT VOLTAGE

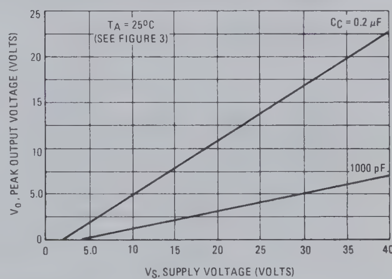
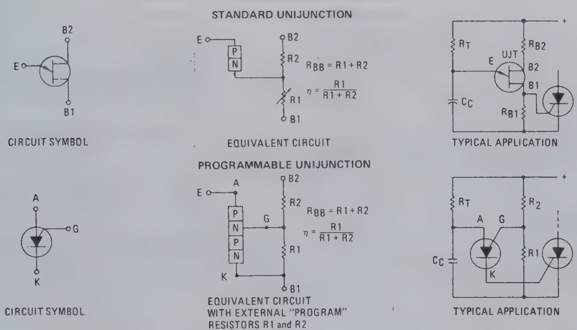


FIGURE 8 – STANDARD UNIJUNCTION
COMPARED TO PROGRAMMABLE UNIJUNCTION



TYPICAL PEAK CURRENT BEHAVIOR

2N6116

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

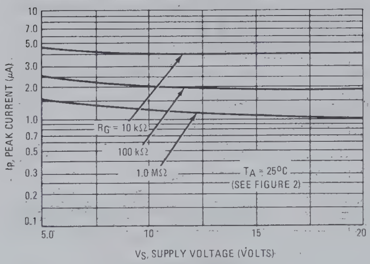
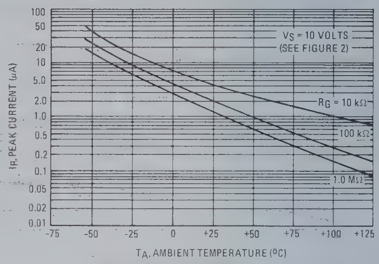


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



2N6117

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

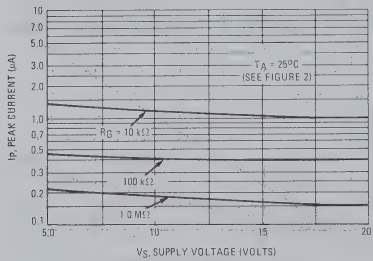
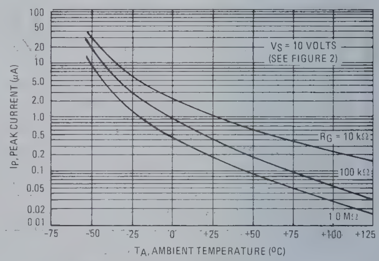


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



2N6118

FIGURE 13 – EFFECT OF SUPPLY VOLTAGE AND R_G

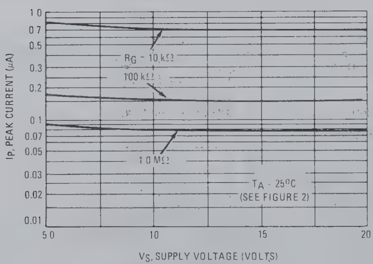
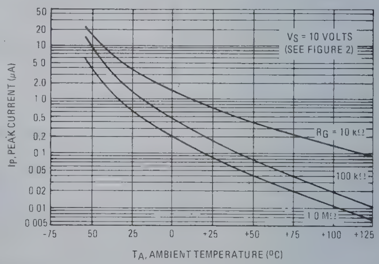


FIGURE 14 – EFFECT OF TEMPERATURE AND R_G

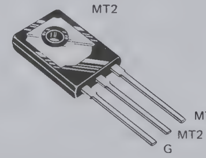


MOTOROLA

2N6151
thru
2N6156

TRIACS
(THYRISTORS)

10 AMPERES RMS



SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- All Diffused and Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two (2N6154, 2N6155, 2N6156) or Four Modes (2N6151, 2N6152, 2N6153)

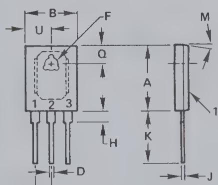
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
* Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +100°C) ½ Sine Wave 50 to 60 Hz, Gate Open Peak Principle Voltage	V_{DRM}		Volts
2N6151, 2N6154		200	
2N6152, 2N6155		400	
2N6153, 2N6156		600	
*Peak Gate Voltage	V_{GM}	10	Volts
*On-State Current RMS (T_C = −40 to +75°C)	$I_{T(RMS)}$	10	Amp
Full Cycle Sine Wave 50 to 60 Hz (T_C = +90°C)		5.0	
*Peak Surge Current (One Full Cycle, 60 Hz, T_J = +75°C) preceded and followed by 10 A Current	I_{TSM}	100	Amp
Circuite Fusing Considerations (T_J = −40 to +100°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (T_J = +75°C, Pulse Width = 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power (T_J = +75°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	−40 to +100	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C
*Mounting Torque (6-32 Screw), Note 2	—	8.0	in. lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
* Thermal Resistance, Junction to Case	R_{JC}	2.0	°C/W
Thermal Resistance Case to Ambient	$R_{\theta CA}$	50	°C/W

*Indicates JEDEC Registered Data.



STYLE 4:
PIN 1. MT 1
2. MT 2
3. GATE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255

CASE 90-05

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 100°C, Gate Open	I_{DRM}	–	–	2.0	mA
*On-State Voltage (Either Direction) I_{TM} = 14 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.8	Volts
Gate Trigger Current, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	I_{GT}				mA
MT2 (+), G(+) All Types		–	6.0	50	
MT2 (+), G(–) 2N6151 thru 2N6153		–	6.0	75	
MT2 (–), G(–) All Types		–	10	50	
MT2 (–), G(+) 2N6151 thru 2N6153		–	25	75	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –40°C All Types		–	–	100	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –40°C 2N6151 thru 2N6153		–	–	125	
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	V_{GT}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(–) 2N6151 thru 2N6153		–	0.9	2.5	
MT2 (–), G(–) All Types		–	1.1	2.0	
MT2 (–), G(+) 2N6151 thru 2N6153		–	1.4	2.5	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –40°C All Types		–	–	2.5	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –40°C 2N6151 thru 2N6153		–	–	3.0	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 100°C					
*MT2 (+), G(+); MT2 (–), G(–) All Types		0.2	–	–	
*MT2 (+), G(–); MT2 (–), G(+) 2N6151 thru 2N6153		0.2	–	–	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA	I_H				mA
T_C = 25°C		–	6.0	40	
T_C = –40°C		–	–	75*	
*Turn-On Time Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 14 A Gate Source Voltage = 12 V, R_S = 100 Ohms, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	tgt	–	1.5	2.0	μs
Blocking Voltage Application Rate at Commutation, f = 60 Hz, T_C = 75°C On-State Conditions: I_{TM} = 14 A, Pulse Width = 4.0 ms, di/dt = 5.3 A/ms Off-State Conditions: Main Terminal Voltage = Rated V_{DRM} (200 μs min), Gate Source Voltage = 0 V, R_S = 100 Ω	dv/dt	–	5.0	–	V/μs

*Indicates JEDEC Registered Data

NOTES:
1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19522 #6 or equivalent). Mounting torque in excess of 8 in. lbs. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common.
   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +230°C.

Trigger devices are recommended for gating on Triacs
Triggers Provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

Electrical Characteristics	For General Usage		For Lamp Dimmer
Symbol	MBS4991	MBS4992	MBS100
V_S =	6.0 – 10 V	7.5–9.0 V	3.0–5.0 V
I_S =	350 μA Max	120 μA Max	100–400 μA
$V_{S1}–V_{S2}$ =	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient = 0.02%/°C Typ			

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

2.3

FIGURE 1 – AVERAGE CURRENT DERATING

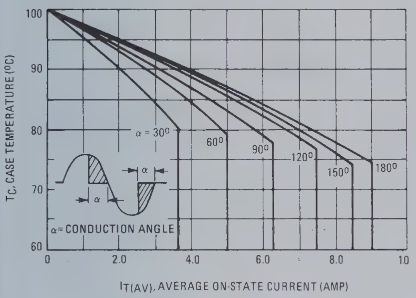
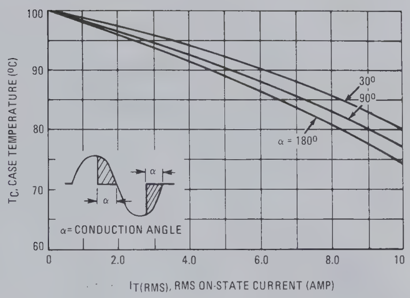


FIGURE 2 – RMS CURRENT DERATING



2.3

FIGURE 3 – POWER DISSIPATION

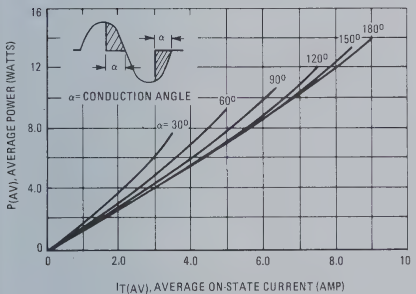


FIGURE 4 – POWER DISSIPATION

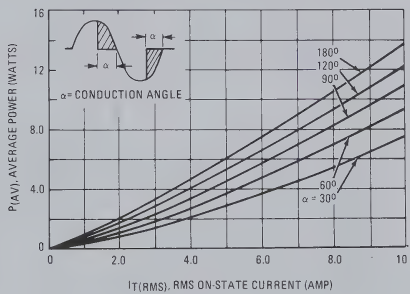


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

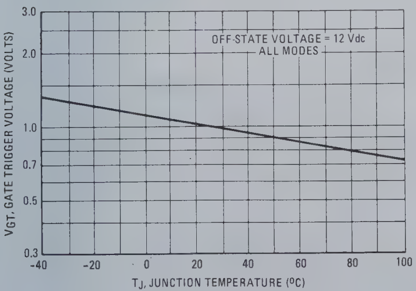


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

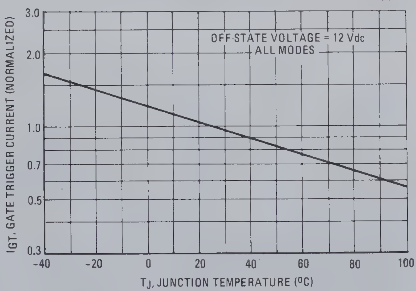


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

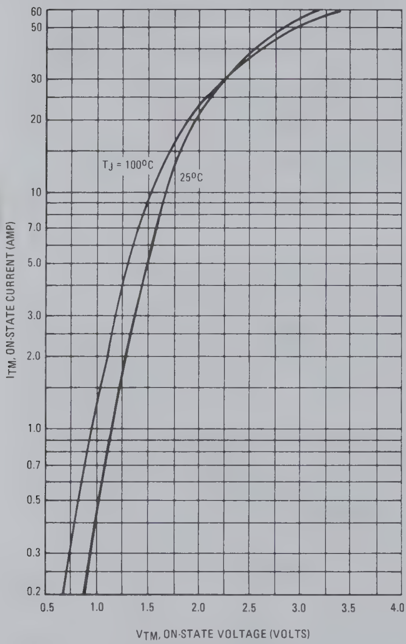


FIGURE 8 – TYPICAL HOLDING CURRENT

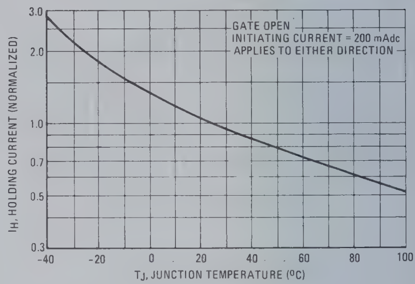


FIGURE 9 – MAXIMUM ALLOWABLE SURGE CURRENT

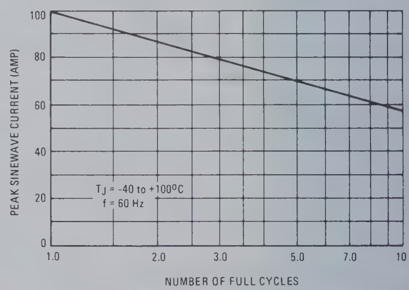
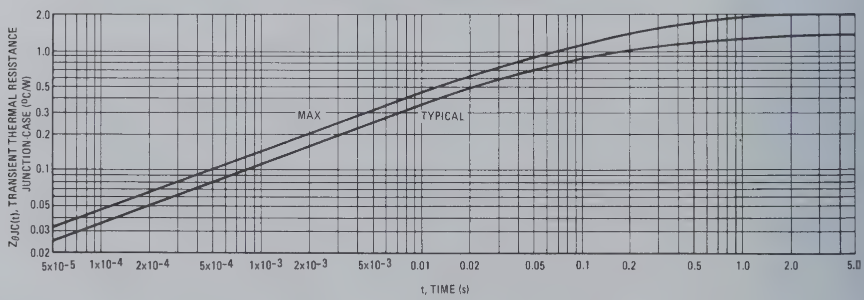


FIGURE 10 – THERMAL RESPONSE



MOTOROLA

2N6157 thru 2N6165

TRIACS

30 AMPERES RMS
200–600 VOLTS

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Isolated Stud for Ease of Assembly
- Gate Triggering Guaranteed In All 4 Quadrants

MAXIMUM RATINGS

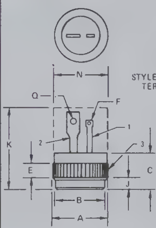
Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = -65 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open *Peak Principal Voltage 2N6157, 2N6160, 2N6163 2N6158, 2N6161, 2N6164 2N6159, 2N6162, 2N6165	V_{DRM}	 200 400 600	Volts
*Peak Gate Voltage	V_{GM}	10	Volts
*RMS On-State Current (T_C = -65 to +85°C) (T_C = +100°C) Full Sine Wave, 50 to 60 Hz	$I_{T(RMS)}$	 30 20	Amp
*Peak Non-Repetitive Surge Current (One Full Cycle of surge current at 60 Hz, preceeded and followed by a 30 ARMS current, T_J = +125°C)	I_{TSM}	250	Amp
Circuit Fusing Considerations (T_J = -65 to +125°C, t = 1.0 to 8.3 ms)	I^2t	210	A^2s
*Peak Gate Power (T_J = +80°C, Pulse Width = 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power (T_J = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-65 to +125	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
*Stud Torque 2N6160 thru 2N6165	–	30	in. lb.

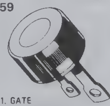
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

*Indicates JEDEC Registered Data.

2N6157-59



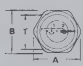


STYLE 3
TERM. 1. GATE
2. MAIN TERMINAL 1
3. MAIN TERMINAL 2

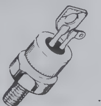
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12 73	12.83	0.501	0.505
B	11 81	12 06	0.465	0.475
C	8.39	9 65	0.330	0.380
E	2 54	–	0 100	–
F	0 89	2 16	0.035	0 085
J	2 04	2 46	0.080	0.097
K		20 32	–	0.800
N		12 95	–	0.510
Q	1 65	4 06	0.065	0.160

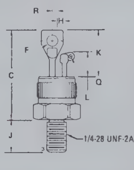
CASE 174-03

2N6160-62



STYLE 2
PIN 1 MT 1
2 GATE
3 MT 2



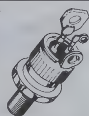


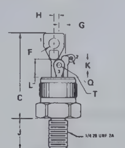
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15 34	15.60	0 604	0 614
B	14 00	14.20	0 551	0 559
C	26.67	30.23	1 050	1 190
F	3.43	4 06	0 135	0 160
H	2.29 REF		0 090 REF	
J	10.67	11.56	0.420	0 455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
[illegible]	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

2N6163-65

STYLE 2.
1. MT 1
2 GATE
3. MT 2





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0 551	0.559
B	12 73	12.83	0 501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1 60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6 48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3 43	3.81	0.135	0 150

CASE 311-01

2.3

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
* Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 125°C	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage (Either Direction) I_{TM} = 42 A Peak, Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.5	2.0	Volts
Gate Trigger Current, Continuous dc (1) Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms	I_{GT}				mA
MT2 (+), G(+)		–	15	60	
MT2 (+), G(–)		–	20	70	
MT2 (–), G(–)		–	20	70	
MT2 (–), G(+)		–	30	100	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –65°C		–	–	200	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –65°C		–	–	250	
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms	V_{GT}				Volts
MT2 (+), G(+)		–	0.8	2.0	
MT2 (+), G(–)		–	0.7	2.1	
MT2 (–), G(–)		–	0.85	2.1	
MT2 (–), G(+)		–	1.1	2.5	
*All Quadrants, T_C = –65°C)		–	–	3.4	
*Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = +125°C		0.2	–	–	
Holding Current Main Terminal Voltage = 12 Vdc, Gate Open Initiating Current = 500 mA	I_H				mA
MT2 (+)		–	8	70	
MT2 (–)		–	10	80	
*Either Direction, T_C = –65°C		–	–	200	
*Turn-On Time Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 42 A, Gate Source Voltage = 12 V, R_S = 50 Ohms, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	t_{gt}	–	1.0	2.0	μs
Blocking Voltage Application Rate at Commutation, f = 60 Hz, T_C = 85°C On-State Conditions: I_{TM} = 42A, Pulse Width = 4.0 ms, di/dt = 17.5 A/ms Off State Conditions: Main Terminal Voltage = Rated V_{DRM} (200 μs min), Gate Source Voltage = 0 V, R_S = 50 Ω	dv/dt(c)	–	5.0	–	V/μs

*Indicates JEDEC Registered Data.
(1) All voltage polarity reference to main terminal 1.

FIGURE 1 — RMS CURRENT DERATING

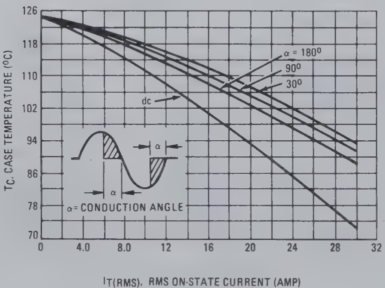


FIGURE 2 — POWER DISSIPATION

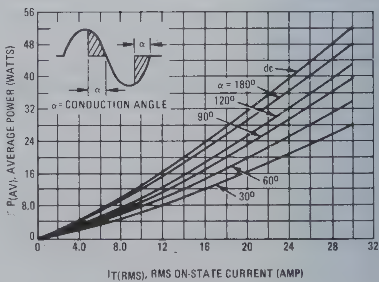


FIGURE 3 — TYPICAL GATE TRIGGER VOLTAGE

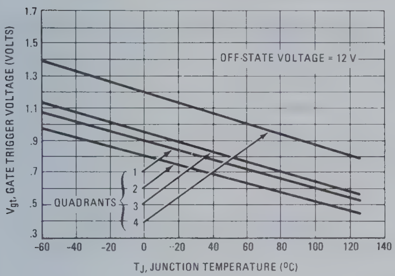


FIGURE 5 — MAXIMUM ON-STATE CHARACTERISTICS

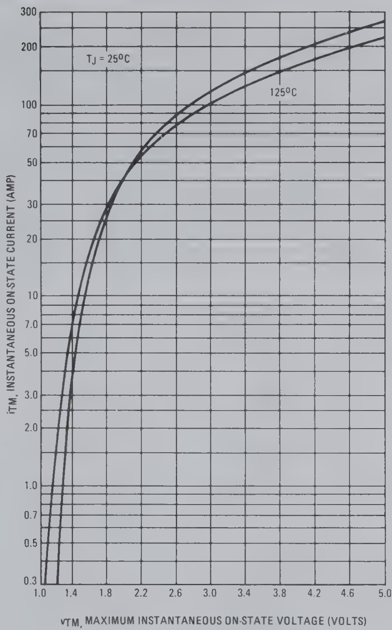
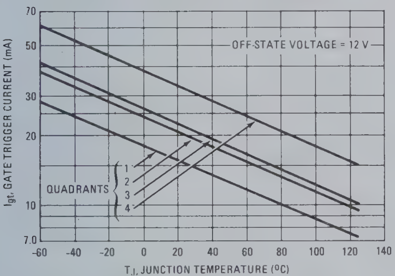


FIGURE 4 — TYPICAL GATE TRIGGER CURRENT



2.3

FIGURE 6 — TYPICAL HOLDING CURRENT

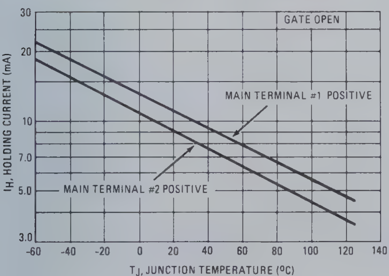


FIGURE 7 — MAXIMUM ALLOWABLE SURGE CURRENT

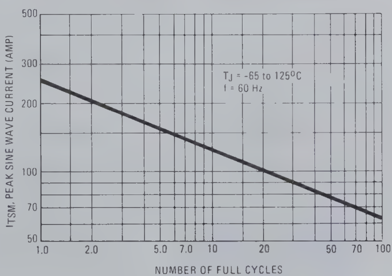
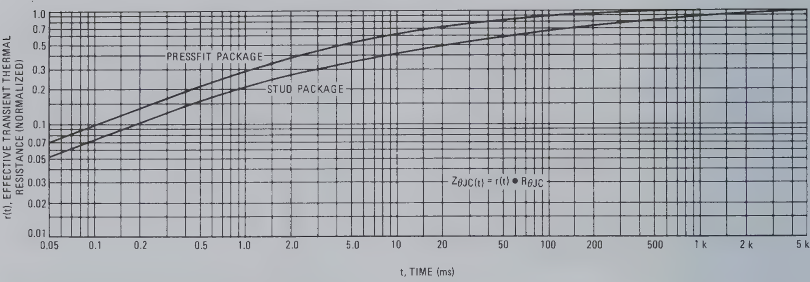


FIGURE 8 — TYPICAL THERMAL RESPONSE



2.3

MOTOROLA

2N6167 thru 2N6170

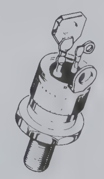
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for industrial and consumer applications such as power supplies; battery chargers; temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current – I_{TSM} = 240 Amp
- Rugged Construction in Isolated Stud Package

SILICON CONTROLLED RECTIFIER

20 AMPERES RMS
100–600 VOLTS



MAXIMUM RATINGS

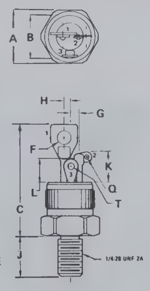
Rating	Symbol	Value	Unit
*Peak Repetitive Forward and Reverse Blocking Voltage (1) (T_J = −40°C to +100°C) 2N6167 / 2N6168 / 2N6169 / 2N6170	V_{DRM} V_{RRM}	100 / 200 / 400 / 600	Volts
*Non-Repetitive Peak Reverse Blocking Voltage (t ⩽ 5.0 ms) 2N6167 / 2N6168 / 2N6169 / 2N6170	V_{RSM}	150 / 250 / 450 / 650	Volts
*Average Forward Current (T_C = −40 to +65°C) (+85°C)	$I_{T(AV)}$	13 / 6.5	Amp
*Peak Surge Current (One cycle, 60 Hz) (T_C = +65°C) (1.5 ms pulse @ T_J = 100°C Preceeded and followed by no current or Voltage	I_{TSM}	240 / 560	Amp
Circuit Fusing (T_J = −40 to +100°C) (t = 1.0 to 8.3 ms)	I^2t	235	A^2s
*Peak Gate Power	P_{GM}	5.0	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GFM}	2.0	Amp
*Operating Junction Temperature Range	T_J	−40 to +100	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C
*Stud Torque	–	30	in. lb.

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

*Indicates JEDEC Registered Data.

(1) Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.



STYLE 1:
1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

CASE 311-01

2.3

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM}, gate open, T_J = 100°C)	I_{DRM}				mA
2N6167			1.0	2.0	
2N6168		–	1.0	2.5	
2N6169			1.0	3.0	
2N6170			1.0	4.0	
*Peak Reverse Blocking Current (V_R = Rated V_{RRM}, gate open, T_J = 100°C)	I_{RRM}				mA
2N6167			1.0	2.0	
2N6168		–	1.0	2.5	
2N6169		–	1.0	3.0	
2N6170			1.0	4.0	
*Peak Forward "On" Voltage (I_{TM} = 41 A Peak)	V_{TM}		1.5	1.7	Volts
Gate Trigger Current, Continuous dc (V_D = 12 V, R_L = 24 Ω) *T_C = −40°C	I_{GT}	–	-	75	mA
T_C = 25°C			2.1	40	
Gate Trigger Voltage, Continuous dc (V_D = 12 V, R_L = 24 Ω) *T_C = −40°C	V_{GT}	-	0.8	2.5	Volts
T_C = 25°C		–	0.63	1.6	
Holding Current (V_D = 12 V, gate open, I_T = 200 mA) *T_C = −40°C	I_H		–	90	mA
T_C = 25°C		–	3.5	50	
*Turn-On Time ($t_d + t_r$) (I_{TM} = 41 Adc, V_D = Rated V_{DRM}, I_{GT} = 200 mAdc, Rise Time ≤ 0.05 μs, Pulse Width = 10 μs)	t_{on}	–	–	1.0	μs
Turn-Off Time	t_{off}				μs
(I_{TM} = 10 A, I_R = 10 A)			25	–	
(I_{TM} = 10 A, I_R = 10 A, T_J = 100°C)		–	40	-	
Forward Voltage Application Rate (T_J = 100°C, V_D = Rated V_{DRM})	dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

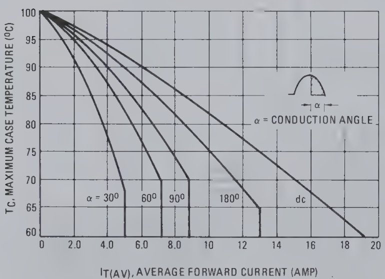


FIGURE 2 – POWER DISSIPATION

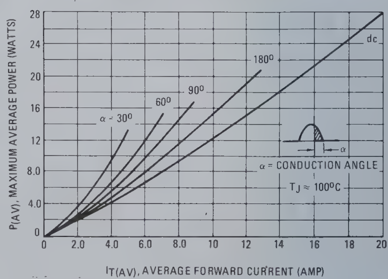


FIGURE 3 – MAXIMUM ON-STATE CHARACTERISTICS

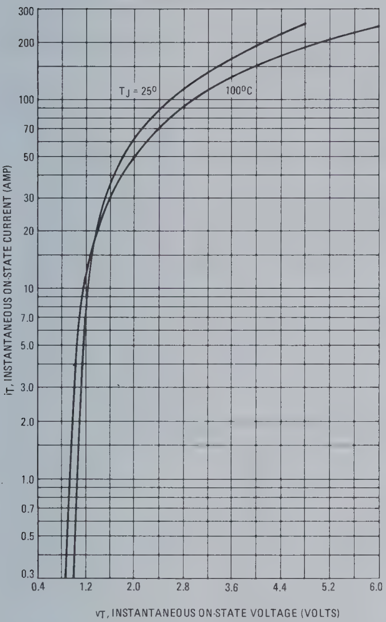
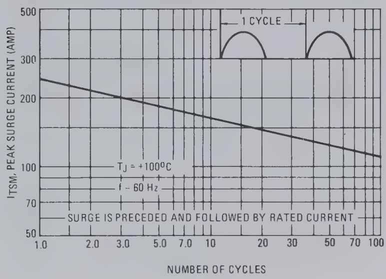


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT



2.3

FIGURE 5 – CHARACTERISTICS AND SYMBOLS

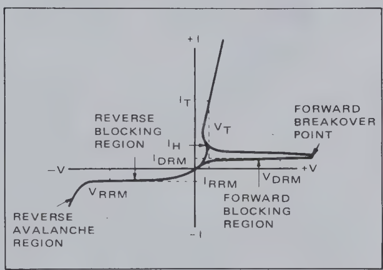


FIGURE 6 – THERMAL RESPONSE

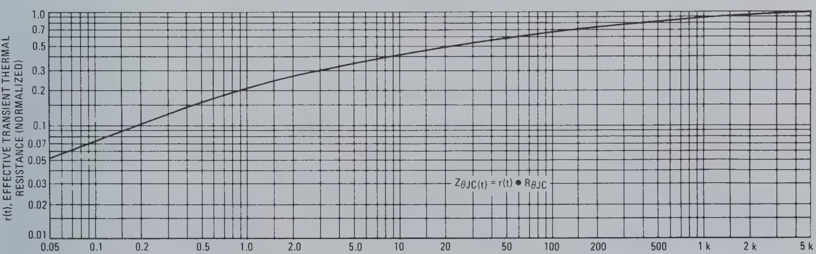


FIGURE 7 – TYPICAL GATE TRIGGER CURRENT

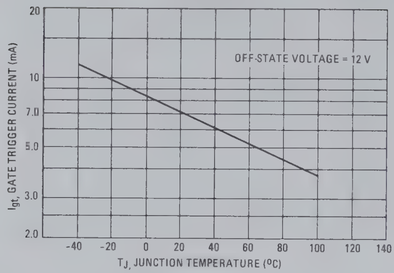
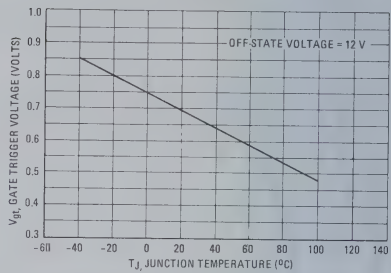
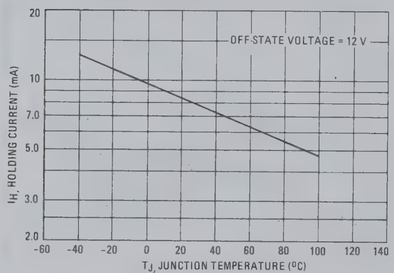


FIGURE 8 – TYPICAL GATE TRIGGER VOLTAGE



2.3

FIGURE 9 – TYPICAL HOLDING CURRENT



2N6236 thru 2N6241

MOTOROLA

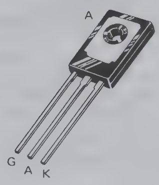
REVERSE BLOCKING TRIODE THYRISTORS

. . . PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Passivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Recommended Electrical Replacement for C 106

SILICON CONTROLLED RECTIFIERS

4.0 AMPERES RMS
30 thru 600 VOLTS



2.3

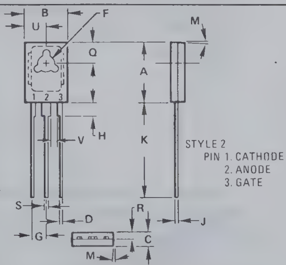
MAXIMUM RATINGS (T_C = 110°C unless otherwise noted.)

Rating		Symbol	Value	Unit
*Repetitive Peak Forward and Reverse Blocking Voltage (Note 1) (1/2 Sine Wave) (R_{GK} = 1000 ohms, T_C = −40 to +110°C)	2N6236	V_{DRM} V_{RRM}	30	Volts
	2N6237		50	
	2N6238		100	
	2N6239		200	
	2N6240		400	
	2N6241		600	
*Non-Repetitive Peak Reverse Blocking Voltage (1/2 Sine Wave, R_{GK} = 1000 ohms, T_C = −40 to +110°C)	2N6236	V_{RSM}	50	Volts
	2N6237		100	
	2N6238		150	
	2N6239		250	
	2N6240		450	
	2N6241		650	
*Average On-State Current (T_C = −40 to +90°C)		$I_{T(AV)}$	2.6	Amp
(T_C = +100°C)			1.6	
*Surge On-State Current (1/2 Sine Wave, 60 Hz, T_C = +90°C)		I_{TSM}	25	Amp
(1/2 Sine Wave, 1.5 ms, T_C = +90°C)			35	
Circuit Fusing (T_C = −40 to 110°C, t = 1.0 to 8.3 ms)		I^2t	2.6	A^2s
*Peak Gate Power (Pulse Width = 10 μs, T_C = 90°C)		P_{GM}	0.5	Watts
*Average Gate Power (t = 8.3 ms, T_C = 90°C)		$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current		I_{GM}	0.2	Amp
Peak Reverse Gate Voltage		V_{RGM}	6.0	Volts
*Operating Junction Temperature Range		T_J	−40 to +110	°C
*Storage Temperature Range		T_{stg}	−40 to +150	°C
Mounting Torque (Note 2)		—	6.0	in.lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	3.0	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	—	75	°C/W

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02		0.040	–

CASE 77-04 TO-126

ELECTRICAL CHARACTERISTICS (T_C = 25°C and R_{GK} = 1000 ohms unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (Note 1) (Rated V_{DRM}, T_C = 110°C)	I_{DRM}	–	–	200	μA
*Peak Reverse Blocking Current (Note 1) (Rated V_{RRM}, T_C = 110°C)	I_{RRM}	–	–	200	μA
*Peak Forward "On" Voltage (I_{TM} = 8.2 A Peak, Pulse Width = 1 to 2 ms, 2% Duty Cycle)	V_{TM}	–	–	2.2	Volts
Gate Trigger Current (Continuous dc) (Note 3)	I_{GT}				μA
(V_{AK} = 12 Vdc, R_L = 24 Ohms)		–	–	200	
*(V_{AK} = 12 Vdc, R_L = 24 Ohms, T_C = −40°C)		–	–	500	
Gate Trigger Voltage (Continuous dc) (Source Voltage = 12 V, R_S = 50 Ohms) *(V_{AK} = 12 Vdc, R_L = 24 Ohms, T_C = −40°C)	V_{GT}	–	–	1.0	Volts
Gate Non-Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 Ohms, T_C = 110°C)	V_{GD}	0.2	–	–	Volts
Holding Current	I_H				mA
(V_{AK} = 12 Vdc, I_{GT} = 2.0 mA) T_C = 25°C		–	–	5.0	
*(Initiating On-State Current = 200 mA) T_C = −40°C		–	–	10	
*Total Turn-On Time (Source Voltage = 12 V, R_S = 6.0 k Ohms) (I_{TM} = 8.2 A, I_{GT} = 2.0 mA, Rated V_{DRM}) (Rise Time = 20 ns, Pulse Width = 10 μs)	t_{gt}	–	–	2.0	μs
Forward Voltage Application Rate (V_D = Rated V_{DRM}, T_C = 110°C)	dv/dt	–	10	–	V/μs

*Indicates JEDEC Registered Data

2.3

NOTES:

1. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of compression washer (B52200-F006 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-209 B)
   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C. For optimum results, an activated flux (oxide removing) is recommended.
3. Measurement does not include R_{GK} current.

CURRENT DERATING

FIGURE 1 — MAXIMUM CASE TEMPERATURE

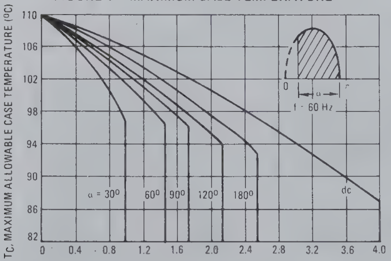
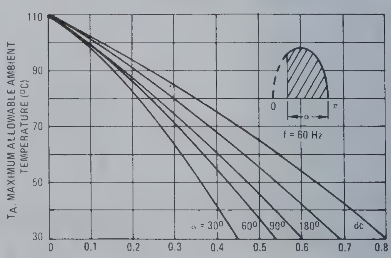


FIGURE 2 — MAXIMUM AMBIENT TEMPERATURE



2N6342 thru 2N6349

MOTOROLA

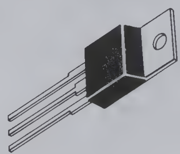
BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342, 2N6343, 2N6344, 2N6345) or Four Modes (2N6346, 2N6347, 2N6348,2N6349)
- For 400 Hz Operation, Consult Factory
- 12 Ampere Devices Available as 2N6342A thru 2N6349A

TRIACS

8 AMPERES RMS
50–800 VOLTS



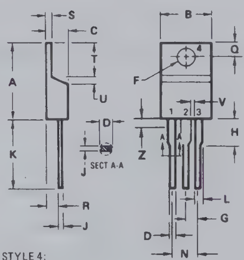
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = −40 to +100°C) ½ Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
2N6342,2N6346		200	
2N6343,2N6347		400	
2N6344,2N6348		600	
2N6345,2N6349		800	
*RMS On-State Current (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +90°C)	$I_{T(RMS)}$	8.0 4.0	Amp
*Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = +80°C) preceded and followed by 10 Rated Current	I_{TSM}	100	Amp
Circuit Fusing (T_J = −40 to +100°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (T_C = +80°C, Pulse Width = 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Peak Gate Voltage	V_{GM}	10	Volts
*Operating Junction Temperature Range	T_J	−40 to +125	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
* Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

*Indicates JEDEC Registered Data.



STYLE 4:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220 AB
All JEDEC dimensions and notes apply

2.3

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Off-State Current V_D = Rated V_{DRM} @ T_J = 100°C, Gate Open	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage I_{TM} = 11 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.55	Volts
Gate Trigger Current, Continuous dc V_D = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	I_{GT}				mA
MT2 (+), G(+) All Types		–	12	50	
MT2 (+), G(–) 2N6346 thru 49		–	12	75	
MT2 (–), G(–) All Types		–	20	50	
MT2 (–), G(+) 2N6346 thru 49		–	35	75	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –40°C All Types		–	–	100	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –40°C 2N6346 thru 49, MAC221		–	–	125	
Gate Trigger Voltage, Continuous dc V_D = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	V_{GT}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(–) 2N6346 thru 49		–	0.9	2.5	
MT2 (–), G(–) All Types		–	1.1	2.0	
MT2 (–), G(+) 2N6346 thru 49		–	1.4	2.5	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –40°C All Types		–	–	2.5	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –40°C 2N6346 thru 49, MAC221		–	–	3.0	
V_D = Rated V_{DRM}, R_L = 10k Ohms, T_J = 100°C					
*MT2 (+), G(+); MT2 (–), G(–) All Types		0.2	–	–	
*MT2 (+), G(–); MT2 (–), G(–) 2N6346 thru 49, MAC221		0.2	–	–	
*Holding Current V_D = 12 Vdc, Gate Open I_T = 200 mA	I_H				mA
T_C = 25°C		–	6.0	40	
*T_C = –40°C		–	–	75	
*Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 11 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	tgt	–	1.5	2.0	μs
Critical Rate of Rise of Commutation Voltage V_D = Rated V_{DRM}, I_{TM} = 11 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(c)	–	5.0	–	V/μs

*Indicates JEDEC Registered Data

FIGURE 1 — RMS CURRENT DERATING

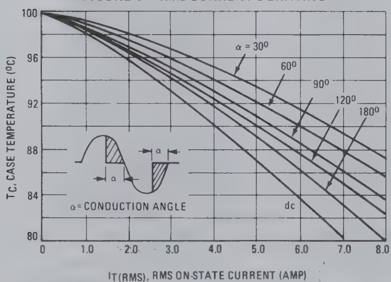


FIGURE 2 — ON-STATE POWER DISSIPATION

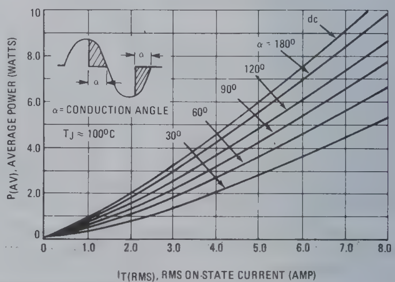


FIGURE 3 — TYPICAL GATE TRIGGER VOLTAGE

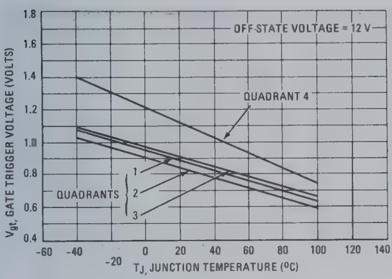


FIGURE 4 — TYPICAL GATE TRIGGER CURRENT

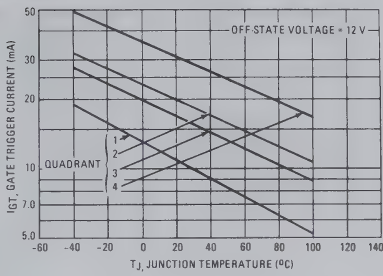


FIGURE 5 — ON-STATE CHARACTERISTICS

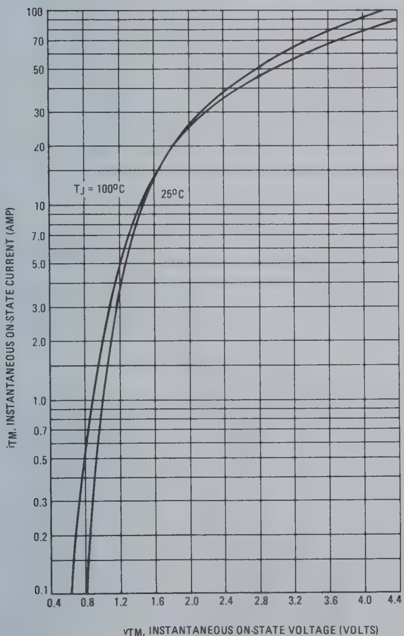


FIGURE 6 — TYPICAL HOLDING CURRENT

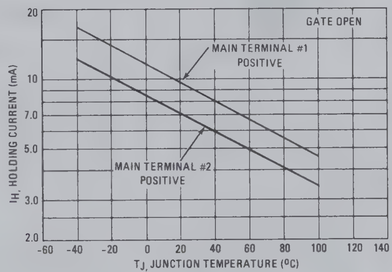


FIGURE 7 — MAXIMUM NON-REPETITIVE SURGE CURRENT

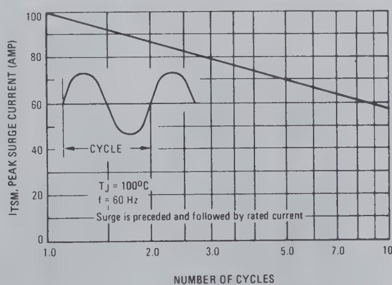
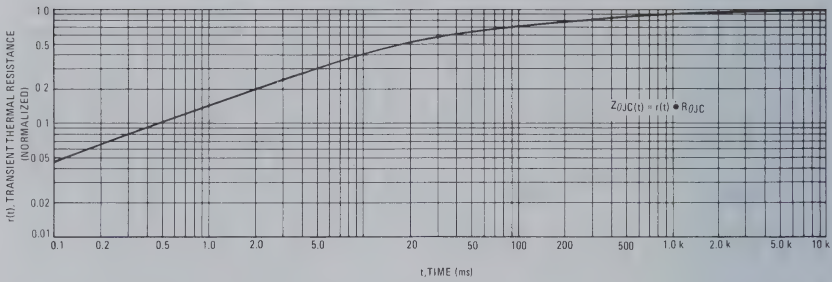


FIGURE 8 — TYPICAL THERMAL RESPONSE

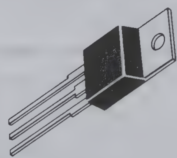


2.3

2N6342A thru 2N6349A

TRIACS

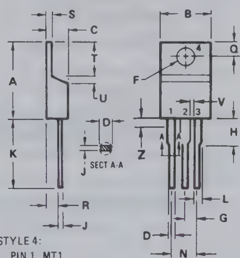
12 AMPERES RMS
200–800 VOLTS



BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342A, 2N6343A, 2N6344A, 2N6345A) or Four Modes (2N6346A, 2N6347A, 2N6348A, 2N6349A)
- For 400 Hz Operation, Consult Factory
- 8 Ampere Devices Available as 2N6342 thru 2N6349



STYLE 4:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220 AB
All JEDEC dimensions and notes apply

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = −40 to +110°C) ½ Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
2N6342A, 2N6346A		200	
2N6343A, 2N6347A		400	
2N6344A, 2N6348A		600	
2N6345A, 2N6349A		800	
*RMS On-State Current (Full cycle, Sine Wave, 50 to 60 Hz) T_C = +80°C	$I_{T(RMS)}$	12	Amp
T_C = +95°C		6.0	
*Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_C = +80°C, Preceded and Followed by Rated Current)	I_{TSM}	120	Amps
Circuit Fusing (T_J = −40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	59	A^2s
*Peak Gate Power (T_C = +80°C, Pulse Width = 2.0 μs	P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Peak Gate Voltage	V_{GM}	±10	Volts
*Operating Junction Temperature Range	T_J	−40 to +125	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R\theta_{JC}$	2.0	°C/W
*Indicates JEDEC Registered Data.			

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Off-State Current V_D = Rated V_{DRM}, T_J = 110°C, Gate Open	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage (Either Direction) I_{TM} = 17 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.75	Volts
Gate Trigger Current, Continuous dc V_D = 12 Vdc, R_L = 100 ohms Minimum Gate Pulse Width = 2.0 μs	I_{GT}				mA
MT2 (+), G(+) All Types		–	6.0	50	
MT2 (+), G(–) 2N6346A thru 2N6349A		–	6.0	75	
MT2 (–), G(–) All Types		–	10	50	
MT2 (–), G(+) 2N6346A thru 2N6349A		–	25	75	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –40°C All Types		–	–	100	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –40°C 2N6346A thru 2N6349A		–	–	125	
*Peak Gate Trigger Voltage V_D = 12 Vdc, R_L = 100 ohms Minimum Gate Pulse Width = 2.0 μs	V_{GT}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(–) 2N6346A thru 2N6349A		–	0.9	2.5	
MT2 (–), G(–) All Types		–	1.1	2.0	
MT2 (–), G(+) 2N6346A thru 2N6349A		–	1.4	2.5	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –40°C All Types		–	–	2.5	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –40°C 2N6346A thru 2N6349A		–	–	3.0	
V_D = Rated V_{DRM}, R_L = 10k ohms, T_J = 100°C					
*MT2 (+), G(+); MT2 (–), G(–) All Types		0.2	–	–	
*MT2 (+), G(–); MT2 (–), G(+) 2N6346A thru 2N6349A		0.2	–	–	
Holding Current (Either Direction)	I_H				mA
V_D = 12 Vdc, Gate Open, I_T = 200 mA, T_C = 25°C		–	6.0	40	
V_D = 12 Vdc, Gate Open, I_T = 200 mA, *T_C = –40°C		–	–	75	
*Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 17A I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	tgt	–	1.5	2.0	μs
Critical Rate of Rise of Commutation Voltage V_D = Rated V_{DRM}, I_{TM} = 17A, Commutating di/dt = 6.5 A/ms, Gate Unenergized T_C = 80°C	dv/dt(c)	–	5.0	–	V/μs

*Indicates JEDEC Registered Data

FIGURE 1 – RMS CURRENT DERATING

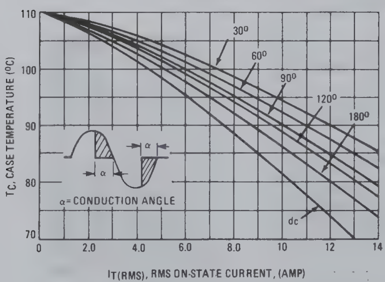


FIGURE 2 – ON-STATE POWER DISSIPATION

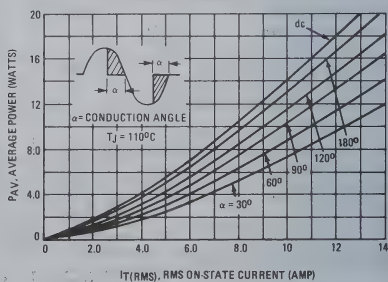


FIGURE 3 — TYPICAL GATE TRIGGER VOLTAGE

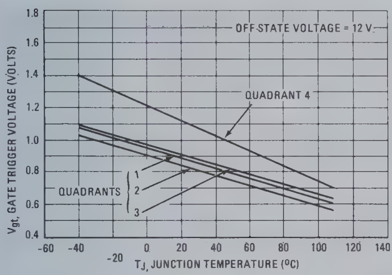


FIGURE 4 — TYPICAL GATE TRIGGER CURRENT

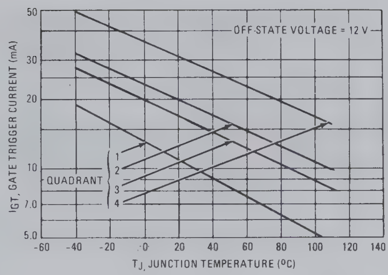


FIGURE 5 — ON-STATE CHARACTERISTICS

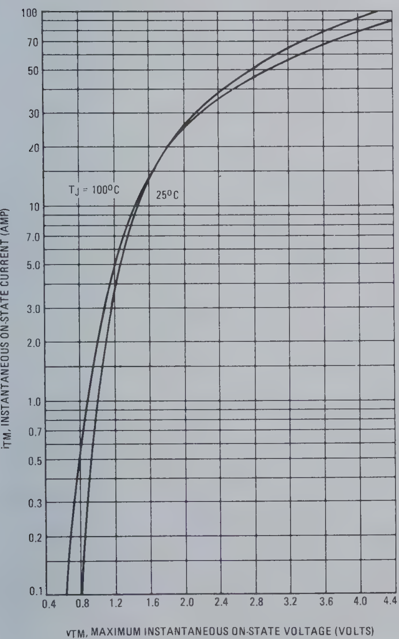


FIGURE 6 — TYPICAL HOLDING CURRENT

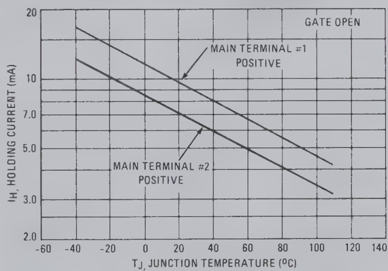
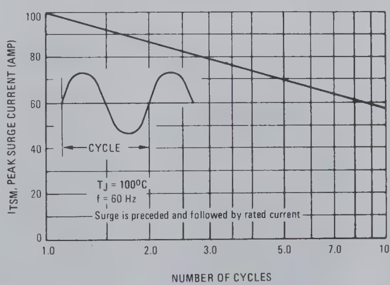
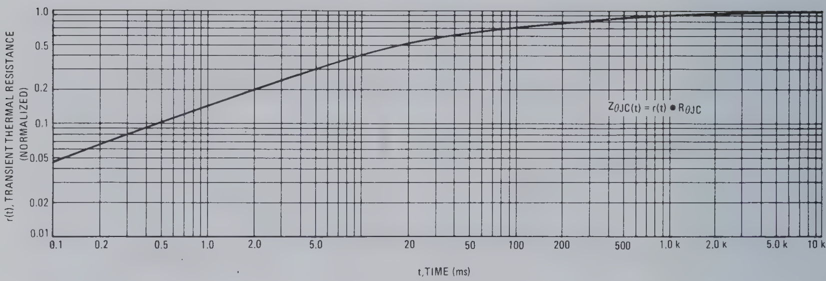


FIGURE 7 — MAXIMUM NON-REPETITIVE SURGE CURRENT



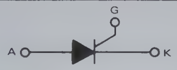
2.3

FIGURE 8 — TYPICAL THERMAL RESPONSE



2N6394 thru 2N6399 MCR220-5 MCR220-7 MCR220-9

MOTOROLA



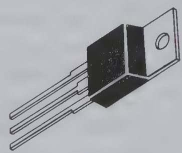
SILICON CONTROLLED RECTIFIERS

12 AMPERES RMS
50–800 VOLTS

REVERSE BLOCKING TRIODE THYRISTORS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts



2.3

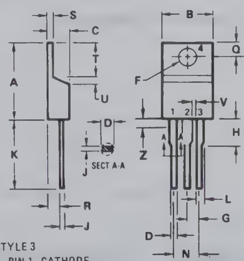
*MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (T_J = –40 to 125°C)	2N6394	V_{RRM} V_{DRM}	50	Volts
	2N6395		100	
	2N6396		200	
	MCR220-5		300	
	2N6397		400	
	MCR220-7		500	
	2N6398		600	
	MCR220-9		700	
	2N6399		800	
RMS On-State Current (All Conduction Angles)	T_C = 90°C	$I_{T(RMS)}$	12	Amps
Peak Non-Repetitive Surge Current (1/2 cycle, Sine Wave, 60 Hz, T_J = 125°C)		I_{TSM}	100	Amps
Circuit Fusing (T_J = –40 to +125°C, t = 1.0 to 8.3 ms)		I^2t	40	A^2s
Forward Peak Gate Power		P_{GM}	20	Watts
Forward Average Gate Power		$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current		I_{GM}	2.0	Amps
Operating Junction Temperature Range		T_J	–40 to +125	°C
Storage Temperature Range		T_{stg}	–40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

*Indicates JEDEC Registered Data.



STYLE 3
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220 AB
All JEDEC dimensions and notes apply

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
* Peak Forward Blocking Current (V_D = Rated V_{DRM} @ T_J = 125°C)	I_{DRM}	–	–	2.0	mA
* Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ T_J = 125°C)	I_{RRM}	–	–	2.0	mA
* Forward "On" Voltage (I_{TM} = 24 A Peak)	V_{TM}	–	1.7	2.2	Volts
* Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms)	I_{GT}	–	5.0	30	mA
* Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms)	V_{GT}	–	0.7	1.5	Volts
(V_D = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)	V_{GD}	0.2	–	–	Volts
* Holding Current (V_D = 12 Vdc)	I_H	–	6.0	40	mA
Turn-On Time (I_{TM} = 12 A, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})	t_{gt}	–	1.0	2.0	μs
Turn-Off Time (V_D = Rated V_{DRM})	t_q				μs
(I_{TM} = 12 A, I_R = 12 A)		–	15	–	
(I_{TM} = 12 A, I_R = 12 A, T_J = 125°C)		–	35	–	
Critical Rate-of-Rise of Off-State Voltage Exponential (V_D = Rated V_{DRM}, T_J = 125°C)	dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – CURRENT DERATING

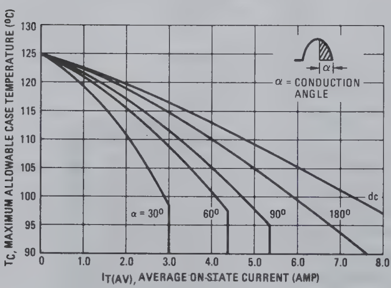


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

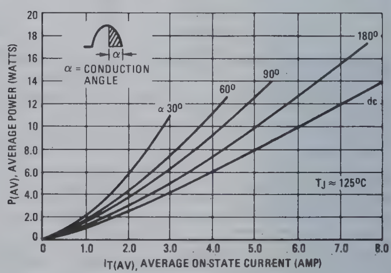


FIGURE 3 – ON-STATE CHARACTERISTICS

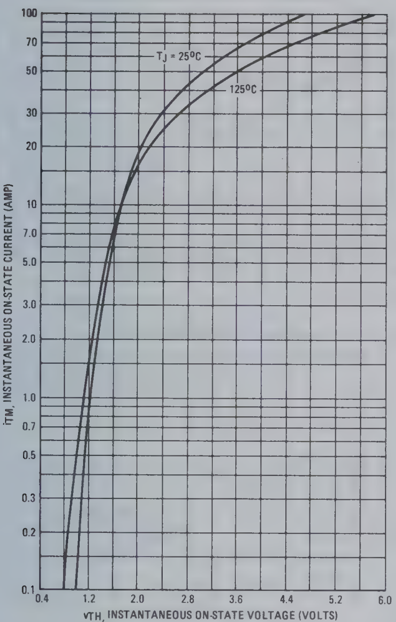
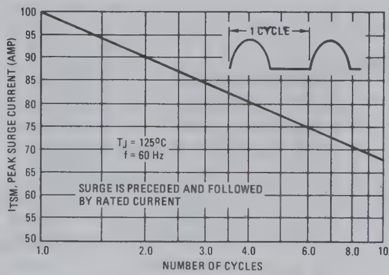
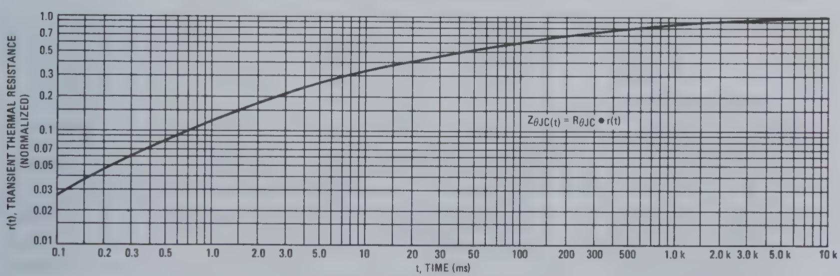


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT



2.3

FIGURE 5 – THERMAL RESPONSE



2.3

TYPICAL CHARACTERISTICS

FIGURE 6 — PULSE TRIGGER CURRENT

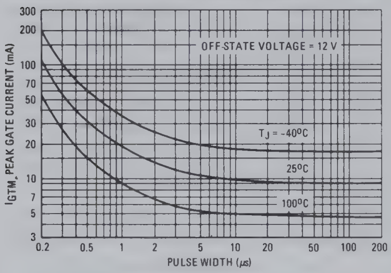


FIGURE 7 — GATE TRIGGER CURRENT

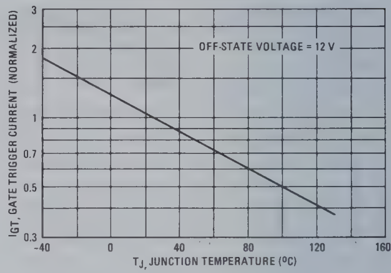


FIGURE 8 — GATE TRIGGER VOLTAGE

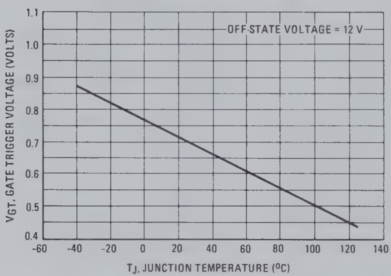
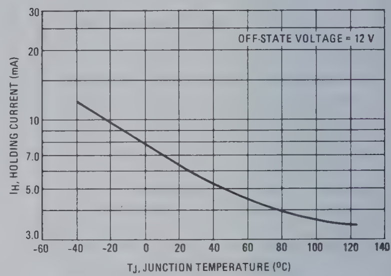


FIGURE 9 — HOLDING CURRENT

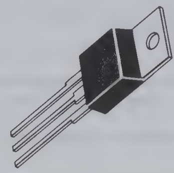


MOTOROLA

2N6400 thru 2N6405 MCR221-5 MCR221-7 MCR221-9

SILICON CONTROLLED RECTIFIER

16 AMPERES RMS
50–800 VOLTS



REVERSE BLOCKING TRIODE THYRISTORS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts

2.3

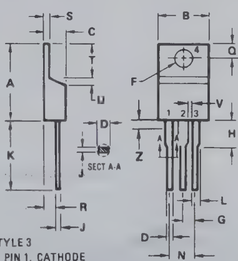
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Voltage	V_{RRM} V_{DRM}		Volts
2N6400		50	
2N6401		100	
2N6402		200	
MCR221-5		300	
2N6403		400	
MCR221-7		500	
2N6404		600	
MCR221-9		700	
2N6405		800	
RMS On-State Current, $T_C = 90^oC$	$I_{T(RMS)}$	16	Amps
Average On-State Current	$I_{T(AV)}$	10	Amps
Peak Non-Repetitive Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz, $T_J = 125^oC$)	I_{TSM}	160	Amps
Circuit Fusing ($T_J = -40$ to $+125^oC$, t = 1.0 to 8.3 ms)	I^2t	100	A^2s
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	−40 to +125	^oC
Storage Temperature Range	T_{stg}	−40 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	$^oC/W$

*Indicates JEDEC Registered Data.



STYLE 3
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220 AB
All JEDEC dimensions and notes apply

2.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM} @ $T_J = 125^oC$)		I_{DRM}	–	–	2.0	mA
*Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ $T_J = 125^oC$)		I_{RRM}	–	–	2.0	mA
*Peak On-State Voltage (I_{TM} = 32 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)		V_{TM}	–	–	1.7	Volts
*Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 50 Ohms)		I_{GT}	–	5.0	30	mA
*Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 50 Ohms)	$T_C = 25^oC$	V_{GT}	–	0.7	1.5	Volts
	$T_C = -40^oC$		–	–	2.5	
(V_D = Rated V_{DRM}, R_L = 50 Ohms)	$T_C = +125^oC$		0.2	–	–	
*Holding Current (V_D = 12 Vdc)	$T_C = 25^oC$	I_H	–	6.0	40	mA
	*$T_C = -40^oC$		–	–	60	
Turn-On Time (I_{TM} = 16 A, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})		t_{gt}	–	1.0	–	μs
Turn-Off Time (I_{TM} = 16 A, I_R = 16 A, V_D = Rated V_{DRM})	$T_C = 25^oC$	t_q	–	15	–	μs
	$T_J = +125^oC$		–	35	–	
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform)	$T_J = +125^oC$	dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

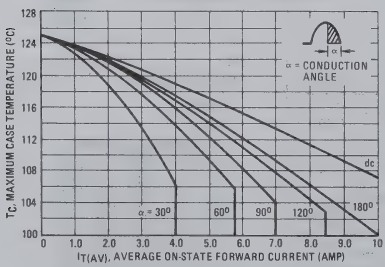


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

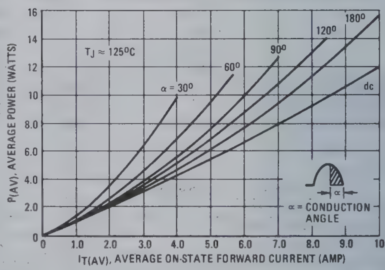


FIGURE 3 — ON-STATE CHARACTERISTICS

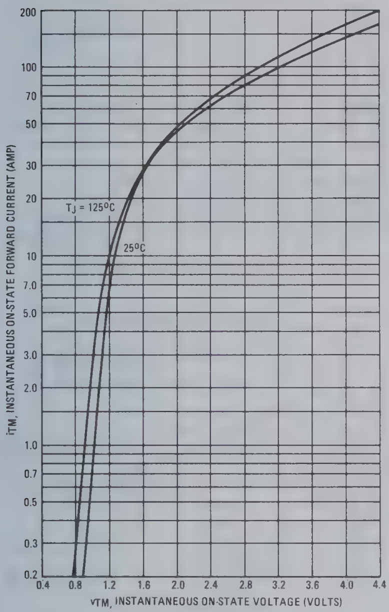


FIGURE 4 — MAXIMUM NON-REPETITIVE SURGE CURRENT

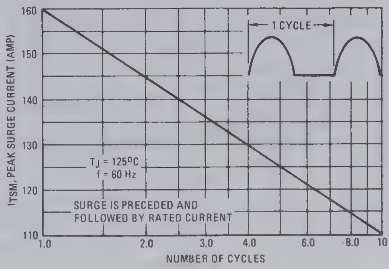
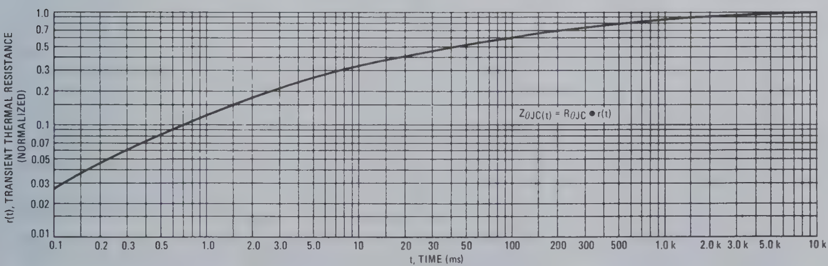


FIGURE 5 — THERMAL RESPONSE



TYPICAL TRIGGER CHARACTERISTICS

FIGURE 6 – PULSE TRIGGER CURRENT

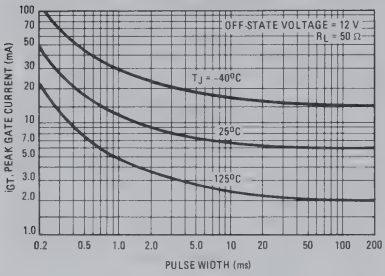
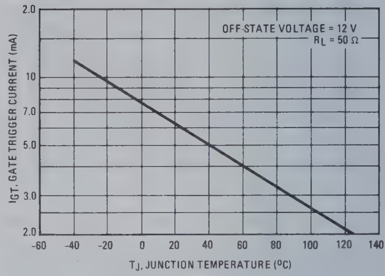


FIGURE 7 – GATE TRIGGER CURRENT



2.3

FIGURE 8 – GATE TRIGGER VOLTAGE

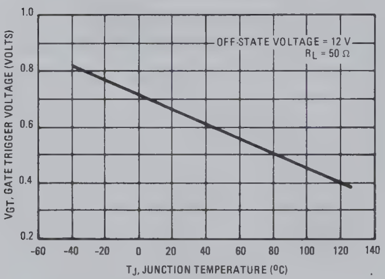
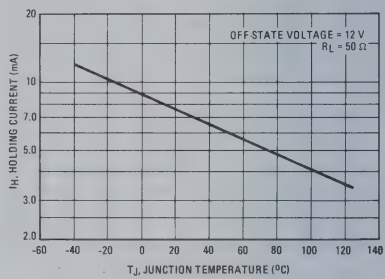


FIGURE 9 – HOLDING CURRENT

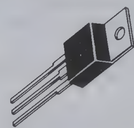


MOTOROLA

2N6504 thru 2N6509
MCR225-5 MCR225-7 MCR225-9 MCR225-12

THYRISTORS

25 AMPERES RMS
50–1000 VOLTS



2.3

25 AMPERES RMS SILICON CONTROLLED RECTIFIERS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supply crowbar circuits.

- Glass Passivated Junctions with Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Constructed for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 1000 Volts
- 300 A Surge Current Capability

MAXIMUM RATINGS

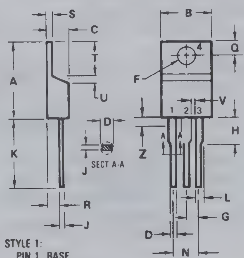
Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (1)	V_{RRM}		Volts
*2N6504		50	
*2N6505		100	
*2N6506		200	
MCR225-5		300	
*2N6507		400	
MCR225-7		500	
*2N6508		600	
MCR225-9		700	
*2N6509		800	
MCR225-12		1000	
Forward Current (T_C = 85°C) (All Conduction Angles)	$I_{T(RMS)}$ $I_{T(AV)}$	25 16	Amps
Peak Nonrepetitive Surge Current — 8.3 ms (1/2 Cycle, Sine Wave) 1.5 ms	I_{TSM}	300 350	Amps
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221-02
TO-220AB

All JEDEC dimensions and notes apply

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_J = 125°C)	V_{DRM}				Volts
*2N6504		50	—	—	
*2N6505		100	—	—	
*2N6506		200	—	—	
MCR225-5		300	—	—	
*2N6507		400	—	—	
MCR225-7		500	—	—	
*2N6508		600	—	—	
MCR225-9		700	—	—	
*2N6509		800	—	—	
MCR225-12		1000	—	—	
*Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)	I_{DRM}	—	—	2.0	mA
*Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)	I_{RRM}	—	—	2.0	mA
*Forward "On" Voltage (1) (I_{TM} = 50 A)	V_{TM}	—	—	1.8	Volts
*Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms) T_C = 25°C	I_{GT}	—	—	40	mA
T_C = −40°C		—	25	75	
*Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms, T_C = −40°C)	V_{GT}	—	1.0	1.5	Volts
Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)	V_{GD}	0.2	—	—	Volts
*Holding Current (Anode Voltage = 12 Vdc, T_C = −40°C)	I_H	—	35	40	mA
*Turn-On Time (I_{TM} = 25 A, I_{GT} = 50 mAdc)	t_{gt}	—	1.5	2.0	µs
Turn-Off Time (V_{DRM} = rated voltage)	t_q				µs
(I_{TM} = 25 A, I_R = 25 A)		—	15	—	
(I_{TM} = 25 A, I_R = 25 A, T_J = 125°C)		—	35	—	
Critical Rate of Rise of Off-State Voltage (Gate Open, Rated V_{DRM}, Exponential Waveform)	dv/dt	—	50	—	V/µs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

FIGURE 1 — AVERAGE CURRENT DERATING

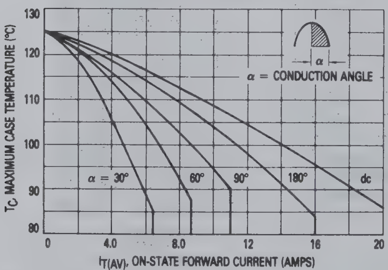


FIGURE 2 — MAXIMUM ON-STATE POWER DISSIPATION

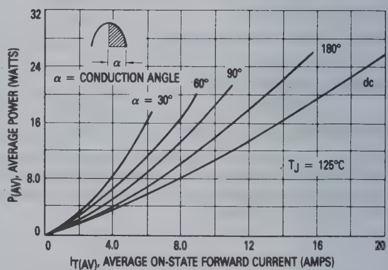


FIGURE 3 — MAXIMUM FORWARD VOLTAGE

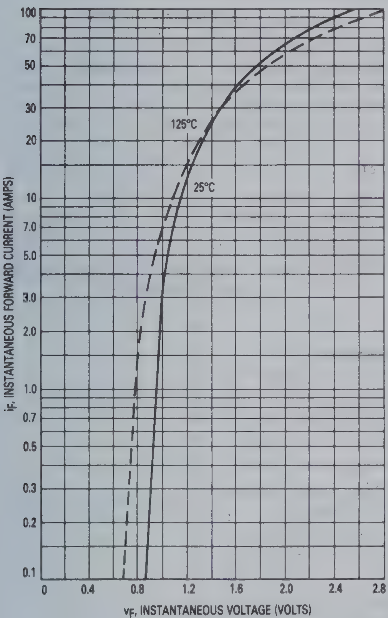


FIGURE 4 — MAXIMUM NON-REPETITIVE SURGE CURRENT

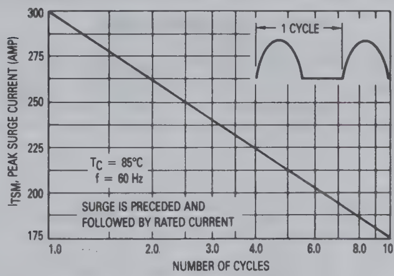


FIGURE 5 — CHARACTERISTICS AND SYMBOLS

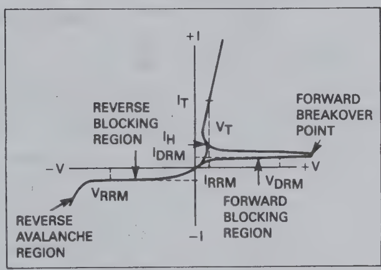
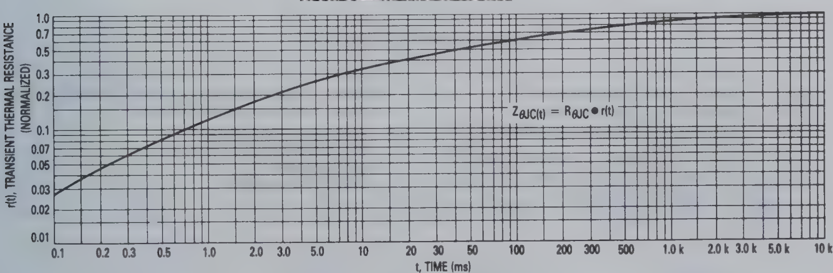


FIGURE 6 — THERMAL RESPONSE



2.3

TYPICAL TRIGGER CHARACTERISTICS

FIGURE 7 — GATE TRIGGER CURRENT

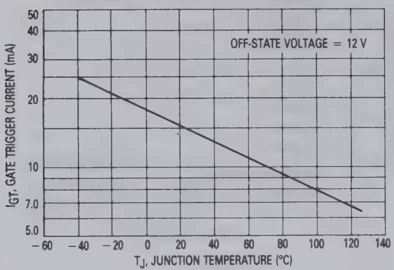


FIGURE 8 — GATE TRIGGER VOLTAGE

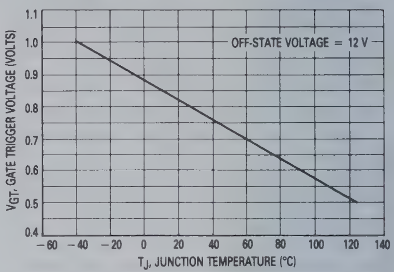
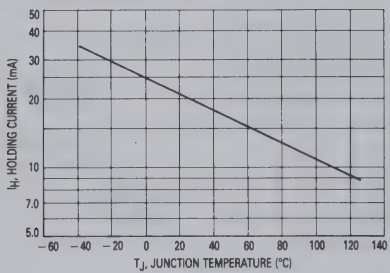


FIGURE 9 — HOLDING CURRENT



THYRISTOR APPLICATION NOTES

AN-240 SCR Power Control Fundamentals
AN-295 Suppressing RFI in Thryistor Circuits
AN-443 Directional and Speed Control for Series, Universal and Shunt Motors
AN-482 Electronic Speed Control of Appliance Motors
AN-527 Theory, Characteristics and Applications of the Programmable Unijunction Transistor
AN-725 A Low-Cost 80 V-1.5 A Color TV Power Supply

To obtain copies of these notes list the AN number(s) on your company letterhead and send your request to:

Technical Information Center
Motorola Semiconductor Products, Inc.
P.O. Box 20912
Phoenix, Arizona 85036

MOTOROLA

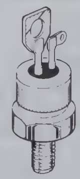
REVERSE BLOCKING TRIODE THYRISTOR

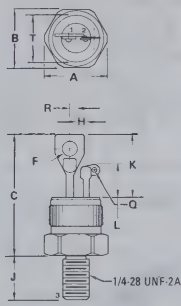
. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Blocking Voltage to 800 Volts

SILICON CONTROLLED RECTIFIER

35 AMPERE RMS
25-800 VOLTS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

CASE 263-03
Similar to TO-48

MAXIMUM RATINGS ($T_J = 125^oC$ unless otherwise noted.)

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (1) (T_C = –65 to +125°C)	C35U	V_{DRM} or V_{RRM}	25	Volts
	C35F		50	
	C35A		100	
	C35G		150	
	C35B		200	
	C35H		250	
	C35C		300	
	C35D		400	
	C35E		500	
	C35M		600	
	C35S		700	
	C35N		800	
Non-Repetitive Peak Reverse Voltage (T_C = –65 to +125°C, V < 5.0 ms)	C35U	V_{RSM}	35	Volts
	C35F		75	
	C35A		150	
	C35G		225	
	C35B		300	
	C35H		350	
	C35C		400	
	C35D		500	
	C35E		600	
	C35M		720	
	C35S		840	
	C35N		960	
RMS On-State Current (All Conduction Angles)		$I_{T(RMS)}$	35	Amp
Peak Non-Repetitive Surge Current (One cycle, 60 Hz)		I_{TSM}	225	Amp
Circuit Fusing (t = 1.0 to 8.3 ms)		I^2t	75	A^2s
Peak Gate Power		P_{GM}	5	Watts
Average Gate Power		$P_{G(AV)}$	0.5	Watt
Peak Reverse Gate Voltage		V_{GRM}	5	Volts
Operating Junction Temperature Range		T_J	-65 to +125	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

THERMAL CHARCTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.7	°C/W

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

2.3

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Reverse or Forward Blocking Current (V_D = Rated V_{DRM}, T_C = +125°C) (V_R = Rated V_{RRM}, T_C = 125°C)	C35U,F,A,G	I_{DRM} or I_{RRM}	–	–	13	mA
	C35B		–	–	12	
	C35H		–	–	11	
	C35C		–	–	10	
	C35D		–	–	8	
	C35E		–	–	6	
	C35M		–	–	5	
	C35S		–	–	4.5	
	C35N		–	–	4	
Average Forward or Reverse Blocking Current (V_D = Rated V_{DRM}, T_C = +125°C) (V_R = Rated V_{RRM}, T_C = 125°C)	C35U,F,A,G	I_{DRM} (AV) or I_{RRM} (AV)	–	–	6.5	mA
	C35B		–	–	6	
	C35H		–	–	5.5	
	C35C		–	–	5	
	C35D		–	–	4	
	C35E		–	–	3	
	C35M		–	–	2.5	
	C35S		–	–	2.25	
	C35N		–	–	2	
Peak On-State Voltage (I_{TM} = 50.3 A peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2.0%)		V_{TM}	–	–	2	Volts
Gate Trigger Current, Continuous dc (V_D = 12 Vdc, R_L = 50 Ω)		I_{GT}	–	6	40	mA
(V_D = 12 Vdc, R_L = 50 Ω, T_C = –65°C)			–	–	80	
Gate Trigger Voltage, Continuous dc (V_D = 12 Vdc, R_L = 50 Ω, T_C = –65°C to +125°C)		V_{GT}	–	–	3	Volts
(V_D = Rated V_{DRM}, R_L = 1000 Ω, T_C = 125°C)			.25			
Holding Current (V_D = 24 Vdc, Gate Supply = 10 V, 20 Ω, 45 μs minimum pulse width, I_T = 0.5A)		I_H	–	–	100	mA
Critical Rate of Rise of Forward Blocking Voltage V_D = Rated V_{DRM}, T_C = +125°C)	C35U,F,M,S,N	dv/dt	10	–	–	V/μs
	C35A,G,B,H		20	–	–	
	C35C,D,E		25	–	–	

FIGURE 1 — CURRENT DERATING (HALF-WAVE RECTIFIED SINE WAVE)

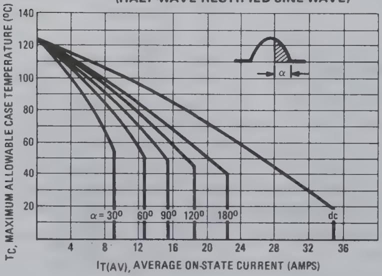
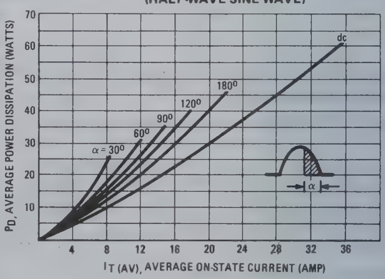


FIGURE 2 — POWER DISSIPATION (HALF-WAVE SINE WAVE)



MOTOROLA

C106 series

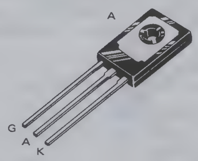
REVERSE BLOCKING TRIODE THYRISTORS

. . . Glassivated PNPN devices designed for high-volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Glassivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability

SILICON CONTROLLED RECTIFIER

4 AMPERES RMS
15 thru 600 VOLTS



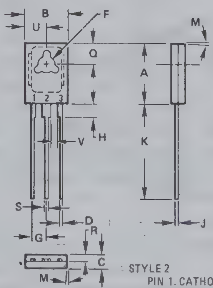
MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage R_{GK} = 1 kΩ T_C = −40° to 110°C	C106Q	V_{DRM} OR V_{RRM}	15	Volts
	C106Y		30	
	C106F		50	
	C106A		100	
	C106B		200	
	C106C		300	
	C106D		400	
	C106E		500	
	C106M		600	
RMS Forward Current (All Conduction Angles)		$I_{T(RMS)}$	4	Amp
Average Forward Current T_A = 30°C		$I_{T(AV)}$	2.55	Amp
Peak Non-Repetitive Surge Current (1/2 Cycle, 60 Hz, T_J = −40 to +110°C)		I_{TSM}	20	Amp
Circuit Fusing t > 1.5 ms		I^2t	0.5	A^2s
Peak Gate Power		P_{GM}	0.5	Watt
Average Gate Power		$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current		I_{GFM}	0.2	Amp
Peak Reverse Gate Voltage		V_{GRM}	6	Volts
Operating Junction Temperature Range		T_J	−40 to +110	°C
Storage Temperature Range		T_{stg}	−40 to +150	°C
Mounting Torque (Note 1)			6	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W

NOTE 1. Torque rating applies with use of compression washer (B52200F006). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-290 B)
For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C. For optimum results, an activated flux (oxide removing) is recommended.



STYLE 2
PIN 1. CATHODE
2. ANODE
3. GATE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

2.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Rated V_{DRM}, R_{GK} = 1000 Ohms, $T_J = 25^oC$) (Rated V_{DRM}, R_{GK} = 1000 Ohms, $T_J = 110^oC$)	I_{DRM}	 – –	 – –	 10 100	μA
Peak Reverse Blocking Current (Rated V_{RRM}, R_{GK} = 1000 Ohms, $T_J = 25^oC$) (Rated V_{RRM}, R_{GK} = 1000 Ohms, $T_J = 110^oC$)	I_{RRM}	 – –	 – –	 10 100	μA
Forward "On" Voltage (I_{FM} = 4 A Peak)	V_{TM}	–	–	2.2	Volts
Gate Trigger Current (Continuous dc) (V_{AK} = 6 Vdc, R_L = 100 Ohms) (V_{AK} = 6 Vdc, R_L = 100 Ohms, $T_C = -40^oC$)	I_{GT}	 – –	 30 75	 200 500	μA
Gate Trigger Voltage (Continuous dc) $T_J = 25^oC$ (V_{AK} = 6 Vdc, R_L = 100 Ohms, R_{GK} = 1000 Ohms) $T_J = -40^oC$ (V_{AK} = Rated V_{DRM}, R_L = 3000 Ohms, R_{GK} = 1000 Ohms, $T_J = 110^oC$)	V_{GT}	0.4 0.5 0.2	– – –	0.8 1 –	Volts
Holding Current $T_J = 25^oC$ (V_D = 12 Vdc, R_{GK} = 1000 Ohms) $T_J = -40^oC$ $T_J = +110^oC$	I_{HX}	0.3 0.4 0.14	– – –	3 6 2	mA
Forward Voltage Application Rate ($T_J = 110^oC$, R_{GK} = 1000 Ohms, V_D = Rated V_{DRM})	dv/dt	–	8	–	V/μs
Turn-On Time	t_{gt}	–	1.2	–	μs
Turn-Off Time	t_q	–	40	–	μs

2.3

FIGURE 1 – AVERAGE CURRENT DERATING

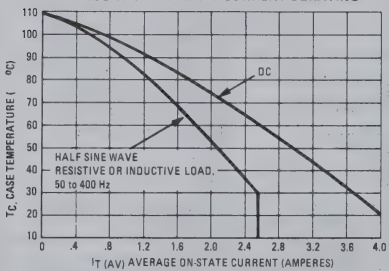
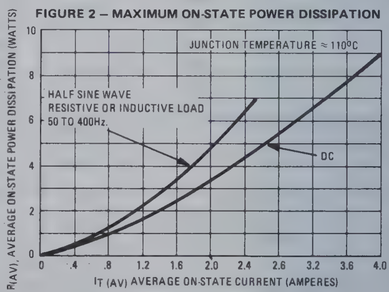
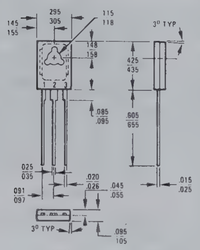


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

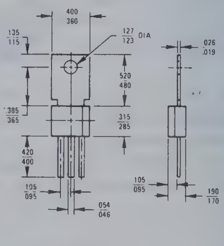


Package Interchangeability

The dimensional diagrams below compare the critical dimensions of the Motorola C-106 package with competitive devices. It has been demonstrated that the smaller dimensions of the Motorola package make it compatible in most lead-mount and chassis-mount applications. The user is advised to compare all critical dimensions for mounting compatibility.



Motorola C-106 Package



Competitive C-106 Package

MOTOROLA

C122 series

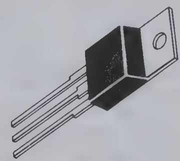
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 600 Volts
- Different Lead Form Configurations, Suffix (2) thru (6) available, see Thyristor Selection Guide for Information

SILICON CONTROLLED RECTIFIER

8 AMPERES RMS
50–600 VOLTS



2.3

MAXIMUM RATINGS

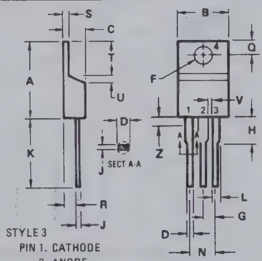
Rating (Note 2)	Symbol	Value	Unit
Repetitive Peak Off-State Voltage Repetitive Peak Reverse Voltage	V_{DRM} V_{RRM}		Volts
C122F		50	
C122A		100	
C122B		200	
C122C		300	
C122D		400	
C122E		500	
C122M		600	
Non-Repetitive Peak Reverse Voltage	V_{RSM}		Volts
C122F		75	
C122A		200	
C122B		300	
C122C		400	
C122D		500	
C122E		600	
C122M		700	
Forward Current RMS (All Conduction Angles) $T_C \leq 75^oC$	$I_{T(RMS)}$	8	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz,)	I_{TSM}	90	Amps
Circuit Fusing Considerations t = 8.3 ms	I^2t	34	A^2s
Forward Peak Gate Power (t = 10 μs)	P_{GM}	5	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	−40 to +100	^oC
Storage Temperature Range	T_{stg}	−40 to +125	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8	$^oC/W$

(1) V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

(2) Add lead form suffix designator "( )" to part number for lead configurations 2 thru 6. See Thyristor Selection Guide for information.



STYLE 3
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221-02
TO-220 AB

All JEDEC dimensions and notes apply

NOTE: SUFFIX (1) Lead Configuration Available as standard.

2.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}) $T_C = 25^oC$ $T_C = 100^oC$	I_{DRM}	– –	– –	0.1 0.5	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}) $T_C = 25^oC$ $T_C = 100^oC$	I_{RRM}	– –	– –	0.1 0.5	mA
Peak On-State Voltage (1) (I_{TM} = 16 A Peak, $T_C = 25^oC$)	V_{TM}	–	–	1.83	Volts
Gate Trigger Current (Continuous dc) (V_D = 6 V, R_L = 91 Ohms, $T_C = 25^oC$) (V_D = 6 V, R_L = 45 Ohms, $T_C = -40^oC$)	I_{GT}	 – –	 – –	 25 40	mA
Gate Trigger Voltage (Continuous dc) (V_D = 6 V, R_L = 91 Ohms, $T_C = 25^oC$) (V_D = 6 V, R_L = 45 Ohms, $T_C = -40^oC$) (V_D = Rated V_{DRM}, R_L = 1000 Ohms, $T_C = 100^oC$)	V_{GT}	 – – 0.2	 – – –	 1.5 2 –	Volts
Holding Current (V_D = 24 Vdc, I_T = 0.5 A, 0.1 to 10 ms Pulse, Gate Trigger Source = 7 V, 20 Ohms) $T_C = 25^oC$ $T_C = -40^oC$	I_H	 – –	 – –	 30 60	mA
Turn-Off Time (V_D = Rated V_{DRM}) (I_{TM} = 8 A, I_R = 8A)	tq	–	50	–	μs
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Linear, $T_C = 100^oC$)	dv/dt	–	50	–	V/μs

(1) Pulse Test: Pulse Width = 1 ms, Duty Cycle ≤ 2%.

FIGURE 1 – CURRENT DERATING (HALF-WAVE)

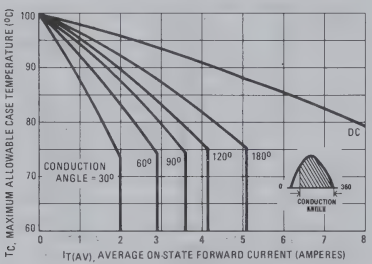


FIGURE 2 – CURRENT DERATING (FULL-WAVE)

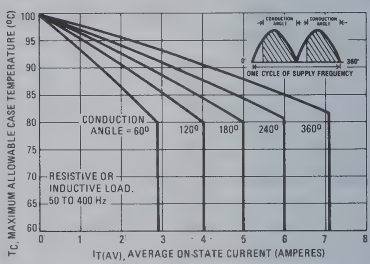


FIGURE 3 – MAXIMUM POWER DISSIPATION (HALF-WAVE)

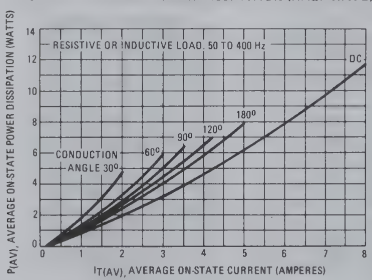
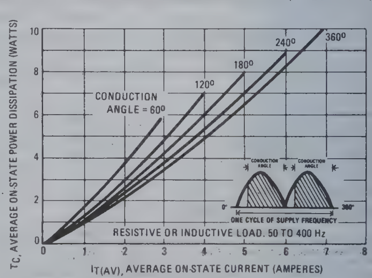


FIGURE 4 – MAXIMUM POWER DISSIPATION (FULL-WAVE)



MOTOROLA

C228
C228( )3
C229
series

REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 300 Amp
- Low Forward "On" Voltage — 1.2 V (Typ) @ I_{TM} = 35 Amp
- Practical Level Triggering and Holding Characteristics — 10 mA (Typ) @ T_C = 25°C
- Rugged Construction in Either Pressfit, Stud, or Isolated Stud Packages
- Glass Passivated Junctions for Maximum Reliability

SILICON CONTROLLED RECTIFIER

35 AMPERES RMS
50 thru 600 VOLTS

MAXIMUM RATINGS

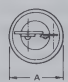
Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (1) (T_J = -40 to +125°C)	V_{DRM} and V_{RRM}		Volts
C229F, C228F, C228F3		50	
C229A, C228A, C228A3		100	
C229B, C228B, C228B3		200	
C229C, C228C, C228C3		300	
C229D, C228D, C228D3		400	
C229E, C228E, C228E3		500	
C229M, C228M, C228M3		600	
Non-Repetitive Reverse Voltage (T_J = -40 to +125°C)	V_{RSM}		Volts
C229F, C228F, C228F3		75	
C229A, C228A, C228A3		150	
C229B, C228B, C228B3		300	
C229C, C228C, C228C3		400	
C229D, C228D, C228D3		500	
C229E, C228E, C228E3		600	
C229M, C228M, C228M3		720	
Forward Current RMS	$I_{T(RMS)}$	35	Amp
Peak Surge Current (one cycle, 60 Hz) (T_C = -40 to +125°C)	I_{TSM}	300	Amp
Circuit Fusing Considerations (T_C = -40 to +125°C) (t = 1.0 to 8.3 ms)	I^2t	370	A^2s
Peak Gate Power	P_{GM}	5	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Forward Gate Current	I_{GM}	2	Amp
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
C228 and C229 Series		1.7	
C228( ) 3 Series		1.85	

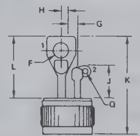
(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.

C229 Series



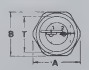
STYLE 1:
1. CATHODE
2. GATE
CASE ANODE

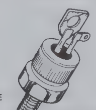
CASE 310-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0 501	0.505
F	-	4 06	-	0.160
G	2.16	2.41	0.085	0.095
H	1.52	1.78	0.060	0.070
J	7.62	8.89	0.300	0.350
K		26.67	–	1.050
L	-	17 02	–	0.670
Q	1.40	2.16	0.055	0.085

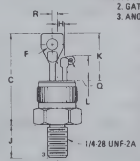
C228 Series





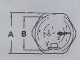
STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

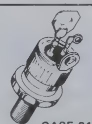
CASE 263-03



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1 190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

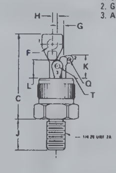
C228( ) 3 Series





STYLE 1:
1. CATHODE
2. GATE
3. ANODE

CASE 311-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	-	32.51	–	1.280
F	–	4 06	–	0 160
G	2.16	2.41	0.085	0.095
H	1.60	2 01	0.063	0 079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Rated V_{DRM}, with gate open) T_C = 25°C T_C = 125°C	I_{DRM}	– –	– –	1 3	mA
Peak Reverse Blocking Current (Rated V_{RRM}) T_C = 25°C T_C = 125°C	I_{RRM}	– –	– –	1 3	mA
Forward "On" Voltage (I_{TM} = 100 A Peak)	V_{TM}	–	–	1.9	Volts
Gate Trigger Current (V_D = 12 Vdc, R_L = 80 Ohms, T_C = 25°C) (V_D = 6 Vdc, R_L = 50 Ohms, T_C = -40°C)	I_{GT}	 – –	 – –	 40 80	mA
Gate Trigger Voltage (V_D = 12 Vdc, R_L = 80 Ohms, T_C = 25°C) (V_D = 6 Vdc, R_L = 80 Ohms, T_C = -40°C)	V_{GT}	 – –	 – –	 2.5 3	Volts
Gate Trigger Voltage (Rated V_{DRM}, R_L = 1000 Ohms, T_C = +125°C)	V_{GT}	0.2	–	–	Volts
Holding Current (Anode Voltage = 24 V, gate open) T_C = 25°C T_C = -40°C	I_H	– –	– –	75 150	mA
Turn-On Time (t_d + t_r) (I_{TM} = 35 Adc, I_{GT} = 40 mAdc)	t_{on}	–	1.0	–	μs
Turn-Off Time (I_{TM} = 10 A, I_R = 10 A) (I_{TM} = 10 A, I_R = 10 A, T_C = 100°C)	t_{off}	 – –	 20 35	 – –	μs
Forward Voltage Application Rate (T_C = 100°C)	dv/dt	–	50	–	V/μs

2.3

FIGURE 1 – CURRENT DERATING (HALF-WAVE RECTIFIED SINE WAVE)

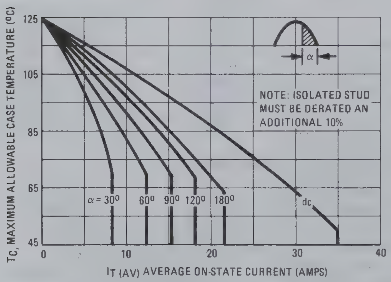
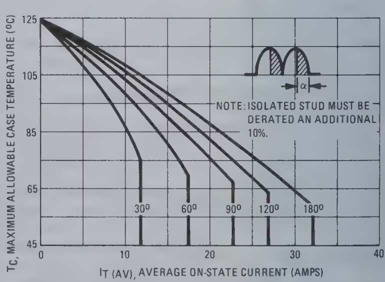


FIGURE 2 – CURRENT DERATING (FULL-WAVE RECTIFIED SINE WAVE)



C230, 231
C230( )3, 231( )3
C232, 233
series

MOTOROLA

REVERSE BLOCKING TRIODE-THYRISTOR

. . . designed for industrial and consumer applications such as power supplies; battery chargers; temperature, motor, light, and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 250 Amp
- Low Forward "On" Voltage — 1.2 V (Typ) @ I_{TM} = 25 Amp
- Practical Level Triggering and Holding Characteristics — 10 mA (Typ) @ $T_C = 25^{\circ}C$
- Rugged Construction in Either Pressfit, Stud or Isolated Stud
- Glass Passivated Junctions for Maximum Reliability

SILICON CONTROLLED RECTIFIER

25 AMPERES RMS
50 thru 600 VOLTS

MAXIMUM RATINGS ($T_C = 100^{\circ}C$ unless otherwise noted)

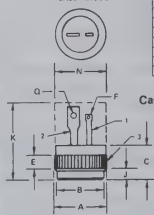
Rating	Suffix	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (1) (T_C = −40 to +100°C) All Types	F	V_{DRM} and V_{RRM}	50	Volts
	A		100	
	B		200	
	C		300	
	D		400	
	E		500	
	M		600	
Non-Repetitive Reverse Voltage (T_C = −40 to 100°C) All Types	F	V_{RSM}	75	Volts
	A		150	
	B		300	
	C		400	
	D		500	
	E		600	
	M		720	
Forward Current RMS		$I_{T(RMS)}$	25	Amp
Peak Surge Current (One Cycle, 60 Hz)(T_C = −40 to 100°C)		I_{TSM}	250	Amp
Circuit Fusing (T_C = −40 to +100°C)(t = 1.0 to 8.3 ms)		I^2t	260	A^2s
Peak Gate Power		P_{GM}	5	Watts
Average Gate Power		$P_{G(AV)}$	0.5	Watt
Peak Forward Gate Current		I_{GM}	2	Amp
Operating Junction Temperature Range		T_J	−40 to +100	°C
Storage Temperature Range		T_{stg}	−40 to +125	°C
Stud Torque		—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
Pressfit and Stud			1.00	
Isolated Stud			1.15	

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.

STYLE 1
1. GATE
2. CATHODE
CASE. ANODE

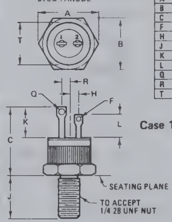


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12 73	12 83	0 501	0 505
B	11 81	12 06	0 465	0 475
C	8 39	9.65	0.330	0 380
E	2.54	-	0 100	-
F	0.89	2.16	0 035	0 085
J	2 04	2.46	0 080	0.097
K		20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0 160

Case 174-03

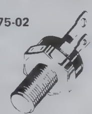
C232 and C233 series

STYLE 1.
TERM. 1. CATHODE
2. GATE
STUD. ANODE



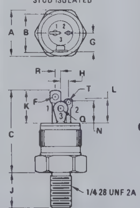
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0 551	0 559
C	20 70	24 13	0 815	0.950
F	0.89	2 16	0 035	0.085
H	2.29 REF		0 090 REF	
J	10 67	11.56	0.420	0.455
K	9 78	10.54	0.385	0.415
L	6 99	7 75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

Case 175-02



C230 and 231 series

STYLE 1
1. CATHODE
2. GATE
3. ANODE
STUD ISOLATED



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14 00	14.20	0.551	0.559
B	12 73	12.83	0.501	0 505
C	–	26.16	-	1.030
F	1.65	4.06	0.065	0.160
G	–	6.48	–	0.255
H	2.16	2.41	0.085	0.095
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
R	1.52	1.78	0.060	0.070
T	0.89	2.16	0.035	0.085

Case 235-02

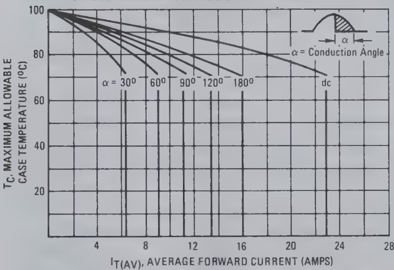
C230( )3 and C231( )3 series

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Currrent (V_D = Rated V_{DRM}, with gate open) (V_R = Rated V_{RRM}) T_C = 25°C / T_C = 100°C	I_{DRM} or I_{RRM}	– / –	– / –	0.5 / 1.0	mA
Forward "On" Voltage (I_{TM} = 100 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_{TM}	–	–	1.9	Volts
Gate Trigger Current, C230, C230( )3, C232 series (V_D = 12 Vdc, R_L = 120 Ohms) / (V_D = 12 Vdc, R_L = 60 Ohms) T_C = −40°C	I_{GT}	– / –	– / –	25 / 40	mA
Gate Trigger Current, C231, C231( )3, C233 (V_D = 12 Vdc, R_L = 120 Ohms) / (V_D = 12 Vdc, R_L = 60 Ohms) T_C = −40°C	I_{GT}	– / –	– / –	9.0 / 20	mA
Gate Trigger Voltage (V_D = 12 Vdc, R_L = 120 Ohms) / (V_D = 12 Vdc, R_L = 60 Ohms) T_C = −40°C / (V_D = Rated V_{DRM}, R_L = 1000 Ohms) T_C = +100°C	V_{GT}	– / – / 0.2	– / – / –	1.5 / 2.0 / –	Volts
Holding Current (V_D = 24 V, gate open, I_T = 0.5 A) / T_C = −40°C	I_H	– / –	– / –	50 / 100	mA
Turn-On Time ($t_d + t_r$) (I_{TM} = 25 Adc, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})	t_{gt}	–	1.0	–	μs
Turn-Off Time (I_{TM} = 10 A, I_R = 10 A, Pulse Width = 50 μs, dv/dt = 20 V/μs, V_D = Rated V_{DRM}) / T_C = 100°C	t_q	– / –	25 / 35	– / –	μs
Forward Voltage Application Rate (V_D = Rated V_{DRM}) T_C = 100°C	dv/dt	–	100	–	V/μs

FIGURE 1 – CURRENT DERATING FOR PRESSFIT AND NON-ISOLATED STUD



NOTE: Derating is for Pressift and Stud Devices. Isolated stud devices must be derated an additional 15%. For example, the max T_C @ 16 A (180° conduction angle) is 70°C, a derating of 30°C. Isolated stud devices must be derated 34.5°C; therefore, the maximum T_C is 65.5°C.

FIGURE 2 – ON-STATE POWER DISSIPATION versus ON-STATE CURRENT

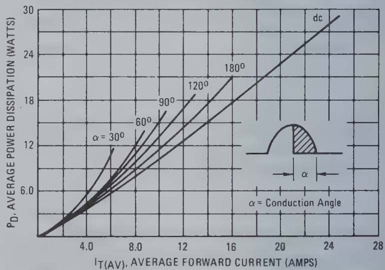


FIGURE 3 – GATE CURRENT VARIATION WITH TEMPERATURE

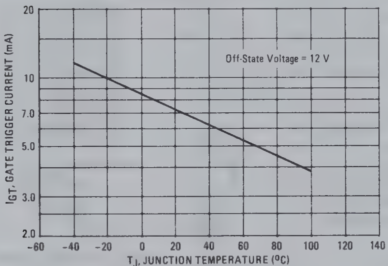
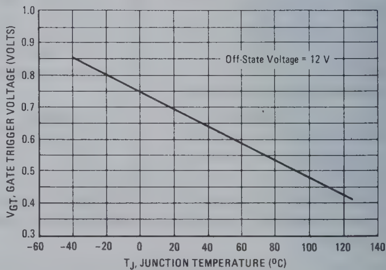


FIGURE 4 – GATE VOLTAGE VARIATION WITH TEMPERATURE

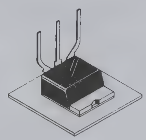


CT15/CT15A SERIES
15 AMPERES RMS
CT223/CT223A SERIES
25 AMPERES RMS

MOTOROLA

TRIACS

200–800 VOLTS



2.3

SILICON BIDIRECTIONAL TRIODE THYRISTORS

...designed primarily for industrial and consumer applications for full-wave control of ac loads such as solid-state relays, appliance controls, power supplies, heating controls, motor controls, welding equipment, and power switching systems.

- Electrical Isolation from Mounting Surface
- Capable of 2500 V RMS Isolation
- Glass Passivated and Center Gate Geometry
- Gate Triggering Guaranteed in:
  - Three Modes (CT223 series)
  - Four Modes (CT15A/223A series)
- Devices With Solder Backing Available
  (Add Suffix M to Device Type)

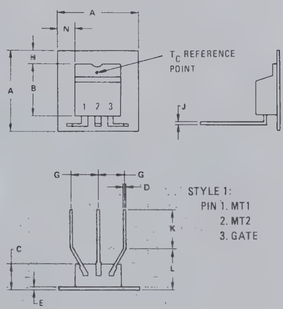
MAXIMUM RATINGS (T_J = –40 to +125°C unless otherwise noted)

Rating	Symbol	CT series 15	CT series 223	Unit
Repetitive Peak Off-State Voltage 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}			Volts
CT15 or CT223 –4, A4		200	200	
–5, A5		300	300	
–6, A6		400	400	
–7, A7		500	500	
–8, A8		600	600	
–9, A9		700	700	
–10, A10		800	800	
RMS On-State Current (T_C = 90°C for CT15/15A) (T_C = 80°C for CT223/223A)	$I_{T(RMS)}$	15 —	— 25	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	150	250	Amps
Circuit Fusing (t = 8.3 ms)	I^2t	90	260	A^2s
Average Gate Power	$P_{G(AV)}$	0.5	0.5	Watts
Peak Gate Current (10 μs)	I_{GM}	2.0	2.0	Amps
Operating Junction Temperature Range	T_J	–40 to +125		°C
Storage Temperature Range	T_{stg}	–40 to +125		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Maximum Value		Unit
Thermal Resistance, Junction to Case (DC)	$R_{\theta JC}$	2.0	1.2	°C/W

Notes:
1. To order a three mode Triac, a hyphen is required between the series type and voltage indicator number, for example, CT223-6. For a four mode triac, the hyphen is replaced by the letter A, for example, CT223A6.
2. Devices with solder backing available by adding suffix M. For example, CT223A6M. The recommended solder temperature is 225°C (max.) for a duration of five minutes (max.).
3. A nominal value of 0.3°C/watt is recommended for the case temperature reference point to heat sink thermal resistance for thermal design considerations



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	17.53	18.03	0.690	0.710
B	10.92	11.43	0.430	0.450
C	4.83	5.33	0.190	0.210
D	0.64	0.89	0.025	0.035
E	0.51	0.76	0.020	0.030
G	5.46	5.97	0.215	0.235
H	3.30	3.56	0.130	0.140
J	0.36	0.56	0.014	0.022
K	6.98	8.26	0.275	0.325
L	6.60	7.62	0.260	0.300
N	3.56	4.06	0.140	0.160

CASE 335-01

2.3

ELECTRICAL CHARACTERISTICS

(All voltage polarity reference to MT1; applies to either polarity of MT2 to MT1; T_C = 25°C unless otherwise noted)

Characteristic	Symbol	CT15/15A Min	CT15/15A Typ	CT15/15A Max	CT223/223A Min	CT223/223A Typ	CT223/223A Max	Unit
Peak Blocking Current T_C = 125°C V_D = Rated V_{DRM}, Gate Open	I_{DRM}	–	–	2.0	–	–	2.0	mA
Peak On-State Voltage Pulse Width = 1 ms, Duty Cycle 2% I_{TM} = 21 A Peak I_{TM} = 35 A Peak	V_{TM}	 – –	 1.3 –	 1.6 –	 – –	 – 1.4	 – 1.85	Volts
Peak Gate Trigger Current V_D = 12 Vdc, R_L = 50 Ohms, Pulse Width = 10 µs	I_{GTM}	See Table 1						mA
Peak Gate Trigger Voltage V_D = 12 Vdc, R_L = 50 Ohms, Pulse Width = 10 µs	V_{GTM}	See Table 1						Volts
Peak Gate Non-Trigger Voltage V_D = Rated V_{DRM}, R_L = 10 Ω, T_C = 125°C	V_{GD}	0.2	–	–	0.2	–	–	Volts
Holding Current V_D = 12 Vdc, Gate Open, R_L = 40 Ohms	I_H	–	6.0	40	–	10	50	mA
Turn-On Time V_D = Rated V_{DRM} I_{TM} = 21 A, I_G = 120 mA I_{TM} = 35 A, I_G = 200 mA	tgt	 – –	 1.5 –	 – –	 – –	 – 1.5	 – –	µs
Critical Rate-of-Rise of Commutation Voltage V_D = Rated V_{DRM}, I_{TM} = 21 A, Commutating di/dt = 8 A/ms, T_C = 90°C V_D = Rated V_{DRM}, I_{TM} = 35 A, Commutating di/dt = 14 A/ms, T_C = 80°C	dv/dt (c)	 – –	 5.0 –	 –	 –	 – 5.0	 – –	V/µs
Critical Rate-of-Rise of Off-State Voltage (Exponential Rise) V_D = Rated V_{DRM}, Gate Open, T_C = 125°C	dv/dt	–	100	–	–	100	–	V/µs

TABLE 1. PEAK GATE TRIGGER CURRENT AND VOLTAGE

Symbol	Polarity	CT Series 15	CT Series 15A	CT Series 223	CT Series 223A
I_{GT1}	MT2(+), G(+)	50 mA	50	50	50
I_{GT2}	MT2(+), G(–)	–	75	50	50
I_{GT3}	MT2(–), G(–)	50	50	50	50
I_{GT4}	MT2(–), G(+)	–	75	–	75
V_{GT1}	MT2(+), G(+)	2.0 volts	2.0	2.0	2.0
V_{GT2}	MT2(+), G(–)	–	2.5	2.0	2.0
V_{GT3}	MT2(–), G(–)	2.0	2.0	2.0	2.0
V_{GT4}	MT2(–), G(+)	–	2.5	–	2.5

FIGURE 1 – CURRENT DERATING

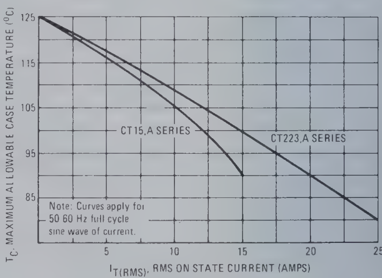
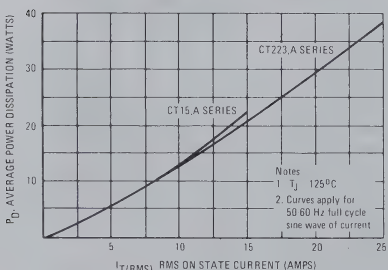


FIGURE 2 – ON-STATE POWER DISSIPATION



MAC15
MAC15A

MOTOROLA

BIDIRECTIONAL TRIODE THYRISTORS

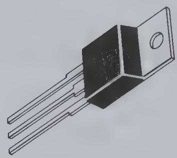
. . . designed primarily for full-wave ac control applications, such as solid-state relays, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

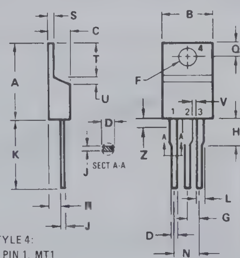
- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (MAC15)
  Four Modes (MAC15A)

TRIACS

15 AMPERES RMS
200–800 VOLTS

2.3





STYLE 4:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.60	15.75	0.575	0.620
B	9.65	10 29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0 025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2 67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0 562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0 210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221-02
TO-220 AB
All JEDEC dimensions and notes apply

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = -40 to 125°C)	V_{DRM}		Volts
MAC15-4, MAC15A-4		200	
MAC15-6, MAC15A-6		400	
MAC15-8, MAC15A-8		600	
MAC15-10, MAC15A-10		800	
Peak Gate Voltage	V_{GM}	10	Volts
On-State Current RMS Full Cycle Sine Wave 50 to 60 Hz (T_C = +90°C)	$I_{T(RMS)}$	15	Amp
Circuit Fusing	I^2t	93	A^2sec
Peak Surge Current (One Full Cycle, 60 Hz, T_C = +80°C) preceded and followed by rated current	I_{TSM}	150	Amp
Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs	P_{GM}	20	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current	I_{GM}	2.0	Amp
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and either polarity of MT2 to MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current V_D = Rated V_{DRM} @ T_J = 125°C, Gate Open	I_{DRM}	–	–	2	mA
Peak On-State Voltage I_{TM} = 21 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%	V_{TM}	–	1.3	1.6	Volts
Peak Gate Trigger Current V_D = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2 μs	I_{GTM}				mA
MT2 (+), G(+) – MAC15, MAC15A		–	–	50	
MT2 (+), G(–) – MAC15A		–	–	75	
MT2 (–), G(–) – MAC15, MAC15A		–	–	50	
MT2 (–), G(+) – MAC15A		–	–	75	
Peak Gate Trigger Voltage V_D = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2 μs	V_{GTM}				Volts
MT2 (+), G(+) – MAC15, MAC15A		–	0.9	2	
MT2 (+), G(–) – MAC15A		–	0.9	2.5	
MT2 (–), G(–) – MAC15, MAC15A		–	1.1	2	
MT2 (–), G(+) – MAC15A		–	1.4	2.5	
V_D = Rated V_{DRM}, R_L = 10k Ohms, T_J = 110°C					
MT2 (+), G(+); MT2 (–), G(–) – MAC15, MAC15A		0.2	–	–	
MT2 (+), G(–); MT2 (–), G(+) – MAC15A		0.2	–	–	
Holding Current (Either Direction) V_D = 12 Vdc, Gate Open I_T = 200 mA	I_H	–	6	40	mA
Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 17 A I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs	tgt	–	1.5	2	μs
Critical Rate of Rise of Commutation Voltage V_D = Rated V_{DRM}, I_{TM} = 21 A, Commutating di/dt = 8 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(c)	–	5	–	V/μs

2.3

FIGURE 1 – RMS CURRENT DERATING

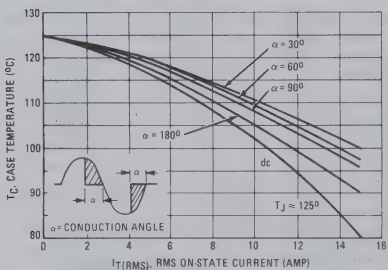


FIGURE 2 – ON-STATE POWER DISSIPATION

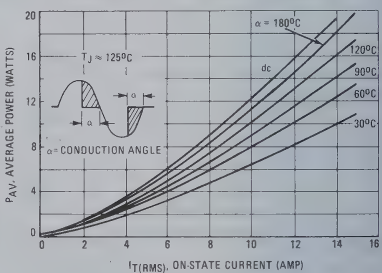


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

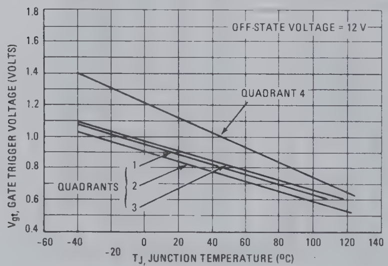


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

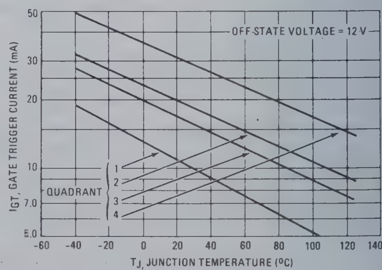


FIGURE 5 — ON-STATE CHARACTERISTICS

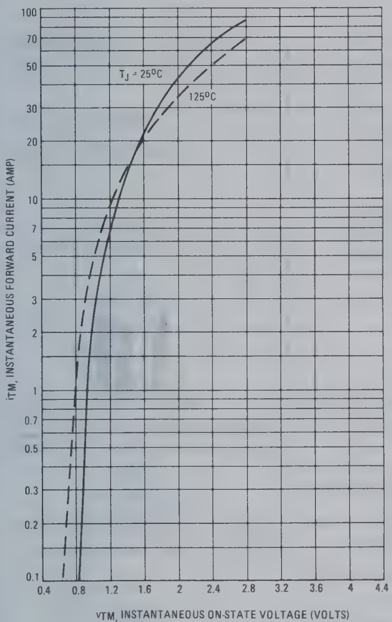


FIGURE 6 — TYPICAL HOLDING CURRENT

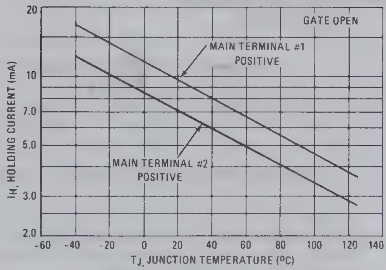


FIGURE 7 — MAXIMUM NON-REPETITIVE SURGE CURRENT

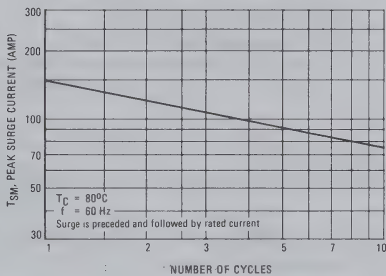
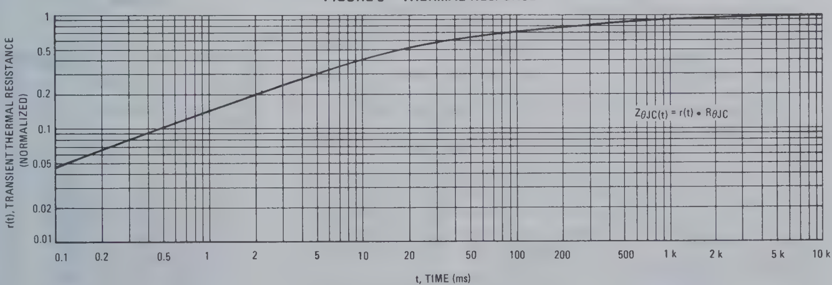


FIGURE 8 — THERMAL RESPONSE



MAC20/MAC20A

15 AMPERES RMS

MAC25/MAC25A

25 AMPERES RMS

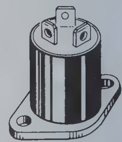
MAC50/MAC50A

40 AMPERES RMS

MOTOROLA

TRIACS

200–800 VOLTS



SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and consumer applications for full-wave control of ac loads such as appliance controls, power supplies, solid-state relays, heating controls, motor controls, welding equipment, and power switching systems.

- Electrically Isolated From Mounting Base
- Isolation Voltage of 2500 Volts RMS
- Quick Connect/Disconnect Terminals
- Glass-Passivated and Center Gate Geometry
- Gate Triggering Guaranteed in Three Modes (MAC20/25/50)
  Four Modes (MAC20A/25A/50A)

2.3

MAXIMUM RATINGS (T_J = 0 to +125°C unless otherwise noted)

Rating	Symbol	MAC series 20	25	50	Unit
Repetitive Peak Off-State Voltage 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}				Volts
MAC20/25/50-4, MAC20A/25A/50A-4		← 200 →			
MAC20/25/50-5, MAC20A/25A/50A-5		← 300 →			
MAC20/25/50-6, MAC20A/25A/50A-6		← 400 →			
MAC20/25/50-7, MAC20A/25A/50A-7		← 500 →			
MAC20/25/50-8, MAC20A/25A/50A-8		← 600 →			
MAC20/25/50-9, MAC20A/25A/50A-9		← 700 →			
MAC20/25/50-10, MAC20A/25A/50A-10		← 800 →			
RMS On-State Current	$I_{T(RMS)}$				Amps
(T_C = 100°C for MAC20/A)		15	–	–	
T_C = 90°C for MAC25/A)		–	25	–	
(T_C = 70°C for MAC50/A)		–	–	40	
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	150	250	300	Amps
Circuit Fusing (t = 1 to 8.3 ms)	I^2t	90	260	375	A^2s
Average Gate Power	$P_{G(AV)}$	0.5	0.5	0.75	Watts
Peak Gate Current (10 μs)	I_{GM}	2	2	4	Amps
Operating Junction Temperature Range	T_J	0 to +125			°C
Storage Temperature Range	T_{stg}	-40 to +125			°C

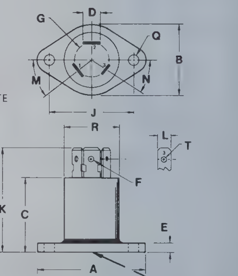
THERMAL CHARACTERISTICS

Characteristic	Symbol	Maximum Value			Unit
Thermal Resistance, Junction to Case (DC)	$R_{\theta JC}$	1.6	1.5	1.4	°C/W
(Apparent)*		1.3	1.0	0.95	

*Defined as: $\dfrac{(125°C - T_C)}{P_{AV}}$ for a 60 Hz full sine wave.

*Gate terminal thickness of .032″ is available. Designate a device with .032″ terminals by adding a T after the device type. For example, MAC20A4T.

STYLE 2:
1. MT1
2. MT2
3. GATE



NOTE:
1. DIMENSIONS D AND F APPLY TO TERM 1 AND 2.
2. MT1 AND MT2 THICKNESSES ARE A NOMINAL 0.032″. GATE TERMINAL THICKNESS IS A NOMINAL 0.020″.*

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	26.67	–	1.050
C	–	27.30	–	1.075
D	6.22	6.48	0.245	0.255
E	3.02	3.33	0.119	0.131
F	–	1.78	–	0.070
G	12.19	12.70	0.480	0.500
J	29.90	30.40	1.177	1.197
K	35.56	37.08	1.400	1.460
L	4.57	4.95	0.180	0.195
M	35°	40°	35°	40°
N	30°	35°	30°	35°
Q	3.81	4.09	0.150	0.161
R	19.81	22.35	0.780	0.880
T	–	1.52	–	0.060

CASE 326-01

ELECTRICAL CHARACTERISTICS
(All voltage polarity reference to MT1; applies to either polarity of MT2 to MT1; T_C = 25°C unless otherwise noted)

Characteristic		Symbol	MAC20/20A			MAC25/25A			MAC50/50A			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Peak Blocking Current V_D = Rated V_{DRM}, Gate Open	T_C = 125°C	I_{DRM}	—	—	2	—	—	2	—	—	2	mA
	T_C = 25°C		—	—	0.1	—	—	0.1	—	—	0.1	
Peak On-State Voltage Pulse Width = 1 ms, Duty Cycle 2%		V_{TM}										Volts
I_{TM} = 21 A Peak	MAC20/20A		—	1.3	1.6	—	—	—	—	—	—	
I_{TM} = 35 A Peak	MAC25/25A		—	—	—	—	1.4	1.7	—	—	—	
I_{TM} = 56 A Peak	MAC50/50A		—	—	—	—	—	—	—	1.65	1.75	
Peak Gate Trigger Current V_D = 12 Vdc, R_L = 50 Ohms, Pulse Width = 2 μs		I_{GTM}										mA
MT2 (+), G (+); MT2 (−), G (−); MT2 (+), G (−)			—	15	50	—	20	70	—	20	70	
MT2 (−), G (+)	A Suffix Only		—	30	75	—	35	100	—	35	100	
Peak Gate Trigger Voltage V_D = 12 Vdc, R_L = 50 Ohms, Pulse Width = 2 μs		V_{GTM}										Volts
MT2 (+), G (+); MT2 (−), G (−); MT2 (+), G (−)			—	0.9	2	—	1.1	2	—	1.1	2	
MT2 (−), G (+)	A Suffix Only		—	1.4	2.5	—	1.3	2.5	—	1.3	2.5	
V_D = Rated V_{DRM}, R_L = 10 kΩ, T_C = 125°C			0.2	—	—	0.2	—	—	0.2	—	—	
Holding Current V_D = 12 Vdc, Gate Open, R_L = 40 Ohms		I_H	—	6	40	—	10	75	—	10	75	mA
Turn-On Time V_D = Rated V_{DRM},		tgt										μs
I_{TM} = 21 A, I_G = 120 mA	MAC20/20A		—	1.5	—	—	—	—	—	—	—	
I_{TM} = 35 A, I_G = 200 mA	MAC25/25A		—	—	—	—	1.5	—	—	—	—	
I_{TM} = 56 A, I_G = 200 mA	MAC50/50A		—	—	—	—	—	—	—	1.5	—	
Critical Rate-of-Rise of Commutation Voltage		dv/dt(c)										V/μs
V_D = Rated V_{DRM}, I_{TM} = 21 A, Commutating di/dt = 8 A/ms, T_C = 100°C	MAC20/20A		5	30	—	—	—	—	—	—	—	
V_D = Rated V_{DRM}, I_{TM} = 35 A, Commutating di/dt = 16 A/ms, T_C = 90°C	MAC25/25A		—	—	—	5	30	—	—	—	—	
V_D = Rated V_{DRM}, I_{TM} = 56 A, Commutating di/dt = 22 A/ms, T_C = 70°C	MAC50/50A		—	—	—	—	—	—	5	30	—	
Critical Rate-of-Rise of Off-State Voltage (Exponential Rise) V_D = Rated V_{DRM}, Gate Open, T_C = 125°C		dv/dt	—	100	—	—	100	—	—	75	—	V/μs

2.3

FIGURE 1 — CURRENT DERATING

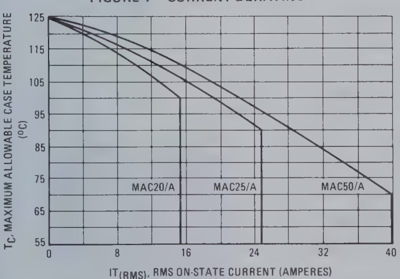
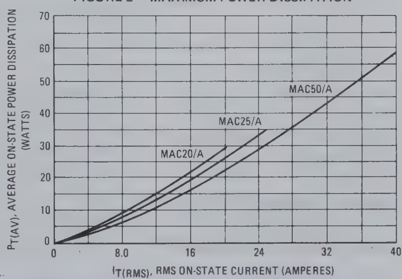


FIGURE 2 — MAXIMUM POWER DISSIPATION

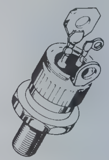


MAC80-6, MAC80-8
MAC81-6, MAC81-8

MOTOROLA

TRIACS (THYRISTORS)

30 AND 40 AMPERES RMS
400 AND 600 VOLTS



SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for soft starting input capacitors on switching power supplies. See Motorola SWITCHMODE brochure for all line operated power supply devices.

- Photo Glass Passivated Junctions
- Isolated Stud for Ease of Assembly
- Gate Triggering Guaranteed In All 4 Quadrants
- Allows Longer Hold Up Time Design for Low Line Conditions

2.3

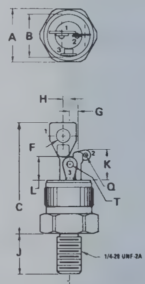
MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Repetitive Peak Off-State Voltage (1)		V_{DROM}		Volts
(T_J = –50 to +110°C) Gate Open	MAC80-6		400	
	MAC80-8		600	
(T_J = –50 to +110°C) Gate Open	MAC81-6		400	
	MAC81-8		600	
On-State Current RMS (Conduction Angle = 360°C)		$I_{T(RMS)}$		Amps
T_C = +65°C	MAC80-6, 8		40	
T_C = +55°C	MAC81-6, 8		30	
Peak Surge Current (One Full Cycle, 60 Hz)		I_{TSM}	300	Amps
Fusing Current (T_J = –40 to +100°C, t = 1.25 to 10 ms)		I^2t	450	A^2s
Peak Gate Power (Pulse Width = 1.0 μs)		P_{GM}	40	Watts
Average Gate Power		$P_{G(AV)}$	0.75	Watts
Peak Gate Current		I_{GM}	2	Amps
Operating Junction Temperature Range		T_J	–65 to +110	°C
Storage Temperature Range		T_{stg}	–65 to +150	°C
Stud Torque		—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.9	°C/W

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.



STYLE 2:
1. MT1
2. GATE
3. MT2

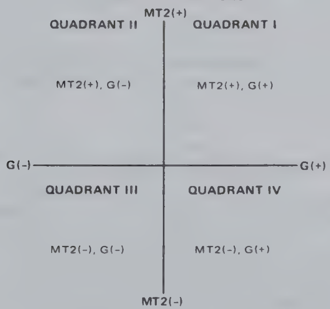
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C		32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

ISOLATED STUD
CASE 311-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Off-State Current (Either Direction) (Rated V_{DROM} @ T_J = 110°C, Gate Open)		I_{DROM}	—	—	4	mA
Maximum On-State Voltage (Either Direction) (I_T = 100 A Peak)	MAC80-6, 8 MAC81-6, 8	V_{TM}	— —	1.8 2.1	2.5 2.5	Volts
Gate Trigger Current, Continuous dc (1) (V_D = 12 Vdc, R_L = 30 Ohms) $V_{MT2\ (+)}$, $V_{G(+)}$ $V_{MT2\ (+)}$, $V_{G(-)}$ $V_{MT2\ (-)}$, $V_{G(-)}$ $V_{MT2\ (-)}$, $V_{G(+)}$		I_{GT}	 — — — —	 15 30 20 40	 50 80 50 80	mA
Gate Trigger Voltage, Continuous dc (V_D = 12 Vdc, R_L = 30 Ohms) (V_D = Rated V_{DROM}, R_L = 125 Ohms, T_C = 100°C)		V_{GT}	 — 0.2	 1.35 —	 2.5 —	Volts
Holding Current (V_D = 12 Vdc, Gate Open Initiating Current = 150 mA)		I_H	—	—	60	mA
Gate Controlled Turn-On Time (Rated V_{DROM}, I_T = 45 A, I_{GT} = 200 mA, Rise Time = 0.1 μs)		t_{gt}	—	1.7	3.0	μs
Critical Rate of Rise of Commutation Voltage, On-State Conditions: (di/dt = 16 A/ms, Gate Unenergized, V_D = Rated V_{DROM}, $I_{T(RMS)}$ = 30 A, T_C = 65°C)		dv/dt(C)	3.0	20	—	V/μs

QUADRANT DEFINITIONS



MAC97, A, B
Series

MOTOROLA

SILICON BIDIRECTIONAL TRIODE THYRISTORS

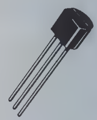
. . . designed for use in solid state relays, MPU interface, TTL logic and any other light industrial or consumer application. Supplied in an inexpensive TO-92 package which is readily adaptable for use in automatic insertion equipment.

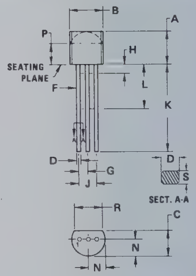
- One-Piece, Injection-Molded Unibloc Package
- Sensitive Gate Triggering in Four Trigger Modes for all possible Combinations of Trigger Sources, and Especially Suitable for Circuits that Source Gate Drives.
- All Diffused and Glassivated Junctions for Maximum Uniformity of Parameters and Reliability
- Available in TO-5 or TO-18 Leadforms

2.3

TRIACS

0.6 AMPERE RMS
30-600 VOLTS





STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	
N	2.03	2.67	0.080	0.105
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
(TO-226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (T_J = –40 to +110°C) Note 1 ½ Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
MAC 97 or MAC 97A or MAC 97B 1		30	
2		60	
3		100	
4		200	
5		300	
6		400	
7		500	
8		600	
On-State RMS Current Full Cycle Sine Wave 50 to 60 Hz, (T_C = +50°C)	$I_{T(RMS)}$	0.6	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = 110°C	I_{TSM}	8.0	Amp
Circuit Fusing Considerations (T_J = –40 to +110°C, t = 8.3 ms)	I^2t	0.26	A^2s
Peak Gate Voltage ($t \leq 2.0\ \mu s$)	V_{GM}	5.0	Volts
Peak Gate Power ($t \leq 2.0\ \mu s$)	P_{GM}	5.0	Watts
Average Gate Power(T_C = 80°C, $t \leq 8.3$ ms)	$P_{G(AV)}$	0.1	Watt
Peak Gate Current ($t \leq 2.0\ \mu s$)	I_{GM}	1.0	Amp
Operating Junction Temperature Range	T_J	-40 to +110	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Note 1) V_D = Rated V_{DRM} @ $T_J = 110^oC$	I_{DRM}	–	–	0.1	mA
Peak On-State Voltage (Either Direction) I_{TM} = 0.85 A Peak; Pulse Width ⩽ 2.0 ms, Duty Cycle ⩽ 2.0%	V_{TM}	–	–	1.9	Volts
Gate Trigger Current, Continuous dc V_D = 12 Vdc, R_L = 100 Ohms	I_{GT}	See Table 1			mA
Gate Trigger Voltage, Continuous dc V_D = 12 Vdc, R_L = 100 Ohms	V_{GT}				Volts
MT2(+), G(+) All Types		–	–	2.0	
MT2(+), G(–) All Types		–	–	2.0	
MT2(–), G(–) All Types		–	–	2.0	
MT2(–), G(+) All Types		–	–	2.5	
V_D = Rated V_{DRM}, R_L = 10 k ohms, $T_J = 110^oC$ MT2(+), G(+); MT2(–), G(–); MT2(+), G(–) All Types		0.1	–	–	
MT2(–), G(+) All Types		0.1	–	–	
Holding Current V_D = 12 Vdc, I_{TM} = 200 mA, Gate Open	I_H	–	–	10	mA
Gate Controlled Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 1.0 A pk, I_G = 25 mA	tgt	–	2.0	–	μs
Critical Rate of Rise of Commutation Voltage V_D = Rated V_{DRM}, I_{TM} = 0.84 μA pk Commutating di/dt = 0.32 A/ms, Gate Unenergized, $T_C = 50°C$	dv/dt(C)	–	5.0	–	V/μs
Critical Rate of Rise of Off-State Voltage V_D = Rated V_{DRM} Exponential Waveform, $T_C = 110^oC$	dv/dt	–	25	–	V/μs

NOTE:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

QUADRANT DEFINITIONS

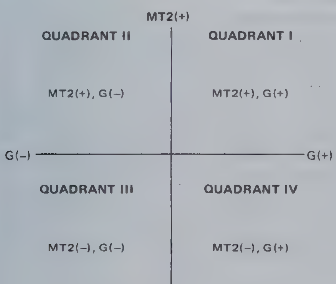


TABLE 1 — MAXIMUM GATE TRIGGER CURRENTS
(V_D = 12 V, R_L = 100 Ω)

Quadrant and Polarity	MAC Series			Unit
	97	97A	97B	
I MT2(+), G(+)	10	5.0	3.0	mA
II MT2(+), G(–)	10	5.0	3.0	mA
III MT2(–), G(–)	10	5.0	3.0	mA
IV MT2(–), G(+)	10	7.0	5.0	mA

2.3

FIGURE 1 — RMS CURRENT DERATING
(Reference: Case Temperature)

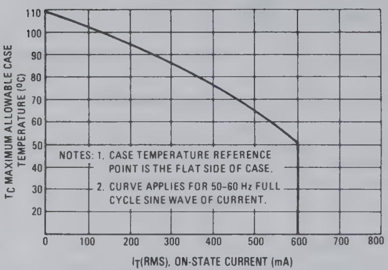


FIGURE 2 — ON-STATE CHARACTERISTICS

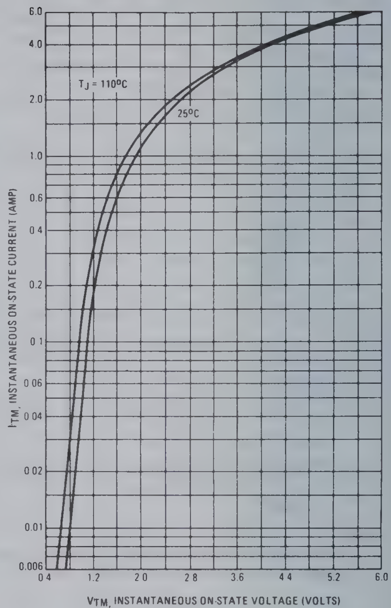


FIGURE 3 — RMS CURRENT DERATING
(Reference: Ambient Temperature)

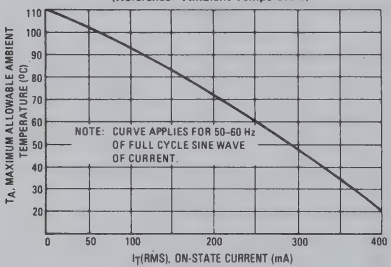


FIGURE 4 — ON-STATE POWER DISSIPATION

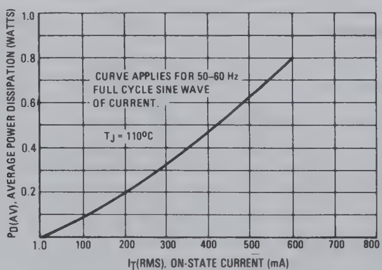


FIGURE 5 — NORMALIZED GATE TRIGGER CURRENT

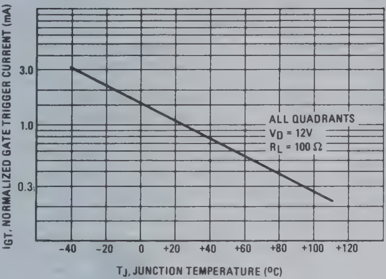


FIGURE 6 — NORMALIZED GATE TRIGGER VOLTAGE

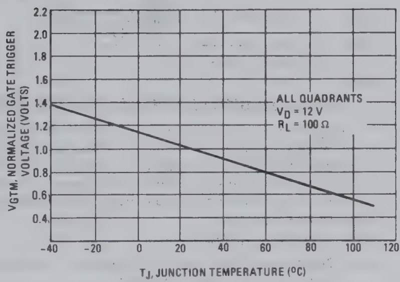


FIGURE 7 — NORMALIZED HOLD CURRENT

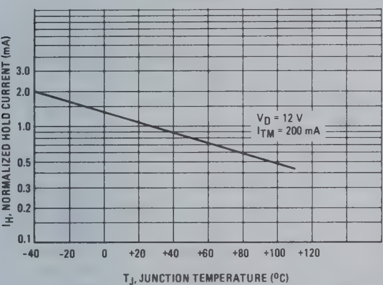


FIGURE 8 — MAXIMUM ALLOWABLE SURGE CURRENT

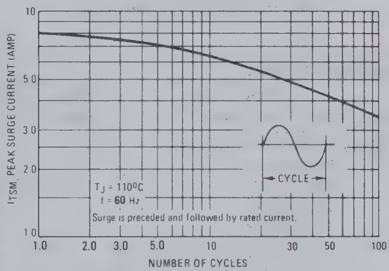
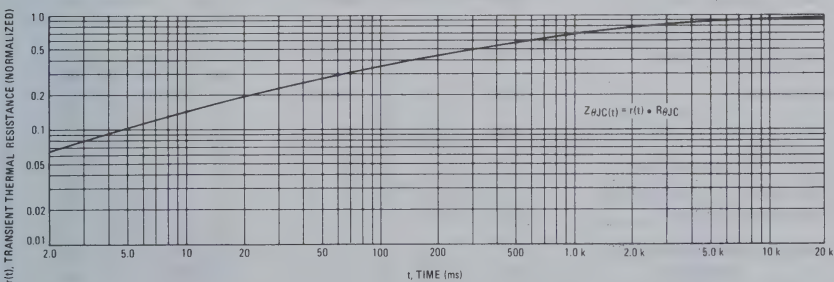


FIGURE 9 — THERMAL RESPONSE

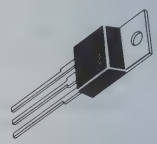


MAC210, A
Series

MOTOROLA

TRIACS
(THYRISTORS)

10 AMPERES RMS
200-800 VOLTS



SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Three Modes (MAC210 Series) or Four Modes (MAC210A Series)

2.3

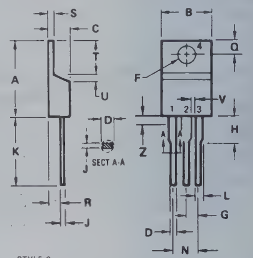
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (1) (T_J = −40 to +125°C) ½ Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
MAC210-4, A4		200	
MAC210-5, A5		300	
MAC210-6, A6		400	
MAC210-7, A7		500	
MAC210-8, A8		600	
MAC210-9, A9		700	
MAC210-10, A10		800	
On-State Current RMS (T_C = +70°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	10	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_C = +70°C) preceded and followed by Rated Current	I_{TSM}	100	Amp
Circuit Fusing Considerations (T_C = +70°C, t = 1.0 to 8.3 ms)	I^2t	35	A^2s
Peak Gate Power (T_C = +70°C, Pulse Width = 10 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +70°C, t = 8.3 ms)	$P_{G(AV)}$	0.35	Watt
Peak Gate Current (T_C = +70°C, Pulse Width = 10 μs)	I_{GM}	2.0	Amp
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.



STYLE 2.
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220 AB
All JEDEC dimensions and notes apply

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM}, Gate Open T_J = +125°C	I_{DRM}	—	—	0.1 0.5	mA
Peak On-State Voltage (Either Direction) I_{TM} = 14 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0%	V_{TM}	—	1.2	1.65	Volts
Gate Trigger Current, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs MT2(+), G(+) All Types MT2(+), G(−) All Types MT2(−), G(−) All Types MT2(−), G(+) MAC210A	I_{GT}	 — — — —	 12 12 20 35	 50 50 50 80	mA
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs MT2(+), G(+) All Types MT2(+), G(−) All Types MT2(−), G(−) All Types MT2(−), G(+) MAC210A Main Terminal Voltage = Rated V_{DRM}, R_L = 10k ohms, T_J = +125°C MT2(+), G(+); MT2(−), G(−); MT2(+), G(−) All Types MT2(−), G(+) MAC210A	V_{GT}	 — — — — 0.2 0.2	 0.9 0.9 1.1 1.4 — —	 2.5 2.5 2.5 3.5 — —	Volts
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 500 mA, T_C = +25°C	I_H	—	6.0	50	mA
Turn-On Time Rated V_{DRM}, I_{TM} = 14 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	t_{gt}	—	1.5	2.0	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 14 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = +70°C	$dv/dt_{(c)}$	5.0	—	—	V/μs
Critical Rate of Rise of Off-State Voltage (V_D = V_{DROM}, Exponential Voltage Rise, Gate Open, T_C = +70°C)	dv/dt	100	—	—	V/μs
Maximum Rate of Change of On-State Current (Rated V_{DROM}, I_{TM} = 14 A Peak, I_{GT} = 100 mA, T_C = +70°C, tr = 0.1 μs)	di/dt	—	—	150	A/μs

2.3

FIGURE 1 — CURRENT DERATING

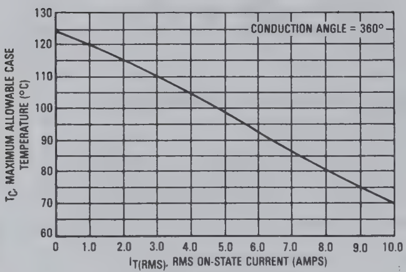


FIGURE 2 — POWER DISSIPATION

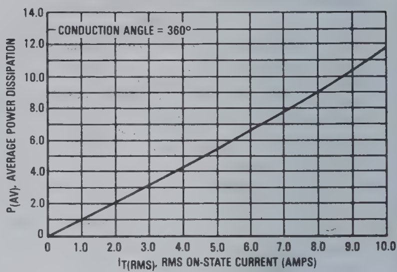


FIGURE 3 — MAXIMUM ON-STATE CHARACTERISTICS

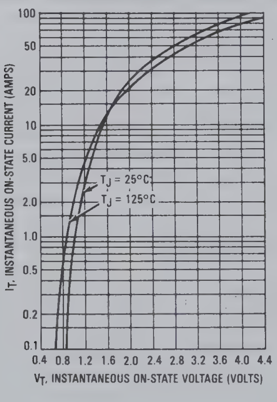


FIGURE 4 — MAXIMUM NON-REPETITIVE SURGE CURRENT

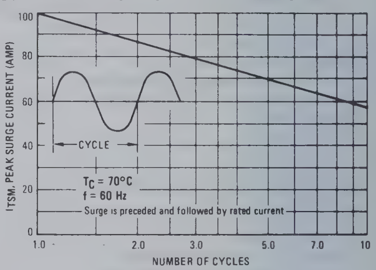


FIGURE 5 — TYPICAL GATE TRIGGER VOLTAGE

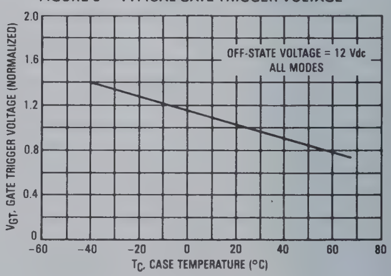


FIGURE 6 — TYPICAL GATE TRIGGER CURRENT

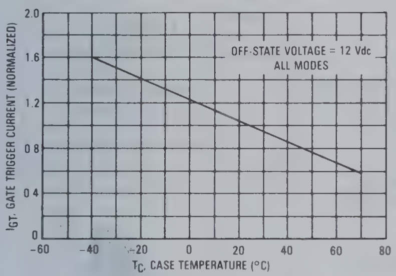
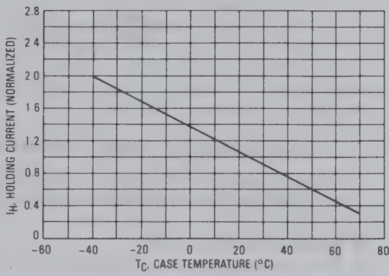
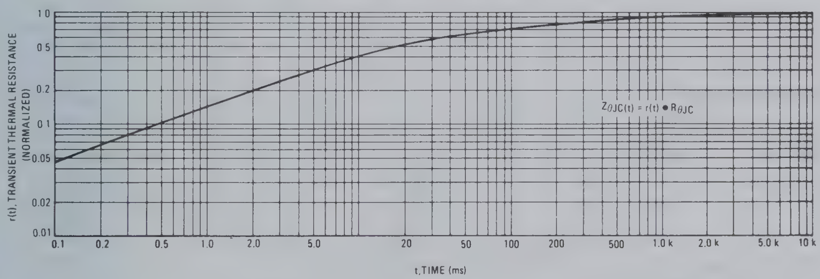


FIGURE 7 — TYPICAL HOLDING CURRENT



2.3

FIGURE 8 — THERMAL RESPONSE



MOTOROLA

TRIACS (THYRISTORS)

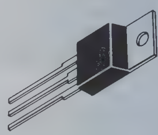
8 AMPERES RMS
200-800 VOLTS

SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

2.3

- Blocking Voltage to 800 Volts
- Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- TO-220 Construction Low Thermal Resistance, High Heat Dissipation and Durability



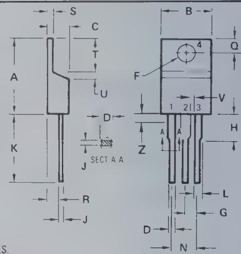
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (1) Gate Open MAC218, A - 4	V_{DRM}	200	Volts
- 5		300	
- 6		400	
- 7		500	
- 8		600	
- 9		700	
- 10		800	
On-State Current RMS (Conduction Angle = 360°C) (T_C = +80°C)	$I_{T(RMS)}$	8.0	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	100	Amp
Fusing Current (T_J = −40 to +100°C, t = 1 to 8.3 ms)	I^2t	35	A^2s
Peak Gate Power (T_C = +80°C, Pulse Width = 2.0 μs)	P_{GM}	16	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.35	Watt
Peak Gate Trigger Current (Pulse Width = 1.0 μs)	I_{GTM}	4.0	Amp
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.



NOTES.
1 DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3
3 DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4. DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
5 CONTROLLING DIMENSION INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0 380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0 025	0.035
F	3 61	3 73	0 142	0 147
G	2 41	2 67	0 095	0 105
H	2.79	3.93	0 110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0 562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0 055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 4
PIN 1 MAIN TERMINAL 1
2 MAIN TERMINAL 2
3 GATE
4 MAIN TERMINAL 2

CASE 221A-02
TO-220 AB

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Off-State Current (Either Direction) (Rated V_{DROM} @ T_J = 125°C, Gate Open)		I_{DROM}	—	—	2.0	mA
Peak On-State Voltage (Either Direction) (I_{TM} = 11.3 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle < 2%)		V_{TM}	—	1.7	2.0	Volts
(I_{TM} = 30 A Peak)	MAC218A		—	—	2.0	
Gate Trigger Current, Continuous dc (V_D = 12 Vdc, R_L = 12 Ω)		I_{GT}	—	—	—	mA
Trigger Mode						
MT2 (+), Gate (+)	MAC218		—	—	50	
MT2 (+), Gate (−)	MAC218		—	—	80	
MT2 (−), Gate (−)	MAC218		—	—	50	
MT2 (+), Gate (+)	MAC218A		—	—	25	
MT2 (+), Gate (−)	MAC218A		—	—	60	
MT2 (−), Gate (−)	MAC218A		—	—	25	
MT2 (−), Gate (+)	MAC218A		—	—	60	
Gate Trigger Voltage, Continuous dc		V_{GT}				Volts
(V_D = 12 Vdc, R_L = 100 Ohms)			—	1.5	2.5	
(V_D = V_{DROM}, R_L = 1000 Ohms, T_C = 125°C)			0.2	—	—	
Holding Current (Either Direction) (V_D = 24 Vdc, Gate Open, Initiating Current = 200 mA)		I_H	—	—	50	mA
	MAC218A		—	—	30	
Critical Rate of Rise of Commutating Off-State Voltage (Rated V_{DROM}, $I_{T(RMS)}$ = 6.0 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C)		$dv/dt_{(c)}$	5.0	—	—	V/μs
Critical Rate of Rise of Off-State Voltage (V_D = V_{DROM}, Exponential Voltage Rise, Gate Open, T_J = 125°C)		dv/dt	100	—	—	V/μs
Maximum Rate of Change of On-State Current (Rated V_{DROM}, I_{TM} = 11.3 A Peak, I_{GT} = 100 mA, T_J = 125°C)		di/dt	—	—	150	A/μs

2.3

FIGURE 1 — CURRENT DERATING

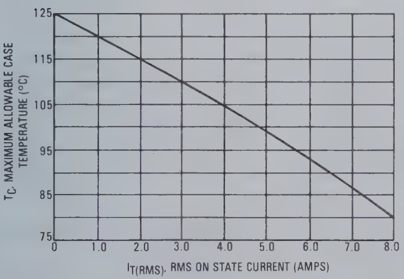


FIGURE 2 — POWER DISSIPATION

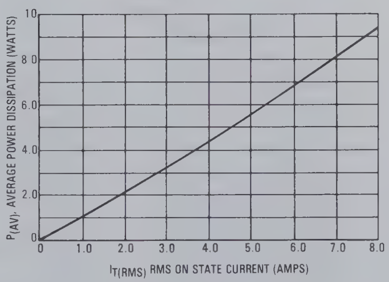


FIGURE 3 — NORMALIZED GATE TRIGGER CURRENT

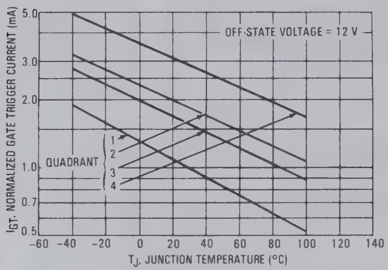
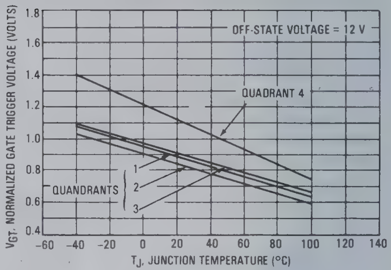
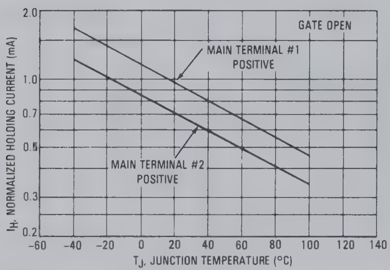


FIGURE 4 — NORMALIZED GATE TRIGGER VOLTAGE



2.3

FIGURE 5 — NORMALIZED HOLDING CURRENT

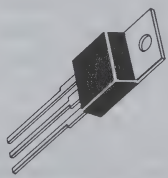


MAC223 series
MAC223A series

MOTOROLA

TRIACS
(THYRISTORS)

25 AMPERES RMS
100-800 VOLTS



SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications such as lighting systems, heater controls, motor controls and power supplies; or wherever full-wave silicon-gate-controlled devices are needed.

- Off-State Voltages to 800 Volts
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged Thermowatt Construction for Thermal Resistance and High Heat Dissipation
- Gate Triggering Guaranteed in Three modes (MAC223 series) or Four Modes (MAC223A) series

2.3

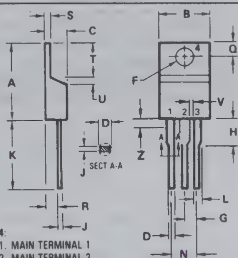
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = −40 to 125°C) Note 1 (1/2 Sine Wave 50 to 60 Hz, Gate Open)	V_{DRM}		Volts
MAC223, MAC223A -3		100	
-4		200	
-5		300	
-6		400	
-7		500	
-8		600	
-9		700	
-10		800	
On-State RMS Current (T_C = 80°C) (Full Cycle Sine Wave 50 to 60 Hz)	$I_{T(RMS)}$	25	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = 125°C)	I_{TSM}	250	Amp
Circuit Fusing (T_J = −40 to 125°C; t = 8.3 ms)	I^2t	260	A^2s
Peak Gate Current (t ⩽ 2.0 μs)	I_{GM}	2.0	Amp
Peak Gate Voltage (t ⩽ 2.0 μs)	V_{GM}	±10	Volts
Peak Gate Power (t ⩽ 2.0 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = 80°C, t ⩽ 8.3 ms)	$P_{G(AV)}$	0.5	Watts
Operating Junction Temperature Range	T_J	-40 to 125	°C
Storage Temperature Range	T_{stg}	-40 to 150	°C
Mounting Torque	—	8.0	in/lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

NOTE 1: Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.



STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	-	0.045	-
Z	-	2.03	-	0.080

CASE 221-A-02
TO-220AB

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Note 1) (V_D = Rated V_{DRM}.) T_J = 125°C / T_J = 25°C	I_{DRM}	—	—	2.0 / 0.020	mA
Peak On-State Voltage (I_{TM} = 35 A Peak, Pulse Width ⩽ 2 ms, Duty Cyle ⩽ 2%)	V_{TM}	—	1.4	1.85	Volts
Gate Trigger Current, Continuous dc (V_D = 12 V, R_L = 100 Ω)	I_{GT}				mA
MT2(+), G(+); MT2(−), G(−), MT2(+), G(−) All Types		—	20	50	
MT2(−), G(+) A Suffix Only		—	30	75	
Gate Trigger Voltage, Continuous dc (V_D = 12 V, R_L = 100 Ω)	V_{GT}				Volts
MT2(+), G(+); MT2(−), G(−), MT2(+), G(−) All Types		—	1.1	2.0	
MT2(−), G(+) A Suffix Only		—	1.3	2.5	
(V_D = Rated V_{DRM}, T_J = 125°C, R_L = 10 k) All Types, All Trigger Modes		0.2	0.4	—	
Holding Current (V_D = 12 V, I_{TM} = 200 mA, Gate Open)	I_H	—	10	50	mA
Gate Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 35 A Peak, I_G = 200 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 125°C)	dv/dt	—	40	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 35 A Peak, Commutating di/dt = 13.4 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5.0	—	V/μs

NOTE 1: Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

FIGURE 1 — RMS CURRENT DERATING

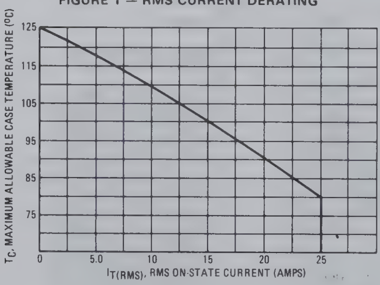


FIGURE 2 — ON-STATE POWER DISSIPATION

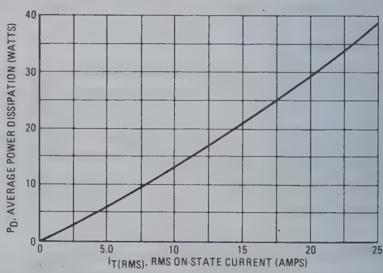


FIGURE 3 — GATE TRIGGER CURRENT

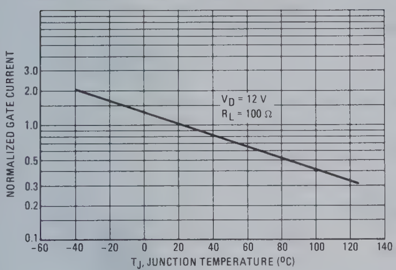
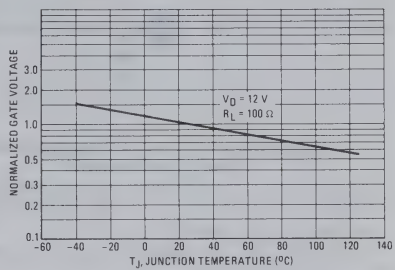


FIGURE 4 — GATE TRIGGER VOLTAGE



2.3

FIGURE 5 — HOLD CURRENT

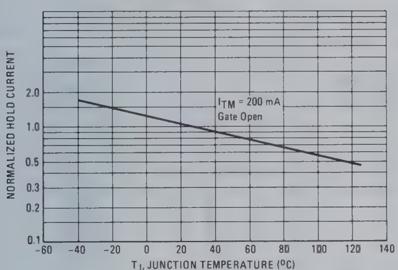
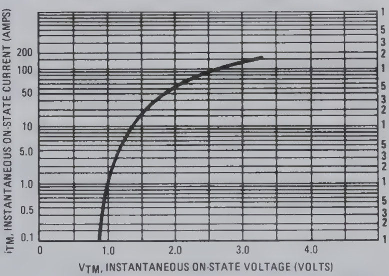


FIGURE 6 — ON-STATE CHARACTERISTICS

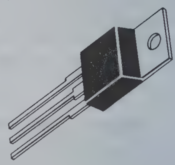


MAC224 series
MAC224A series

MOTOROLA

TRIACS
(THYRISTORS)

40 AMPERES RMS*
200-800 VOLTS



SILICON BIDIRECTIONAL 40 AMPERES RMS*
TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications such as lighting systems, heater controls, motor controls and power supplies.

- Blocking Voltage to 800 Volts
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Gate Triggering Guaranteed in Three Modes (MAC224 series) or Four Modes (MAC224A) series

2.3

MAXIMUM RATINGS

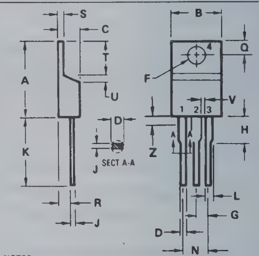
Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = -40 to 125°C) Note 1. (1/2 Sine Wave 50 to 60 Hz, Gate Open)	V_{DRM}		Volts
MAC224, MAC224A -4		200	
-5		300	
-6		400	
-7		500	
-8		600	
-9		700	
-10		800	
On-State RMS Current (T_C = 75°C) (Full Cycle Sine Wave 50 to 60 Hz)	$I_{T(RMS)}$	40*	Amp
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz, T_J = 125°C)	I_{TSM}	350	Amps
Circuit Fusing (T_J = -40 to 125°C, t = 8.3 ms)	I^2t	500	A^2s
Peak Gate Current ($t \leqslant 2.0\ \mu s$)	I_{GM}	±2.0	Amp
Peak Gate Voltage ($t \leqslant 2.0\ \mu s$)	V_{GM}	±10	Volts
Peak Gate Power ($t \leqslant 2.0\ \mu s$)	P_{GM}	20	Watts
Average Gate Power (T_C = 75°C, $t \leqslant 8.3$ ms)	$P_{G(AV)}$	0.5	Watts
Operating Junction Temperature Range	T_J	-40 to 125	°C
Storage Temperature Range	T_{stg}	-40 to 150	°C
Mounting Torque	—	8.0	lb/in

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

Note 1: Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

* This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat sinking when the device is to be used at high sustained currents. (See Figure 1 for maximum case temperatures.)



NOTES:
1. DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
5. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	-	0.045	-
Z	-	2.03	-	0.080

STYLE 4
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

CASE 221A-02
(TO-220AB)

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Note 1) (V_D = Rated V_{DRM}, T_J = 125°C)	I_{DRM}	—	—	2.0	mA
Peak On-State Voltage (I_{TM} = 56 A Peak, Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.4	1.85	Volts
Gate Trigger Current, Continuous dc (V_D = 12 V, R_L = 100 Ω)	I_{GT}				mA
MT2(+), G(+); MT2(+), G(−); MT2(+), G(−) All Types		—	25	50	
MT2(−), G(+) A Suffix Only		—	40	75	
Gate Trigger Voltage, Continuous dc (V_D = 12 V, R_L = 100 Ω)	V_{GT}				Volts
MT2(+), G(+); MT2(−), G(−); MT2(+), G(−) All Types		—	1.1	2.0	
MT2(−), G(+) A Suffix Only		—	1.3	2.5	
Gate Non-Trigger Voltage (V_D = Rated V_{DRM}, T_J = 125°C, R_L = 10 k) All Types, All Trigger Modes	V_{GD}	0.2	—	—	Volts
Holding Current (V_D = 12 Vdc, Gate Open)	I_H	—	30	75	mA
Gate-Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 56 A Peak, I_G = 200 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 125°C)	dv/dt	—	50	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 56 A Peak, Commutating di/dt = 13.4 A/ms, Gate Unenergized, T_C = 75°C)	dv/dt (c)	—	5.0	—	V/μs

Note 1: Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

2.3

FIGURE 1 — RMS CURRENT DERATING

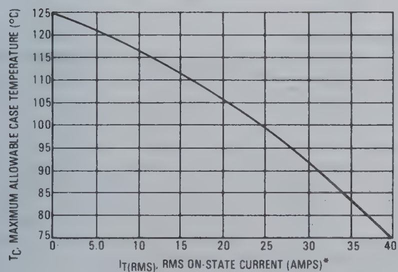
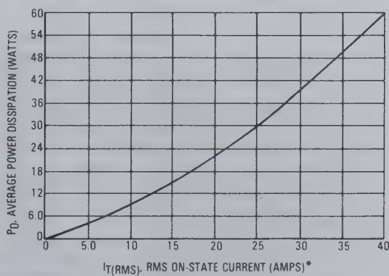


FIGURE 2 — ON-STATE POWER DISSIPATION



*This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat sinking when the device is to be used at high sustained currents.

FIGURE 3 — GATE TRIGGER CURRENT

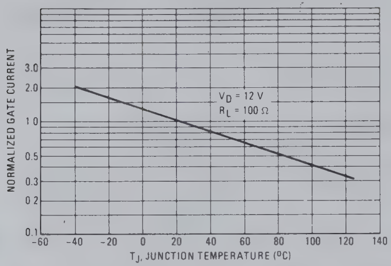
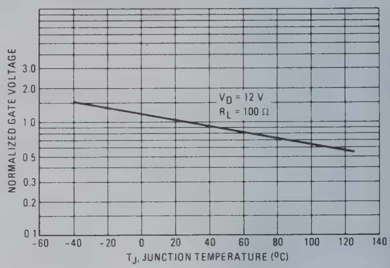


FIGURE 4 — GATE TRIGGER VOLTAGE



2.3

FIGURE 5 — HOLDING CURRENT

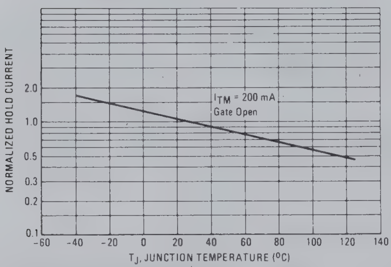


FIGURE 6 — ON-STATE CHARACTERISTICS

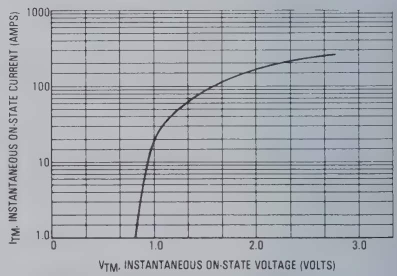
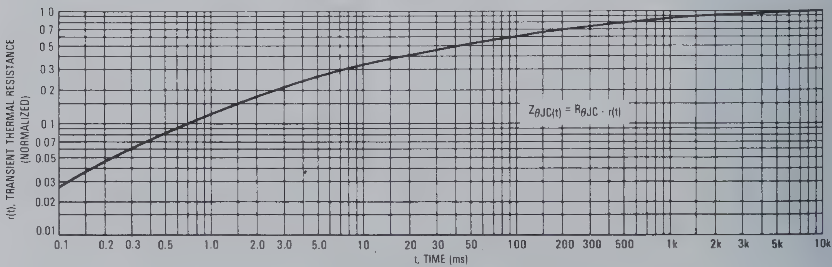


FIGURE 7 — THERMAL RESPONSE



MAC228-2 thru -10
MAC228A2 thru A10

MOTOROLA

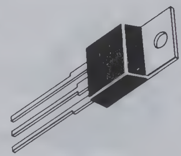
SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and consumer applications for full wave control of ac loads such as appliance controls, heater controls, motor controls, and other power switching applications.

- Sensitive Gate Triggering in Three Trigger Modes for AC Triggering or Sinking Current Sources (MAC228 series)
- Four Mode Triggering (10 mA) for Drive Circuits that Source Current (MAC228A series)
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance and High Heat Dissipation
- Center Gate Geometry for Uniform Current Spreading

TRIACS
(THYRISTORS)

8 AMPERES RMS
25-800 VOLTS



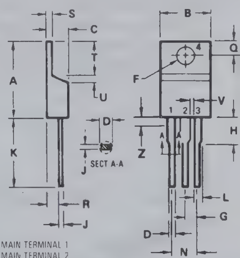
2.3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = −40 to 110°C) Note 1. 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
MAC228 -2, A2		50	
MAC228 -3, A3		100	
MAC228 -4, A4		200	
MAC228 -5, A5		300	
MAC228 -6, A6		400	
MAC228 -7, A7		500	
MAC228 -8, A8		600	
MAC228 -9, A9		700	
MAC228 -10, A10		800	
On-State RMS Current (T_C = 80°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	8.0	Amps
Peak Non-Repetitive Surge Current (One Full Cycle 60 Hz, T_J = 110°C)	I_{TSM}	80	Amps
Circuit Fusing (T_J = −40 to 110°C, t = 8.3 ms)	I^2t	40	A^2s
Peak Gate Current (t ≤ 2 μs)	I_{GM}	±2.0	Amps
Peak Gate Voltage (t ≤ 2 μs)	V_{GM}	±10	Volts
Peak Gate Power (t ≤ 2 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = 80°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.5	Watts
Operating Junction Temperature Range	T_J	−40 to 110	°C
Storage Temperature Range	T_{stg}	−40 to 150	°C
Mounting Torque		8.0	in-lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W



STYLE 4
PIN 1 MAIN TERMINAL 1
2 MAIN TERMINAL 2
3 GATE
4 MAIN TERMINAL 2

NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220 AB

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Note 1) (V_D = Rated V_{DRM}, T_J = 110°C)	I_{DRM}	—	—	2.0	mA
Peak On-State Voltage (I_{TM} = 11 A Peak, Pulse Width ≤ 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	1.5	Volts
Gate Trigger Current, Continuous dc (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(+), G(−); MT2(−), G(−) MAC228 series MT2(+), G(+); MT2(+), G(−); MT2(−), G(−); MT2(−), G(+) MAC228A series	I_{GT}	 — —	 — —	 5.0 10	mA
Gate Trigger Voltage, Continuous dc (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(+), G(−); MT2(−), G(−) MAC228 series MT2(+), G(+); MT2(+), G(−); MT2(−), G(−); MT2(−), G(+) MAC228A series (V_D = Rated V_{DRM}, T_C = 110°C, R_L = 10 k) MT2(+), G(+); MT2(+), G(−); MT2(−), G(−) All Types MT2(−), G(+) MAC228A series	V_{GT}	 — — 0.2 0.2	 — — — —	 2.2 2.5 — —	Volts
Holding Current (V_D = 12 Vdc, I_{TM} = 200 mA, Gate Open)	I_H	—	—	15	mA
Gate-Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 16 A Peak, I_G = 30 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 110°C)	dv/dt	—	25	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 11 A Peak, Commutating di/dt = 5.8 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt (c)	—	5.0	—	V/μs

Note 1: Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

FIGURE 1 — RMS CURRENT DERATING

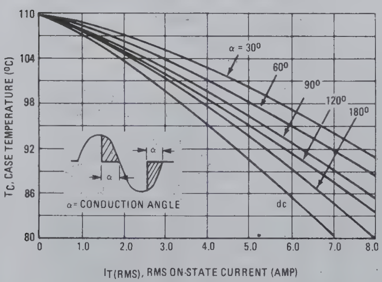
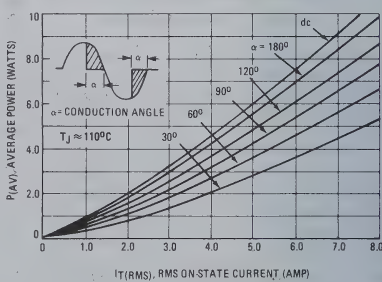


FIGURE 2 — ON-STATE POWER DISSIPATION



MOTOROLA

MAC515/MAC515A
15 AMPERES RMS
MAC525/MAC525A
25 AMPERES RMS

SILICON BIDIRECTIONAL TRIODE THYRISTORS

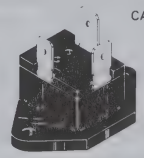
. . . designed for AC control applications requiring large numbers of power cycles and ease of connection. The overmold package is an existing TO-220 device with the leads bent up and fast-on connectors welded in place. The plastic body is molded over the TO-220 for TO-3 type mounting and UL requirements. The MAC515/515A is a 15-Amp device, and the MAC525/525A is a 25-Amp device for the triac series.

- Most Reliable UL Oriented Package
- Externally Isolated With Mica (part number B52600 F016)
- Cost Reduces All New Pressfit and Isolated Stud Designs
- Fast-On Connectors for Easy Assembly
- Terminals Notched for "Wire Wrap" or Solder Connection

TRIACS

200 – 800 VOLTS

CASE 342-01



2.3

MAXIMUM RATINGS

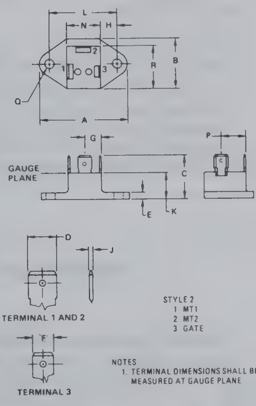
Ratings (Note 1)	Symbol	MAC Series 515	MAC Series 525	Units
Repetitive Peak Off-State Voltage (1/2 Sine Wave 50 to 60 Hz, Gate Open)	V_{DRM}			Volts
MAC515/525A-4		200		
-5		300		
-6		400		
-7		500		
-8		600		
-9		700		
-10		800		
RMS On-State Current (T_C = 95°C) (T_M = 80°C With Mica Insulator)	$I_{T(RMS)}$	15	25	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	150	250	Amps
Circuit Fusing (t = 8.3 ms)	I^2t	170	260	A^2s
Peak Gate Current (t ≤ 2.0 μs)	I_{GM}	2	2	Amps
Peak Gate Voltage (t ≤ 2.0 μs)	V_{GM}	± 10	± 10	Volts
Peak Gate Power (t ≤ 2.0 μs)	P_{GM}	20	20	Watts
Average Gate Power (T_C = 80°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.5	0.5	Watts
Operating Junction Temperature Range	T_J	−40 to +125		°C
Storage Temperature Range	T_{stg}	−40 to +150		°C
Mounting Torque (Note 2)	—	6		in.lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max 515	Max 525	Unit
Thermal Resistance, Junction To Case	$R_{\theta JC}$	2.0	1.0	°C/W

Note 1: Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltages such that the voltage applied exceeds the rated blocking voltage at room temperature (≈ 25°C).

Note 2: Insert greased external isolator between the plastic TO-3 type base and heat sink. Secure with two 6 x 32 screws, lock washers and nuts. Tighten to 6-inch pound torque maximum for best heat transfer, lowest mechanical stress, and highest reliability.



STYLE 2
1 MT1
2 MT2
3 GATE

NOTES
1. TERMINAL DIMENSIONS SHALL BE MEASURED AT GAUGE PLANE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.62	1.510	1.560
B	21.85	24.38	0.860	0.960
C	22.86	25.40	0.900	1.000
D	6.28	6.42	0.247	0.253
E	2.80	4.06	0.110	0.160
F	4.68	4.82	0.184	0.190
G	6.86	8.12	0.270	0.320
H	7.24	8.00	0.285	0.315
J	0.79	0.83	0.031	0.033
K	14.48	15.49	0.570	0.610
L	29.85	30.35	1.175	1.195
N	14.48	15.49	0.570	0.610
P	10.67	12.19	0.420	0.480
Q	3.81	4.19	0.150	0.165
R	17.78	19.30	0.700	0.760

CASE 342-01

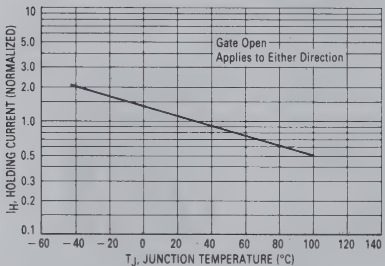
2.3

ELECTRICAL CHARACTERISTICS (All Voltage Polarity Reference to MT1; Applies to either Polarity of MT2 to MT1; T_C = 25°C unless Otherwise Noted.)

Characteristic	Symbol	MAC515/515A			MAC525/525A			Unit
		Min	Typ	Max	Min	Typ	Max	
Peak Blocking Current (V_D = Rated V_{DRM}, Gate Open) T_C = 125°C T_C = 25°C	I_{DRM}	— —	— —	2.0 0.1	— —	— —	2.0 0.1	mA
Peak On-State Voltage (Pulse Width = 1 ms, Duty Cycle 2%) I_{TM} = 21 A Peak I_{TM} = 35 A Peak	V_{TM}	— —	1.3 —	1.80 —	— —	— 1.4	— 1.75	V
Gate Trigger Current, Continuous dc (V_D = 12 Vdc, R_L = 100 Ohms) MT2(+), G(+); MT2(−), G(−); MT2(+), G(−) MT2(−), G(+) A Suffix Only	I_{GT}	— —	15 30	50 75	— —	20 35	50 75	mA
Gate Trigger Voltage, Continuous dc (V_D = 12 Vdc, R_L = 100 Ohms, Pulse Width = 10 μs) MT2(+), G(+); MT2(−), G(−); MT2(+), G(−) MT2(−), G(+) A Suffix Only (V_D = Rated V_{DRM}, R_L = 10 KΩ, T_C = 125°C)	V_{GT}	 — 0.2	0.9 1.4 —	2.0 2.5 —	— — 0.2	1.1 1.3 —	2.0 2.5 —	V
Holding Current (V_D = 12 Vdc, Gate Open, R_L = 40 Ohms)	I_H	—	6.0	40	—	10	50	mA
Turn-On Time (V_D = Rated V_{DRM} I_{TM} = 21 A, I_G = 120 mA I_{TM} = 35 A, I_G = 200 mA	t_{gt}	— —	1.5 —	— —	— —	 1.5	— —	μs
Critical Rate-Of-Rise Of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 21 A Commutating di/dt = 8 A/ms, T_C = 100°C) (V_D = Rated V_{DRM}, I_{TM} = 35 A Commutating di/dt = 16 A/ms, T_C = 90°C)	dv/dt(c)	— —	5.0 —	— —	— —	— 5.0	— —	V/μs
Critical Rate-Of-Rise Of Off-State Voltage, Exponential Rise (V_D = Rated V_{DRM} Gate Open, T_C = 125°C)	dv/dt	—	50	—	—	50	—	V/μs

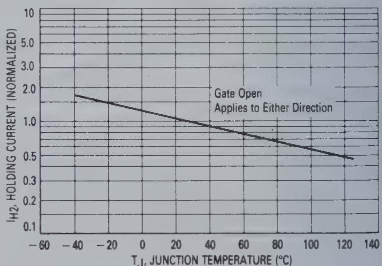
MAC515/515A

FIGURE 1 — TYPICAL HOLDING CURRENT



MAC525/525A

FIGURE 2 — TYPICAL HOLDING CURRENT



MAC515/515A

FIGURE 3 — MAXIMUM ON-STATE CHARACTERISTICS

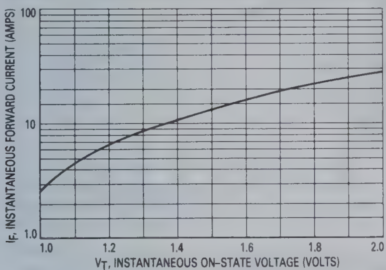


FIGURE 5 — RMS CURRENT DERATING

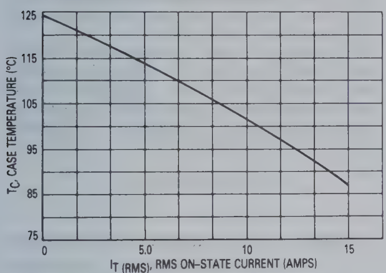
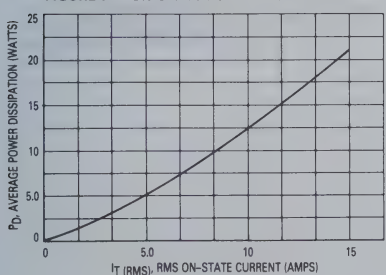


FIGURE 7 — ON-STATE POWER DISSIPATION



MAC525/525A

FIGURE 4 — MAXIMUM ON-STATE CHARACTERISTICS

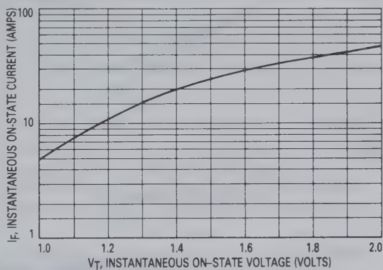


FIGURE 6 — RMS CURRENT DERATING

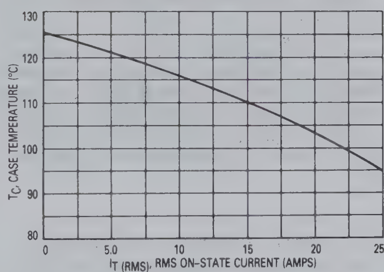
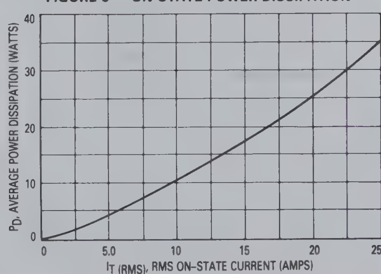


FIGURE 8 — ON-STATE POWER DISSIPATION



2.3

FIGURE 9 — TYPICAL GATE TRIGGER CURRENT

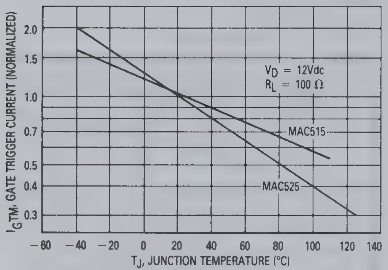
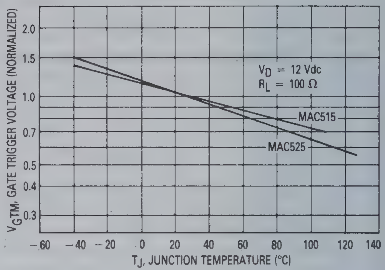


FIGURE 10 — TYPICAL GATE TRIGGER VOLTAGE



MECHANICAL CONSTRUCTION OF POWER THYRISTOR PACKAGES FOR SWITCHING APPLICATIONS

Thyristors replace relays for reasons of maintenance, space, and cost effectiveness. It is imperative that the mechanical construction of thyristors be consistent with these goals. The overmold package is the state-of-the-art realization of the above, backed by an instant performance record from years of development in the TO-220 package.

Motorola has power-cycled TO-220 devices 110,000 times at 15 amperes with only one failure (see report R 79-8A) and power-cycled the overmold 40,000 times, successfully. Tests for temperature cycle, temperature storage, thermal shock, moisture resistance, and vibration, also passed.

The internal construction of the overmold package (Figure 11) has only one layer of 95/5 solder, and inherent chip-to-heat spreader, interface. Internally isolated devices must have several layers of solder, including soft solder around the isolator. Typically, the solder layers will fail, as the number of power cycles are increased.

FIGURE 11 — EXTERNALLY ISOLATED DEVICE

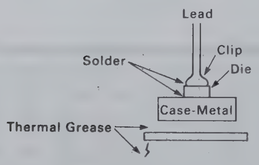
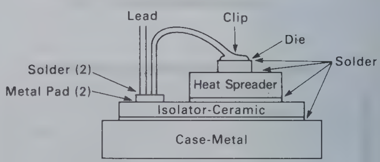
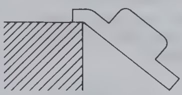


FIGURE 12 — TYPICAL INTERNALLY ISOLATED DEVICE



The overmold package is stronger than aluminum and equal to the steel TO-3 package in bending moment (Figure 13). The plastic flange eliminates isolation hardware and prevents screw-burr shorts through the isolator. The phenolic plastic meets UL flammability requirements and is designed for UL voltage spacing requirements.

FIGURE 13 — BENDING MOMENT



2.3

Comparison of the current handling capability of internally isolated devices can be done on the dashed line of Figures 14 and 15. The equivalent position (dashed line) is the same as the heat sink temperature (T_C) of the internally isolated device.

FIGURE 14 — ISOLATED RMS CURRENT DERATING

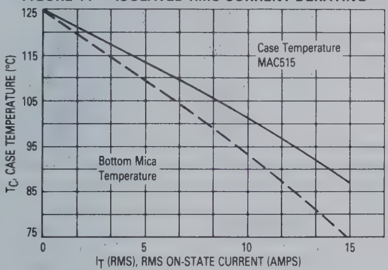
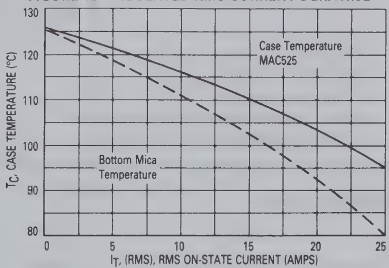


FIGURE 15 — ISOLATED RMS CURRENT DERATING



For externally isolated package:

R_θTotal = R_θChip + R_θSolder + R_θHeader + R_θGrease + R_θIsolator + R_θGrease + R_θHeatsink

For internally isolated package:

R_θTotal = R_θChip + R_θSolder (1) + R_θHeat Spreader + R_θSolder (2) + R_θIsolator + R_θSolder (3) + R_θHeader + R_θGrease + R_θHeatsink

The same power and the same heatsink will give higher T_C externally isolated than T_C internally isolated because of their relative position in the thermal equation. Both parts will have the same T_J.

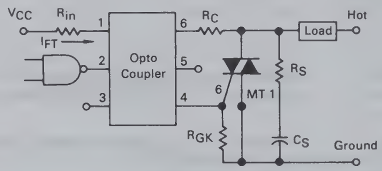
MAC3010 MAC3020
MAC3030 MAC3040
series

MOTOROLA

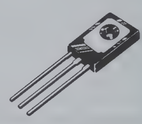
TRIACS
(THYRISTORS)

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed for full-wave ac power control applications, and specifically designed to be used in conjunction with MOC30XX opto couplers in circuits similar to that shown below.



- Input to Output Isolation to 7.5 kV
- Zero Crossover Firing
- Low Drive Currents
- Load Can Be in Either Hot or Ground Line
- Load Current Controlled Up to 40 A



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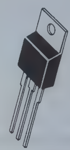

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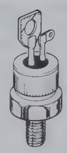


-40

-401

2.3

MAXIMUM RATINGS

Rating	Symbol	Current Ratings						Unit
		−4	−8	−15	−25	−40	−401	
On-State RMS Current (see Figure 1) (Full Cycle Sine Wave 50 to 60 Hz)	$I_{T(RMS)}$	4.0	8.0	15	25	40	40	Amps
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz, T_J = 110°C)	I_{TSM}	30	80	150	250	300	300	Amps
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 8.3 ms)	I^2t	3.6	26	90	260	370	370	A^2sec
Peak Gate Voltage (t ≤ 2.0 μs)	V_{GM}	±5	±10	±10	±10	±10	±10	Volts
Peak Gate Power (t ≤ 2.0 μs)	P_{GM}	10	20	20	20	20	20	Watts
Average Gate Power (T_C = 80°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.5	0.5	0.5	0.5	0.5	0.5	Watts
Peak Gate Current (t ≤ 2.0 μs)	I_{GM}	11	12	12	12	12	12	Amps
Operating Junction Temperature Range	T_J	*	-40 to +125			*		°C
Storage Temperature Range	T_{stg}	-40 to +150						°C
Mounting Torque	—	6.0	8.0	8.0	8.0	30	30	in. lb.
MAC3010/MAC3030 MAC3020/MAC3040	V_{DRM}	250 400	250 400	250 400	250 400	250 400	250 400	Volts

THERMAL CHARACTERISTICS

Characteristic	Symbol	−4	−8	−15	−25	−40	−401	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	2.2	2.0	1.2	0.9	0.9	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	60	60	60	1.0	1.0	°C/W

*T_J −40° to + 100°C.

—4 CURRENT RATING

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Note 1) (V_D = T_J = 110°C)	I_{DRM}	—	—	2.0	mA
Peak On-State Voltage (Either Direction) (I_{TM} = 6 A Peak; Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2.0%)	V_{TM}	—	—	2.0	Volts
Gate Trigger Current, Continuous dc (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(–), G(–)	I_{GT}	—	—	30	mA
Gate Trigger Voltage, Continuous dc (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(–), G(–)	V_{GT}	—	—	2.0	Volts
(R_L = 10 k Ω, T_J = 110°C) MT2(+), G(+); MT1(–), G(–)		0.2	—	—	
Holding Current (V_D = 12 V, I_{TM} = 200 mA, Gate Open)	I_H	—	—	40	mA
Gate Controlled Turn-On Time (I_{TM} = 6 A pk, I_G = 100 mA)	tgt	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage (I_{TM} = 6 A pk, Commutating di/dt = 3.1 A/ms, Gate Unenergized, T_C = 85°C)	dv/dt(C)	—	5.0	—	V/μs
Critical Rate of Rise of Off-State Voltage (Exponential Waveform, T_C = 110°C)	dv/dt	—	20	—	V/μs

Note 1: Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

2.3

FIGURE 1 — CURRENT DERATING AND POWER DISSIPATION REFERENCE: CASE TEMPERATURE

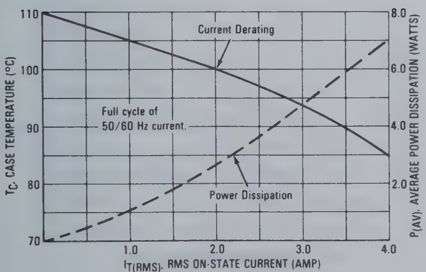
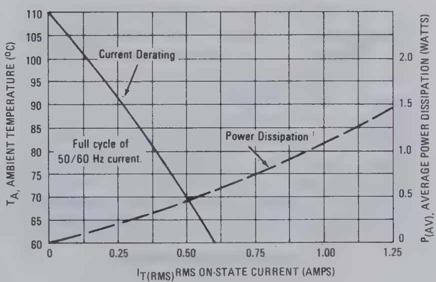


FIGURE 1A — POWER DISSIPATION REFERENCE: AMBIENT TEMPERATURE



—8, —15, —25 CURRENT RATINGS

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Note 1) (T_J = 125°C)	I_{DRM}	—	—	2.0	mA
Peak On-State Voltage (ITM = $\sqrt{2}$ $I_{T(RMS)}$ A Peak; Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2.0%) MAC3030-8 MAC3030-15 MAC3030-25	V_{TM}	 — — —	 — — —	 1.6 1.6 1.85	Volts
Gate Trigger Current, Continuous dc (V_D = 12 V, R_L = 100 Ohms) MT2(+), G(+); MT2(−), G(−) All Types	I_{GT}	—	—	40	mA
Gate Trigger Voltage, Continuous dc (V_D = 12 V, R_L = 100 Ohms) MT2(+), G(+); MT2(−), G(−) All Types (T_J = 125°C, R_L = 10 k Ohms) MT2(+), G(+); MT2(−), G(−) All Types	V_{GT}	 — 0.2	 — —	 2.0 —	Volts
Holding Current (V_D = 12 V, I_{TM} = 200 mA, Gate Open)	I_H	—	—	40	mA
Gate Controlled Turn-On Time (I_{TM} = :2 $I_{T(RMS)}$ A Peak, I_G = 100 mA)	tgt	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage (I_{TM} = :2 $I_{T(RMS)}$ A Peak, Commutating di/dt = 0.52 $I_{T(RMS)}$ A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(C)	—	5.0	—	V/μs
Critical Rate of Rise of Off-State Voltage (Exponential Waveform, T_C = 125°C)	dv/dt	40	—	—	V/μs

Note 1: Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

FIGURE 2 — RMS CURRENT DERATING

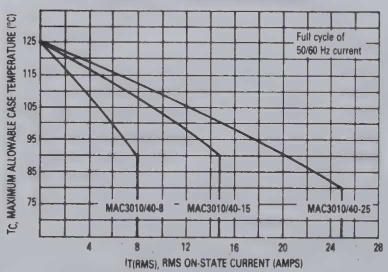
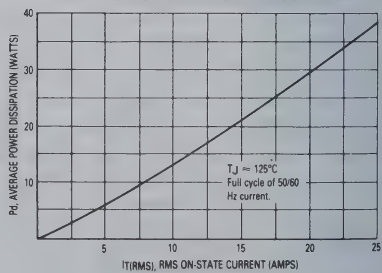


FIGURE 3 — ON-STATE POWER DISSIPATION



—40, —40I Current Ratings

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Note 1) (T_J = 110°C)	I_{DRM}	—	—	2.0	mA
Peak On-State Voltage (Either Direction) (I_{TM} = 56 A Peak; Pulse Width ⩽ 2.0 ms, Duty Cycle ⩽ 2.0%)	V_{TM}	—	—	1.85	Volts
Gate Trigger Current, Continuous dc (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(−), G(−)	I_{GT}	—	—	40	mA
Gate Trigger Voltage, Continuous dc (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(−), G(−)	V_{GT}	—	—	2.0	Volts
(R_L = 10 k Ω, T_J = 110°C) MT2(+), G(+); MT1(−), G(−)		0.2	—	—	
Holding Current (V_D = 12 V, I_{TM} = 200 mA, Gate Open)	I_H	—	—	50	mA
Gate Controlled Turn-On Time (I_{TM} = 56 A pk, I_G = 200 mA)	tgt	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage (I_{TM} = 56 A pk, Commutating di/dt = 22 A/ms, Gate Unenergized, T_C = 60°C)	dv/dt(C)	5.0	—	—	V/μs
Critical Rate of Rise of Off-State Voltage (Exponential Waveform, T_C = 110°C)	dv/dt	30	—	—	V/μs

Note 1: Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

2.3

FIGURE 4 — RMS CURRENT DERATING

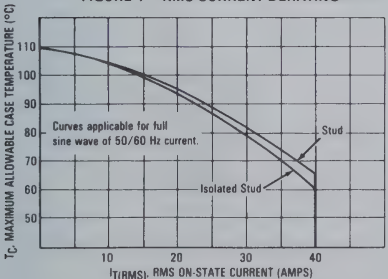
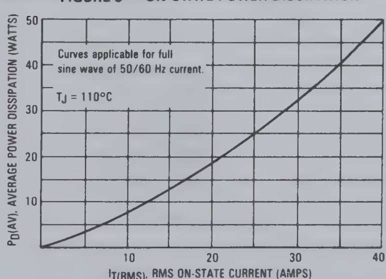


FIGURE 5 — ON-STATE POWER DISSIPATION



2.3

USING THE MOC OPTO COUPLERS AND MAC TRIAC SERIES DEVICES

The MOCXXXX Opto Coupler can be used as a triac driver with MACXXXX-X by selecting R_C to limit the surge current thru the coupler and yet supply enough gate drive to the triac to guarantee complete turn on. The maximum surge current rating of the coupler (I_{TSM}) determines the minimum value of R_C:

$$R_C\,(\text{min}) = \frac{V_{in}(\text{pk})}{I_{TSM}\,(\text{coupler})}$$

For high line 110 Vac nominal voltage: $V_{in}(\text{pk}) = 187$ V.

$$R_C\,(\text{min}) = \frac{187\text{ V}}{1.2\text{ A}} = 155.8\text{ ohms}$$

In practice, this would be a 180 ohm resistor.

The maximum gate drive required determines the maximum value of R_C:

$$R_C\,(\text{max}) = \frac{V_{IH}-V_{TM}}{I_{GT}(\text{triac})}$$

Where V_{IH} is the inhibit voltage of the coupler and V_{TM} is the on-state voltage of the triac in the coupler.

For the MOC3040 and MAC3040 −25 V_{IH} = 40 V. V_{TM} = 3.0 V, and I_{GT} = 40 mA.

$$R_C\,(\text{max}) = \frac{40\text{ V}-3.0\text{ V}}{40\text{ mA}} = 930\text{ ohms}$$

In practice, the gate is driven two or three times I_{GT} to guarantee complete turn on. R_C (max) would be 460 ohms or 310 ohms.

The line voltage at turn on is:

$$V_{\text{Line at turn on}} = R_C \cdot I_{GT} + V_{TM}(\text{coupler}) + V_{GT}(\text{triac})$$

For the above example $V_{GT}(\text{triac})$ = 2.0 V, I_{GT} = 80 mA, R_C = 210 ohms.

$$V_{\text{Line at turn on}} = (210)(0.08\text{ A}) + 3.0\text{V} + 2.0\text{V} = 22\text{ V}$$

Resistive Loads

Resistive heating elements and incandescent lamps are typical loads for the triac. Cold incandescent lamps can draw 5-6 times their hot RMS value on start up. The triac must be specified to sustain the repetitive surge (I_{TSM}). In practice, the RMS value is chosen at two times actual so the surge rating of the triac will be very high.

Inductive Loads

Motors, solenoids, and magnets are typical problem loads for the triac and coupler. Since the triac turns off as the current approaches zero, but the inductive voltage is still high, it appears to the triac as a rise in applied voltage. If this rate of rise in voltage exceeds the dv/dt commutating of the triac or the dv/dt static of the coupler, the triac will turn back on.

Snubber Network

When the dv/dt of the circuit exceeds the capability of the coupler or triac, a R_SC_S network is placed across the main terminals of the triac. In most applications the snubber used for the triac will also protect the coupler. The R_S also limits the energy from the C_S destroying the gate region on the first use of the triac.

Since the power factor of the board (cosine of the I-V phase shift) is not always known, a typical design can be a starting point for scope verification.

For power factor = 0.1, 110 V nominal line.

$$V_{\text{turn off voltage}} = V_{pk}\sin\phi \approx V_{pk} \approx 187\text{ V}$$

Setting the dv/dt $_C$ (triac) equal to the circuit $V_{\text{Turn off}}$ over the snubber time constant and solving for R_S:

$$\text{dv/dt C (triac)} = \frac{V_{\text{Turn off}}}{R_S C_S}$$

$$R_S = \frac{V_{\text{Turn off}}}{\text{dv/dt (c) } C_S}$$

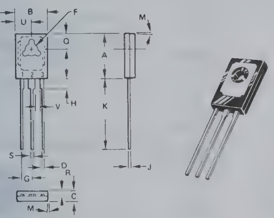
For MAC3030-25 dv/dt (c) = 5.0 V/μs, and choosing C_S = 0.1 μF

$$R_S = \frac{187\text{ V}}{(5.0\text{ V}/\mu\text{s})(0.1\ \mu\text{F})}$$

$$R_S = 374\text{ ohms}$$

In practice, R_S is selected empirically. For more details see AN780A.

OUTLINE DIMENSIONS

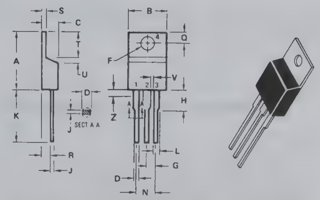


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10 80	11 05	0.425	0 435
B	7 49	7 75	0 295	0 305
C	2 41	2 67	0 095	0 105
D	0.51	0.66	0 020	0 026
F	2.92	3 18	0.115	0 125
G	2.31	2 46	0 091	0 097
H	1.27	2 41	0.050	0 095
J	0 38	0 64	0 015	0 025
K	15.11	16.64	0.595	0 655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0 158
R	1.14	1 40	0.045	0 055
S	0 64	0.89	0 025	0.035
U	3.68	3.94	0 145	0.155
V	1.02	–	0.040	–

STYLE 5
PIN 1 MT1
2 MT2
3 GATE

NOTES
1 LEADS, TRUE POSITIONED WITHIN 0.25 mm (0 010) DIA TO DIM "A" & "B" AT MAXIMUM MATERIAL CONDITION
2 MT = MAIN TERMINAL

CASE 77-04
TO-126

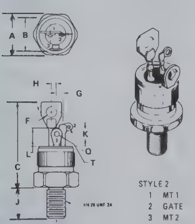


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14 60	15 75	0 575	0 620
B	9 65	10 29	0 380	0 405
C	4 06	4 82	0 160	0 190
D	0 64	0 89	0 025	0 035
F	3 61	3 73	0 142	0 147
G	2 41	2 67	0 095	0 105
H	2 79	3 93	0 110	0 155
J	0 36	0 56	0 014	0.022
K	12 70	14 27	0 500	0 562
L	1 14	1 39	0 045	0.055
N	4 83	5 33	0 190	0.210
Q	2 54	3 04	0 100	0 120
R	2 04	2 79	0 080	0 110
S	1 14	1 39	0 045	0 055
T	5 97	6 48	0 235	0 255
U	0 00	1 27	0 000	0 050
V	1 14	–	0.045	–
Z	–	2 03	–	0.080

STYLE 4
PIN 1. MT1
2. MT2
3. GATE
4 MT2

NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3

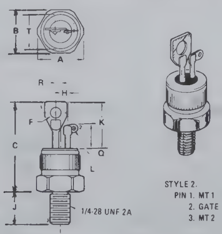
CASE 221A-02



STYLE 2
1 MT 1
2 GATE
3 MT 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12 73	12.83	0 501	0.505
C	–	32 51	-	1.280
F		4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1 60	2 01	0.063	0.079
J	10.67	11 56	0.420	0.455
K	7 62	8.89	0.300	0 350
L	6.48	6.99	0 255	0.275
Q	1.40	2 16	0.055	0.085
T	3 43	3 81	0 135	0 150

CASE 311-01



STYLE 2.
PIN 1. MT 1
2. GATE
3. MT 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0 559
C	26 67	30.23	1.050	1 190
F	3.43	4 06	0.135	0.160
H	2 29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1 40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

2.3

MBS4991
MBS4992

MOTOROLA

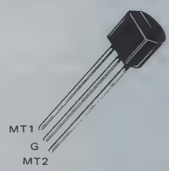
SILICON BIDIRECTIONAL SWITCH (PLASTIC)

BIDIRECTIONAL DIODE THYRISTORS

. . . designed for full-wave triggering in Triac phase control circuits, half-wave SCR triggering application and as voltage level detectors. Supplied in an inexpensive plastic TO-92 package for high-volume requirements, this low-cost plastic package is readily adaptable for use in automatic insertion equipment.

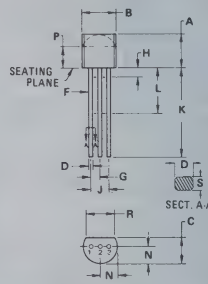
- Low Switching Voltage — 8.0 Volts Typical
- Uniform Characteristics in Each Direction
- Low On-State Voltage — 1.7 Volts Maximum
- Low Off-State Current — 0.1 μA Maximum
- Low Temperature Coefficient — 0.02 %/°C Typical

2.3



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Dissipation	P_D	500	mW
DC Forward Current	I_F	200	mA
DC Gate Current (off-state only)	$I_{G(off)}$	5.0	mA
Repetitive Peak Forward Current (1.0% Duty Cycle, 10 μs Pulse Width, $T_A = 100°C$)	$I_{FM(rep)}$	2.0	Amp
Non-Repetitive Forward Current 10 μs Pulse Width, $T_A = 25°C$	$I_{FM(nonrep)}$	6.0	Amp
Operating Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-92
PLASTIC

2.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Switching Voltage		V_S				Vdc
	MBS4991		6.0	8.0	10	
	MBS4992		7.5	8.0	9.0	
Switching Current		I_S				μAdc
	MBS4991		–	175	500	
	MBS4992		–	90	120	
Switching Voltage Differential		$\|V_{S1}-V_{S2}\|$				Vdc
	MBS4991		–	0.3	0.5	
	MBS4992		–	0.1	0.2	
Gate Trigger Current (V_F = 5.0 Vdc R_L = 1.0 K ohm)	MBS4992	I_{GF}	–	–	100	μAdc
Holding Current		I_H				mAdc
	MBS4991		–	0.7	1.5	
	MBS4992		–	0.2	0.5	
Off-State Blocking Current		I_B				μAdc
(V_F = 5.0 Vdc, T_A = 25°C)	MBS4991		–	0.08	1.0	
(V_F = 5.0 Vdc, T_A = 85°C)	MBS4991		–	2.0	10	
(V_F = 5.0 Vdc, T_A = 25°C)	MBS4992		–	0.08	0.1	
(V_F = 5.0 Vdc, T_A = 100°C)	MBS4992		–	6.0	10	
Forward On-State Voltage		V_F				Vdc
(I_F = 175 mAdc)	MBS4991		–	1.4	1.7	
(I_F = 200 mAdc)	MBS4992		–	1.5	1.7	
Peak Output Voltage (C_c = 0.1 μF, R_L = 20 ohms, (Figure 7)		V_o	3.5	4.8	–	Vdc
Turn-On Time (Figure 8)		t_{on}	–	1.0	–	μs
Turn-Off Time (Figure 9)		t_{off}	–	30	–	μs
Temperature Coefficient of Switching Voltage (-50 to +125°C)		T_C	–	+0.02	–	%/°C

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – SWITCHING VOLTAGE versus TEMPERATURE

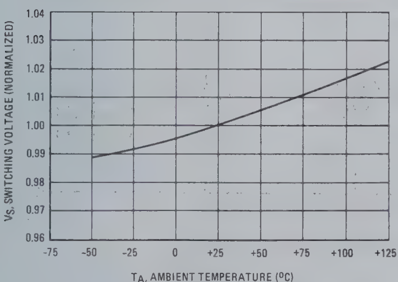
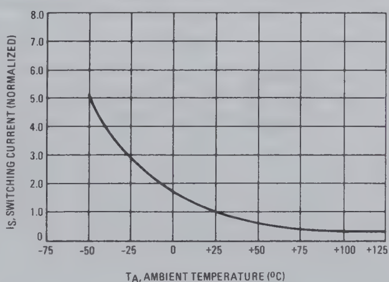


FIGURE 2 – SWITCHING CURRENT versus TEMPERATURE



2.3

FIGURE 3 — HOLDING CURRENT versus TEMPERATURE

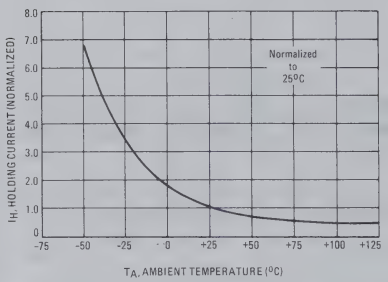


FIGURE 4 — OFF-STATE BLOCKING CURRENT versus TEMPERATURE

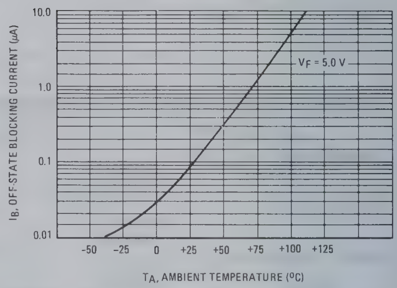


FIGURE 5 — ON-STATE VOLTAGE versus FORWARD CURRENT

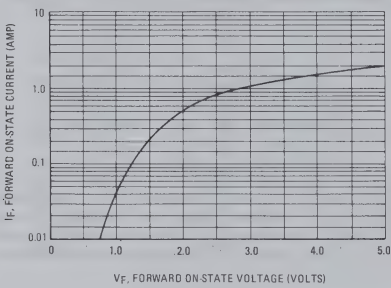


FIGURE 6 — PEAK OUTPUT VOLTAGE (FUNCTION OF R_L AND C_c)

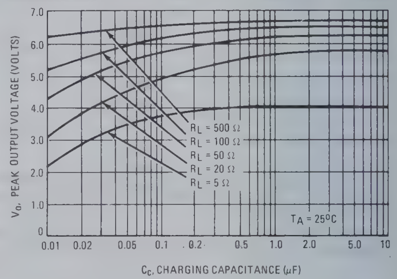


FIGURE 7 — PEAK OUTPUT VOLTAGE TEST CIRCUIT

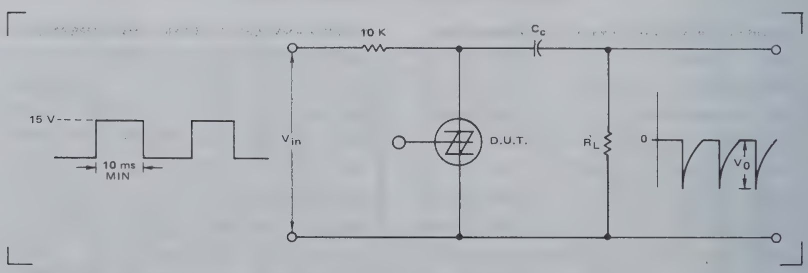
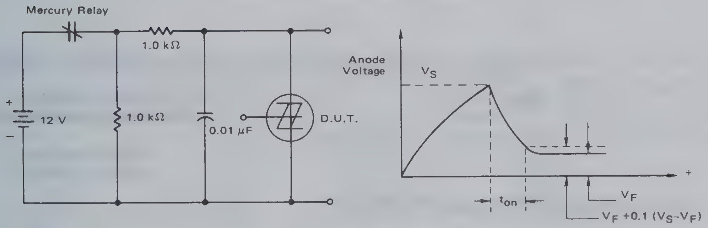
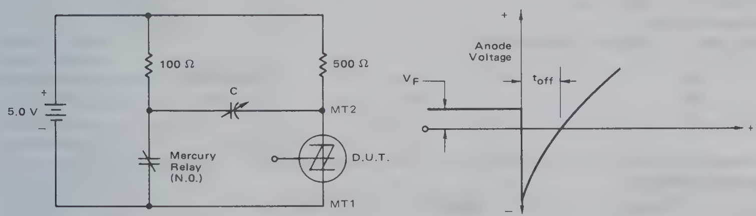


FIGURE 8 — TURN-ON TIME TEST CIRCUIT



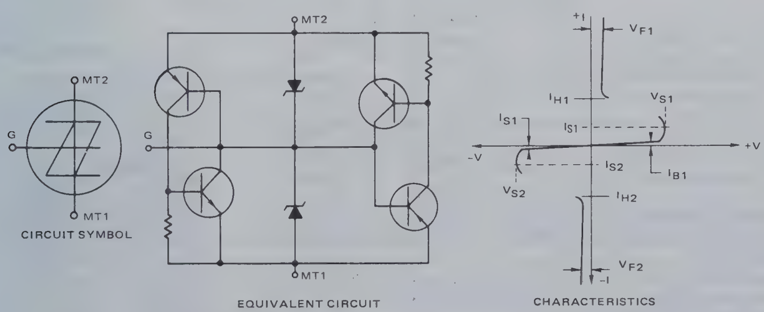
Turn-on time is measured from the time V_S is achieved to the time when the anode voltage drops to within 90% of the difference between V_S and V_F.

FIGURE 9 — TURN-OFF TIME TEST CIRCUIT

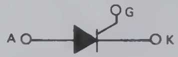


With the SBS in conduction and the relay contacts open, close the contacts to cause anode A2 to be driven negative. Decrease C until the SBS just remains off when anode A2 becomes positive. The turn-off time, t_{off}, is the time from initial contact closure and until anode A2 voltage reaches zero volts.

FIGURE 10 — DEVICE EQUIVALENT CIRCUIT, CHARACTERISTICS AND SYMBOLS

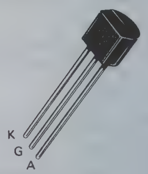


MOTOROLA



PLASTIC SILICON CONTROLLED RECTIFIERS

1.5 AMPERE RMS
50 thru 600 VOLTS



PLASTIC SILICON CONTROLLED RECTIFIERS

. . . designed and tested for repetitive peak operation required for CD ignition, fuel ignitors, flash circuits, motor controls and low-power switching applications.

- 150 Amperes for 2 μs Safe Area
- High dv/dt
- Very Low VF at High Current
- Low-Cost TO-92
- KAG Pinout Available As MCR23 Series

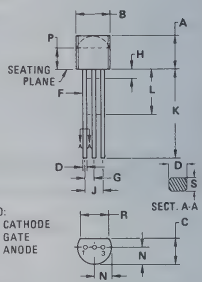
2.3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Blocking Voltage	V_{RRM}		Volts
MCR22-2		50	
MCR22-3		100	
MCR22-4		200	
MCR22-5		300	
MCR22-6		400	
MCR22-7		500	
MCR22-8		600	
On-State Current RMS (All Conduction Angles)	$I_{T(RMS)}$	1.5	Amps
Peak Nonrepetitive Surge Current, $T_A = 25°C$ (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	15	Amps
Circuit Fusing Considerations, $T_A = 25°C$ (t = 2.0 to 8.3 ms)	I^2t	0.9	A^2s
Peak Gate Power, $T_A = 25°C$	P_{GM}	0.5	Watts
Average Gate Power, $T_A = 25°C$	$P_{G(AV)}$	0.1	Watts
Peak Forward Gate Current, $T_A = 25°C$ (300 μs, 120 PPS)	I_{FGM}	0.2	Amps
Peak Reverse Gate Voltage	V_{RGM}	5.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Lead Solder Temperature (Lead Length ≥ 1/16″ from case, 10 s Max)	—	+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	50	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	160	°C/W



STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70 mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70 mm (0.5") FROM SEATING PLANE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

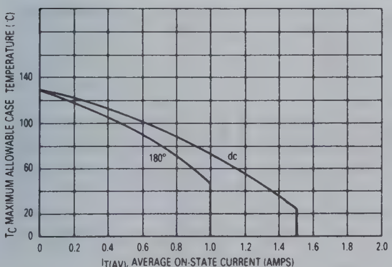
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted. R_{GK} = 1000 Ohms.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_C = 125°C)	MCR22-2	V_{DRM}	50	—	—	Volts
	MCR22-3		100	—	—	
	MCR22-4		200	—	—	
	MCR22-5		300	—	—	
	MCR22-6		400	—	—	
	MCR22-7		500	—	—	
	MCR22-8		600	—	—	
Peak Forward Blocking Current		I_{DRM}	—	—		μA
(Rated V_{DRM}, T_C = 25°C)					10	
(Rated V_{DRM}, T_C = 125°C)					200	
Peak Reverse Blocking Current		I_{RRM}	—	—		μA
(Rated V_{RRM}, T_C = 25°C)					10	
(Rated V_{RRM}, T_C = 125°C)					200	
Forward "On" Voltage (I_{TM} = 1.0 A peak)		V_{TM}	—	1.2	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 1)	T_C = 25°C	I_{GT}	—	30	200	μA
(Anode Voltage = 6.0 Vdc, R_L = 100 Ohms)	T_C = −40°C		—	—	500	
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}	—	—	0.8	Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = −40°C		—	—	1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C	V_{GD}	0.1	—	—	
Holding Current	T_C = 25°C	I_H	—	2.0	5.0	mA
(Anode Voltage = 12 Vdc)	T_C = −40°C		—	—	10	
Forward Voltage Application Rate (T_C = 125°C)		dv/dt	—	25	—	V/μs
Turn-On Time		t_{on}	—	1.2	—	μs
Turn-Off Time		t_{off}	—	40	—	μs

NOTE 1. R_{GK} Current Not Included in Measurement

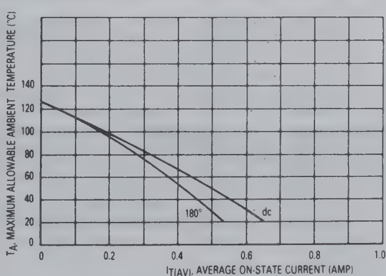
CURRENT DERATING

FIGURE 1 — MAXIMUM CASE TEMPERATURE



$R_{\theta JC}$ = 50°C/W
COOLING TIME = 3.0 ms
T_J = 125°C

FIGURE 2 — MAXIMUM AMBIENT TEMPERATURE



$R_{\theta JA}$ = 160°C/W
COOLING TIME = 3.0 ms
T_J = 125°C

2.3

2.3

FIGURE 3 — TYPICAL FORWARD VOLTAGE

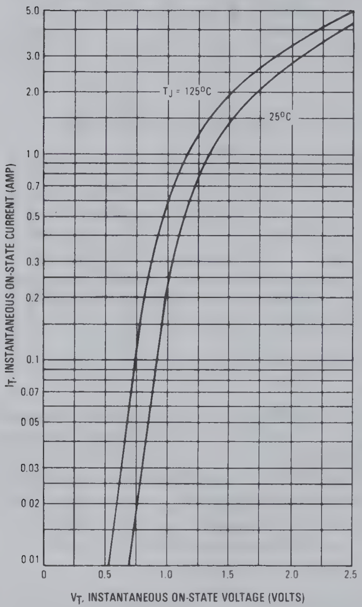


FIGURE 4 — PEAK REPETITIVE CAPACITOR DISCHARGE CURRENT

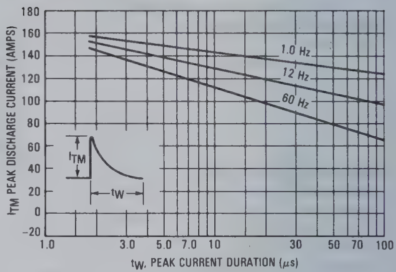


FIGURE 5 — PEAK REPETITIVE SINUSOIDAL CURVE

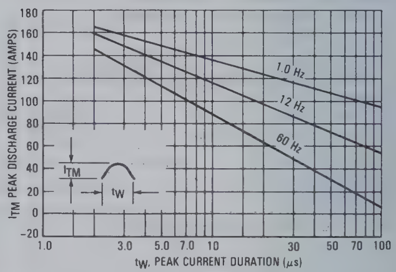
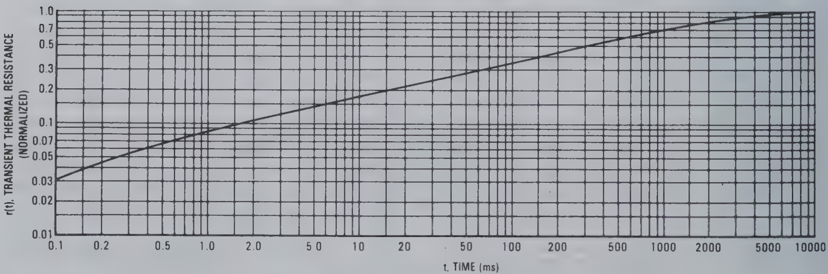


FIGURE 6 — THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 7 — GATE TRIGGER VOLTAGE

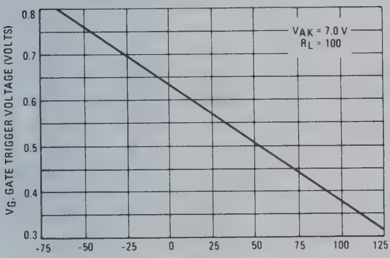


FIGURE 8 — TYPICAL GATE TRIGGER CURRENT

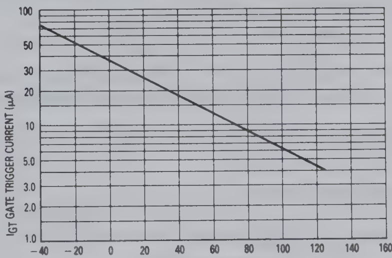


FIGURE 9 — HOLDING CURRENT

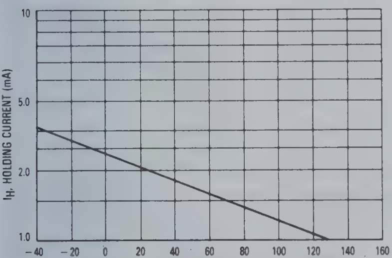
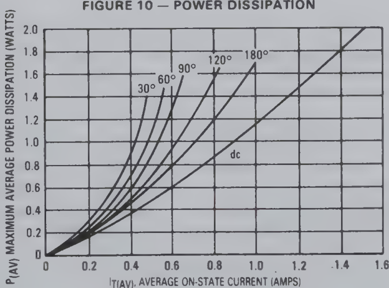


FIGURE 10 — POWER DISSIPATION



THYRISTOR APPLICATION NOTES

AN-240	SCR Power Control Fundamentals
AN-295	Suppressing RFI in Thyristor Circuits
AN-443	Directional and Speed Control for Series, Universal and Shunt Motors
AN-482	Electronic Speed Control of Applicance Motors
AN-527	Theory, Characteristics and Applications of the Programmable Unijunction Transistor
AN-568	A Fuse-Thyristor Coordinator Primer
AN-599	Mounting Techniques for Metal Packaged Power Semiconductors

To obtain copies of these notes list the AN number(s) on your company letterhead and send your request to:

Technical Information Center
Motorola Semiconductor Products, Inc.
P.O. Box 20912
Phoenix, Arizona 85036

2.3

MCR63-1 thru 10
MCR64-1 thru 10
MCR65-1 thru 10

MOTOROLA

REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for industrial and consumer applications such as power supplies; battery chargers; temperature, motor, light, and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 550 Amp
- Rugged Construction in Either Pressfit, Stud, or Isolated Stud
- Glass Passivated Junctions for Maximum Reliability

SILICON CONTROLLED RECTIFIER

55 AMPERES RMS
25–800 VOLTS

CASE 310-01
MCR63 series

CASE 311-01
MCR65 series

CASE 263-03
MCR64 series

2.3

MAXIMUM RATINGS

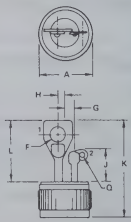
Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage	V_{DRM}(1) or V_{RRM}		Volts
MCR63, MCR64, MCR65 -1		25	
-2		50	
-3		100	
-4		200	
-5		300	
-6		400	
-7		500	
-8		600	
-9		700	
-10		800	
Non-Repetitive Peak Reverse Blocking Voltage ($t \leq 5.0$ ms)	V_{RSM}		Volts
MCR63, MCR64, MCR65 -1		35	
-2		75	
-3		150	
-4		300	
-5		400	
-6		500	
-7		600	
-8		700	
-9		800	
-10		900	
Forward Current RMS	$I_{T(RMS)}$	55	Amp
Peak Surge Current (One cycle, 60 Hz) (T_J = -40 to +125°C)	I_{TSM}	550	Amp
Circuit Fusing Considerations (T_J = -40 to +125°C)(t = 1.0 to 8.3 ms)	I^2t	1255	A^2s
Peak Gate Power	P_{GFM}	20	Watts
Average Gate Power (Pulse Width ≤ 2 μs)	$P_{GF(AV)}$	0.5	Watt
Peak Forward Gate Current	I_{GFM}	2.0	Amp
Peak Gate Voltage — Forward	V_{GFM}	10	Volts
Reverse	V_{GRM}	10	
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque	–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Pressfit and Stud		1.0	
Isolated Stud		1.1	

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.

MCR63 series

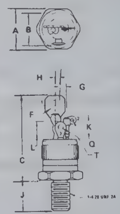


STYLE 1
1. CATHODE
2 GATE
CASE ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12 73	12 83	0 501	0 505
F		4 06		0 160
G	2 16	2 41	0.085	0 095
H	1.52	1.78	0 060	0 070
J	7 62	8 89	0 300	0 350
K		26 67		1 050
L	–	17 02	–	0 670
Q	1 40	2 16	0 055	0 085

CASE 310-01

MCR65 series

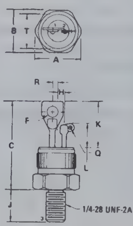


STYLE 1
1 CATHODE
2. GATE
3 ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14 00	14 20	0 551	0 559
B	12 73	12.83	0 501	0 505
C	–	32.51	–	1 280
F	–	4.06		0 160
G	2.16	2.41	0 085	0 095
H	1.60	2.01	0 063	0 079
J	10 67	11 56	0.420	0 455
K	7.62	8.89	0 300	0 350
L	6 48	6 99	0 255	0 275
Q	1.40	2.16	0 055	0.085
T	3 43	3.81	0 135	0 150

CASE 311-01

MCR64 series



STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15 34	15 60	0 604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1 050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0 670
L	7.62	8.89	0 300	0.350
Q	1.40	2 16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}, with gate open, T_J = 125°C)	I_{DRM}	–	2.0	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}, with gate open, T_J = 125°C)	I_{RRM}	–	2.0	mA
Forward "On" Voltage (I_{TM} = 175 A Peak)	V_{TM}	–	2.0	Volts
Gate Trigger Current (Continuous dc)	I_{GT}			mA
(V_D = 12 V, R_L = 50 Ω) T_C = 25°C		–	40	
T_C = –40°C		–	75	
Gate Trigger Voltage (Continuous dc)	V_{GT}			Volts
(V_D = 12 V, R_L = 50 Ω) T_C = 25°C		–	3.0	
T_C = –40°C		–	3.5	
(V_D = Rated V_{DRM}, R_L = 1.0 kΩ, T_J = 125°C)		0.2	–	
Holding Current (V_D = 12 V, R_L = 50 Ω, Gate Open)	I_H	–	60	mA
Forward Voltage Application Rate (T_J = 125°C, V_D = Rated V_{DRM})	dv/dt	50	–	V/μs

2.3

FIGURE 1 – AVERAGE CURRENT DERATING

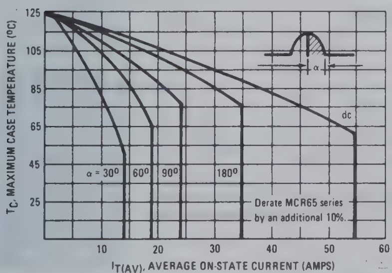
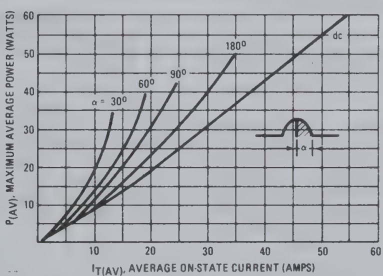


FIGURE 2 – POWER DISSIPATION

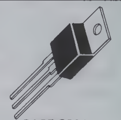


MCR67 series
MCR68 series
(12 Amperes RMS)
MCR69 series
(25 Amperes RMS)

MOTOROLA

SILICON CONTROLLED RECTIFIERS

25 thru 100 VOLTS



CASE 221A
MCR68, 69

CASE 86
MCR67

REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for overvoltage protection in crowbar circuits.

- Glass-Passivated Junctions for Greater Parameter Stability and Reliability
- Center-Gate Geometry for Uniform Current Spreading Enabling High Discharge Current
- Small Rugged, Thermowatt or Metal Packages Constructed for Low Thermal Resistance for Maximum Power Dissipation and Durability
- High Capacitor Discharge Current
  300 Amps (MCR67, 68)
  750 Amps (MCR69)

2.3

MAXIMUM RATINGS

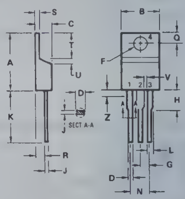
Rating	Symbol	MCR67	MCR68	MCR69	Unit
		Value			
Repetitive Peak Forward or Reverse Blocking Voltage (Note 1) (T_J = −40 to +125°C)	V_{DRM} or V_{RRM}				Volts
MCR67,68,69 -1		← 25 →			
-2		← 50 →			
-3		← 100 →			
Peak Discharge Current (Note 2)	I_{TM}	300	300	750	Amps
On-State Current (T_C = 85°C) (1/2 Cycle, Sine Wave, 60 Hz)	$I_{T(RMS)}$ $I_{T(AV)}$	12 8	12 8	25 16	Amps
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	100	100	300	Amps
Circuit Fusing (t ≤ 8.3 ms)	I^2t	40	40	375	A^2s
Critical Rate-of-Rise of Current (Note 3)	di/dt	75		100	A/μs
Peak Gate Current (t ≤ 2.0 μs)	I_{GM}	2.0			Amps
Peak Gate Power (t ≤ 2.0 μs)	P_{GM}	20			Watts
Average Gate Power	$P_{G(AV)}$	0.5			Watt
Operating Junction Temperature Range	T_J	−40 to +125			°C
Storage Temperature Range	T_{stg}	−40 to +150			°C
Mounting Torque	—	15	8	8	in.lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	MCR67	MCR68	MCR69	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	2.0	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	← 60 →			°C/W

NOTES:

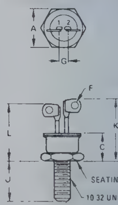
1. V_{DRM} for all types can be applied on a continuous basis over the operating junction temperature range without recurring damage. Ratings apply for open or shorted gate conditions or negative voltage on the gate. Devices should not be tested for blocking voltage such that the supply voltage exceeds the rating of the device.
2. Ratings apply for t_w = 1.0 ms. See Figure 1 for I_{TM} capability for various duration of an exponentially decaying current waveform. t_w is defined as 5 time constants of an exponentially decaying current pulse.
3. Test Conditions: I_G = 150 mA, V_D = Rated V_{DRM}, I_{TM} = Rated Value, T_J = 125°C.



STYLE 3
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

CASE 221A-02
TO-220 AB
MCR68/MCR69 series

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080



NOTE
1. DIM L & H APPLIES TO ALL LEADS

STYLE 1
PIN 1. GATE
2. CATHODE
STUD. ANODE

CASE 86-01
MCR67 series

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		11.10	-	0.437
C		7.87	-	0.310
F	1.78 TYP		0.070 TYP	
G	2.29	2.79	0.090	0.110
J	10.72	11.48	0.422	0.452
K		16.76		0.660
L		15.49		0.610

NOTE
1. DIM "G" MEASURED AT CAN

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Note 1) (V_D = Rated V_{DRM}, T_J = 125°C)	I_{DRM}	–	–	2.0	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}, T_J = 125°C)	I_{RRM}	–	–	2.0	mA
Forward On-State Voltage	V_{TM}				Volts
(I_{TM} = 24 Amps) (Note 2) MCR67,68		–	–	2.2	
(I_{TM} = 50 Amps) (Note 2) MCR69		–	–	1.8	
(I_{TM} = 300 Amps, t_w = 1.0 ms) (Note 3) MCR67,68		–	6.0	–	
(I_{TM} = 750 Amps, t_w = 1.0 ms) (Note 3) MCR69		–	6.0	–	
Gate Trigger Current (V_D = 12 V, R_L = 100 Ω)	I_{GT}	2.0	7.0	30	mA
Gate Trigger Voltage	V_{GT}				Volts
(V_D = 12 Volts, R_L = 100 Ω)		–	0.65	1.5	
(V_D = Rated V_{DRM}, R_L = 1.0 kΩ, T_J = 125°C)		0.2	0.40	–	
Holding Current (I_{TM} = 100 mA, Gate-Open)	I_H	3.0	15	50	mA
Latching Current (V_D = 12 Vdc, I_G = 150 mA, $t_r \leq 50$ μs)	I_L	–	–	60	mA
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Gate Open, Exponential Waveform, T_J = 125°C)	dv/dt	10	–	–	V/μs
Gate Controlled Turn-On Time (Note 4) (V_D = Rated V_{DRM}, I_G = 150 mA)	t_{gt}				μs
(I_{TM} = 24 Amps, peak) MCR67,68		–	1.0	–	
(I_{TM} = 50 Amps, peak) MCR69		–	1.0	–	

NOTES:

1. V_{DRM} for all types can be applied on a continuous basis over the operating junction temperature range without incurring damage. Ratings apply for open or shorted gate condtiions or negative voltage on the gate. Devices should not be tested for blocking voltage such that the supply voltage exceeds the rating of the device.
2. Pulse duration ≤ 300 μs, duty cycle ≤ 2%.
3. Ratings apply for t_w = 1.0 ms. See Figure 1 for I_{TM} capability for various durations of an exponentially decaying current waveform. t_w is defined as 5 time constants of an exponentially decaying current pulse.
4. The gate controlled turn-on time in a crowbar circuit will be influenced by the circuit inductance.

2.3

FIGURE 1 – PEAK CAPACITOR DISCHARGE CURRENT

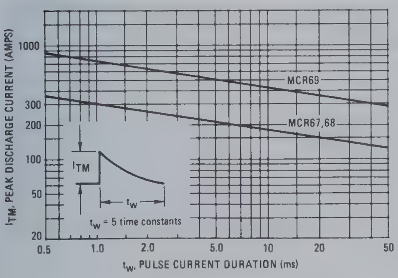


FIGURE 2 – PEAK CAPACITOR DISCHARGE CURRENT DERATING

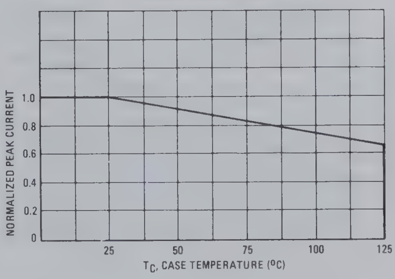


FIGURE 3 – CURRENT DERATING
MCR67,68

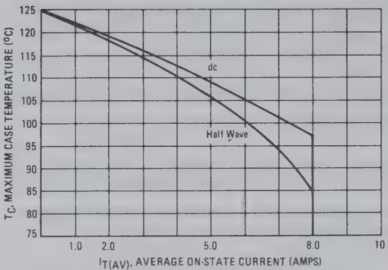


FIGURE 4 – CURRENT DERATING
MCR69

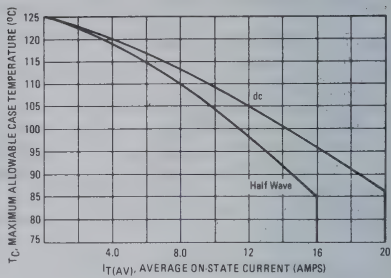


FIGURE 5 – MAXIMUM POWER DISSIPATION
MCR67,68

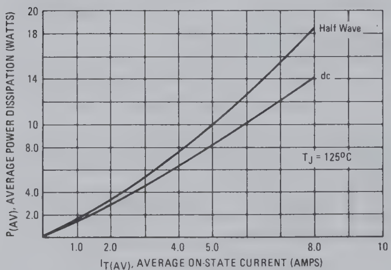


FIGURE 6 – MAXIMUM POWER DISSIPATION
MCR69

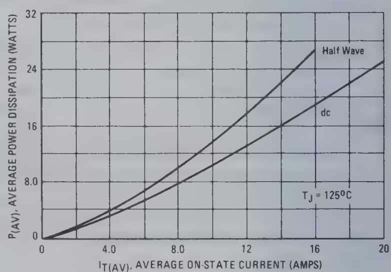


FIGURE 7 – THERMAL RESPONSE

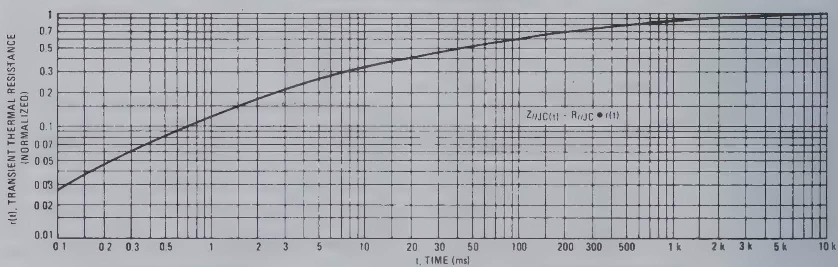


FIGURE 8 — GATE TRIGGER CURRENT

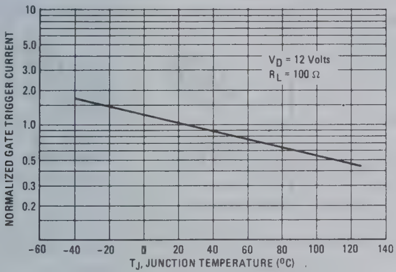
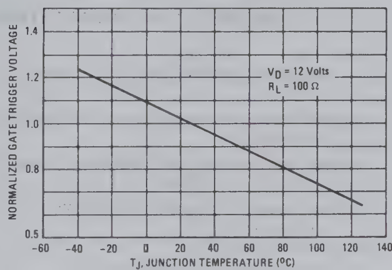
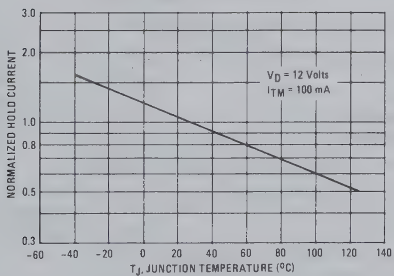


FIGURE 9 — GATE TRIGGER VOLTAGE



2.3

FIGURE 10 — HOLDING CURRENT



MCR70 series
(35 Amperes RMS)

MCR71 series
(55 Amperes RMS)

MOTOROLA

SILICON CONTROLLED RECTIFIERS

25 thru 100 VOLTS

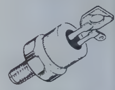
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for overvoltage protection in crowbar circuits.

- Glass-Passivated Junctions for Greater Parameter Uniformity and Reliability
- Center-Gate Geometry for Uniform Current Spreading Enabling High Peak Current Capability
- High Capacitor Discharge Current Capability
  850 Amps (MCR70)
  1700 Amps (MCR71)
- Hermetically-Sealed Metal Packages

2.3

CASE 175
MCR70 series



CASE 263
MCR71 series

MAXIMUM RATINGS

Rating	Symbol	Value MCR70	Value MCR71	Unit
Repetitive Peak Forward or Reverse Blocking Voltage (Note 1)	V_{DRM} or V_{RRM}			Volts
MCR70,71-1		25		
MCR70,71-2		50		
MCR70,71-3		100		
Peak Discharge Current (Note 2)	I_{TM}	850	1700	Amps
On-State Current ($T_C \leqslant 75^{\circ}C$)	$I_{T(RMS)}$	35	55	Amps
	$I_{T(AV)}$	22	35	
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, $T_J = 125^{\circ}C$)	I_{TSM}	350	550	Amps
Circuit Fusing ($t \leqslant 8.3$ ms)	I^2t	510	1255	A^2s
Critical Rate of Rise of Current (Note 3)	di/dt	100	200	A/μs
Forward Peak Gate Power ($t \leqslant 20\ \mu s$)	P_{GM}	20		Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5		Watts
Forward Peak Gate Current ($t \leqslant 20\ \mu s$)	I_{GM}	2.0		Amps
Operating Junction Temperature Range	T_J	−40 to +125		°C
Storage Temperature Range	T_{stg}	−40 to +150		°C
Mounting Torque	—	30		in.lb.

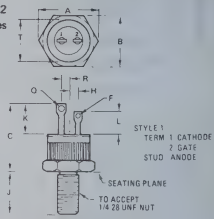
THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

NOTES:

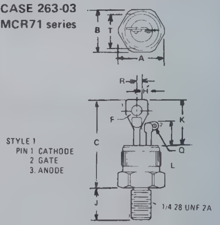
1. The rated voltage can be applied over the rated operating junction temperatures without incurring damage. Ratings apply for shorted-open or shorted-gate conditions or negative voltage on the gate. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltages.
2. Rating is for $t_w = 1.0$ ms. See Figure 1 for I_{TM} limits of an exponentially decaying current pulse of various durations.
3. Test Conditions: $I_G = 150$ mA, V_D = Rated V_{DRM}, I_{TM} = Rated Value, $T_J \leqslant 125^{\circ}C$.

CASE 175-02
MCR70 series



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

CASE 263-03
MCR71 series



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Note 1) (V_D = Rated V_{DRM}, T_J = 125°C)		I_{DRM}	–	–	2.0	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}, T_J = 125°C)		I_{RRM}	–	–	2.0	mA
On-State Voltage (Note 2)		V_{TM}				Volts
(I_{TM} = 70 A)	MCR70 series		–	1.5	1.85	
(I_{TM} = 175 A)	MCR71 series		–	1.7	2.1	
(I_{TM} = 850 A, t_w = 1.0 ms) Note 3	MCR70 series		–	6.0	–	
(I_{TM} = 1700 A, t_w = 1.0 ms) Note 3	MCR71 series		–	7.0	–	
Gate Trigger Current (V_D = 12 V, R_L = 100 Ω)		I_{GT}	2.0	10	30	mA
Gate Trigger Voltage		V_{GT}				Volts
(V_D = 12 V, R_L = 100 Ω)			–	1.0	1.5	
(V_D = Rated V_{DRM}, R_L = 1.0 kΩ, T_J = 125°C)			0.2	–	–	
Holding Current (I_{TM} = 0.5 A, Gate-Open)		I_H	3.0	15	50	mA
Latching Current (V_D = 12 V, I_G = 150 mA, $t_r \leq 50$ µs)		I_L	–	30	60	mA
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Gate Open, Exponential Waveform, T_C = 125°C)		dv/dt	10	–	–	V/µs
Turn-On Time (Note 3) (V_D = Rated V_{DRM}, I_G = 150 mA)		t_{on}				µs
(I_{TM} = 70 Amps, peak)	MCR70 series		–	1.0	–	
(I_{TM} = 110 Amps, peak)	MCR71 series		–	1.2	–	

NOTES:

1. The rated voltages can be applied over the rated operating junction temperatures without incurring damage. Ratings apply for shorted-open or shorted-gate conditions or negative voltage on the gate. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltages.
2. Duty Cycle ≤ 1%, Pulse Width ≤ 300 µs.
3. Characteristic applies for t_w = 1.0 ms. t_w is defined as 5 time constants of an exponentially decaying current pulse.
4. The gate controlled turn-on time in a crowbar circuit will be influenced by the circuit inductance.

2.3

FIGURE 1 – PEAK CAPACITOR DISCHARGE CURRENT

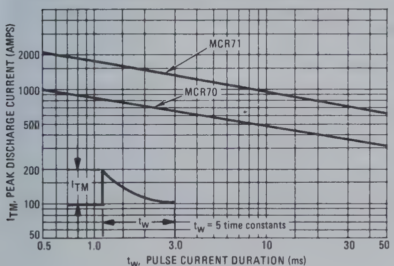
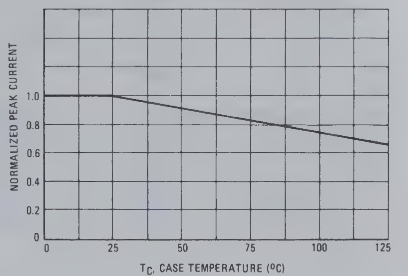


FIGURE 2 – PEAK CAPACITOR DISCHARGE CURRENT DERATING



2.3

FIGURE 3 – AVERAGE CURRENT DERATING
MCR70

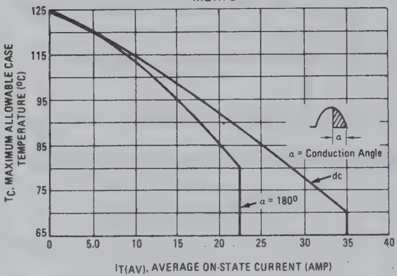


FIGURE 4 – POWER DISSIPATION
MCR70

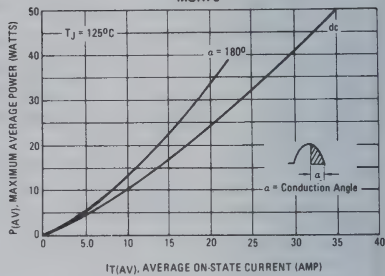


FIGURE 5 – CURRENT DERATING
MCR71

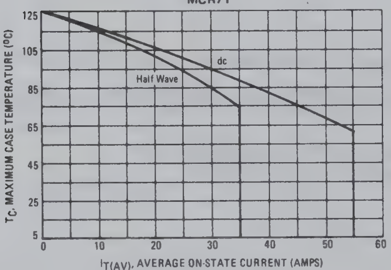


FIGURE 6 – POWER DISSIPATION
MCR71

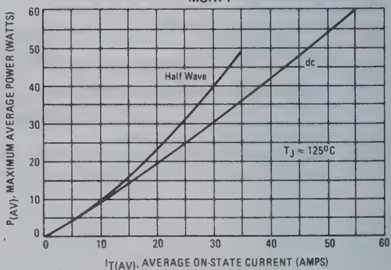


FIGURE 7 – TYPICAL THERMAL RESPONSE

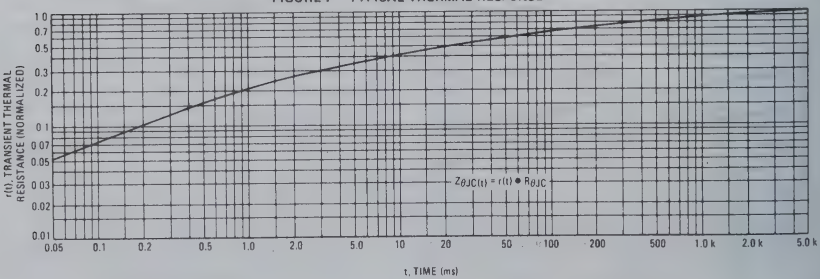


FIGURE 8 — GATE TRIGGER CURRENT

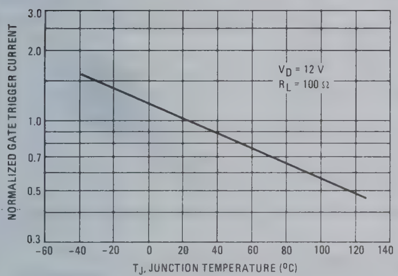
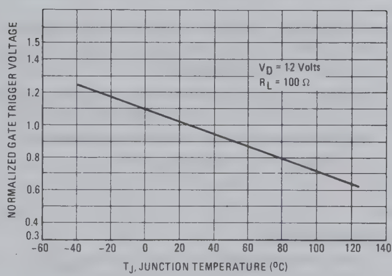
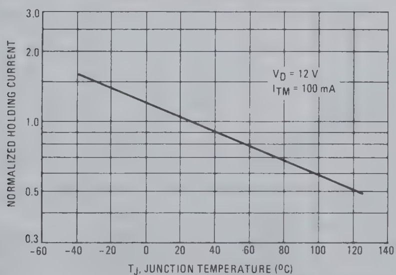


FIGURE 9 — GATE TRIGGER VOLTAGE



2.3

FIGURE 10 — HOLDING CURRENT



MCR72-1
thru
MCR72-8

MOTOROLA

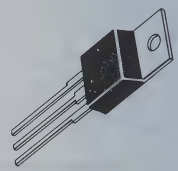
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for industrial and consumer applications such as temperature, light and speed control; process and remote controls; warning systems; capacitive discharge circuits and MPU interface.

- Center Gate Geometry for Uniform Current Density
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Low Trigger Currents, 200 μA Maximum for Direct Driving from Integrated Circuits

SILICON CONTROLLED RECTIFIER

8 AMPERES RMS
25 thru 600 VOLTS



2.3

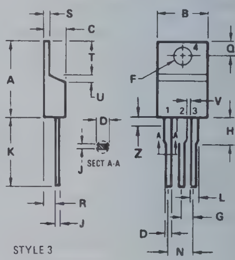
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Foward and Reverse Blocking Voltage (Note 1) (T_J = −40 to 110°C) (1/2 Sine Wave, R_{GK} = 1 kΩ)	V_{DRM} or V_{RRM}		Volts
MCR72-1		25	
MCR72-2		50	
MCR72-3		100	
MCR72-4		200	
MCR72-5		300	
MCR72-6		400	
MCR72-7		500	
MCR72-8		600	
On-State RMS Current (T_C = 83°C)	$I_{T(RMS)}$	8.0	Amps
Peak Non-Repetitive Surge Current (1/2 Cycle, 60 Hz, T_J = −40 to 110°C)	I_{TSM}	100	Amps
Circuit Fusing (t = 1 to 8.3 ms)	I^2t	40	A^2s
Peak Gate Voltage (t ⩽ 10 μs)	V_{GM}	±5.0	Volts
Peak Gate Current (t ⩽ 10 μs)	I_{GM}	1.0	Amp
Peak Gate Power (t ⩽ 10 μs)	P_{GM}	5.0	Watts
Average Gate Power	$P_{G(AV)}$	0.75	Watt
Operating Junction Temperature Range	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Mounting Torque	—	8.0	in-lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

NOTE 1: Ratings apply for negative gate voltage or R_{GK} = 1 kΩ. Devices shall not have a positive gate voltage concurrently with a negative voltage on the anode. Devices should not be tested with a constant current source for forward and reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.



STYLE 3
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C, R_{GK} = 1 kΩ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Note 1) (T_J = 110°C, V_D = Rated V_{DRM})	I_{DRM}	—	—	500	μA
Peak Reverse Blocking Current (Note 1) (T_J = 110°C, V_R = Rated V_{RRM})	I_{RRM}	—	—	500	μA
On-State Voltage (I_{TM} = 16 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.7	2.0	Volts
Gate Trigger Current, Continuous dc (Note 2) (V_D = 12 V, R_L = 100 Ω)	I_{GT}	—	30	200	μA
Gate Trigger Voltage, Continuous dc	V_{GT}				Volts
(V_D = 12 V, R_L = 100 Ω)		—	0.5	1.5	
(V_D = Rated V_{DRM}, R_L = 10 kΩ, T_J = 110°C)		0.1	—	—	
Holding Current (V_D = 12 V, I_{TM} = 100 mA)	I_H	—	—	6.0	mA
Critical Rate of Rise of Forward Blocking Voltage (V_D = Rated V_{DRM}, T_J = 110°C, Exponential Waveform)	dv/dt	—	10	—	v/μs
Gate Controlled Turn On Time (V_D = Rated V_{DRM}, I_{TM} = 16 A, I_G = 2 mA)	t_{gt}	—	1.0	—	μs

NOTES:

1. Ratings apply for negative gate voltage or R_{GK} = 1 kΩ. Devices shall not have a positive gate voltage concurrently with a negative voltage on the anode. Devices should not be tested with a constant current source for forward and reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Does not include R_{GK} current.

2.3

FIGURE 1 — AVERAGE CURRENT DERATING

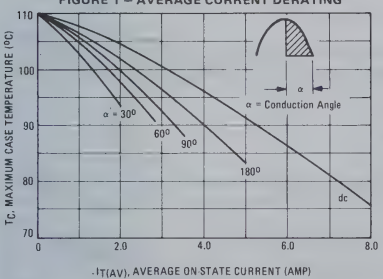


FIGURE 2 — ON-STATE POWER DISSIPATION

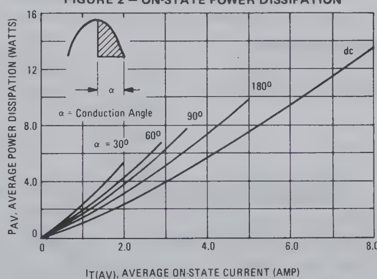


FIGURE 3 — NORMALIZED GATE CURRENT

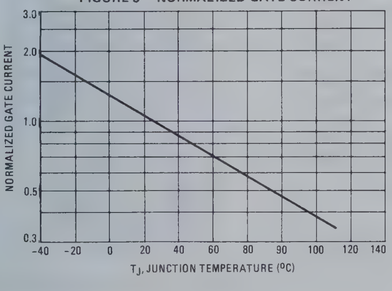
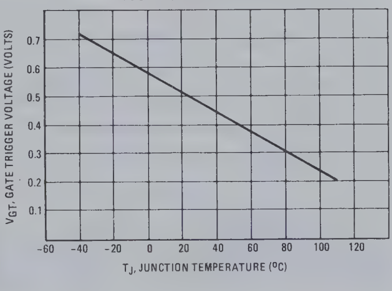


FIGURE 4 — GATE VOLTAGE



MOTOROLA

REVERSE BLOCKING TRIODE THYRISTORS

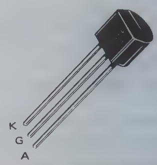
PNPN devices designed for high volume, line-powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

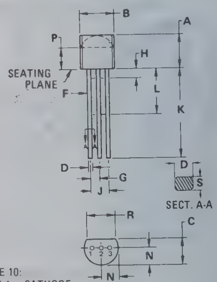
- Sensitive Gate Trigger Current — 200 μA Maximum
- Low Reverse and Forward Blocking Current — 100 μA Maximum, T_C = 125°C
- Low Holding Current — 5.0 mA Maximum
- Glass-Passivated Surface for Reliability and Uniformity
- Also Available with TO-5 or TO-18 Lead Form

2.3

PLASTIC SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
100 to 600 VOLTS





STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage	V_{RRM}		Volts
MCR100-3		100	
MCR100-4		200	
MCR100-5		300	
MCR100-6		400	
MCR100-7		500	
MCR100-8		600	
Forward Current RMS (See Figures 1 & 2) (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
Peak Forward Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.415	A^2s
Peak Gate Power — Forward, T_A = 25°C	P_{GM}	0.1	Watt
Average Gate Power — Forward, T_A = 25°C	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current — Forward, T_A = 25°C (300 μs, 120 PPS)	I_{GFM}	1.0	Amp
Peak Gate Voltage — Reverse	V_{GRM}	5.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-65 to +110	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Lead Solder Temperature (<1/16" from case, 10 s max)	—	+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (T_C = 125°C)	MCR100-3 MCR100-4 MCR100-5 MCR100-6 MCR100-7 MCR100-8	V_{DRM}	100 200 300 400 500 600		Volts
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C)		I_{DRM}	–	100	μA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C)		I_{RRM}	–	100	μA
Forward "On" Voltage (Note 1) (I_{TM} = 1.0 A peak @ T_A = 25°C)		V_{TM}	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 2) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	–	200	μA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms) (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 25°C T_C = −40°C T_C = 125°C	V_{GT}	– – 0.1	0.8 1.2 –	Volts
Holding Current (Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = 25°C T_C = −40°C	I_H	– –	5.0 10	mA

NOTE:
1. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
2. R_{GK} current is not included in measurement.

FIGURE 1 — MCR100-7, MCR100-8 CURRENT DERATING (REFERENCE: CASE TEMPERATURE)

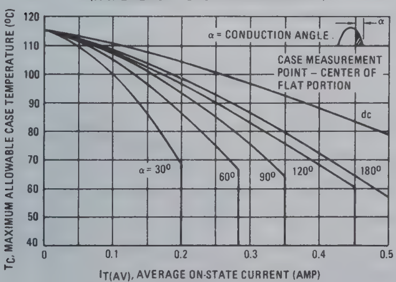
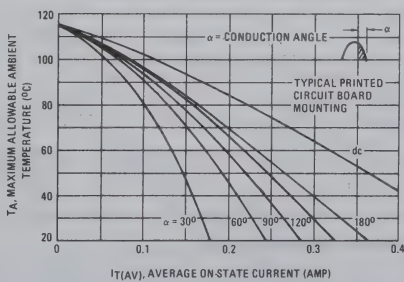


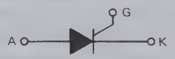
FIGURE 2 — MCR100-7, MCR100-8 CURRENT DERATING (REFERENCE: AMBIENT TEMPERATURE)



2.3

MCR101 thru MCR104

MOTOROLA



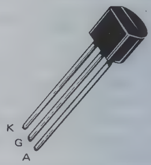
REVERSE BLOCKING TRIODE THYRISTOR

. . . Annular PNPN devices designed for low cost, high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 100 μA Maximum, $T_C = 85^oC$
- Low Holding Current – 5.0 mA Maximum
- Passivated Surface for Reliability and Uniformity
- Also available with TO-5 or TO-18 Lead Form

SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
15 thru 100 VOLTS



2.3

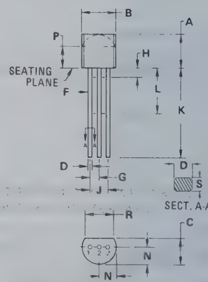
MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (R_{GK} = 1000 ohms, $T_C = +85^oC$) MCR101	V_{RRM}	15	Volts
MCR102		30	
MCR103		60	
MCR104		100	
Forward Current RMS (See Figures 1 & 2) (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
Peak Forward Surge Current, $T_A = 25^oC$ (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	Amp
Circuit Fusing Considerations, $T_A = 25^oC$ (t = 1.0 to 8.3 ms)	I^2t	0.415	A^2s
Peak Gate Power – Forward, $T_A = 25^oC$	P_{GM}	0.1	Watt
Average Gate Power – Forward, $T_A = 25^oC$	$P_{G(AV)}$	0.01	Watt
Peak Gate Current – Forward, $T_A = 25^oC$ (300 μs, 120 PPS)	I_{GM}	1.0	Amp
Peak Gate Voltage – Reverse	V_{GM}	4.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	–40 to +85	^oC
Storage Temperature Range	T_{stg}	–40 to +150	^oC
Lead Solder Temperature (<1/16″ from case, 10 s max)	–	+230	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	$^oC/W$

(1) Temperature reference point for all case temperature is center of flat portion of package.
($T_C = +85^oC$ unless otherwise noted.)



STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H		2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

2.3

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (Note 1) (T_C = 85°C)	MCR101 MCR102 MCR103 MCR104	V_{DRM}	15 30 60 100	– – – –	Volts
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 85°C)		I_{DRM}	–	100	μA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 85°C)		I_{RRM}	–	100	μA
Forward "On" Voltage (Note 2) (I_{TM} = 1.0 A peak @ T_A = 25°C)		V_{TM}	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 3) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	–	200	μA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C T_C = -65°C T_C = 85°C	V_{GT} V_{GD}	– – 0.1	0.8 1.2 –	Volts
Holding Current (Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = 25°C T_C = -65°C	I_H	– –	5.0 10	mA

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
3. R_{GK} current is not included in measurement.

FIGURE 1 – CURRENT DERATING (REFERENCE: CASE TEMPERATURE)

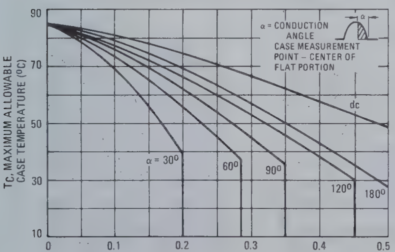
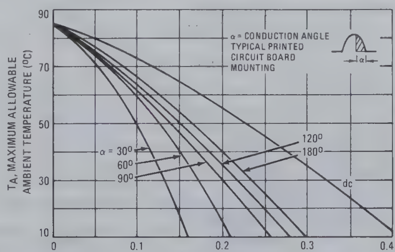


FIGURE 2 – CURRENT DERATING (REFERENCE: AMBIENT TEMPERATURE)



MCR106-1
thru
MCR106-8

MOTOROLA

REVERSE BLOCKING TRIODE THYRISTORS

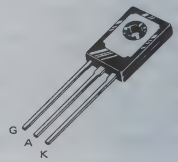
. . . PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

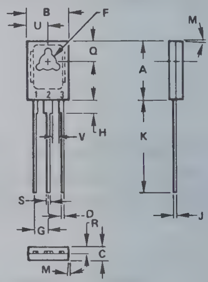
- Glass-Passivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability.

2.3

SILICON CONTROLLED RECTIFIERS

4.0 AMPERES RMS
30 thru 600 VOLTS





STYLE 2
PIN 1. CATHODE
2. ANODE
3. GATE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3^o TYP		3^o TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04 TO-126

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (Note 1) MCR106-1	V_{RRM}	30	Volts
-2		60	
-3		100	
-4		200	
-5		300	
-6		400	
-7		500	
-8		600	
RMS Forward Current (All Conduction Angles)	$I_{T(RMS)}$	4.0	Amp
Average Forward Current $T_C = 93^oC$ or $T_A = 30^oC$	$I_{T(AV)}$	2.55	Amp
Peak Non-Repetitive Surge Current (1/2 cycle, 60 Hz, $T_J = -40$ to $+110^oC$)	I_{TSM}	25	Amp
Circuit Fusing Considerations ($T_J = -40$ to $+110^oC$, t = 1.0 to 8.3 ms)	I^2t	2.6	A^2s
Peak Gate Power	P_{GM}	0.5	Watt
Average Gate Power	$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current	I_{GM}	0.2	Amp
Peak Reverse Gate Voltage	V_{RGM}	6.0	Volts
Operating Junction Temperature Range	T_J	-40 to +110	^oC
Storage Temperature Range	T_{stg}	-40 to +150	^oC
Mounting Torque (Note 2)	—	6.0	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.0	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^oC/W$

ELECTRICAL CHARACTERISTICS (T_C = 25°C and R_{GK} = 1000 ohms unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_J = 110°C, Note 1)	MCR106-1	V_{DRM}	30	–	–	Volts
	-2		60	–	–	
	-3		100	–	–	
	-4		200	–	–	
	-5		300	–	–	
	-6		400	–	–	
	-7		500			
	-8		600			
Peak Forward Blocking Current (Rated V_{DRM}, T_J = 110°C)		I_{DRM}	–	–	200	μA
Peak Reverse Blocking Current (Rated V_{RRM}, T_J = 110°C)		I_{RRM}	–	–	200	μA
Forward "On" Voltage (I_{TM} = 4.0 A Peak)		V_{TM}	–	–	2.0	Volts
Gate Trigger Current (Continuous dc) Note 3		I_{GT}				μA
(V_{AK} = 7.0 Vdc, R_L = 100 ohms)			–	–	200	
(V_{AK} = 7.0 Vdc, R_L = 100 ohms, T_C = −40°C)			–	–	500	
Gate Trigger Voltage (Continuous dc) (V_{AK} = 7.0 Vdc, R_L = 100 ohms, T_C = 25°C)		V_{GT}	–	–	1.0	Volts
Gate Non-Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 ohms, T_J = 110°C)		V_{GD}	0.2	–	–	Volts
Holding Current (V_{AK} = 7.0 Vdc, T_C = 25°C)		I_H	–	–	5.0	mA
Forward Voltage Application Rate (T_J = 110°C)		dv/dt	–	10	–	V/μs

NOTES:

1. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of compression washer (B52200-F006 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN209B).
For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C. For optimum results, an activated flux (oxide removing) is recommended.
3. R_{GK} current is not included in measurement.

CURRENT DERATING

FIGURE 1 – MAXIMUM CASE TEMPERATURE

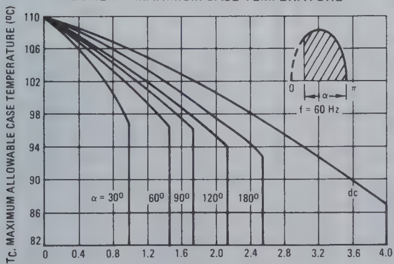
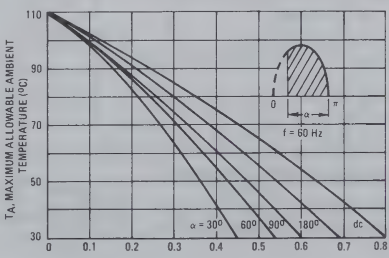


FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE

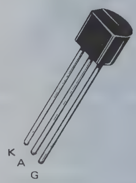


MCR115
MCR120

MOTOROLA

PLASTIC SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
100 and 200 VOLTS



2.3

REVERSE BLOCKING TRIODE THYRISTORS

. . . Annular PNPN devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current — 200 μA Maximum
- Low Reverse and Forward Blocking Current — 100 μA Maximum, T_C = 110°C
- Low Holding Current — 5.0 mA Maximum
- Passivated Surface for Reliability and Uniformity
- Also Available with TO-5 or TO-18 Lead Form

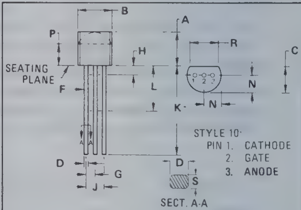
MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage	V_{RRM}		Volts
MCR115		150	
MCR120		200	
Forward Current RMS (See Figures 1 & 2) (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
Peak Forward Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.415	A^2s
Peak Gate Power — Forward, T_A = 25°C	P_{GM}	0.1	Watt
Average Gate Power — Forward, T_A = 25°C	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current — Forward, T_A = 25°C (300 μs, 120 PPS)	I_{GFM}	1.0	Amp
Peak Gate Voltage — Reverse	V_{GRM}	5.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Lead Solder Temperature (<1/16″ from case, 10 s max)	—	+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

(1) Temperature reference point for all case temperatures in center of flat portion of package. (T_C = +110°C unless otherwise noted.)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	
L	6.35		0.250	–
N	2.03	2.92	0.080	0.115
P	2.92		0.115	
R	3.43		0.135	
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (Note 1) (T_C = 110°C)	 MCR115 MCR120	V_{DRM}	 150 200	 - –	Volts
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 110°C)		I_{DRM}	–	100	μA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 110°C)		I_{RRM}	–	100	μA
Forward "On" Voltage (Note 2) (I_{TM} = 1.0 A peak @ T_A = 25°C)		V_{TM}	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 3) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	–	200	μA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms) (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 25°C T_C = -65°C T_C = 110°C	V_{GT} V_{GD}	– – 0.1	0.8 1.2 –	Volts
Holding Current (Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = 25°C T_C = -65°C	I_H	– –	5.0 10	mA

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
3. R_{GK} current is not included in measurement.

2.3

FIGURE 1 – CURRENT DERATING (REFERENCE: CASE TEMPERATURE)

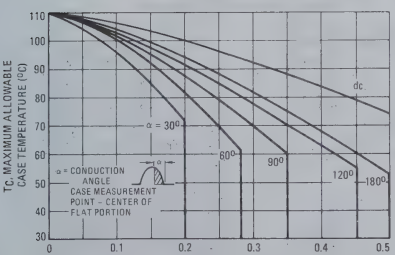
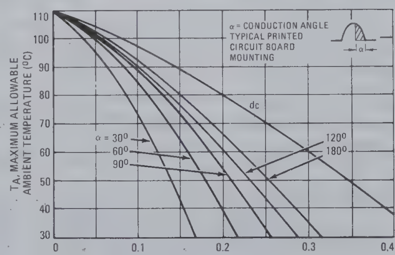
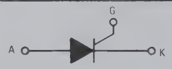


FIGURE 2 – CURRENT DERATING (REFERENCE: AMBIENT TEMPERATURE)



MCR201 thru MCR206

MOTOROLA



SILICON CONTROLLED RECTIFIERS

0.5 AMPERE RMS
15–200 VOLTS

REVERSE BLOCKING TRIODE THYRISTORS

. . . Annular PNPN devices designed for industrial/military applications such as relay and lamp drivers, small motor controllers and drivers for larger thyristors, and in sensing and detection circuits.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 100 μA Maximum, T_C = 125°C
- Low Holding Current – 5.0 mA Maximum
- Passivated Surface for Reliability and Uniformity
- TO-18 Hermetically Sealed Metal Package

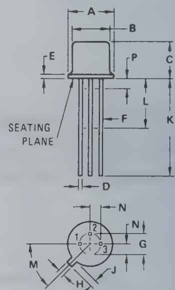
2.3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Off-State and Reverse Voltage	V_{DRM} V_{RRM}		Volts
MCR201		15	
MCR202		30	
MCR203		60	
MCR204		100	
MCR205		150	
MCR206		200	
RMS On-State Current (All Conduction Angles)(See Figs. 4 & 5)	$I_{T(RMS)}$	0.5	Amp
Peak Non-Repetitive Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	6.0	Amp
Circuit Fusing Considerations, (t = 1.0 to 8.3 ms)	I^2t	0.15	A^2s
Peak Forward Gate Power	P_{GM}	0.1	Watt
Average Forward Gate Power	$P_{GF(AV)}$	0.01	Watt
Peak Forward Gate Current (300 μs, 120 PPS)	I_{GFM}	1.0	Amp
Peak Reverse Gate Voltage	V_{GRM}	4.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	150	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	400	°C/W



STYLE 6:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E	–	0.762	–	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC notes and dimensions apply.

CASE 22-03
(TO-18)

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C)		I_{DRM}	–	100	µA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C)		I_{RRM}	–	100	µA
Peak On-State Voltage (I_{TM} = 1.2 A peak, lmS, Duty Cycle ≤ 1%)		V_{TM}	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 1) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C T_C = −65°C	I_{GT}	– –	200 350	µA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C T_C = −65°C T_C = 125°C	V_{GT}	– – 0.1	0.8 1.2 –	Volts
Holding Current (Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = 25°C T_C = −65°C	I_H	– –	5.0 10	mA

1. R_{GK} current is not included in measurement.

2.3

FIGURE 1 – CURRENT DERATING (REFERENCE: CASE TEMPERATURE)

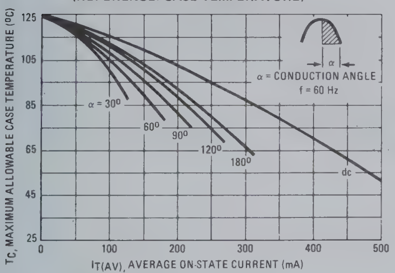


FIGURE 2 – POWER DISSIPATION

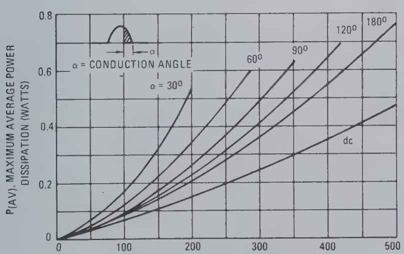


FIGURE 3 – FORWARD VOLTAGE

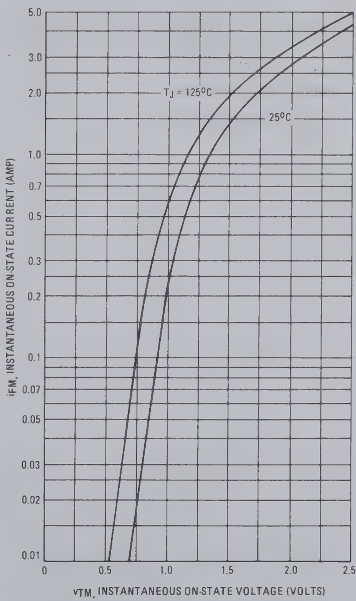


FIGURE 4 — SURGE RATINGS

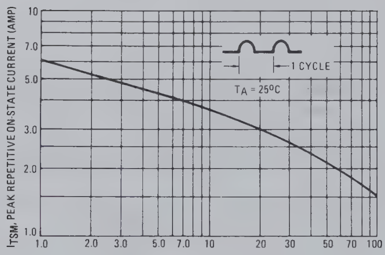
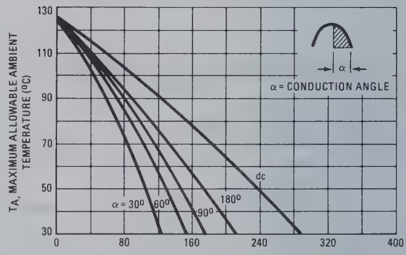
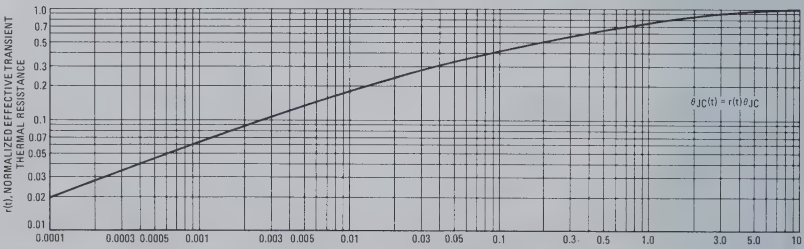


FIGURE 5 — CURRENT DERATING (REFERENCE: AMBIENT TEMPERATURE)



2.3

FIGURE 6 — THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 7 — GATE TRIGGER VOLTAGE

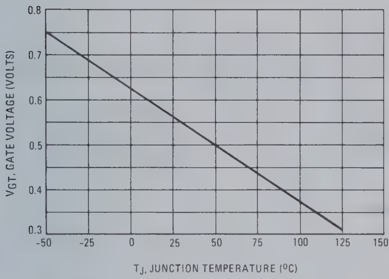


FIGURE 8 — GATE TRIGGER CURRENT

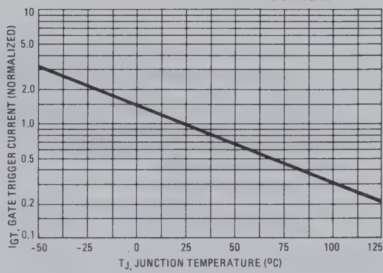
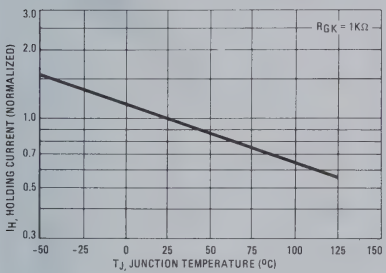


FIGURE 9 — HOLDING CURRENT



2.3

MCR218 Series

MOTOROLA

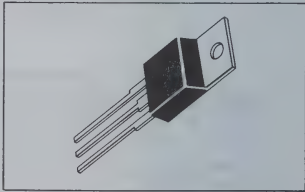
SILICON-CONTROLLED RECTIFIERS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass-Passivated Junctions
- Blocking Voltage to 800 Volts
- TO-220 Construction — Low Thermal Resistance, High Heat Dissipation and Durability

THYRISTORS

8 AMPERES RMS
50-800 VOLTS



2.3

MAXIMUM RATINGS

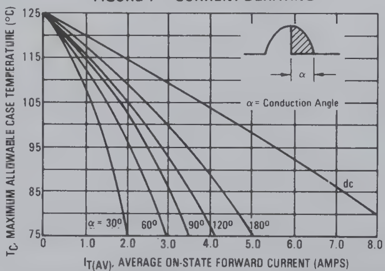
Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage Repetitive Peak Reverse Voltage MCR218-2 -3 -4 -5 -6 -7 -8 -9 -10	V_{RRM} V_{DRM}	 50 100 200 300 400 500 600 700 800	Volts
Forward Current RMS (All Conduction Angles)	$I_{T(RMS)}$	8.0	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz)	I_{TSM}	80	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	34	A^2s
Forward Peak Gate Power	P_{GM}	5.0	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

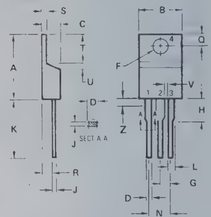
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

FIGURE 1 — CURRENT DERATING





NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION. INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

CASE 221A-02
TO-220 AB

All JEDEC dimensions and notes apply.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Rated V_{DRM}, T_J = 125°C)	I_{DRM}	—	—	2.0	mA
Peak Reverse Blocking Current (Rated V_{RRM}, T_J = 125°C)	I_{RRM}	—	—	2.0	mA
Peak On-State Voltage (1) (I_{TM} = 16 A Peak)	V_{TM}	—	1.5	1.8	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ohms)	I_{GT}	—	10	25	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ohms) (Rated V_{DRM}, R_L = 1000 Ohms, T_J = 125°C)	V_{GT}	 — 0.2	 — —	 2.5 —	Volts
Holding Current (Anode Voltage = 24 Vdc, Peak Initiating On-State Current = 0.5 A, 0.1 to 10 ms Pulse, Gate Trigger Source = 7.0 V, 20 Ohms)	I_H	—	16	30	mA
Critical Rate of Rise of Off-State Voltage (Rated V_{DRM}, Exponential Waveform, Gate Open, T_J = 125°C)	dv/dt	100	—	—	V/μs
Maximum Rate of Change of On-State Current (Rated V_{DRM}, I_{TM} = 16 A Peak, I_{GT} = 100 mA, T_J = 125°C)	di/dt	—	100	—	A/μs

(1) Pulse Test: Pulse Width = 1.0 ms, Duty Cycle ≤ 2%.

2.3

FIGURE 2 — ON-STATE POWER DISSIPATION

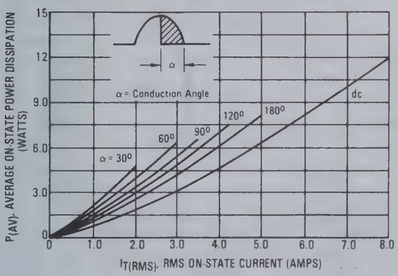


FIGURE 3 — NORMALIZED GATE TRIGGER CURRENT

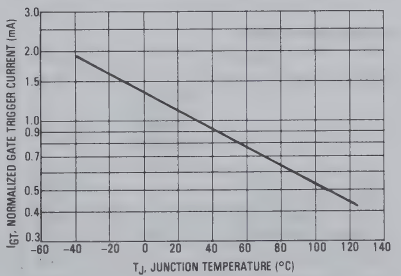


FIGURE 4 — NORMALIZED GATE TRIGGER VOLTAGE

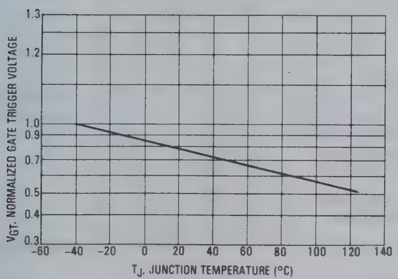
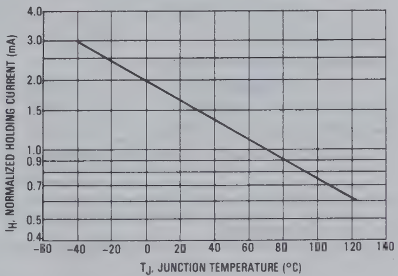


FIGURE 5 — NORMALIZED HOLDING CURRENT



MCR264-4
thru
MCR264-12

MOTOROLA

40 AMPERES RMS*
SILICON CONTROLLED RECTIFIERS

. . . designed for back-to-back SCR output devices for solid state relays or applications requiring high surge operation.

- Photo Glass Passivated Blocking Junctions for High Temperature Stability, Center Gate for Uniform Parameters
- 400 Amperes Surge Capability
- Blocking Voltage to 1000 Volts

2.3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (1)	V_{RRM}		Volts
MCR264-4		200	
MCR264-6		400	
MCR264-8		600	
MCR264-10		800	
MCR264-12		1000	
Forward Current (T_C = 80°C) (All Conduction Angles)	$I_{T(RMS)}$ $I_{T(AV)}$	40* 25*	Amps
Peak Nonrepetitive Surge Current — 8.3 ms (1/2 Cycle, Sine Wave) 1.5 ms	I_{TSM}	400 450	Amps
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watts
Forward Peak Gate Current (300 μs, 120 PPS)	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C

THERMAL CHARACTERISTICS

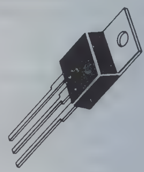
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

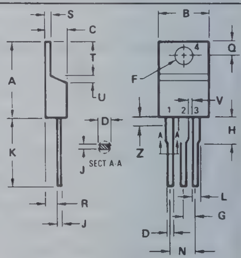
(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

*This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat sinking when the device is to be used at high sustained currents. (See Figure 1 for maximum case temperatures.)

THYRISTORS

40 AMPERES RMS*
200-1000 VOLTS





NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3
3 DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
5 CONTROLLING DIMENSION INCH

STYLE 3
PIN 1 CATHODE
2 ANODE
3 GATE
4 ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220AB

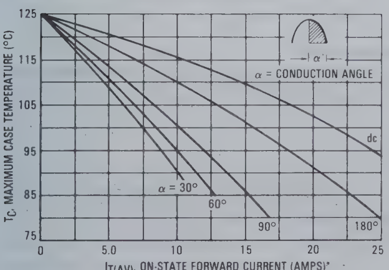
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_J = 125°C)	MCR264-4	V_{DRM}	200	—	—	Volts
	MCR264-6		400	—	—	
	MCR264-8		600	—	—	
	MCR264-10		800	—	—	
	MCR264-12		1000	—	—	
Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)		I_{DRM}	—	—	2.0	mA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)		I_{RRM}	—	—	2.0	mA
Forward "On" Voltage (1) (I_{TM} = 80 A)		V_{TM}	—	1.6	2.0	Volts
Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		I_{GT}	—	15	50	mA
(T_C = −40°C)			—	30	90	
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		V_{GT}	—	1.0	1.5	Volts
Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)		V_{GD}	0.2	—	—	Volts
Holding Current (Anode Voltage = 12 Vdc)		I_H	—	30	60	mA
Turn-On Time (I_{TM} = 40 A, I_{GT} = 60 mAdc)		t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (Gate Open, Rated V_{DRM}, Exponential Waveform)		dv/dt	—	50	—	V/μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

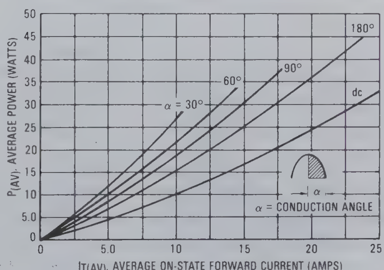
2.3

FIGURE 1 — AVERAGE CURRENT DERATING



*This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat sinking when the device is to be used at high sustained currents.

FIGURE 2 — MAXIMUM ON-STATE POWER DISSIPATION



2.3

FIGURE 3 — GATE TRIGGER CURRENT

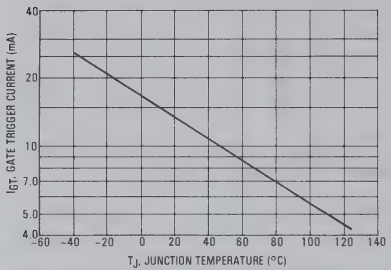


FIGURE 4 — NEW GATE TRIGGER VOLTAGE

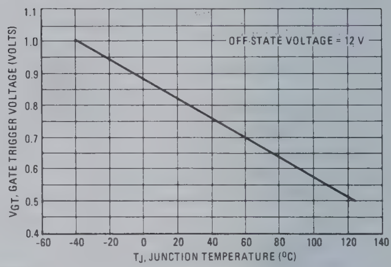


FIGURE 5 — HOLDING CURRENT

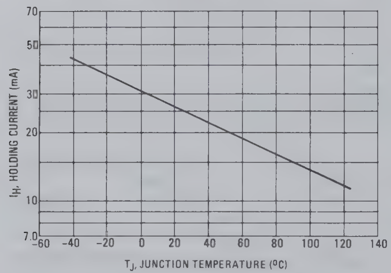


FIGURE 6 — TYPICAL FORWARD VOLTAGE

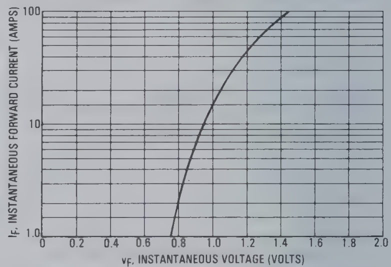
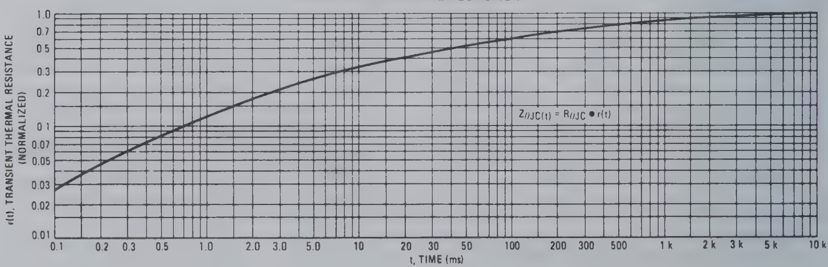


FIGURE 7 — THERMAL RESPONSE



MOTOROLA

MCR265-2 thru MCR265-10

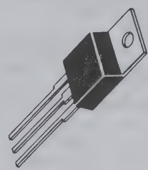
55 AMPERES RMS* SILICON CONTROLLED RECTIFIERS

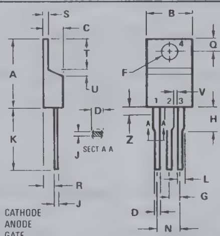
. . . designed for inverse parallel SCR output devices for solid state relays, welders, battery chargers, motor controls or applications requiring high surge operation.

- Photo Glass Passivated Blocking Junctions for High Temperature Stability, Center Gate for Uniform Parameters
- 550 Amperes Surge Capability
- Blocking Voltage to 800 Volts

THYRISTORS

55 AMPERES RMS*
50-800 VOLTS





STYLE 3:
PIN 1 CATHODE
2 ANODE
3. GATE
4. ANODE

NOTES:
1. DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3
3 DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5 CONTROLLING DIMENSION INCH

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (1)	V_{RRM}		Volts
MCR265-2		50	
MCR265-4		200	
MCR265-6		400	
MCR265-8		600	
MCR265-10		800	
Forward Current (T_C = 70°C) (All Conduction Angles)	$I_{T(RMS)}$ $I_{T(AV)}$	55* 35*	Amps
Peak Nonrepetitive Surge Current — 8.3 ms (1/2 Cycle, Sine Wave)	I_{TSM}	550	Amps
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watts
Forward Peak Gate Current (300 μs, 120 PPS)	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.9	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage

* This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat sinking when the device is to be used at high sustained currents (See Figure 1 for maximum case temperatures.)

2.3

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_J = 125°C)	MCR265-2	V_{DRM}	50	—	—	Volts
	MCR265-4		200	—	—	
	MCR265-6		400	—	—	
	MCR265-8		600	—	—	
	MCR265-10		800	—	—	
Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)		I_{DRM}	—	—	2.0	mA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)		I_{RRM}	—	—	2.0	mA
Forward "On" Voltage (1) (I_{TM} = 110 A)		V_{TM}	—	1.5	1.9	Volts
Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		I_{GT}	—	20	50	mA
(T_C = −40°C)			—	40	90	
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		V_{GT}	—	1.0	1.5	Volts
Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)		V_{GD}	0.2	—	—	Volts
Holding Current (Anode Voltage = 12 Vdc)		I_H	—	30	75	mA
Turn-On Time (I_{TM} = 55 A, I_{GT} = 200 mAdc)		t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (Gate Open, Rated V_{DRM}, Exponential Waveform)		dv/dt	—	50	—	V/μs

(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤ 2%.

FIGURE 1 — AVERAGE CURRENT DERATING

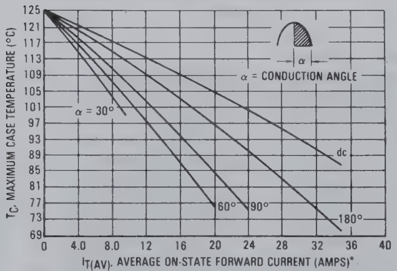
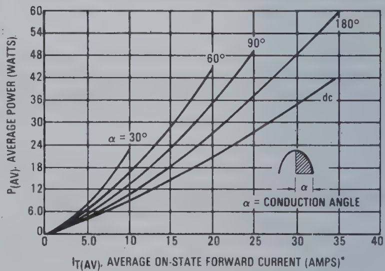


FIGURE 2 — MAXIMUM ON-STATE POWER DISSIPATION



*This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat sinking when the device is to be used at high sustained currents.

FIGURE 3 — GATE TRIGGER CURRENT

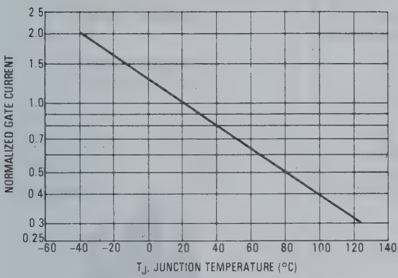
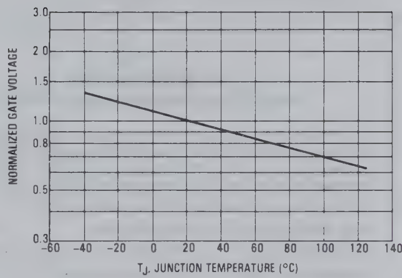


FIGURE 4 — GATE TRIGGER VOLTAGE



2.3

FIGURE 5 — HOLDING CURRENT

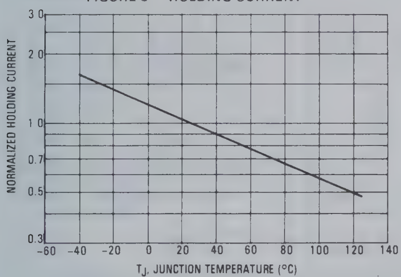


FIGURE 6 — ON-STATE CHARACTERISTICS

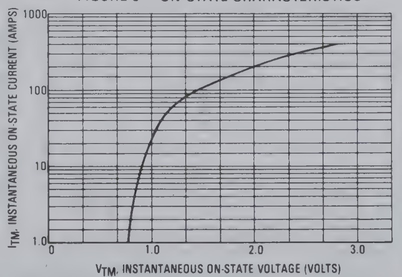
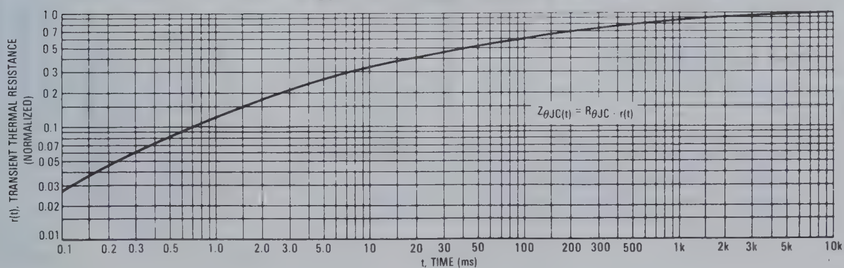


FIGURE 7 — THERMAL RESPONSE



MCR525-4
thru
MCR525-10

MOTOROLA

2.3

THYRISTORS

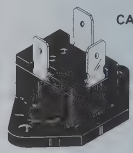
25 AMPERES RMS
200 – 800 VOLTS

25 AMPERES RMS
SILICON CONTROLLED RECTIFIERS

. . . designed for ac control applications requiring large numbers of power cycles and ease of connection. The overmold package is an existing TO-220 device with fast-on connectors welded in place. The plastic body is molded over the TO-220 for TO-3 type mounting and UL requirements.

- Most Reliable UL Oriented Package
- Cost Reduces All New Pressfit and Isolated Stud Designs
- Fast-On Connectors for Easy Assembly
- Terminals Notched for "Wire Wrap" or Solder Connection
- Externally Isolated with Mica (part number B52600 F016)

CASE 342-01



MAXIMUM RATINGS

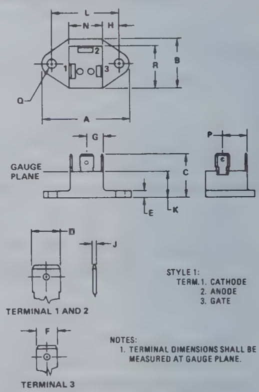
Rating (Note 1)	Symbol	Value	Unit
Peak Reverse Blocking Voltage (1)	V_{RRM} or V_{DRM}		Volts
MCR525-4		200	
-5		300	
-6		400	
-7		500	
-8		600	
-9		700	
-10		800	
RMS On-State Current (T_C = 85°C) (T_M = 70°C with Mica Insulator)	$I_{T(RMS)}$	25	Amps
Peak Non-Repetitive Surge Current – 8.3 ms (1/2 Cycle, Sine Wave) 1.5 ms	I_{TSM}	300 350	Amps
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Mounting Torque (Note 2)	—	6	in.lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

Note 1. Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltages, such that the voltage applied exceeds the rated blocking voltage at room temperature (≈ 25°C)

Note 2. Insert greased external isolator between the plastic TO-3 type base and heat sink. Secure with two 6 x 32 screws, lock washers and nuts. Tighten to 6-inch pound torque maximum for best heat transfer, lowest mechanical stress, and highest reliability.



STYLE 1:
TERM. 1. CATHODE
2. ANODE
3. GATE

NOTES:
1. TERMINAL DIMENSIONS SHALL BE MEASURED AT GAUGE PLANE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.62	1.510	1.560
B	21.85	24.38	0.860	0.960
C	22.86	25.40	0.900	1.000
D	6.28	6.42	0.247	0.253
E	2.80	4.06	0.110	0.160
F	4.68	4.82	0.184	0.190
G	6.86	8.12	0.270	0.320
H	7.24	8.00	0.285	0.315
J	0.79	0.83	0.031	0.033
K	14.48	15.49	0.570	0.610
L	29.85	30.35	1.175	1.195
N	14.48	15.49	0.570	0.610
P	10.67	12.19	0.420	0.480
Q	3.81	4.19	0.150	0.165
R	17.78	19.30	0.700	0.760

CASE 342-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (1)	MCR525-4	V_{DRM}	200	—	—	Volts
	-5		300	—	—	
	-6		400	—	—	
	-7		500	—	—	
	-8		600	—	—	
	-9		700	—	—	
	-10		800	—	—	
Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)		I_{DRM}	—	—	2	mA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)		I_{RRM}	—	—	2	mA
Forward "On" Voltage (1) (I_{TM} = 50 A)		V_{TM}	—	—	2.0	Volts
Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		I_{GT}	—	—	40	mA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		V_{GT}	—	1	1.5	Volts
Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)		V_{GD}	0.2	—	—	Volts
Holding Current (Anode Voltage = 12 Vdc)		I_H	—	—	40	mA
Turn-On Time (I_{TM} = 25 A, I_{GT} = 50 mAdc)		t_{gt}	—	1.5		μs
Turn-Off Time (V_{DRM} = rated voltage)		t_q				μs
(I_{TM} = 25 A, I_R = 25 A)			—	15	—	
(I_{TM} = 25 A, I_R = 25 A, T_J = 125°C)			—	35	—	
Critical Rate of Rise of Off-State Voltage (Gate Open, Rated V_{DRM}, Exponential Waveform)		dv/dt	—	50	—	V/μs

(1) Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%

FIGURE 1 — HOLDING CURRENT

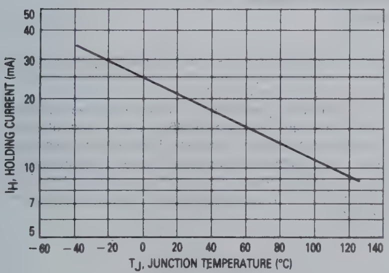
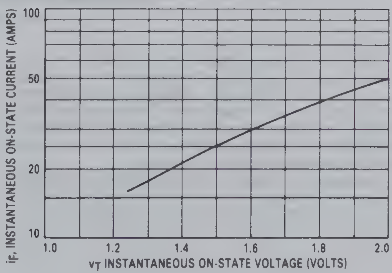


FIGURE 2 — MAXIMUM FORWARD VOLTAGE



2.3

FIGURE 3 — RMS CURRENT DERATING

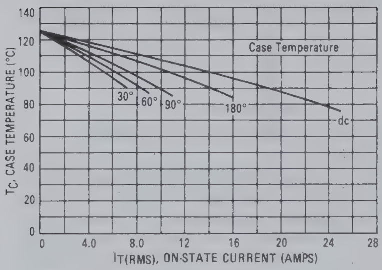


FIGURE 4 — MAXIMUM ON-STATE POWER DISSIPATION

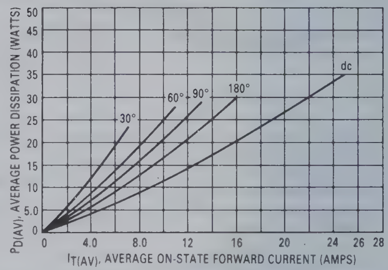


FIGURE 5 — GATE TRIGGER CURRENT

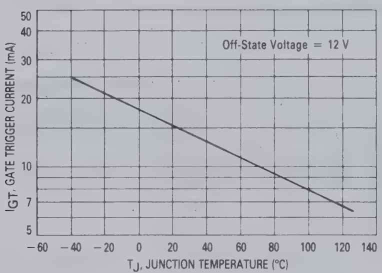
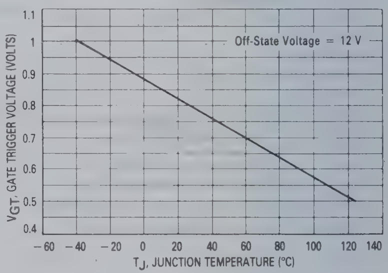


FIGURE 6 — GATE TRIGGER VOLTAGE



MECHANICAL CONSTRUCTION OF POWER THYRISTOR PACKAGES FOR SWITCHING APPLICATIONS

Thyristors replace relays for reasons of maintenance, space, and cost effectiveness. It is imperative that the mechanical construction of thyristors be consistent with these goals. The overmold package is the state-of-the-art realization of the above, backed by an instant performance record from years of development in the TO-220 package.

Motorola has power-cycled TO-220 devices 110,000 times at 15 amperes with only one failure (see report R 79-8A) and power-cycled the overmold 40,000 times, successfully. Tests for temperature cycle, temperature storage, thermal shock, moisture resistance, and vibration, also passed.

The internal construction of the overmold package (Figure 7) has only one layer of 95/5 solder, and inherent chip-to-heat spreader, interface. Internally isolated devices (Figure 8) must have several layers of solder, including soft solder around the isolator. Typically, the solder layers will fail, as the number of power cycles are increased.

FIGURE 7 — EXTERNALLY ISOLATED DEVICE

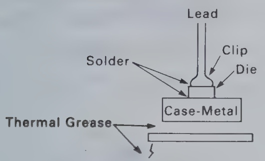
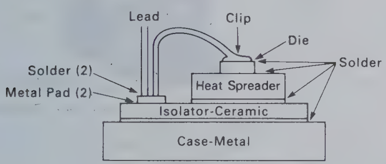
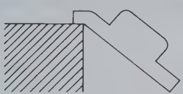


FIGURE 8 — TYPICALLY ISOLATED DEVICE



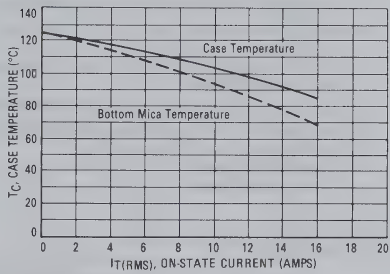
The overmold package is stronger than aluminum and equal to the steel TO-3 package in bending moment (Figure 9). The plastic flange eliminates isolation hardware and prevents screw-burr shorts through the isolator. The phenolic plastic meets UL flammability requirements and is designed for UL voltage spacing requirements.

FIGURE 9 — BENDING MOMENT



Comparison of the current handling capability of internally isolated devices can be done on the dashed line of Figure 10. The equivalent position (dashed line) is the same as the heat sink temperature (T_C) of the internally isolated device.

FIGURE 10 — RMS CURRENT DERATING



For externally isolated package:

R_θTotal = R_θChip + R_θSolder + R_θHeader + R_θGrease + R_θIsolator + R_θGrease + R_θHeatsink

For internally isolated package:

R_θTotal = R_θChip + R_θSolder (1) + R_θHeat Spreader + R_θSolder (2) + R_θIsolator + R_θSolder (3) + R_θHeader + R_θGrease + R_θHeatsink

The same power and the same heatsink will give higher T_C externally isolated than T_C internally isolated because of their relative position in the thermal equation. Both parts will have the same T_J.

2.3

MCR568
(12 Amperes RMS)
MCR569
(25 Amperes RMS)

MOTOROLA

Advance Information

SILICON-CONTROLLED RECTIFIERS

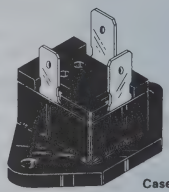
. . . designed for overvoltage protection in crowbar circuits.

- Glass-Passivated Junctions for Greater Parameter Stability and Reliability
- Center-Gate Geometry for Uniform Current Spreading Enabling High Discharge Current
- Externally Isolated with Mica Part Number B52600F016
- Cost Reduces All New Pressfit and Isolated Stud Designs
- High Capacitor Discharge Current
  300 Amps (MCR568)
  750 Amps (MCR569)

2.3

SILICON-CONTROLLED CROWBAR RECTIFIERS

25 thru 400 VOLTS



Case 342-01

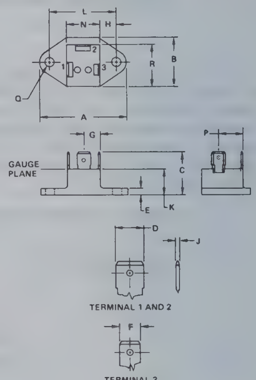
MAXIMUM RATINGS

Rating	Symbol	MCR568 Value	MCR569 Value	Unit
Repetitive Peak Forward or Reverse Blocking Voltage (Note 1) MCR568, 569 -1	V_{DRM} or V_{RRM}	← 25 →		Volts
-2		← 50 →		
-3		← 100 →		
-6		← 400 →		
Peak Discharge Current (Note 2)	I_{TM}	300	750	Amps
On-State Current (T_C = 85°C) (1/2 Cycle, Sine Wave, 60 Hz)	$I_{T(RMS)}$ $I_{T(AV)}$	12 8	25 16	Amps
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	100	300	Amps
Circuit Fusing ($t \leqslant 8.3$ ms)	I^2t	40	375	A^2s
Critical Rate-of-Rise of Current (Note 3)	di/dt	75	100	A/μs
Peak Gate Current ($t \leqslant 2.0\ \mu s$)	I_{GM}	2.0		Amps
Peak Gate Power ($t \leqslant 2.0\ \mu s$)	P_{GM}	20		Watts
Average Gate Power	$P_{G(AV)}$	0.5		Watt
Operating Junction Temperature Range	T_J	-40 to +125		°C
Storage Temperature Range	T_{stg}	-40 to +150		°C
Mounting Torque	—	6	6	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	MCR568	MCR569	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.0	1.5	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	← 60 →		°C/W

NOTES:
1. V_{DRM} for all types can be applied on a continuous basis without damage. Ratings apply for open or shorted gate conditions or negative voltage on the gate. Devices should not be tested for blocking voltage such that the supply voltage exceeds the rating of the device.
2. Ratings apply for t_w = 1.0 ms. t_w is defined as 5 time constants of an exponentially decaying current pulse.
3. Test Conditions: I_G = 150 mA, V_D = Rated V_{DRM}, I_{TM} = Rated Value, T_J = 125°C.



STYLE 1
TERM 1 CATHODE
2 ANODE
3. GATE

NOTES.
1. TERMINAL DIMENSIONS SHALL BE MEASURED AT GAUGE PLANE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.62	1.510	1 560
B	21.85	24.38	0 860	0.960
C	22.86	25 40	0.900	1.000
D	6.28	6.42	0.247	0.253
E	2.80	4 06	0 110	0.160
F	4.68	4.82	0.184	0.190
G	6.86	8 12	0 270	0.320
H	7 24	8.00	0.285	0.315
J	0.79	0.83	0.031	0.033
K	14.48	15.49	0.570	0.610
L	29.85	30.35	1.175	1 195
N	14.48	15.49	0.570	0.610
P	10.67	12 19	0.420	0.480
Q	3.81	4.19	0 150	0.165
R	17.78	19.30	0.700	0.760

Case 342-01

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Note 1) (V_D = Rated V_{DRM}, T_J = 125=C)	I_{DRM}	—	—	2.0	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}, T_J = 125=C)	I_{RRM}	—	—	2.0	mA
Forward On-State Voltage	V_{TM}				Volts
(I_{TM} = 24 Amps) (Note 2) MCR568		—	—	2.2	
(I_{TM} = 50 Amps) (Note 2) MCR569		—	—	2.0	
(I_{TM} = 300 Amps, t_w = 1.0 ms) (Note 3) MCR568		—	6.0	—	
(I_{TM} = 750 Amps, t_w = 1.0 ms) (Note 3) MCR569		—	6.0	—	
Gate Trigger Current (V_D = 12 V, R_L = 100 Ω)	I_{GT}	2.0	7.0	30	mA
Gate Trigger Voltage	V_{GT}				Volts
(V_D = 12 V, R_L = 100 Ω)		—	0.65	1.5	
(V_D = Rated V_{DRM}, R_L = 1.0 kΩ, T_J = 125°C)		0.2	0.40	—	
Holding Current (I_{TM} = 100 mA, Gate-Open)	I_H	3.0	15	50	mA
Latching Current (V_D = 12 Vdc, I_G = 150 mA, $t_r \leqslant 50\ \mu s$)	I_L	—	—	60	mA
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Gate Open, Exponential Waveform, T_J = 125°C)	dv/dt	10	—	—	V/μs
Gate-Controlled Turn-On Time (Note 4) (V_D = Rated V_{DRM}, I_G = 150 mA)	t_{gt}				μs
(I_{TM} = 24 Amps, peak) MCR568		—	1.0	—	
(I_{TM} = 50 Amps, peak) MCR569		—	1.0	—	

NOTES:

1. V_{DRM} for all types can be applied on a continuous basis over the operating juction temperature range without incurring damage. Ratings apply for open or shorted gate conditions or negative voltage on the gate. Devices should not be tested for blocking voltage such that the supply voltage exceeds the rating of the device.
2. Pulse duration $\leqslant 300\ \mu s$, duty cycle $\leqslant 2\%$.
3. Ratings apply for t_w = 1.0 ms. t_w is defined at 5 time constants of an exponentially decaying current pulse.
4. The gate-controlled turn-on time in a crowbar circuit will be influenced by the circuit inductance.

MCR729-5
thru
MCR729-10

MOTOROLA

REVERSE BLOCKING TRIODE THYRISTOR

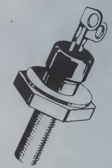
. . . fast switching, high-voltage Silicon Controlled Rectifiers especially designed for pulse modulator applications in radar and other similar equipment.

- High-Voltage: V_{DRM} = 300 to 800 Volts
- Turn-On Times: in Nanosecond Range
- Repetitive Pulse Current to 100 Amps
- Stable Switching Characteristics Over an Operating Temperature Range From −65 to +105°C
- Pulse Repetition Rates as High as 10,000 pps

2.3

SILICON CONTROLLED RECTIFIERS

5 AMPERES RMS
300–800 VOLTS

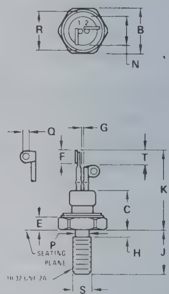


MAXIMUM RATINGS (T_J = 105°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Peak Repetitive Forward Blocking Voltage* (1)	V_{DRM}		Volts
MCR729-5		300	
-6		400	
-7		500	
-8		600	
-9		700	
-10		800	
Peak Repetitive Reverse Blocking Voltage (1)	V_{RRM}	50	Volts
Forward Current RMS	$I_{T(RMS)}$	5	Amps
Average Forward Power	$P_{F(AV)}$	5	Watts
Peak Repetitive On-State Control (PW = 10 μs)	I_{TRM}	100	Amps
Peak Forward Gate Power	P_{GFM}	20	Watts
Average Forward Gate Power	$P_{GF(AV)}$	1	Watt
Peak Forward Gate Current	I_{GFM}	5	Amps
Peak Forward Gate Voltage	V_{GFM}	10	Volts
Peak Reverse Gate Voltage	V_{GRM}	10	Volts
Operating Junction Temperature Range	T_J	−65 to +105	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque		15	in/lb

*Characterized for unilateral applications where reverse blocking capability is not important. Higher V_{ROM} rated units available on request.

(1) Ratings apply for zero or negative gate voltages. Devices shall not have a positive bias to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward and reverse blocking voltages such that the applied voltage exceeds the ratings.



STYLE 1.
PIN 1. CATHODE
2. GATE
STUD – ANODE

NOTE:
1. ALL RULES & NOTES ASSOCIATED WITH REFERENCED TO-64 OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	10.77	11.10	0.424	0.437
C	7.62	10.16	0.300	0.400
E	1.52	4.45	0.060	0.175
F	2.03	3.45	0.080	0.136
G	0.33	–	0.013	–
H	–	1.98	–	0.078
J	10.16	11.51	0.400	0.453
K	17.78	21.72	0.700	0.855
N	–	10.77	–	0.424
P	4.14	4.80	0.163	0.189
Q	1.02	1.91	0.040	0.075
R	10.16	–	0.400	–
S	4.212	4.310	0.1658	0.1697
T	1.52	–	0.060	–

CASE 63-03

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}, T_C = 105°C, gate open)	I_{DRM}	–	0.2	2	mA
Gate Trigger Current (Continuous dc) (V_D = 7 Vdc, R_L = 100 ohms)	I_{GT}	–	10	50	mAdc
Gate Trigger Voltage (Continuous dc) (V_D = 7 Vdc, R_L = 100 ohms)	V_{GT}	–	0.8	1.5	Volts
Holding Current (V_D = 7 Vdc, gate open)	I_H	3	15	–	mA
Forward On Voltage (I_{TM} = 5A, PW ≤ 1mS, Duty Cycle ≤ 1%)	V_{TM}	–	–	2.6	Volts
Dynamic Forward On Voltage (0.5 μs after 50% pt, I_G = 200 mA, V_D = Rated V_{DRM}, $i_{F(pulse)}$ = 30 Amps)	v_{TM}	–	15	25	Volts
Turn-On Time (t_d + t_r) (I_G = 200 mA, V_D = Rated V_{DRM})	t_{on}				ns
(i_{TM} = 30 Amps peak)		–	200	–	
(i_{TM} = 100 Amps peak)		–	400	–	
Turn-On Time Variation (T_C = +25°C to +105°C and −65°C to +25°C, i_{TM} = 30 A)	t_{on}	–	±500	–	ns
Pulse Turn-Off Time ($i_{F(pulse)}$ = 30 Amps, $I_{reverse}$ = 0) (Inductive charging circuit)	t_{rec}	–	15	–	μs
Forward Voltage Application Rate (Linear Rate of Rise) (V_D = Rated V_{DRM}, gate open, T_C = 105°C)	dv/dt	50	–	–	V/μs
Thermal Resistance (Junction to Case)	θ_{JC}	–	–	4	°C/W

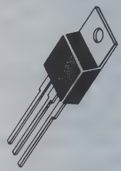
2.3

MCR1000
series

MOTOROLA

TMOS

THYRISTORS
15 AMPERES RMS
200-400-600 VOLTS
ASYMMETRICAL

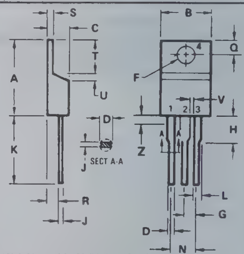


SILICON CONTROLLED RECTIFIERS

. . . designed primarily for very high speed switching, high current pulse applications — laser modulators, printers, florescent lighting, switching power supplies and particle accelerators.

- Asymmetrical Blocking Voltage To 600 V
- Very High dv/dt - 1000 V/μs @ T_J = 125°C*
- Very Fast Switching - t_q @ T_J = 25°C, 8.0 μs Max
- Technology Leadership TMOS SCR
- For More Information See EB-103

2.3



NOTES
1. DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
5. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

CASE 221A-02
TO-220 AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Forward Blocking Voltage MCR1000-4 MCR1000-6 MCR1000-8	V_{DRM}	 200 400 600	Volts
Forward Current RMS (T_C = 25°C) (All Conduction Angles)	$I_{T(RMS)}$	15	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz) T_J = 125°C)	I_{TSM}	90	Amps
Circuit Fusing Considerations (T_J = 0 to +125°C, t = 1.0 to 8.3 ms)	I^2t	34	A^2s
Peak Gate Voltage	V_{GM}	±20	Volts
Forward Peak Gate Current	I_{GM}	1.5	Amps
Operating Junction Temperature Range	T_J	-0 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W

*$R_{GK} \leqslant$ 50K ohms required

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)	I_{DRM}	—	—	2.0	mA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)	I_{RRM}	—	—	2.0	mA
Peak Reverse Blocking Voltage	V_{RRM}	—	—	100	Volts
Forward "On" Voltage (I_{TM} = 20 A Peak)	V_{TM}	—	3.5	4.0	Volts
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)	V_{GT}	—	2.0	2.5	Volts
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)	V_{GD}	0.2	—	—	Volts
Holding Current (Anode Voltage = 12 Vdc)	I_H	—	10	40	mA
Turn-On Time (See Figure 6)	t_{gt}	—	—	200	ns
Turn-Off Time (V_{DRM} = rated voltage) (I_{TM} = 3.0 A, I_R = 2.0 A, dv/dt = 100 V/μs)	t_q	—	6.0	8.0	μs
Forward Voltage Application Rate (T_J = 125°C, R_{GK} ≤ 200 Ω) (See Figure 7)	dv/dt	1000	—	—	V/μs
Maximum Rate of Change of On State Current (Rated V_{DRM}, I_{TM} = 20 A peak, T_J = 125°C)	di/dt	—	—	100	A/μs

2.3

FIGURE 1 — AVERAGE CURRENT DERATING

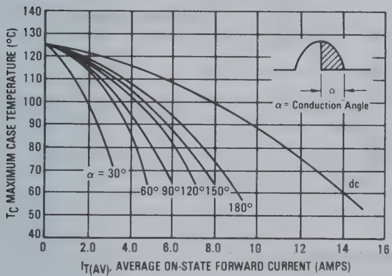


FIGURE 2 — MAXIMUM ON-STATE POWER DISSIPATION

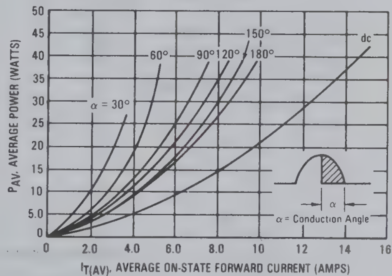


FIGURE 3 — TYPICAL GATE TRIGGER VOLTAGE

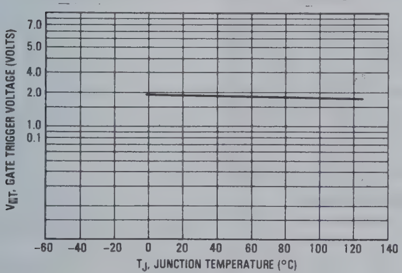


FIGURE 4 — TYPICAL HOLDING CURRENT

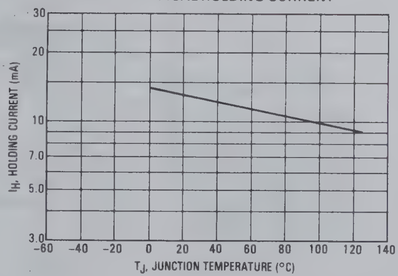


FIGURE 5 — THERMAL RESPONSE

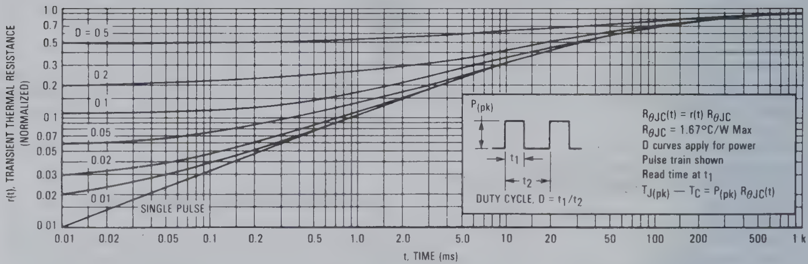


FIGURE 6 — MCR1000 SERIES TYPICAL TURN-ON CIRCUIT WITH CMOS GATING

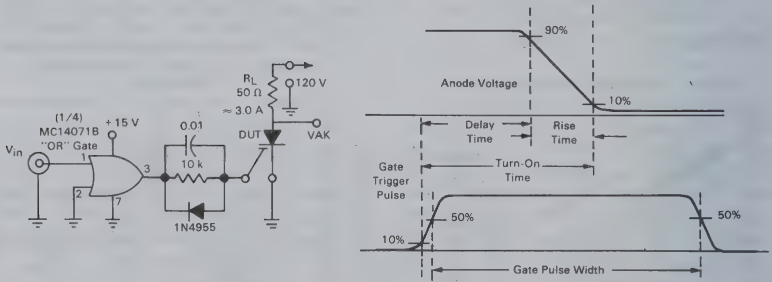
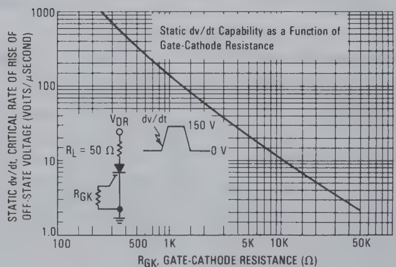


FIGURE 7 — TYPICAL dv/dt CAPABILITY



MOTOROLA

MCR1718-5 thru MCR1718-8

REVERSE BLOCKING TRIODE THYRISTOR

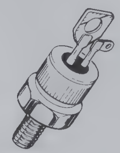
. . . fast switching, high-voltage thyristors especially designed for pulse modulator applications.

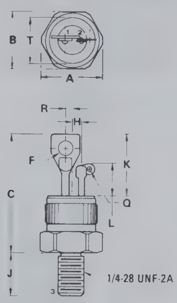
- High-Voltage Capability from 300 to 600 Volts
- Repetitive Pulse Current to 1000 Amp
- Pulse Repetition as High as 4000 pps
- Current Application Rate as High as 1000 A/μs

SILICON CONTROLLED RECTIFIER

25 AMPERES RMS
300 thru 600 VOLTS

2.3





STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Forward or Reverse Blocking Voltage * MCR1718-5 -6 -7 -8	V_{DRM} V_{RRM}	300 400 500 600	Volts
Peak Reverse Blocking Voltage (Transient) (Non-Recurrent 5 ms (max) MCR1718-5 -6 -7 -8	V_{RSM}	400 500 600 700	Volts
Forward Current RMS	$I_{T(RMS)}$	25	Amp
Peak Forward Surge Current (1-10 μs Pulse Width)	I_{TSM}	1000	Amp
Current Application Rate (up to 1000 A peak)	di/dt	1000	A/μs
Circuit Fusing (T_J = −65 to +125°C; t ≦ 1.0 ms	I^2t	250	A^2s
Dynamic Average Power (T_C = 65°C)	$P_{F(AV)}$	30	Watts
Peak Gate Power - Forward	P_{GM}	20	Watts
Average Gate Power - Forward	$P_{G(AV)}$	1.0	Watt
Peak Gate Current - Forward	I_{GM}	5.0	Amp
Peak Gate Voltage	V_{GM}	10	Volts
Operating Junction Temperature Range	T_J	−65 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque	—	30	in.-lb

*V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage.
Ratings apply for zero or negative gate voltage.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Units
Peak Forward Blocking Current (V_D = Rated V_{DRM} with gate open, T_J = 125°C)	I_{DRM}	–	–	8.0	mA
Peak Reverse Blocking Current (V_D = Rated V_{RRM} with gate open, T_J = 125°C)	I_{RRM}	–	–	8.0	mA
Forward "On" Voltage (I_{TM} = 25 Adc)	V_{TM}	–	1.1	1.3	Volts
Dynamic Forward On Voltage (I_{GT} = 500 mA, I_{pulse} = 500 Amps) (1.0 μs after start (10% pt.) of I_{pulse}) (5.0 μs after start (10% pt.) of I_{pulse})	V_{TM}	– –	30 5.0	– –	
Gate Trigger Current (Continuous dc) (V_D = 7Vdc, R_L = 50 Ohms)	I_{GT}	–	10	50	mA
Gate Trigger Voltage (Continuous dc) (V_D = 7 Vdc, R_L = 50 Ohms) (V_D = Rated V_{DRM}, R_L = 50 Ohms, T_J = 125°C)	V_{GT} V_{GD}	– 0.25	0.8 –	1.5 –	Volts
Holding Current (V_D = 7.0 Vdc, Gate Open) (V_D = 7.0 Vdc, Gate Open, T_J = 125°C)	I_H	5.0 –	15 6.0	– –	mA
Circuit Commutated Turn-Off Time (I_F = 500 A, I_R = 10 A, dv/dt = 20 V/μs V_D = Rated V_{DRM}, V_R = Rated V_{RRM}) (Conductive Charging Circuit — Circuit dependent)	t_q	–	20	–	μs
Critical Exponential Rate of Rise (Gate Open, T_J = 125°C, V_D = Rated V_{DRM})	dv/dt	–	100	–	V/μs

(1) V_{DRM} for all types can be supplied on a continuous dc basis without incurring damage.
Ratings apply for zero or negative gate voltage.

MOTOROLA

MCR1906-1 thru MCR1906-8

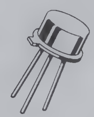
REVERSE BLOCKING TRIODE THYRISTORS

These devices are glassivated planar construction designed for applications in control systems and sensing circuits where low-level gating and holding characteristics are necessary.

- Low-Level Gate Characteristics — I_{GT} = 1.0 mA (Max) @ T_C = 25°C
- Low Holding Current — I_H = 5.0 mA (Max) @ T_C = 25°C
- Glass-to-Metal Bond for Maximum Hermetic Seal

SILICON CONTROLLED RECTIFIERS

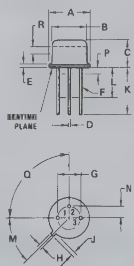
1.6 AMPERES RMS
25 thru 400 VOLTS



2.3

MAXIMUM RATINGS (T_J = 100°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Repetitive Peak Reverse Blocking Voltage	V_{RRM}		Volts
MCR1906-1		25	
MCR1906-2		50	
MCR1906-3		100	
MCR1906-4		200	
MCR1906-5		300	
MCR1906-6		400	
MCR1906-7		500	
MCR1906-8		600	
RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	1.6	Amp
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz, T_J = −40 to +110°C) Preceded and followed by rated current and voltage	I_{TSM}	15	Amp
Peak Gate Power	P_{GM}	0.1	Watt
Average Gate Power	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current	I_{GM}	0.1	Amp
Peak Gate Voltage	V_{GM}	6.0	Volt
Operating Junction Temperature Range	T_J	−65 to +110	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Solder Temperature (>1/16″ From Case, 10 s max.)	–	+230	°C



STYLE 3
PIN 1. CATHODE
2. GATE
3. ANODE (CONNECTED TO CASE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.
CASE 79-02
TO-39

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (R_{GK} = 1000 Ohms)	V_{DRM}				Volt
MCR1906-1		25	–	–	
MCR1906-2		50	–	–	
MCR1906-3		100	–	–	
MCR1906-4		200	–	–	
MCR1906-5		300	–	–	
MCR1906-6		400	–	–	
MCR1906-7		500			
MCR1906-8		600			
Peak Forward Blocking Current (Rated V_{DRM}, R_{GK} = 1000 Ohms, T_J = 110°C)	I_{DRM}	–	–	500	µA
Peak Reverse Blocking Current (Rated V_{RRM}, R_{GK} = 1000 Ohms, T_J = 110°C)	I_{RRM}	–	–	500	µA
Peak On-State Voltage (Pulsed, 1.0 ms max, Duty Cycle ≤ 1.0%) (I_F = 1.0 Adc peak)	V_{TM}	–	–	1.75	Volt
Gate Trigger Current (Continuous dc) (V_{AK} = 7.0 V, R_L = 100 ohms)	I_{GT}	–	–	1.0	mAdc
Gate Trigger Voltage (Continuous dc) (V_{AK} = 7.0 V, R_L = 100 ohms)	V_{GT}	–	–	1.0	Volt
(V_{AK} = Rated V_{DRM}, R_L = 100 ohms, R_{GK} = 1000 Ohms, T_J = 110°C)		0.1	–	–	
Holding Current (V_{AK} = 7.0 V, R_{GK} = 1000 ohms)	I_H	–	–	5.0	mA
Turn-On Time	t_{gt}				µs
(I_{GT} = 10 mA, I_F = 1.0 A)		–	0.8	–	
(I_{GT} = 20 mA, I_F = 1.0 A)		–	0.6	–	
Turn-Off Time (I_F = 1.0 A, I_R = 1.0 A, dv/dt = 20 V/µs, T_J = 110°C)	t_q	–	10	–	µs

CURRENT DERATING

FIGURE 1 – CASE TEMPERATURE REFERENCE

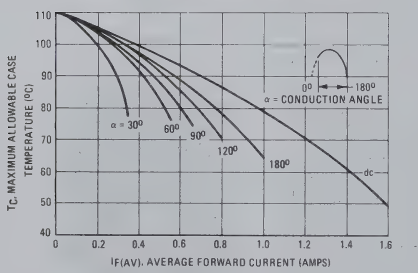
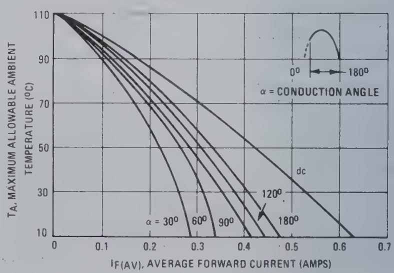


FIGURE 2 – AMBIENT TEMPERATURE REFERENCE



MCR2080, A series

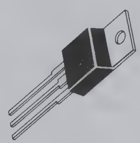
MOTOROLA

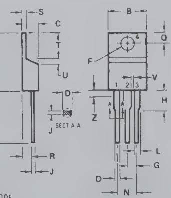
SILICON CONTROLLED RECTIFIERS

. . . designed primarily for high speed inverter and converter applications — selected versions available for vertical deflection for TV circuits, computer terminals, medical monitors, and video games.

- $t_q < 6.0\ \mu s$ @ $I_F = 5.0$ Amps
- Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Blocking Voltage to 800 Volts

THYRISTORS
8.0 AMPERES RMS
200-800 VOLTS





STYLE 3
PIN 1 CATHODE
2 ANODE
3 GATE
4 ANODE

NOTES
1. DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4. DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
5. CONTROLLING DIMENSION INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14 60	15 75	0 575	0 620
B	9 65	10 29	0 380	0 405
C	4 06	4.82	0.160	0 190
D	0 64	0 89	0 025	0 035
F	3.61	3.73	0 142	0 147
G	2 41	2 67	0 095	0 105
H	2 79	3.93	0 110	0 155
J	0 36	0.56	0 014	0 022
K	12 70	14 27	0 500	0 562
L	1.14	1.39	0 045	0 055
N	4.83	5 33	0 190	0 210
Q	2 54	3 04	0 100	0 120
R	2 04	2 79	0.080	0 110
S	1.14	1.39	0 045	0.055
T	5.97	6 48	0 235	0 255
U	0.00	1 27	0 000	0 050
V	1.14	–	0.045	–
Z	–	2.03	–	0 080

CASE 221A-02
TO-220 AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage Peak Repetitive Reverse Voltage	V_{RRM}(1) V_{DRM}		Volts
MCR2080, A-4		200	
MCR2080, A-5		300	
MCR2080, A-6		400	
MCR2080, A-7		500	
MCR2080, A-8		600	
MCR2080, A-9		700	
MCR2080, A-10		800	
Forward Current RMS (All Conduction Angles)	$I_{T(RMS)}$	8.0	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz)	I_{TSM}	90	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	34	A^2s
Forward Peak Gate Power	P_{GM}	5.0	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watts
Forward Peak Gate Current	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

2.3

2.3

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Rated V_{DRM})	T_J = 125°C	I_{DRM}	—	—	3.0	mA
Peak Reverse Blocking Current (Rated V_{DRM})	T_J = 125°C	I_{RRM}	—	—	3.0	mA
Peak On-State Voltage (1)		V_{TM}				Volts
(I_{TM} = 10 A peak)		—	—	—	3.0	
(I_{TM} = 16 A Peak)		—	—	—	4.0	
Gate Trigger Current (Continuous dc) (V_D = 7.0 V, R_L = 100 Ω)		I_{GT}	—	—	50	mA
Gate Trigger Voltage (Continuous dc) (V_D = 7.0 V, R_L = 100 Ω)		V_{GT}	—	—	2.5	Volts
Holding Current (V_D = 7.0 V, R_L = 100 Ω)		I_H	—	—	100	mA
Turn-Off Time (V_{DRM} = Rated Voltage)		t_q				μs
(I_{TM} = 5.0 A, di/dt = 5.0 A/μs,	MCR2080		—	—	10	
Reapplied dv/dt = 50 V/μs)	MCR2080A		—	—	6.0	
Forward Voltage Application Rate		dv/dt	100	150	—	V/μs

(1) Pulse Test: Pulse Width = 1.0 ms, Duty Cycle ≤ 2%

FIGURE 1 — AVERAGE CURRENT DERATING

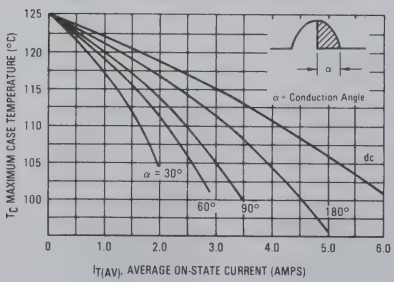


FIGURE 2 — ON-STATE POWER DISSIPATION

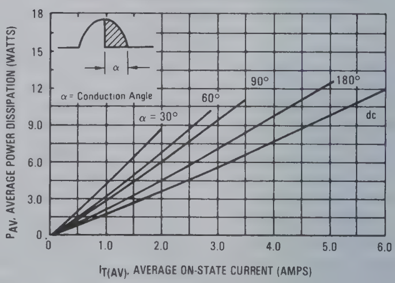


FIGURE 3 — TYPICAL GATE TRIGGER CURRENT

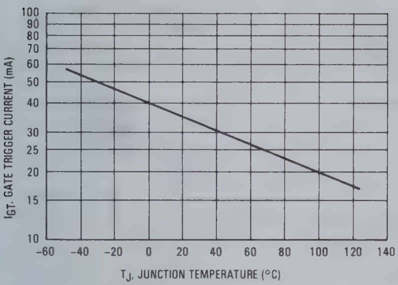
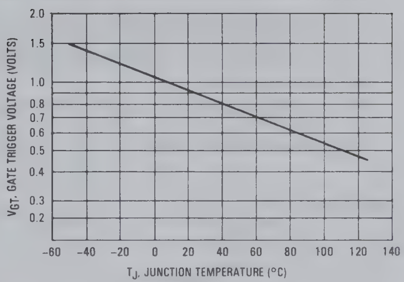


FIGURE 4 — TYPICAL GATE TRIGGER VOLTAGE



2.3

FIGURE 5 — TYPICAL HOLDING CURRENT

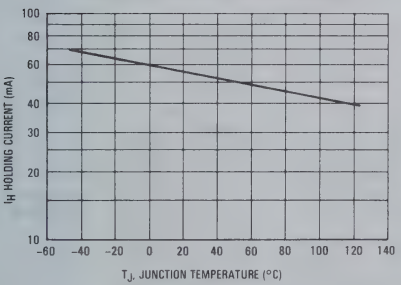
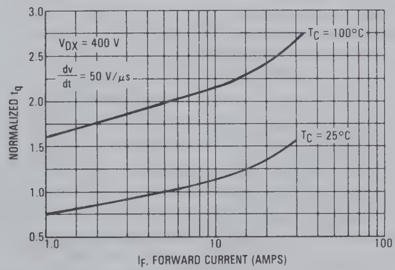


FIGURE 6 — TYPICAL TURN-OFF TIME



MCR2150, A
series

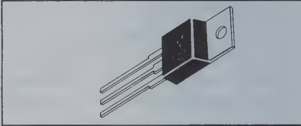
MOTOROLA

SILICON CONTROLLED RECTIFIERS

. . . designed primarily for high speed inverter and converter applications — selected versions available for vertical deflection for TV circuits, computer terminals, medical monitors, and video games.

- $t_q < 4.0\ \mu s$ @ $I_F = 15$ A
- Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Blocking Voltage to 800 Volts

THYRISTORS
15 AMPERES RMS
200-800 VOLTS



2.3

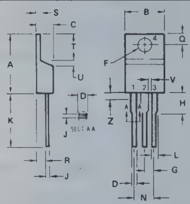
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage Peak Repetitive Reverse Voltage MCR2150, A-4 MCR2150, A-5 MCR2150, A-6 MCR2150, A-7 MCR2150, A-8 MCR2150, A-9 MCR2150, A-10	V_{RRM}(1) V_{DRM}	 200 300 400 500 600 700 800	Volts
Forward Current RMS (All Conduction Angles)	$I_{T(RMS)}$	15	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz)	I_{TSM}	160	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	100	A^2s
Forward Peak Gate Power	P_{GM}	5.0	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watts
Forward Peak Gate Current	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage



STYLE 3
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

NOTES
1. DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
5. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220 AB

FIGURE 1 — AVERAGE CURRENT DERATING

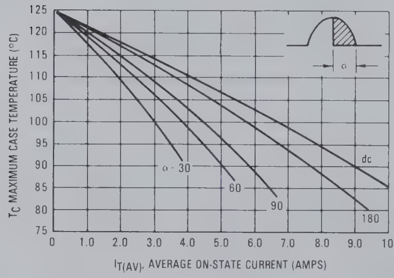
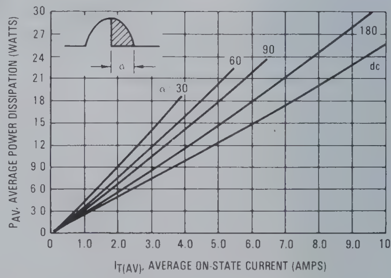


FIGURE 2 — ON-STATE POWER DISSIPATION



ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Rated V_{DRM})	T_J = 125°C	I_{DRM}	—	—	3.0	mA
Peak Reverse Blocking Current (Rated V_{DRM})	T_J = 125°C	I_{RRM}	—	—	3.0	mA
Peak On-State Voltage (1)		V_{TM}				Volts
(I_{TM} = 10 A Peak)			—	—	3.0	
(I_{TM} = 30 A Peak)			—	—	3.75	
Gate Trigger Current (Continuous dc) (V_D = 7.0 V, R_L = 100 Ω)		I_{GT}	—	—	50	mA
Gate Trigger Voltage (Continuous dc) (V_D = 7.0 V, R_L = 100 Ω)		V_{GT}	—	—	2.5	Volts
Holding Current (V_D = 7.0 V, R_L = 100 Ω)		I_H	—	—	100	mA
Turn-Off Time (V_{DRM} = Rated Voltage)		t_q				μs
(I_{TM} = 10 A, di/dt = 5.0 A/μs,	MCR2150		—	3.0	10	
Reapplied dv/dt = 50 V/μs)	MCR2150A		—	—	4.0	
Forward Voltage Application Rate		dv/dt	100	150	—	V/μs

(1) Pulse Test: Pulse Width = 1.0 ms, Duty Cycle ≤ 2%.

2.3

FIGURE 3 — TYPICAL GATE TRIGGER CURRENT

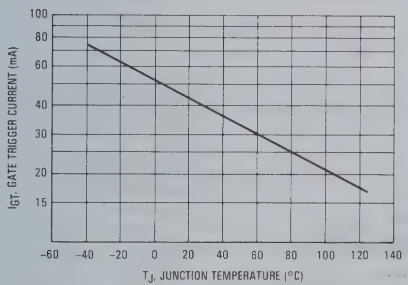


FIGURE 4 — TYPICAL GATE TRIGGER VOLTAGE

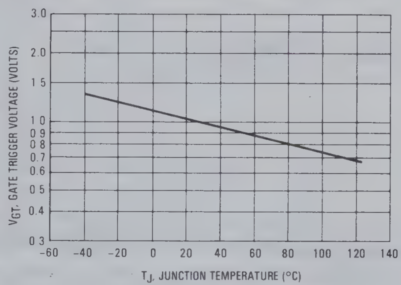


FIGURE 5 — TYPICAL HOLDING CURRENT

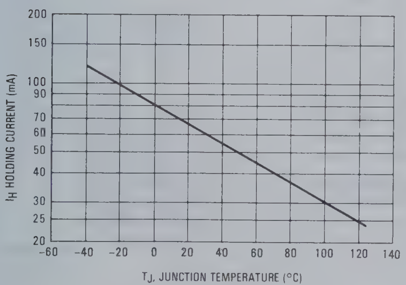
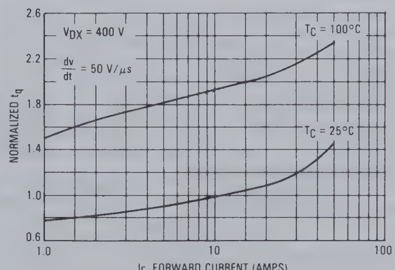


FIGURE 6 — TYPICAL TURN-OFF TIME



MCR3818-1 thru MCR3818-10
MCR3918-1 thru MCR3918-10

MOTOROLA

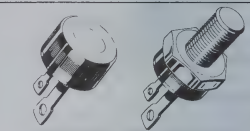
SILICON CONTROLLED RECTIFIER

20 AMPERES RMS
25–800 VOLTS

REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Supplied in Either Pressfit or Stud Package
- High Surge Current Rating — I_{TSM} = 240 Amp
- Low On-State Voltage — 1.2 V (Typ) @ I_{TM} = 20 Amp
- Practical Level Triggering and Holding Characteristics — 40 mA (Max) and 50 mA (Max) @ T_C = 25°C



2.3

MAXIMUM RATINGS

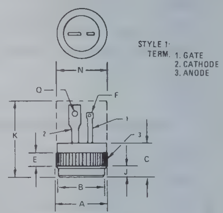
Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Voltage (1)			
MCR3818, MCR3918 - 1	V_{DRM} or V_{RRM}	25	Volts
- 2		50	
- 3		100	
- 4		200	
- 5		300	
- 6		400	
- 7		500	
- 8		600	
- 9		700	
- 10		800	
Non-Repetitive Reverse Blocking Voltage	V_{RSM}		Volts
MCR3818, MCR3918 - 1		35	
-2		75	
-3		150	
- 4		300	
- 5		400	
- 6		500	
- 7		600	
- 8		700	
- 9		800	
- 10		900	
On-State Current RMS	$I_{T(RMS)}$	20	Amp
Average On-State Current (T_C = 67°C)	$I_{T(AV)}$	13	Amp
Circuit Fusing (T_J = -40 to +100°C, t ≤ 8.3 ms)	I^2t	235	A^2s
Peak Non-Repetitive Surge Current (One cycle, 60 Hz, T_J = -40 to +100°C)	I_{TSM}	240	Amp
Peak Gate Power (Maximum Pulse Width = 10 μs)	P_{GM}	5.0	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Forward Gate Current (Maximum Pulse Width = 10 μs)	I_{GM}	2.0	Amp
Peak Gate Voltage	V_{GM}	10	Volts
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque		30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$			°C/W
Pressfit Package		1.0	1.5	
Stud Package		1.1	1.6	

(1)See note on page 2.

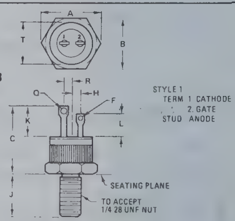
MCR3818 SERIES



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160

CASE 174-03

MCR3918 SERIES



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

CASE 175-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM} @ T_J = 100°C, gate open)	I_{DRM}	–	5.0	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ T_J = 100°C, gate open)	I_{RRM}	–	5.0	mA
Gate Trigger Current (Continuous dc) (2)	I_{GT}			mA
(V_D = 7.0 Vdc, R_L = 100 Ω)		–	40	
(V_D = 7.0 Vdc, R_L = 100 Ω, T_C = –40°C)		–	75	
Gate Trigger Voltage (Continuous dc)	V_{GT}			Volts
(V_D = 7.0 Vdc, gate open)		–	1.5	
(V_D = 7.0 Vdc, R_L = 100 Ω, T_C = –40°C)		–	2.5	
(V_D =Rated V_{DRM}, R_L = 100 Ω, T_J = 100°C)		0.2	–	
Peak On-State Voltage (Pulse Width = 1.0 ms max, duty cycle ≤ 1%)	V_{TM}			Volts
(I_{TM} = 20 A)		–	1.5	
(I_{TM} = 41 A)		–	1.7	
Holding Current	I_H			mA
(V_D = 7.0 Vdc, gate open)		–	50	
(V_D = 7.0 Vdc, gate open, T_C = –40°C)		–	90	
		Typical		
Gate Controlled Turn-On Time ($t_d + t_r$) (I_{TM} = 20 A, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})	t_{gt}	1.0		μs
Circuit Commutated Turn-Off Time	t_q			μs
(I_{TM} = 10 A, I_R = 10 A)		20		
(I_{TM} = 10 A, I_R = 10 A, T_J = 100°C) (V_D = V_{DRM} = rated voltage) (dv/dt = 30 V/μs)		30		
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Wave Form, Gate open, T_J = 100°C)	dv/dt	50		V/μs

(1) V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. These devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

2.3

EFFECT OF TEMPERATURE UPON TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 – GATE TRIGGER CURRENT

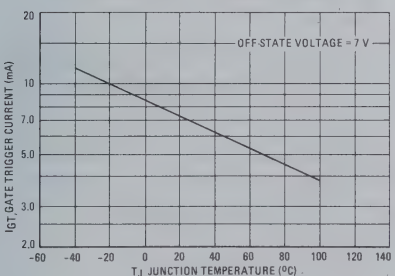
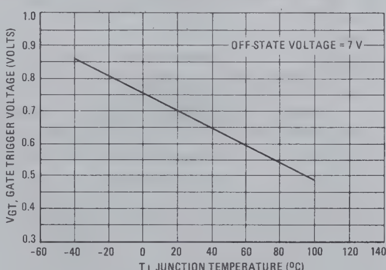


FIGURE 2 – GATE TRIGGER VOLTAGE



MAXIMUM ALLOWABLE NON-REPETITIVE SURGE CURRENT

FIGURE 3 – 60 Hz SURGES

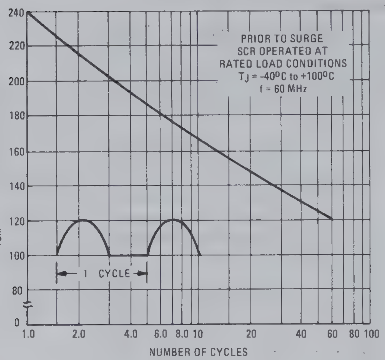


FIGURE 4 – SUB-CYCLE SURGES

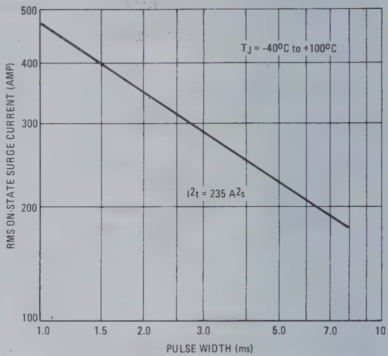


FIGURE 5 – GATE TRIGGER CHARACTERISTICS

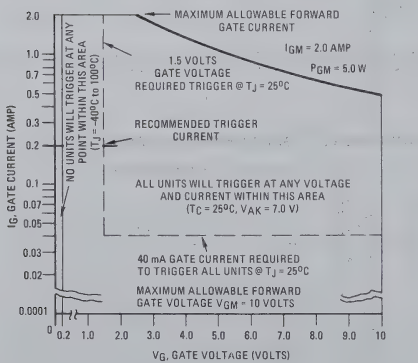
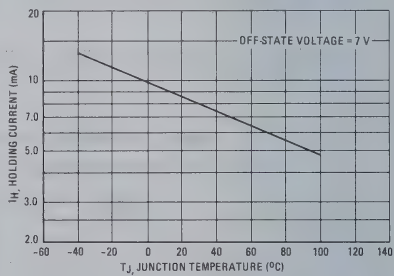


FIGURE 6 – EFFECT OF TEMPERATURE ON TYPICAL HOLDING CURRENT



DERATING AND DISSIPATION FOR RESISTIVE AND INDUCTIVE LOADS (f = 60 to 400 Hz, SINE WAVE)

FIGURE 7 – AVERAGE CURRENT DERATING

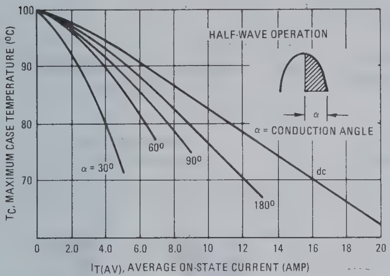
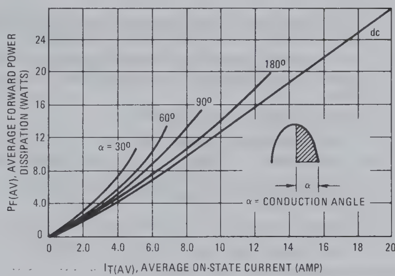


FIGURE 8 – ON-STATE POWER DISSIPATION



2.3

FIGURE 9 – ON-STATE CHARACTERISTICS

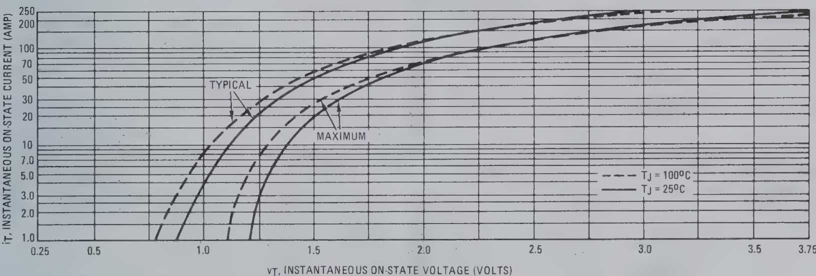


FIGURE 10 – TYPICAL THERMAL RESISTANCE OF PLATES

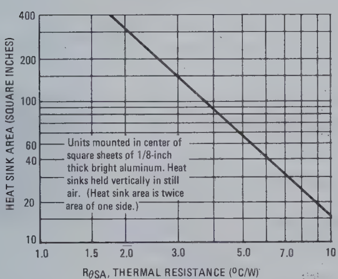
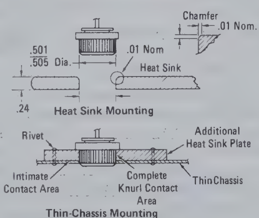


FIGURE 11 – MOUNTING DETAILS FOR PRESSFIT THYRISTORS



The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the rectifier during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the rectifier case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the ' :at sink material. Recommended hardnesses are: copper – less than 50 on the Rockwell F scale; aluminum – less than 65 on the Brinell scale. A heat sink as thin as 1/8" may be used, but the interface thermal resistance will increase in proportion to the reduction of contact area. A thin chassis requires the addition of a back-up plate.

MCR3835-1 thru MCR3835-10
MCR3935-1 thru MCR3935-10

MOTOROLA

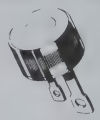
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

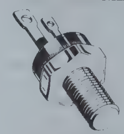
- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 350 Amp
- Low Forward "On" Voltage — 1.2 V (Typ) @ I_{TM} = 35 Amp
- Practical Level Triggering and Holding Characteristics — 10 mA (Typ) @ T_C = 25°C
- Rugged Construction in Either Pressfit or Stud Package
- Glass Passivated Junctions for Maximum Reliability

SILICON CONTROLLED RECTIFIER

35 AMPERES RMS
25–800 VOLTS



CASE 174-03
MCR3835 Series



CASE 175-02
MCR3935 Series

2.3

MAXIMUM RATINGS

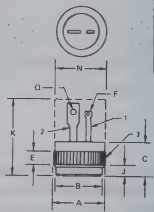
Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage	V_{DRM}(1) V_{RRM}		Volts
MCR3835, MCR3935 -1		25	
-2		50	
-3		100	
-4		200	
-5		300	
-6		400	
-7		500	
-8		600	
-9		700	
-10		800	
Peak Non-Repetitive Reverse Blocking Voltage ($t \leq 5.0$ ms)	V_{RSM}		Volts
MCR3835, MCR3935 -1		35	
-2		75	
-3		150	
-4		300	
-5		400	
-6		500	
-7		600	
-8		700	
-9		800	
-10		900	
Forward Current RMS	$I_{T(RMS)}$	35	Amp
Peak Surge Current (One cycle, 60 Hz) (T_J = -40 to +100°C)	I_{TSM}	350	Amp
Circuit Fusing (T_J = -40 to +100°C) (t = 1.0 to 8.3 ms)	I^2t	510	A^2s
Peak Gate Power	P_{GFM}	5.0	Watts
Average Gate Power	$P_{GF(AV)}$	0.5	Watt
Peak Forward Gate Current	I_{GFM}	2.0	Amp
Peak Gate Voltage — Forward	V_{GFM}	10	Volts
Reverse	V_{GRM}	10	
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque	–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
MCR3835		1.2	
MCR3935		1.3	

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.

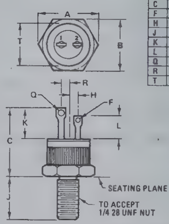
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160



STYLE 1:
TERM. 1. GATE
2. CATHODE
3. ANODE

CASE 174-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505



STYLE 1:
TERM. 1. CATHODE
2. GATE
STUD : ANODE

CASE 175-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}, with gate open, T_J = 100°C)	I_{DRM}	–	1.0	5.0	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}, with gate open, T_J = 100°C)	I_{RRM}	·	1.0	5.0	mA
Forward "On" Voltage (I_{TM} = 35 A Peak)	V_{TM}	–	1.2	1.5	Volts
Gate Trigger Current (Continuous dc) (V_D = 7.0 V, R_L = 100 Ω)	I_{GT}	·	10	40	mA
Gate Trigger Voltage (Continuous dc) (V_D = 7.0 V, R_L = 100 Ω)	V_{GT}	–	0.7	1.5	Volts
(V_D = Rated V_{DRM}, R_L = 100 Ω, T_J = 100°C)	V_{GD}	0.2	–	–	
Holding Current (V_D = 7.0 V, gate open)	I_H	–	10	50	mA
Turn-On Time ($t_d + t_r$) (I_{TM} = 35 Adc, I_{GT} = 40 mAdc)	t_{on}	–	1.0	–	μs
Turn-Off Time (I_{TM} = 10 A, I_R = 10 A)	t_q	–	20	–	μs
(I_{TM} = 10 A, I_R = 10 A, T_J = 100°C)		–	30	–	
Forward Voltage Application Rate (V_D = Rated V_{DRM}, T_J = 100°C)	dv/dt	–	50		V/μs

(1) V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

FIGURE 1 – CURRENT DERATING

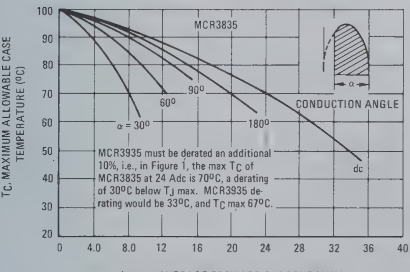


FIGURE 2 – TYPICAL POWER DISSIPATION

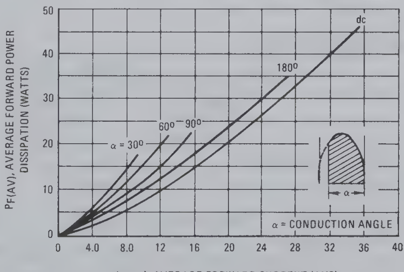


FIGURE 3 – TYPICAL GATE TRIGGER CURRENT

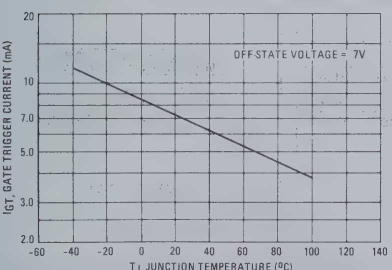
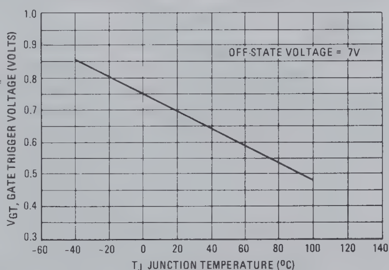
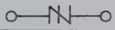


FIGURE 4 – TYPICAL GATE TRIGGER VOLTAGE



2.3

MOTOROLA

MT1  MT2

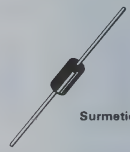
PLASTIC SIDAC HIGH VOLTAGE BILATERAL TRIGGER — HIGH VOLTAGE TRIGGERS

. . . designed for direct interface with the ac power line. Upon reaching the breakover voltage in each direction, the device switches from a blocking state to a low voltage on-state. Conduction will continue like an SCR until the main terminal current drops below the holding current. The plastic axial lead package provides high pulse current capability at low cost. Glass passivation insures reliable operation. Applications are:

- High Pressure Sodium Vapor Lighting
- Strobes and Flashers
- Ignitors
- High Voltage Regulators
- Line Transient Clippers
- Pulse Generators

PLASTIC SIDAC HIGH VOLTAGE BILATERAL TRIGGER

1.0 AMPERE RMS
104 thru 135 VOLTS



Surmetic 50

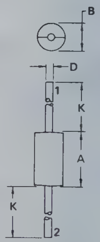
2.3

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Repetitive Breakover Voltage MK1V-115 MK1V-125 MK1V-135	$V_{(BO)}$	 104 110 120	 115 125 135	Volts
Off-State Repetitive Voltage	V_{DRM}	—	±90	Volts
On-State RMS Current (All Conduction Angles)	$I_{T(RMS)}$	—	1.0	Amps
On-State Surge Current (Nonrepetitive) (60 Hz One Cycle Sine Wave, Peak Value)	I_{TSM}	—	20	Amps
Operating Junction Temperature Range	T_J	-40	+125	°C
Storage Temperature Range	T_{stg}	-40	+150	°C
Lead Solder Temperature (Lead Length ⩾ 1/16″ from case, 10 s Max)	—	—	+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	15	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	—	45	°C/W



STYLE 1:
PIN 1. MT1
2. MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

CASE 267-01

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; both directions.)

Characteristic	Symbol	Min	Typ	Max	Unit
Breakover Current (60 Hz Sine Wave)	$I_{(BO)}$	—	—	200	μA
Repetitive Peak Off-State Current (60 Hz Sine Wave, V = V_{DRM})	I_{DRM}	—	—	10	μA
Repetitive Peak On-State Current (T_C = 25°C, Pulse Width = 10 μs, Repetition Frequency, f = 1.0 KHz)	I_{TRM}	—	20	—	Amps
Forward "On" Voltage (I_{TM} = 1.0 A peak)	V_{TM}	—	1.1	1.5	Volts
Dynamic Holding Current (60 Hz Sine Wave, R_S = 0.1 KΩ)	I_H	—	—	100	mA
Switching Resistance	R_S	0.1	—	—	kΩ
Maximum Rate of Change of On-State Current	di/dt	—	50	—	A/μs

2.3

CURRENT DERATING

FIGURE 1 — MAXIMUM CASE TEMPERATURE

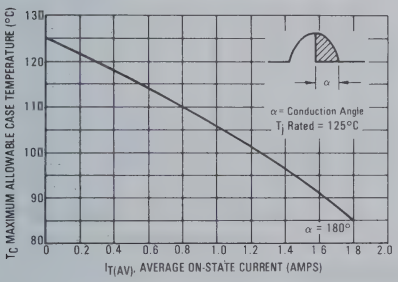


FIGURE 2 — MAXIMUM AMBIENT TEMPERATURE

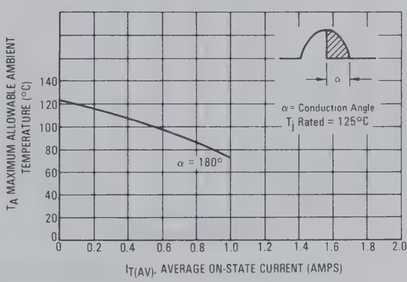


FIGURE 3 — TYPICAL FORWARD VOLTAGE

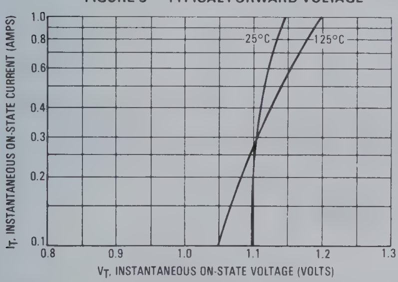
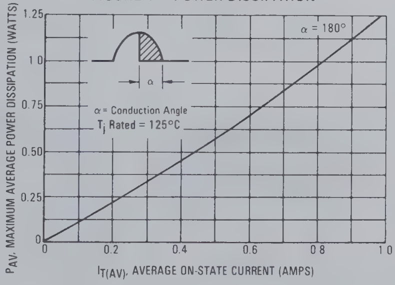


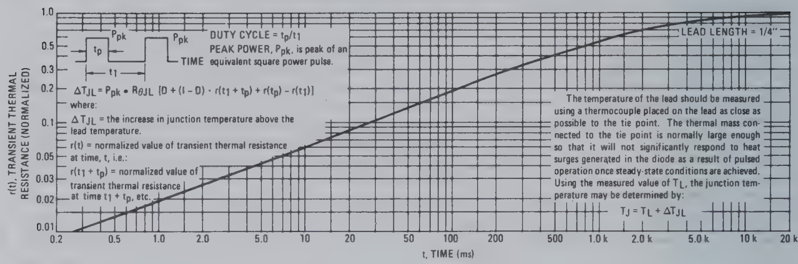
FIGURE 4 — POWER DISSIPATION



2.3

THERMAL CHARACTERISTICS

FIGURE 5 — THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 6 — BREAKOVER CURRENT

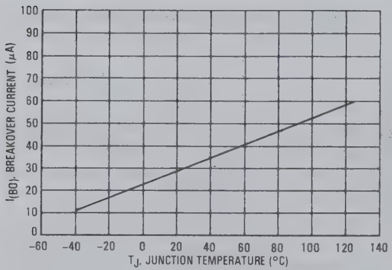


FIGURE 7 — HOLDING CURRENT

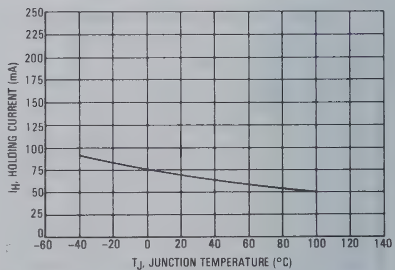
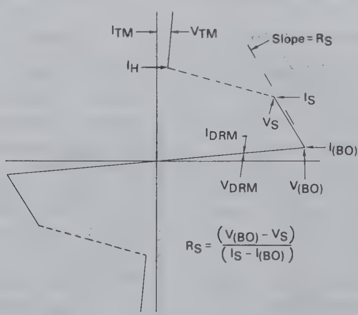


FIGURE 8 — V-1 CHARACTERISTICS



$$R_S = \frac{(V_{(BO)} - V_S)}{(I_S - I_{(BO)})}$$

MOTOROLA

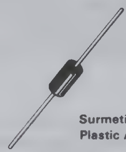
PLASTIC SIDAC HIGH VOLTAGE BILATERAL TRIGGER — HIGH VOLTAGE TRIGGERS

. . . designed for direct interface with the ac power line. Upon reaching the breakover voltage in each direction, the device switches from a blocking state to a low voltage on-state. Conduction will continue like an SCR until the main terminal current drops below the holding current. The plastic axial lead package provides high pulse current capability at low cost. Glass passivation insures reliable operation. Applications are:

- High Pressure Sodium Vapor Lighting
- Strobes and Flashers
- Ignitors
- High Voltage Regulators
- Pulse Generators

PLASTIC SIDAC HIGH VOLTAGE BILATERAL TRIGGER

1.0 AMPERE RMS
240 thru 270 VOLTS



Surmetic 50
Plastic Axial

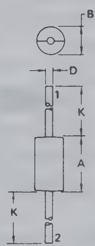
2.3

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Off-State Repetitive Voltage	V_{DRM}	—	±180	Volts
On-State Current RMS (T_L = 100°C; LL = 3/8", 60 Hz Sine Wave Conduction Angle = 180°)	$I_{T(RMS)}$	—	1.0	Amps
On-State Surge Current (Nonrepetitive) (60 Hz One Cycle Sine Wave, Peak Value)	I_{TSM}	—	20	Amps
Maximum Rate of Change of On-State Current	di/dt	—	140	A/μs
Operating Junction Temperature Range	T_J	-40	+125	°C
Storage Temperature Range	T_{stg}	-40	+150	°C
Lead Solder Temperature (Lead Length ≥ 1/16" from Case, 10 Seconds Max)	—	—	+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Thermal Resistance, Junction to Lead (LL = 3/8")	$R_{\theta JL}$	—	15	°C/W



STYLE 1:
PIN 1. MT1
2. MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

CASE 267-01

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; both directions.)

Characteristic	Symbol	Min	Typ	Max	Unit
Breakover Voltage MK1V240 MK1V260 MK1V270	$V_{(BO)}$	220 240 250	— — —	250 270 280	Volts
Breakover Current (60 Hz Sine Wave)	$I_{(BO)}$	—	—	200	μA
Repetitive Peak Off-State Current (60 Hz Sine Wave, V = V_{DRM})	I_{DRM}	—	—	10	μA
Forward "On" Voltage (I_{TM} = 1.0 A peak)	V_{TM}	—	1.1	1.5	Volts
Dynamic Holding Current (60 Hz Sine Wave, R_S = 0.1 kΩ)	I_H	—	—	100	mA
Switching Resistance	R_S	0.1	—	—	kΩ

2.3

CURRENT DERATING

FIGURE 1 — MAXIMUM LEAD TEMPERATURE

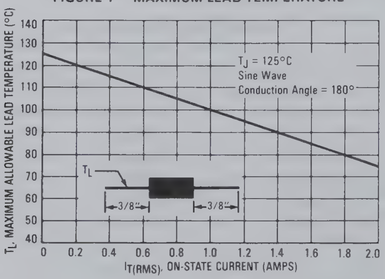


FIGURE 2 — MAXIMUM AMBIENT TEMPERATURE

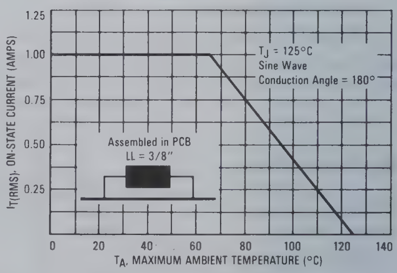


FIGURE 3 — TYPICAL ON-STATE VOLTAGE

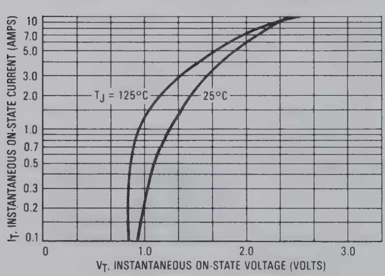
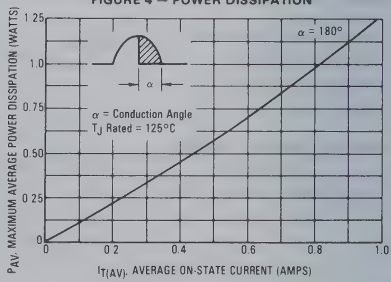
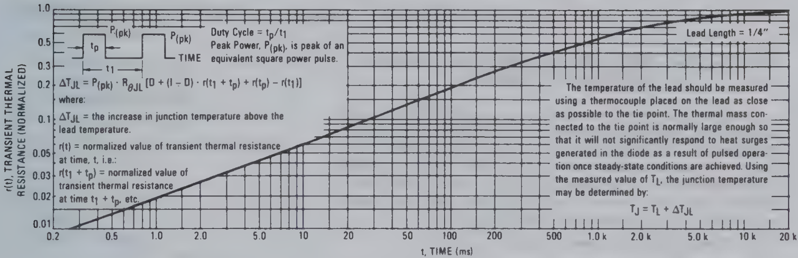


FIGURE 4 — POWER DISSIPATION



THERMAL CHARACTERISTICS

FIGURE 5 — THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 6 — BREAKOVER VOLTAGE

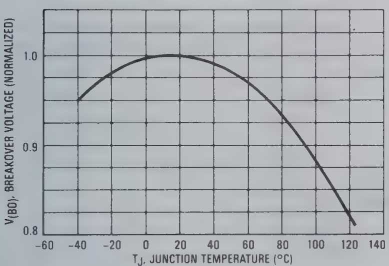


FIGURE 7 — HOLDING CURRENT

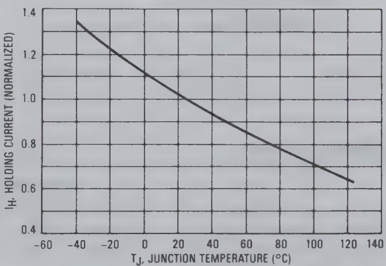


FIGURE 8 — PULSE RATING CURVE

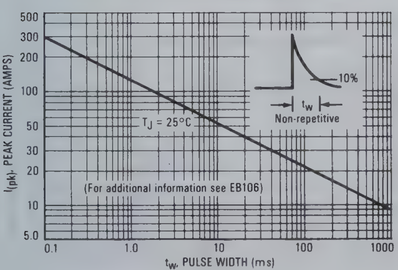
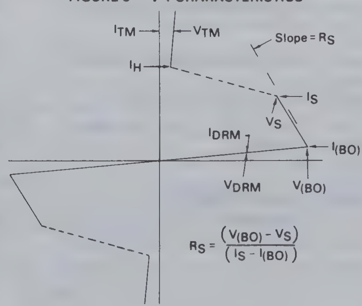


FIGURE 9 — V-1 CHARACTERISTICS



$$R_S = \frac{(V_{(BO)} - V_S)}{(I_S - I_{(BO)})}$$

2.3

MKP9V120 MKP9V240
MKP9V130 MKP9V260
MKP9V270

MOTOROLA

PLASTIC SIDAC HIGH VOLTAGE BILATERAL TRIGGER — HIGH VOLTAGE TRIGGERS

. . . designed for direct interface with the ac power line. Upon reaching the breakover voltage in each direction, the device switches from a blocking state to a low voltage on-state. Conduction will continue like an SCR until the main terminal current drops below the holding current. The plastic axial lead package provides high pulse current capability at low cost. Glass passivation insures reliable operation. Applications are:

- High Pressure Sodium Vapor Lighting
- Strobes and Flashers
- Ignitors
- High Voltage Regulators
- Pulse Generators

2.3

PLASTIC SIDAC HIGH VOLTAGE BILATERAL TRIGGER

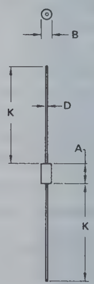
0.9 AMPERE RMS
120 TO 130 VOLTS
240 TO 270 VOLTS

MAXIMUM RATINGS

Rating	Symbol	MKP9V120 MKP9V130	MKP9V240 MKP9V260 MKP9V270	Unit
Off-State Repetitive Voltage	V_{DRM}	±90	±180	Volts
On-State Current RMS (T_L = 80°C, LL = ⅜", conduction angle = 180°, 60 Hz Sine Wave)	$I_{T(RMS)}$	0.9		Amps
On-State Surge Current (Nonrepetitive) (60 Hz One Cycle Sine Wave, Peak Value)	I_{TSM}	4.0		Amps
Maximum Rate of Change of On-State Current	di/dt	90		Amps/μs
Operating Junction Temperature Range	T_J	−40 to +125		°C
Storage Temperature Range	T_{stg}	−40 to +150		°C
Lead Solder Temperature (Lead Length ≥ 1/16" from case, 10 seconds max)	—	230		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Unit	
Thermal Resistance, Junction to Lead LL = ⅜"	$R_{\theta JL}$	40	°C/W



NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH JEDEC DO-41 OUTLINE SHALL APPLY.
2. POLARITY DENOTED BY CATHODE BAND.
3. LEAD DIAMETER NOT CONTROLLED WITHIN "F" DIMENSION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
Breakover Voltage	V_{BO}				
MKP9V120		110	—	125	
MKP9V130		120	—	135	
MKP9V240		220	—	250	Volts
MKP9V260		240	—	270	Volts
MKP9V270		250	—	280	Volts
Repetitive Peak Off-State Current (60 Hz Sine Wave, V = V_{DRM})	I_{DRM}	—	—	5.0	μA
T_J = 125°C		—	—	50	μA
Forward "On" Voltage (I_T = 1.0 A)	V_{TH}		1.3	1.5	Volts
Dynamic Holding Current (60 Hz Sine Wave)	I_H	—	—	100	mA
Switching Resistance	R_S	0.1	—	—	kΩ
Breakover Current (60 Hz Sine Wave)	I_{BO}			200	μA

2.3

FIGURE 1 — MAXIMUM LEAD TEMPERATURE

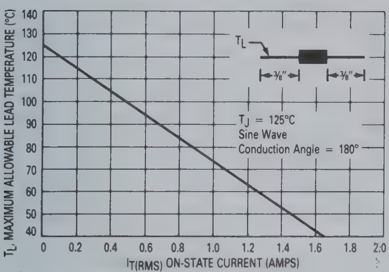


FIGURE 2 — MAXIMUM AMBIENT TEMPERATURE

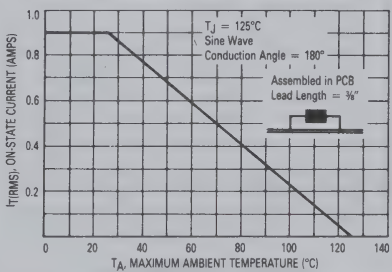


FIGURE 3 — TYPICAL ON-STATE VOLTAGE

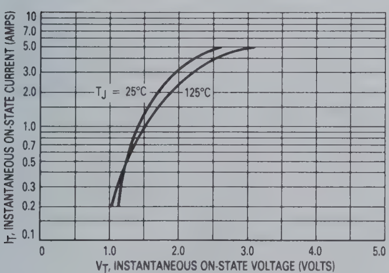
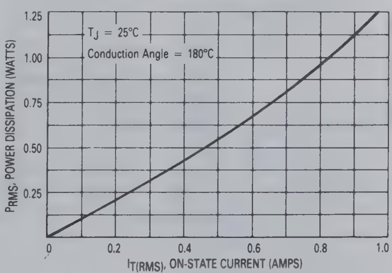
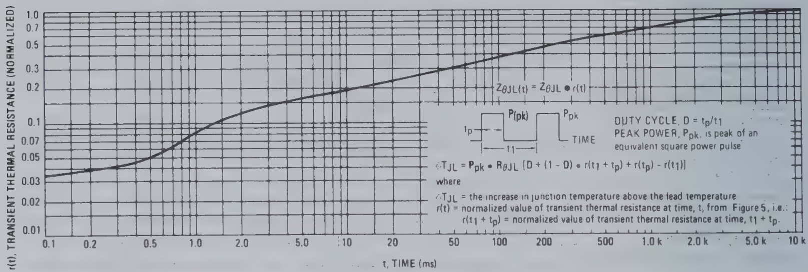


FIGURE 4 — POWER DISSIPATION



THERMAL CHARACTERISTICS

FIGURE 5 — THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 6 — BREAKOVER VOLTAGE

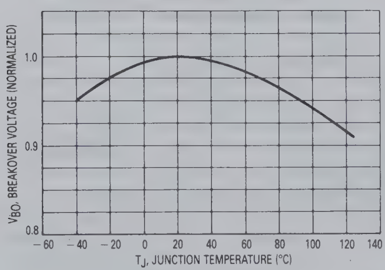


FIGURE 7 — HOLDING CURRENT

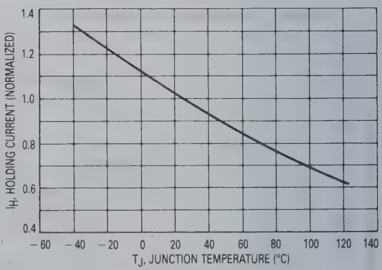


FIGURE 8 — PULSE RATING CURVE

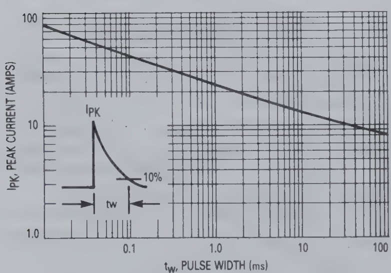
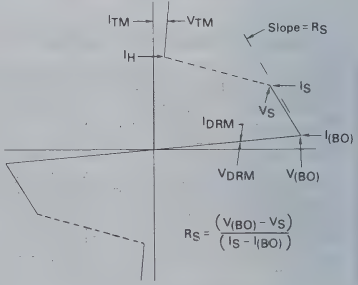


FIGURE 9 — V-I CHARACTERISTICS



MOC633A MOC634A MOC635A MOC640A MOC641A

MOTOROLA

Specifications and Applications Information

OPTICALLY ISOLATED TRIAC DRIVER

VDE approved per Component Standard 0833/6.80, Equipment Standard 0860, internal thickness through insulation 0.4 mm, and all equipment standards with similar or lower requirements.

These devices consist of a gallium-arsenide infrared emitting diode, optically coupled to a silicon bilateral switch. They are designed for applications requiring isolated zero and non-zero crossing triac triggering.

- VDE Approved Per Test Certificate Number 22762
- UL Recognized File Number E54915
- Output Driver Designed for Up to 240 Vac Line
- V_{ISO} Isolation Voltage of 7500 V Peak
- Standard 6-Pin Plastic DIP
- Zero Voltage Crossing — MOC640A, MOC641A
- Phase Controllable — MOC633A, MOC634A, MOC635A

VDE APPROVED
OPTO
COUPLER/ISOLATOR

TRIAC DRIVER OUTPUT

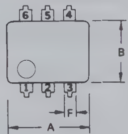
400 VOLTS

2.3

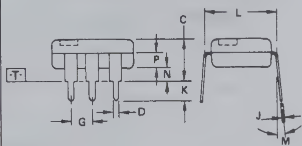
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current — Continuous	I_F	60	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Triac Driver Derate above 25°C	P_D	100 1.33	mW mW/°C
OUTPUT DRIVER MAXIMUM RATINGS			
Off-State Output Terminal Voltage	V_{DRM}	400	Volts
On-State RMS Current T_A = 25°C (Full Cycle, 50 to 60 Hz) T_A = 70°C	$I_{T(RMS)}$	100 50	mA mA
Peak Nonrepetitive Surge Current (PW = 10 ms, DC = 10%)	I_{TSM}	1.2	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 4.0	mW mW/°C
TOTAL DEVICE MAXIMUM RATINGS			
Isolation Surge Voltage* (Peak ac Voltage, 60 Hz, 5 Second Duration)	V_{ISO}	7500	Vac
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	330 4.4	mW mW/°C
Junction Temperature Range	T_J	-55 to +100	°C
Ambient Operating Temperature Range	T_A	-55 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature (10 s)	—	260	°C

*Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating



STYLE 6:
PIN 1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
6. MAIN TERMINAL



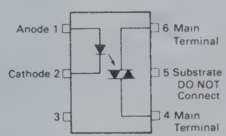
NOTES:
1. DIMENSIONS A AND B ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCES FOR LEADS:
⊕ ∅ 0.13 (0.005) Ⓜ T A Ⓜ B Ⓜ
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.13	8.89	0.320	0.350
B	6.10	6.60	0.240	0.260
C	2.92	5.08	0.115	0.200
D	0.41	0.51	0.016	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	3.81	0.100	0.150
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.38	2.54	0.015	0.100
P	1.27	2.03	0.050	0.080

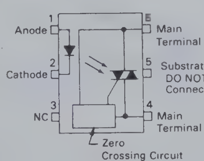
CASE 730A-01

COUPLER SCHEMATICS

MOC633A/634A/635A



MOC640A/641A



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
LED CHARACTERISTICS					
Reverse Leakage Current (V_R = 3.0 V)	I_R	—	0.05	100	μA
Forward Voltage (I_F = 10 mA)	V_F	—	1.2	1.5	Volts
DETECTOR CHARACTERISTICS (I_F = 0 unless otherwise noted)					
Peak Blocking Current, Either Direction (Rated V_{DRM}, Note 1) MOC633A/634A/635A MOC640A/641A	I_{DRM}	— —	10 2.0	100 100	nA
Peak On-State Voltage, Either Direction (I_{TM} = 100 mA Peak) MOC633A/634A/635A MOC640A/641A	V_{TM}	— —	2.5 1.8	3.0 3.0	Volts
Critical Rate of Rise of Off-State Voltage, T_A = 70°C MOC633A/634A/635A MOC640A/641A	dv/dt	— —	10 1000	— —	V/μs
COUPLED CHARACTERISTICS					
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3.0 V, Note 2) MOC633A/640A MOC634A/641A MOC635A	I_{FT}	— — —	15 8.0 5.0	30 15 10	mA
Holding Current, Either Direction MOC633A/634A/635A MOC640A/641A	I_H	— —	100 200	— —	μA
ZERO CROSSING CHARACTERISTICS — MOC640A/641A					
Inhibit Voltage (I_F = Rated I_{FT}, MT1-MT2 Voltage above which device will not trigger.)	V_{IH}	—	15	40	Volts
Leakage in Inhibited State (I_F = Rated I_{FT}, Rated V_{DRM}, Off State)	I_{DRM2}	—	100	300	μA

Note 1. Test voltage must be applied within dv/dt rating.

2. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} and absolute max I_F (60 mA).

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — ON-STATE CHARACTERISTICS

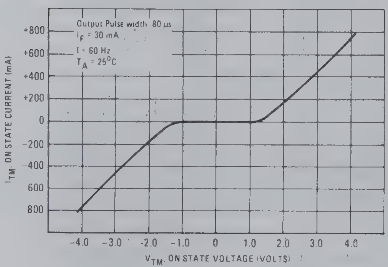
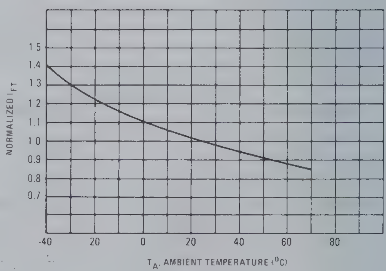


FIGURE 2 — TRIGGER CURRENT versus TEMPERATURE



VDE TESTING INFORMATION

These optocouplers have been approved by VDE per Test Certificate NR22762 to Component Standard VDE0883/6.80 and Equipment Standards VDE0860/8.81 and IEC65, and to all VDE Standards of Electric and Electronic Equipment with similar or lower requirements.

The 0.4 mm separation between internal conductors is accomplished by reinforced insulation for Insulation Group C and Safety Class I and II equipment per VDE0110 and VDE0110B/2.79.

VDE RATINGS

Rating	Symbol	Value	Unit
Ambient Operating Temperature Range	T_A	−55 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Climatic Test Class		55/100/21	
DC Isolation Voltage at 100°C for 1 Minute	$V_{ISO(pk)}$	4.4	kVdc
Nominal Operating Isolation Voltage for Isolation Group C According to VDE0110B	$V_{ISO(nom)}$	500 600	Vac Vdc
Isolation Creepage Path (Figures 3 and 4)	L_{ICP}	8.5 Min	mm
Isolation Clearance (Figure 5)	L_{ICL}	7.9 Min	mm
Internal Thickness Through Insulation	—	0.4 Min	mm
Creepage Current Stability of Insulation According to VDE303 Part 1/10.76	Overmold Undermold	KB100 Min KB600 Min	— —
Surge Isolation Voltage According to IEC65 or VDE0860/8.81	50 Discharges of 10 kV charged 1 nF 12 Discharges Max at 1 Minute		

ENVIRONMENTAL TEST

Environment Test Per VDE0883	Kind of Test	Application	Condition	Duration
Solderability Per DIN 40046 Part 18 or IEC 68-2-20	Ta1 Tb1	Solder Bath Solder Iron 3 mm TIP	260°C 260°C	5 ± 1 sec 5 ± 1 sec
Temperature Cycling Per DIN 40046 Part 14 or IEC 68-2-18	Na	5 Cycles	−55°C/+100°C	Dwell 3 Hrs Transfer 3 Min
Dry Heat Per DIN 40046 Part 4 or IEC 68-2-2	Ba		100°C	16 Hrs
Humid Heat Cycling Per DIN 40046 Part 31 or IEC 68-2-30	Db	6 Cycles	25°C/40°C RH 95%	Dwell 6 Hrs
Cold Per DIN 40046 Part 3 or IEC 68-2-1	Aa		−55°C	16 Hrs
Humid Heat (Long Term) Per DIN 40046 Part 5 or IEC 68-2-3	Ca		40°C RH 95%	21 Days
Vibration Per DIN 40046 Part 8 or IEC 68-2-6	Fc		55 Hz — 2 kHz 10 g	90 Min

ISOLATION CREEPAGE PATH

Denotes the shortest path between two conductive parts measured along the surface of the insulation. i.e., on the optocouplers, it is the shortest distance on the surface of the package between the input and output leads. On the circuit board in which the coupler is mounted, it is the shortest distance across the surface on the board between the solder eyes of the coupler input/output leads. Coupler and circuit board creepage path have to meet the minimum specified distances for the individual VDE equipment norms. (See application section.)

CLEARANCE

Denotes the shortest distance between two conductive parts or between a conductive part and the bonding surface of the equipment, measured through air. (See application sections.)

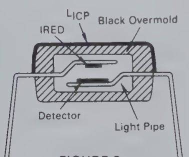


FIGURE 3

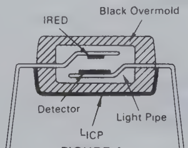


FIGURE 4

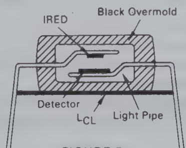


FIGURE 5

Topside Creepage Path L_{ICP} A = 8.5 mm Minimum
Underside Creepage Path L_{ICP} B = 8.5 mm Minimum

Clearance L_{CL} = 7.9 mm Minimum as Supplied

2.3

APPLICATION OF THE MOTOROLA VDE OPTOCOUPLERS

The VDE approval of the Motorola Optocoupler Family is of great importance since VDE follows the wide spread safety recommendations of the International Electrotechnical Commission (IEC) which is accepted and adopted by many European and other countries. The intent of these safety standards is to prevent injury or damage due to electrical shock, fire, energy — mechanical — heat — radiation and chemical hazards. The IEC recommendations provide an ever increasing unifying control over most national standards worldwide. The US and Canada have similar standards and there is a trend to harmonize their standards with the IEC recommendations. This short application note is able to mention only some VDE/IEC equipment safety standards whose primary objective is to enable designers to realize safety requirements at an early design stage and build them into the equipment while incorporating the relevant requirements of these standards.

CIRCUIT BOARD LAYOUT DESIGN RULES

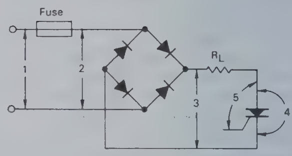
The most demanding and stringent safety requirements are on interfaces between a safety low-voltage circuit [SELV] and a hazardous voltage (240 V power line). The requirements for creepage path and clearance dimensioning are different for each individual equipment norm and also depend on the isolation group and safety class of the equipment and the circuit boards resistance to tracking. Isolation materials are classified for their resistance to tracking creepage current stability from KB 100 to KB ⩽ 600 (see VDE 303). On circuit board materials with a low KB value, the creepage path distance requirements are higher than for materials with a high KB value. In the following examples we therefore show creepage path dimensions for KB 100, the lowest value which is easily met by most circuit board materials.

The least stringent requirements on optocouplers, as well as printboard layouts, are within and inbetween SELV or ELV loops or circuits. (ELV = Electrical Low Voltage which does not meet the safety low voltage requirements.)

In studying the individual equipment norms, the designer will discover that optocouplers are not mentioned in most of these norms. He has to use the requirements for transformers or potted components instead.

Spacing requirements between two live tracks on a PC board within a low or high voltage loop (circuit) should generally meet the VDE requirements for minimum clearance and creepage path dimensions. If they do not, the circuit has to show some sort of current limiting (fuse, high-impedance, etc.) which prevents fire hazard due to an eventual short or sparkover between the two tracks. The VDE testing institute will conduct, in this case, a shorting test and a tracking test (arcing). See VDE 804. Classical cases are rectifiers, thyristors, high-voltage transistors which, sometimes due to their close pinout, might not meet the VDE equipment requirements at a certain voltage.

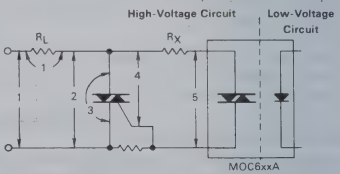
FIGURE 6



1 — Clearance and creepage path **must** meet min requirements
2 — Current limited due to fuse
3, 4 — Current limited due to R_L and fuse
5 — Current limited due to I_{GT}, R_L and fuse

2, 3, 4, 5 — Clearance and creepage path may be smaller than VDE min requirements but **must** meet fire hazard requirements due to short and arcing between the tracks. There shall be no flames or explosion during the test

FIGURE 7

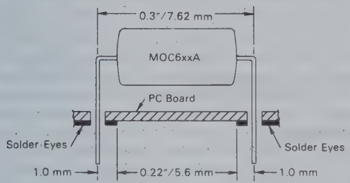


1 Clearance and creepage path **must** meet min requirements
2 Current limited due to R_L
3 Current limited due to R_L
4 Current limited due to I_{GT}
5 Current limited due to I_{GT} and R_X

COUPLER MOUNTING ON A CIRCUIT BOARD

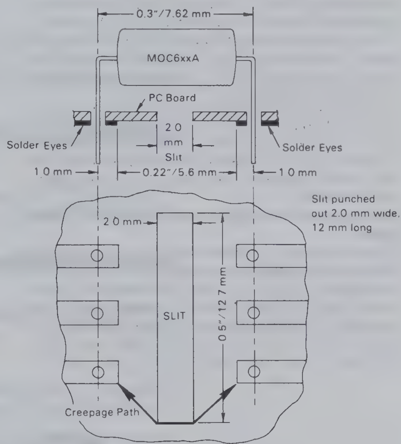
Clearance and Creepage Path Between Input and Output for Optocouplers on a PC Board

FIGURE 8



Input/Output Leads — L = 0.3"/7 62 mm
Clearance Limited Due to PC Board
Solder Eyes — 0.22"/5.6 mm
Creepage Path on PC Board — 0.22"/5.6 mm

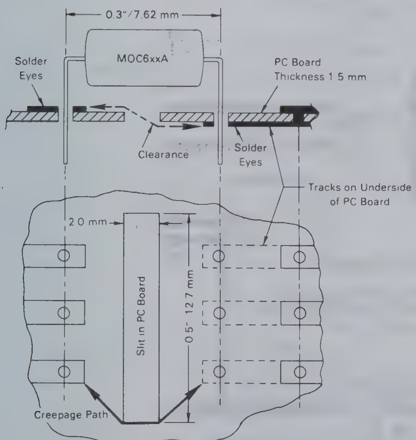
FIGURE 9



VDE equipment norms demanding longer creepage path than 0.22"/5.6 mm can be accomplished by a slit in the PC board between the coupler input and output solder eyes of 2.0 mm width

Input Output Leads — L · 0 3" · 7 62 mm
Clearance on PC Boards — 0.22"/5 6 mm Min
Creepage Path on PC Board — 0 31 /8 0 mm Min

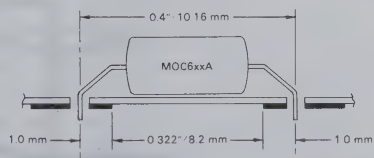
FIGURE 10



If a clearance of 0.23"/6.0 mm and a creepage path of minimum 8.0 mm is required, this is a possible solution

Slit — 0.5"/12.7 mm long, 2.0 mm wide
PC Board Thickness — 1.5 mm
Clearance — 6.0 mm Min
Creepage Path — 8.0 mm Min

FIGURE 11



Where the equipment norms demand a clearance and creepage path of 8 0 mm Min, the coupler input and output leads should be bent to 0.4"/10.16 mm and the printboard layout should be as shown

Safety Coupler Mounting with Spacing — L = 0.4"/10 16 mm
Clearance on PC Board — 0.322"/8 2 mm
Creepage Path on PC Board — 0 322"/8.2 mm

2.3

2.3

PRINTED CIRCUIT BOARD LAYOUT FOR SELV-POWER INTERFACES

The circuit board layout examples shown here are dimensioned so that they provide a safe electrical isolation between metal parts carrying line voltage (called Power Interface) and conductors connected to a SELV circuit.

The required thickness through insulation for the optocoupler can be found in the individual VDE equipment norms. (See examples for safety applications of the MOC600A family at the end of this article.)

Many Class I equipment norms permit the use of parts (modules, PC boards) which meet the Safety Class II dimension and isolation requirements. This enables the designer to take advantage of the less complex and space demanding design of the Class II PC board layout also in Class I classified equipment.

Optocoupler Mounting on PC Boards for Safety Class I

SELV transformers for Class I equipment have a Faraday shield which is connected to earth ground between primary and secondary windings. This is **not** applicable to optocouplers, but creepage path and clearance requirements from safety Class II can be applied. Class I also demands an earth ground track on the circuit board between SELV — and power circuit. Applying the Class I rules, this earth ground track should be between the coupler input and output. However, this can not be done without violating the minimum creepage path and clearance requirements. A possible solution is shown on Figure 14 and Figure 15.

The earth ground track itself has to show a minimum distance to the equipment body (i.e., frame, circuit board enclosure) or to any inactive, active or hazardous track on the circuit board. According to many VDE equipment norms, this creepage path distance for 250 V Max is 4.0 mm. A mechanically unsecured circuit board which can be plugged in and out without a tool and is electrically connected through a standard PC board connector, has to show an isolation of the earth ground track to Class II, which is 8.0 mm. This is because a standard PC connector, as shown in Figure 14, does not guarantee earthing contact **before** there is termination of the life 220 V tracks on the circuit board when plugged in. Another reason for increased spacing is when the circuit board metal enclosure is not securely earth grounded. This is the case when the connection is done with the PC module mounting screws through lacquer or oxide layers to a grounded rack or frame. (See Figure 15.) PC board designs per Figures 14 and 15 account for these possibilities and therefore show dimensions M, N and A, B and D as 8.0 mm instead of 4.0 mm.

FIGURE 12 — OPTOCOUPLER MOUNTING ON PC BOARDS FOR SAFETY CLASS II WITH CREEPAGE PATH AND CLEARANCE

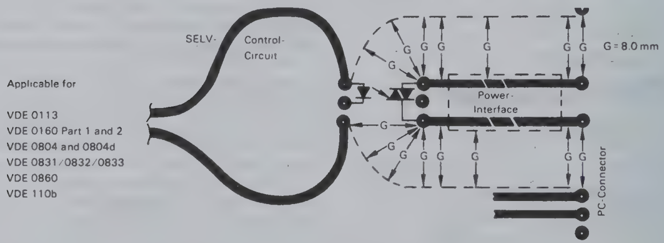
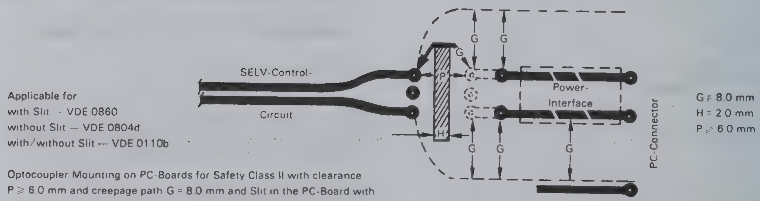


FIGURE 13 — OPTOCOUPLER MOUNTING ON PC BOARDS FOR SAFETY CLASS II WITH CLEARANCE



Optocoupler Mounting on PC-Boards for Safety Class II with clearance P ≥ 6.0 mm and creepage path G = 8.0 mm and Slit in the PC-Board with Slit length = 12.7 mm and Slit thickness H = 2.0 mm

2.3

FIGURE 14 — OPTOCOUPLER MOUNTING ON PC BOARD ACCORDING TO SAFETY CLASS I WITH ONLY ONE PC BOARD PLUG CONNECTION

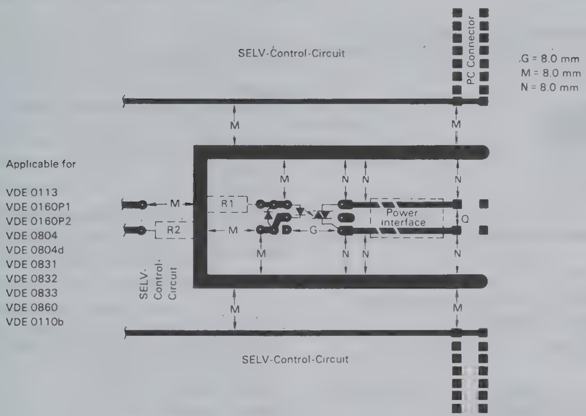
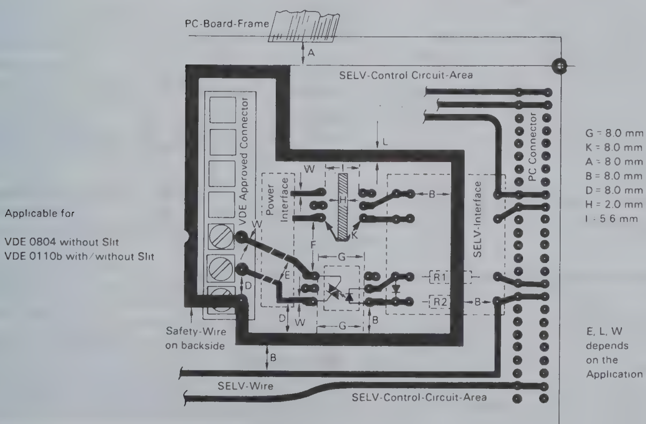


FIGURE 15 — OPTOCOUPLER MOUNTING ON PC BOARD ACCORDING TO SAFETY CLASS I WITH ONE PLUG-CONNECTION FOR THE SELV-CONTROL CIRCUIT AND ONE SCREW-CONNECTION FOR THE POWER-INTERFACE



2.3

EXAMPLES FOR SAFETY APPLICATIONS OF THE MOC600A FAMILY

The VDE approval of the MOC600A family covers many VDE standards for electrical and electronic equipment.

EXAMPLE 1.

VDE Specifications for the electrical equipment of manufacturing and processing machines with rated voltage up to 1000 V (Individual controls) VDE 0113/12.73 and IEC 204

Subclause 4.1.1
Clearances 8.0 mm
Creepage Distance 8.0 mm

Clause 15
Isolation Resistance 1.0 MΩ
Isolation Voltage 1.5 kVac

EXAMPLE 2.

Requirements for electrical trains. VDE 0115/3.65 and VDE 0115A/8.75

Clause 15
Isolation Voltage 2.5 kVac for the VDE 0115-Isolation Group D
Subclause 15A according VDE 110
Clearance 8.0 mm
Creepage Distance 8.0 mm

EXAMPLE 3.

VDE Specifications for the electrical equipment of electrical power installations with electronic devices:

VDE 0160 Part 1/7.71 and VDE 0160 Part 1B/5 76
Clause 13
Subclause 13B and Subclause 24D
Isolation Resistance 1 MΩ
Clause 14 and Subclause 28C
Clearances 8.0 mm
Creepage Distances 8.0 mm
Clause 24
Isolation Voltage 2.7 kVac at 1 minute for the nominal — Operation Isolation Voltage or Working Isolation Voltage of $V_{ISO(nom)}$ = 250 Vac or 300 Vdc

EXAMPLE 4.

VDE 160 Part 2/10.75
Subclause 3 10 and 3.11
Clearance 8.0 mm
Creepage Distance 8.0 mm
Subclause 3.10 and 4 4
Isolation Voltage 3.6 kVdc at 1 minute = for $V_{ISO(nom)}$ = 500 Vac or 600 Vdc
Isolation Resistance 1.0 MΩ

EXAMPLE 5.

Specifications for telecommunications apparatus including data processing equipments

VDE 0804/5.72 and VDE 0804/2.80
Clause 9
Clearance 8.0 mm
Creepage Distance 8.0 mm
Clause 14
Isolation Voltage 2.5 kVac at 1 minute for $V_{ISO(nom)}$ = 250 Vac
Clause 18
Subclause 18C
Isolation Voltage 2.5 kVac at 1 minute for $V_{ISO(nom)}$ = 250 Vac
Subclause 18D
Isolation Resistance 2.0 MΩ

EXAMPLE 6.

Electric signal systems for railroads

VDE 0831/2.80
Clause 4.5 according VDE 110
Clearances 8.0 mm
Creepage Distance 8.0 mm
Clause 4.5 and Subclause 5.9.3
Isolation Voltage 2.0 kVac at 1 minute for $V_{ISO(nom)}$ = 250 Vac

EXAMPLE 7.

Road traffic signal systems

VDE 832/7 81
Subclause 5.2 and 9.2.4
Isolation Voltage according VDE 804 Subclause 14, 2.5 kVac at 1 minute for $V_{ISO(nom)}$ = 250 Vac
Subclause 9.2 according VDE 110
Clearances 8 0 mm
Creepage Distance 8.0 mm
Subclause 9.2.1 according VDE 804

EXAMPLE 8.

Jeopardy alarm systems for fire, hold-up and intrusion general requirements

VDE 0833 Part 1/11.78 and VDE 0833 Part 1A/3.80
Subclause 4.1 according VDE 804
Isolation Voltage 2.5 kVac at 1 minute for $V_{ISO(nom)}$ = 250 Vac
Isolation Resistance 2.0 MΩ at 1 minute
Clearance 8.0 mm
Creepage Distance 8.0 mm

EXAMPLE 9.

Safety requirements for mains operated electronic and related apparatus for household and similar use (Radio, TV, Electronic Organs):

VDE 0860/8.81 and IEC 65, 4 Edition 1976 inclusive amendments 12B (co) 133/134/135/138/139
Clause 10
Subclause 10.1 and Figure 7A
Surge Isolation Voltage
50 Discharges of 10 kV charged 1.0 nF
12 Discharges Max at 1 minute
Subclause 10.3 and Figures 15:
Isolation Resistance higher than 4 MΩ
Isolation voltage higher 4240 Vdc at 1 minute and at T_A = 100 degrees Celsius
Subclause 9.3.8
Minimum thickness through isolation 0.4 mm
Subclause 9.3.4 and 9.3.5 and 4.3.1 and Table 2 and Clause 13 and Figure 13:
Clearances and creepage distance higher than 6.0 mm at 354 V Curve B

MOTOROLA

ZERO VOLTAGE CROSSING OPTICALLY ISOLATED TRIAC DRIVER

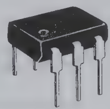
This device consists of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon detector performing the function of a Zero Voltage crossing bilateral triac driver.

They are designed for use with a triac in the interface of logic systems to equipment powered from 115 Vac lines, such as teletypewriters, CRTs, printers, motors, solenoids and consumer appliances, etc.

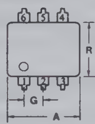
- Simplifies Logic Control of 110 Vac Power
- Zero Voltage Crossing
- High Breakdown Voltage: V_{DRM} = 250 V Min
- High Isolation Voltage: V_{ISO} = 7500 V Min
- Small, Economical, 6-Pin DIP Package
- Same Pin Configuration as MOC3010/3011
- UL Recognized, File No. E54915
- dv/dt of 100 V/μs Typ

OPTO COUPLER

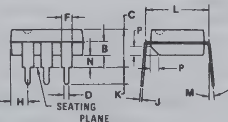
ZERO CROSSING TRIAC DRIVER



2.3



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIAMETER OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.13	8.89	0.320	0.350
B	1.27	2.03	0.050	0.080
C	2.92	5.08	0.115	0.200
D	0.41	0.51	0.016	0.020
F	1.02	1.78	0.040	0.070
G	2.54	BSC	0.100	BSC
H	1.02	2.16	0.040	0.085
J	0.20	0.30	0.008	0.012
K	2.[illegible]	3.81	0.100	0.150
L	7.62	BSC	0.300	BSC
M	0°	15°	0°	15°
N	0.38	2.54	0.015	0.100
P	0.81	0.97	0.032	0.038
R	6.10	6.60	0.240	0.260

STYLE 6:
PIN
1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
6. MAIN TERMINAL

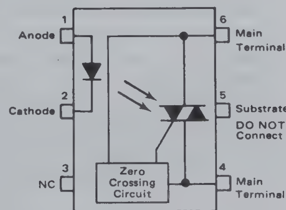
CASE 730-01

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current — Continuous	I_F	50	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Output Driver Derate above 25°C	P_D	120 1.33	mW mW/°C
OUTPUT DRIVER MAXIMUM RATINGS			
Off-State Output Terminal Voltage	V_{DRM}	250	Volts
On-State RMS Current T_A = 25°C (Full Cycle, 50 to 60 Hz) T_A = 85°C	$I_{T(RMS)}$	100 50	mA mA
Peak Nonrepetitive Surge Current (PW = 10 ms)	I_{TSM}	1.2	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 4.0	mW mW/°C
TOTAL DEVICE MAXIMUM RATINGS			
Isolation Surge Voltage (1) (Peak ac Voltage, 60 Hz, 5 Second Duration)	V_{ISO}	7500	Vac
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	330 4.4	mW mW/°C
Junction Temperature Range	T_J	−40 to +100	°C
Ambient Operating Temperature Range	T_A	−40 to + 85	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Soldering Temperature (10 s)	—	260	°C

(1) Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating.

COUPLER SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
LED CHARACTERISTICS					
Reverse Leakage Current (V_R = 3.0 V)	I_R	–	0.05	100	μA
Forward Voltage (I_F = 30 mA)	V_F	–	1.3	1.5	Volts
DETECTOR CHARACTERISTICS (I_F = 0 unless otherwise noted)					
Peak Blocking Current, Either Direction (Rated V_{DRM}, Note 1)	I_{DRM}	–	10	100	nA
Peak On-State Voltage, Either Direction (I_{TM} = 100 mA Peak)	V_{TM}	–	1.8	3.0	Volts
Critical Rate of Rise of Off-State Voltage	dv/dt	–	100	–	V/μs

COUPLED CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3.0 V, Note 2)	I_{FT}				mA
MOC3030		–	–	30	
MOC3031		–	–	15	
Holding Current, Either Direction	I_H	–	100	–	μA

ZERO CROSSING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Inhibit Voltage (I_F = Rated I_{FT}, MT1-MT2 Voltage above which device will not trigger.)	V_{IH}	–	15	25	Volts
Leakage in Inhibited State (I_F = Rated I_{FT}, Rated V_{DRM}, Off State)	I_R	–	100	200	μA

Note 1. Test voltage must be applied within dv/dt rating.

2. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (30 mA for MOC3030, 15 mA for MOC3031) and absolute max I_F (50 mA).

TYPICAL ELECTRICAL CHARACTERISTICS
T_A = 25°C

FIGURE 1 – ON-STATE CHARACTERISTICS

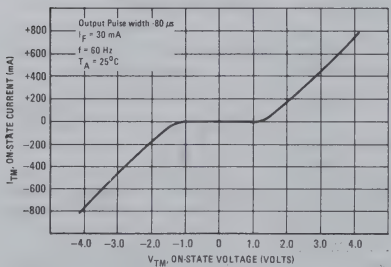


FIGURE 2 – TRIGGER CURRENT versus TEMPERATURE

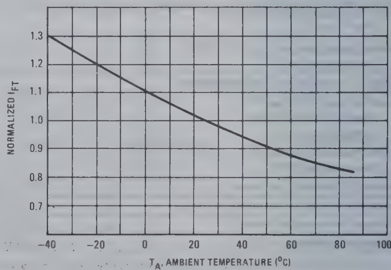
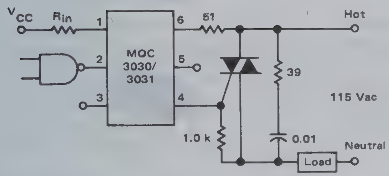


FIGURE 3 — HOT-LINE SWITCHING APPLICATION CIRCUIT

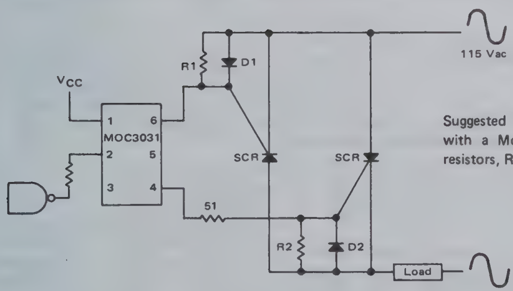


Typical circuit for use when hot line switching is required. In this circuit the "hot" side of the line is switched and the load connected to the cold or neutral side. The load may be connected to either the neutral or hot line.

R_{in} is calculated so that I_F is equal to the rated I_{FT} of the part, 15 mA for the MOC3031 or 30 mA for the MOC3030. The 39 ohm resistor and 0.01 μF capacitor are for snubbing of the triac and may or may not be necessary depending upon the particular triac and load used.

2.3

FIGURE 4 — INVERSE-PARALLEL SCR DRIVER CIRCUIT



Suggested method of firing two, back-to-back SCR's, with a Motorola triac driver. Diodes can be 1N4001; resistors, R1 and R2, are optional 1 k ohm.

MOC3040
MOC3041

MOTOROLA

ZERO VOLTAGE CROSSING
OPTICALLY ISOLATED TRIAC DRIVER

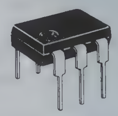
This device consists of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon detector performing the function of a Zero Voltage Crossing bilateral triac driver.

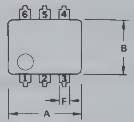
They are designed for use with a triac in the interface of logic systems to equipment powered from 220 Vac lines, such as solid-state relays, industrial controls, motors, solenoids and consumer appliances, etc.

- Simplifies Logic Control of 220 Vac Power
- Zero Voltage Crossing
- High Breakdown Voltage: V_{DRM} = 400 V Min
- High Isolation Voltage: V_{ISO} = 7500 V Min
- Small, Economical, 6-Pin DIP Package
- Same Pin Configuration as MOC3020/3021
- UL Recognized, File No. E54915
- dv/dt of 100 V/μs Typ

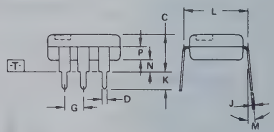
2.3

OPTO
COUPLER / ISOLATOR
ZERO CROSSING
TRIAC DRIVER
400 VOLTS





NOTES
1 DIMENSIONS A AND B ARE DATUMS
2 T IS SEATING PLANE
3 POSITIONAL TOLERANCES FOR LEADS
⌖ | ∅ 0.13 (0.005) Ⓜ | T A Ⓜ B Ⓜ
4 DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL
5 DIMENSIONING AND TOLERANCING PER ANSI Y14 5, 1973

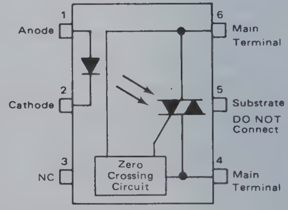


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.13	8.89	0.320	0 350
B	6.10	6.60	0.240	0.260
C	2.92	5.08	0.115	0.200
D	0.41	0.51	0.016	0.020
F	1.02	1 78	0.040	0.070
G	2.54 BSC		0.100 BSC	
J	0 20	0.30	0 008	0.012
K	2.54	3.81	0.100	0.150
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.38	2 54	0.015	0.100
P	1.27	2.03	0.050	0.080

STYLE 6
PIN 1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5 SUBSTRATE
6. MAIN TERMINAL

CASE 730A-01

COUPLER SCHEMATIC



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	6.0	Volts
Forward Current — Continuous	I_F	50	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Output Driver Derate above 25°C	P_D	120 1.33	mW mW/°C
OUTPUT DRIVER MAXIMUM RATINGS			
Off-State Output Terminal Voltage	V_{DRM}	400	Volts
On-State RMS Current T_A = 25°C (Full Cycle, 50 to 60 Hz) T_A = 70°C	$I_{T(RMS)}$	100 50	mA mA
Peak Nonrepetitive Surge Current (PW = 10 ms)	I_{TSM}	1.2	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 4.0	mW mW/°C
TOTAL DEVICE MAXIMUM RATINGS			
Isolation Surge Voltage (1) (Peak ac Voltage, 60 Hz, 5 Second Duration)	V_{ISO}	7500	Vac
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	330 4.4	mW mW/°C
Junction Temperature Range	T_J	-40 to +100	°C
Ambient Operating Temperature Range	T_A	-40 to +70	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Soldering Temperature (10 s)	—	260	°C

(1) Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
LED CHARACTERISTICS					
Reverse Leakage Current (V_R = 6.0 V)	I_R	–	0.05	100	μA
Forward Voltage (I_F = 30 mA)	V_F	–	1.3	1.5	Volts
DETECTOR CHARACTERISTICS (I_F = 0 unless otherwise noted)					
Peak Blocking Current, Either Direction (Rated V_{DRM}, Note 1)	I_{DRM1}	–	2.0	100	nA
Peak On-State Voltage, Either Direction (I_{TM} = 100 mA Peak)	V_{TM}	–	1.8	3.0	Volts
Critical Rate of Rise of Off-State Voltage	dv/dt	–	100	–	V/μs

COUPLED CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3.0 V, Note 2) MOC3040	I_{FT}	–	–	30	mA
MOC3041		–	–	15	
Holding Current, Either Direction	I_H	–	200	–	μA

ZERO CROSSING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Inhibit Voltage (I_F = Rated I_{FT}, MT1-MT2 Voltage above which device will not trigger.)	V_{IH}	–	15	40	Volts
Leakage in Inhibited State (I_F = Rated I_{FT}, Rated V_{DRM}, Off State)	I_{DRM2}	–	100	300	μA

Note 1. Test voltage must be applied within dv/dt rating.

2. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (30 mA for MOC3040, 15 mA for MOC3041) and absolute max I_F (50 mA).

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — ON-STATE CHARACTERISTICS

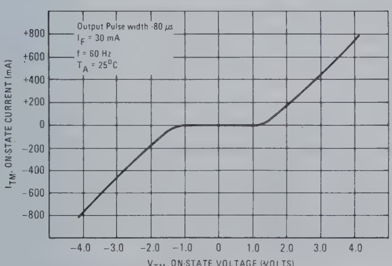


FIGURE 2 — TRIGGER CURRENT versus TEMPERATURE

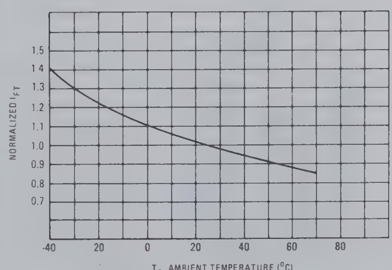
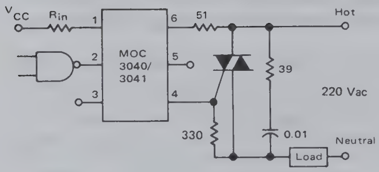


FIGURE 3 – HOT-LINE SWITCHING APPLICATION CIRCUIT

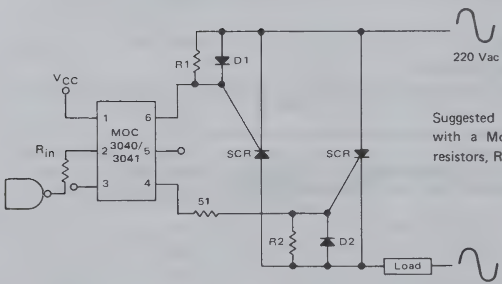


Typical circuit for use when hot line switching is required. In this circuit the "hot" side of the line is switched and the load connected to the cold or neutral side. The load may be connected to either the neutral or hot line.

R_{in} is calculated so that I_F is equal to the rated I_{FT} of the part, 15 mA for the MOC3041 or 30 mA for the MOC3040. The 39 ohm resistor and 0.01 μF capacitor are for snubbing of the triac and may or may not be necessary depending upon the particular triac and load used.

2.3

FIGURE 4 – INVERSE-PARALLEL SCR DRIVER CIRCUIT



Suggested method of firing two, back-to-back SCR's, with a Motorola triac driver. Diodes can be 1N4001; resistors, R1 and R2, are optional 330 ohms.

MOTOROLA

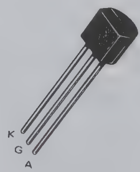
MPU131
MPU132
MPU133

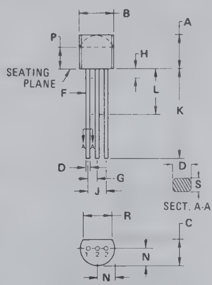
PROGRAMMABLE UNIJUNCTION TRANSISTORS

SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-trigger, oscillator, pulse and timing circuits. The MPU131, MPU132 and MPU133 may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO-92 plastic package for high-volume requirements, this package is readily adaptable for use in automatic insertion equipment.

- Programmable — R_{BB}, η, I_V and I_P.
- Low On-State Voltage — 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current — 5.0 nA Maximum
- High Peak Output Voltage — 11 Volts Typical
- Low Offset Voltage — 0.35 Volt Typical (R_G = 10 k ohms)





STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Dissipation Derate Above 25°C	P_F $1/\theta_{JA}$	375 5.0	mW mW/°C
DC Forward Anode Current Derate Above 25°C	I_T	200 2.67	mA mA/°C
DC Gate Current	I_G	±20	mA
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle 20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
Gate to Cathode Reverse Voltage	V_{GKR}	5.0	Volt
Gate to Anode Reverse Voltage	V_{GAR}	40	Volt
Anode to Cathode Voltage (1)	V_{AK}	±40	Volt
Operating Junction Temperature Range	T_J	-50 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

(1) Anode positive, R_{GK} = 1k ohm
Anode negative, R_{GK} = open

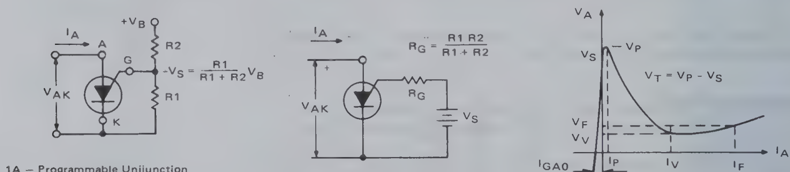
2.3

2.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Peak Current (V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU131	2,9-14	I_P	–	1.25	2.0	μA
	MPU132			–	0.19	0.30	
	MPU133			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	MPU131			–	4.0	5.0	
	MPU132			–	1.20	2.0	
	MPU133				0.70	1.0	
Offset Voltage (V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU131	1	V_T	0.2	0.70	1.6	Volts
	MPU132			0.2	0.50	0.6	
	MPU133			0.2	0.40	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms) (All Types)				0.2	0.35	0.6	
Valley Current (V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU131, 132	1,4,5,	I_V	–	18	50	μA
	MPU133			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	MPU131			70	270	–	
	MPU132, 133			50	270	–	
Gate to Anode Leakage Current (V_S = 40 Vdc, T_A = 25°C, Cathode Open)		–	I_{GAO}	–	1.0	5.0	nAdc
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	30	75	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}	–	5.0	50	nAdc
Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	–	0.8	1.5	Volts
Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	11	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – Programmable Unijunction with "Program" Resistors R1 and R2

1B – Equivalent Test Circuit for Figure 1A used for electrical characteristics testing (also see Figure 2)

1C – Electrical Characteristics

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

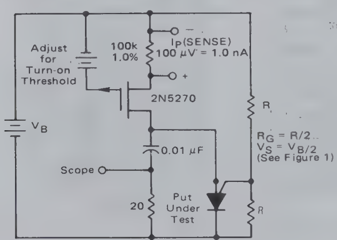
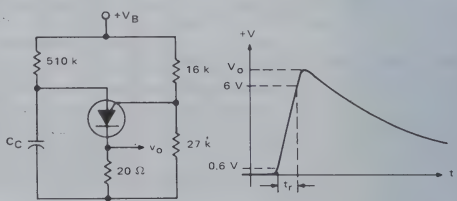


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 — EFFECT OF SUPPLY VOLTAGE

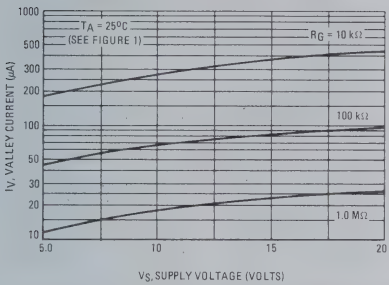


FIGURE 5 — EFFECT OF TEMPERATURE

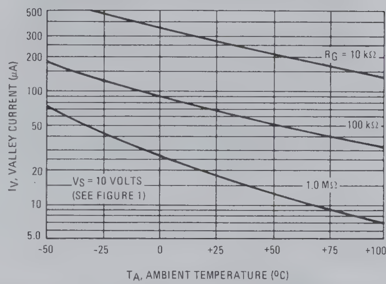


FIGURE 6 — FORWARD VOLTAGE

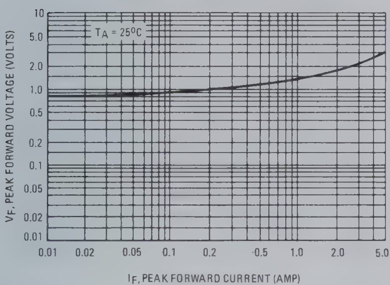


FIGURE 7 — PEAK OUTPUT VOLTAGE

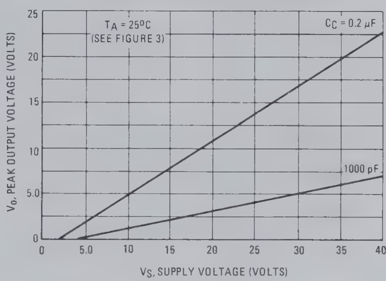
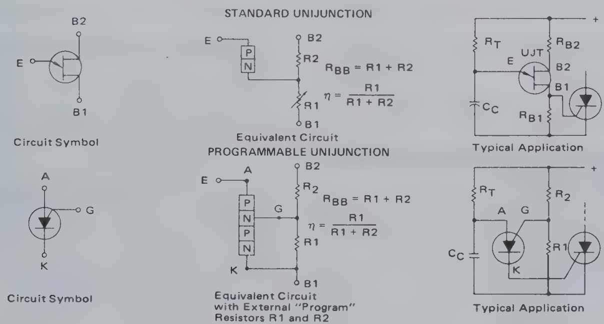


FIGURE 8 — STANDARD UNIJUNCTION COMPARED TO PROGRAMMABLE UNIJUNCTION



TYPICAL PEAK CURRENT BEHAVIOR

MPU131

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

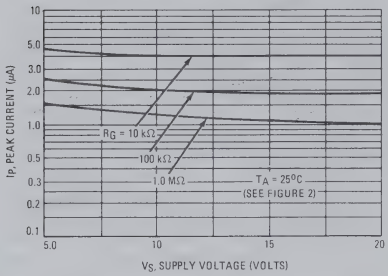
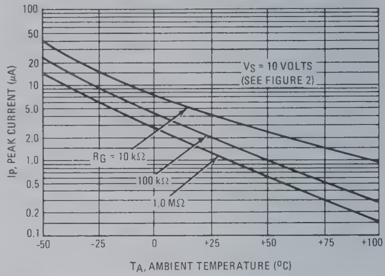


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



MPU132

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

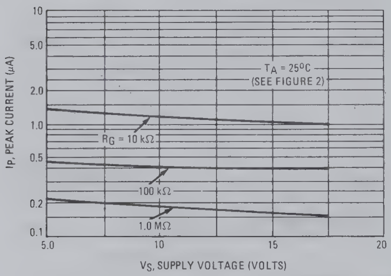
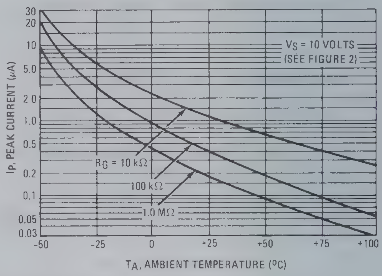


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



MPU133

FIGURE 13 – EFFECT OF SUPPLY VOLTAGE AND R_G

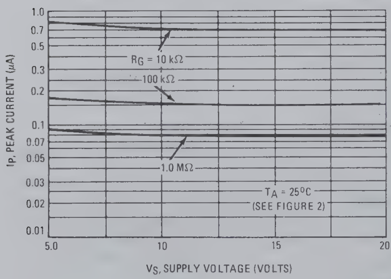
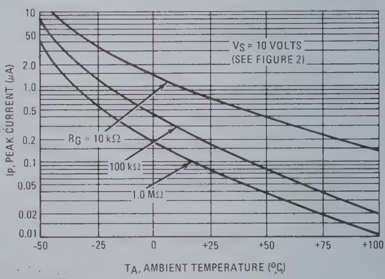
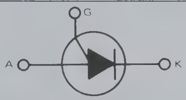


FIGURE 14 – EFFECT OF TEMPERATURE AND R_G



MPU6027
MPU6028



PROGRAMMABLE UNIJUNCTION TRANSISTORS

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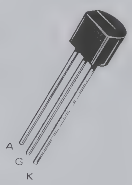
- Programmable — R_{BB}, η, I_V and I_P.
- Low On-State Voltage — 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current — 10 nA Maximum
- High Peak Output Voltage — 11 Volts Typical
- Low Offset Voltage — 0.35 Volt Typical (R_G = 10 k ohms)



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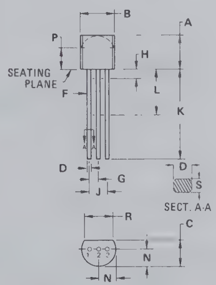


STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-92

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Dissipation (1) Derate Above 25°C	P_F $1/\theta_{JA}$	375 5.0	mW mW/°C
DC Forward Anode Current (2) Derate Above 25°C	I_T	200 2.67	mA mA/°C
DC Gate Current	I_G	+50	mA
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle 20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
Gate to Cathode Reverse Voltage	V_{GKR}	-5.0	Volt
Gate to Anode Reverse Voltage (1)	V_{GAR}	40	Volt
Anode to Cathode Voltage	V_{AK}	+40	Volt
Operating Junction Temperature Range	T_J	-50 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

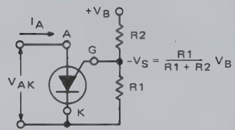
(1) Anode positive, R_{GK} = 1k ohm
Anode negative, R_{GK} = open

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

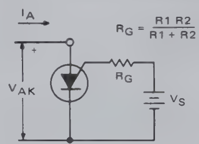
Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Peak Current		2,9,11	I_P				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU6027			–	1.25	2.0	
	MPU6028			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	MPU6027			–	4.0	5.0	
	MPU6028			·	0.70	1.0	
Offset Voltage		1	V_T				Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU6027			0.2	0.70	1.6	
	MPU6028			0.2	0.50	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms)	(Both Types)			0.2	0.35	0.6	
Valley Current		1,4,5,	I_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU6027				18	50	
	MPU6028				18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	MPU6027			70	270	–	
	MPU6028			25	270	–	
Gate to Anode Leakage Current		–	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1.0	10	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	3.0	–	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}		5.0	50	nAdc
Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	–	0.8	1.5	Volts
Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	11	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

2.3

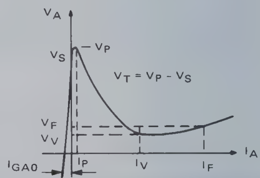
FIGURE 1 — ELECTRICAL CHARACTERIZATION



1A — Programmable Unijunction with "Program" Resistors R1 and R2



1B — Equivalent Test Circuit for Figure 1A used for electrical characteristics testing (also see Figure 2)



1C — Electrical Characteristics

FIGURE 2 — PEAK CURRENT (I_P) TEST CIRCUIT

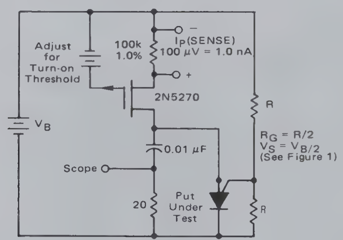
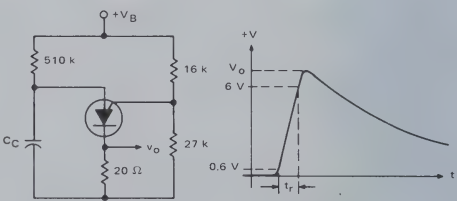


FIGURE 3 — V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

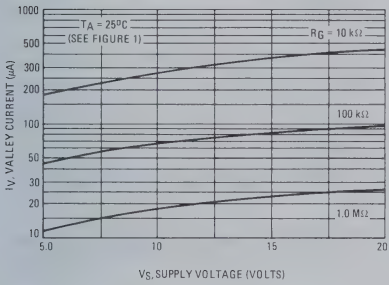
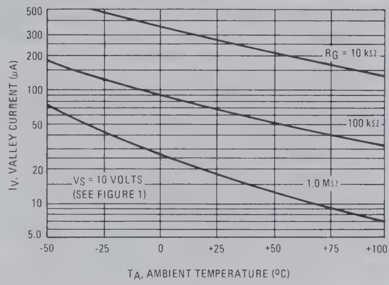


FIGURE 5 – EFFECT OF TEMPERATURE



2.3

FIGURE 6 – FORWARD VOLTAGE

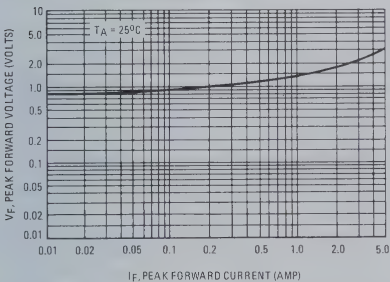


FIGURE 7 – PEAK OUTPUT VOLTAGE

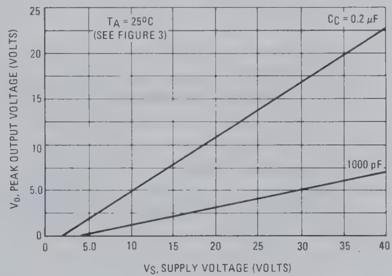
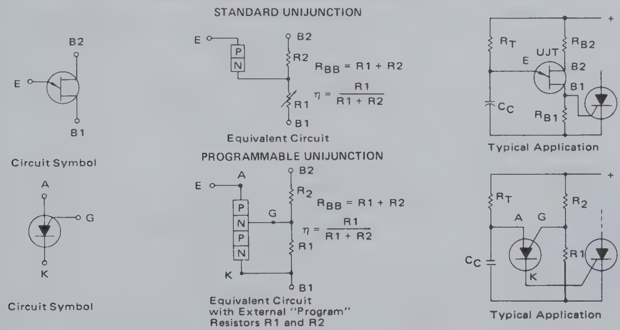


FIGURE 8 – STANDARD UNIJUNCTION COMPARED TO PROGRAMMABLE UNIJUNCTION



TYPICAL PEAK CURRENT BEHAVIOR

MPU6027

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

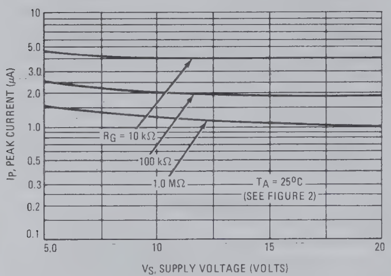
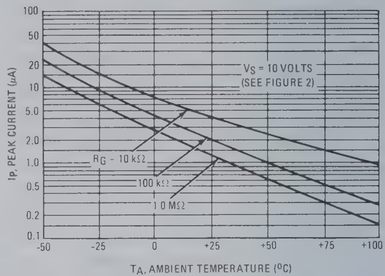


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



MPU6028

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

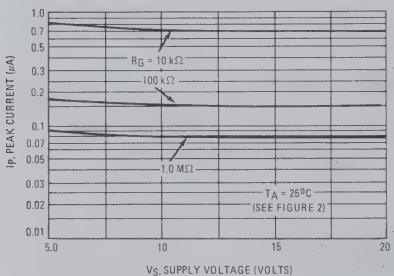
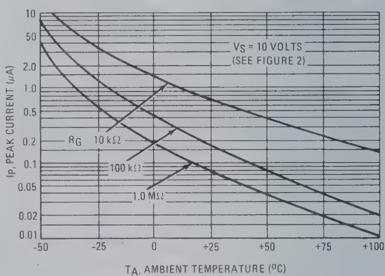
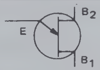


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



MOTOROLA



PN UNIJUNCTION TRANSISTORS

SILICON ANNULAR UNIJUNCTION TRANSISTORS

. . . designed for economical, general purpose use in pulse, timing, oscillator and thyristor trigger circuits.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current**	i_e	1.0	Amp
Emitter Reverse Voltage	V_{EB2}	30	Volts
Interbase Voltage Based upon Power Dissipation at T_A = 25°C	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Derate 3.0 mW/°C increase in ambient temperature.

**Duty Cycle ≤ 1%, PRR = 10 PPS (See Figure 5).

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

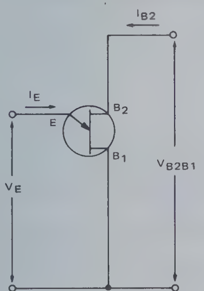
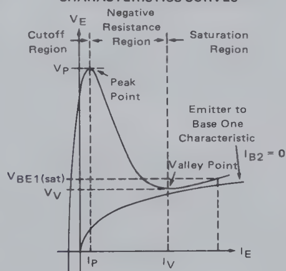
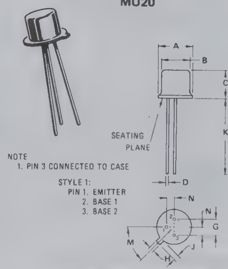


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES



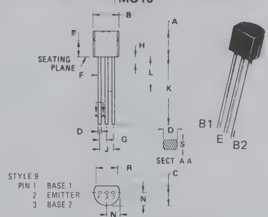
MU20



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	-	0.500	
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A-01
(TO-18 Outline
Except for Lead Position)

MU10



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	-	2.54	-	0.100
J	2.41	2.67	0.095	0.105
K	12.70	-	0.500	-
L	6.35	-	0.250	-
N	2.03	2.92	0.080	0.115
P	2.92	-	0.115	-
R	3.43	-	0.135	
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply

CASE 29-02
(TO-92)
Lead Forms 5 and 18
Shown on Next Page

2.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio* (Test Circuit Figure 4) (V_{B2B1} = 10 V)	η	0.50	–	0.85	–
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)	r_{BB}	4.0	–	10	kΩ
Emitter Saturation Voltage** (V_{B2B1} = 10 V, I_E = 50 mA)	$V_{EB1(sat)}$	–	2.0	–	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)	$I_{B2(mod)}$	–	–	50	mA
Emitter Reverse Current (V_{EB2} = 30 V, I_{B1} = 0)	I_{EB20}	–	–	1.0	µA
Peak-Point Emitter Current (V_{B2B1} = 25 V)	I_P	–	–	5.0	µA
Valley-Point Current** (V_{B2B1} = 20 V, R_{B2} = 100 Ohms)	I_V	1.0	–	–	mA
Base-One Peak Pulse Voltage (Test Circuit Figure 3)	V_{OB1}	3.0	–	–	Volts

* η, intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.45 volt at 25°C @ I_F = 10 µA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

** Pulse Test: Pulse Width ≈ 300 µs, Duty Cycle ≤ 2.0% to avoid internal heating, which may result in erroneous readings.

2.3

FIGURE 3 – V_{OB1} TEST CIRCUIT

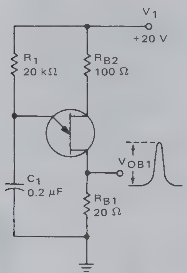
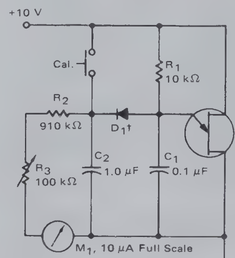
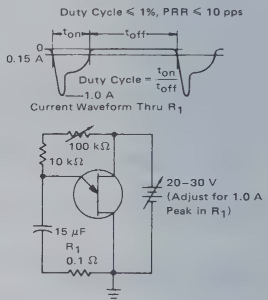


FIGURE 4 – η TEST CIRCUIT

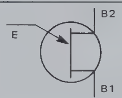


† D_1 diode with the following characteristics:
V_F = 0.45 V @ I_F = 10 µA
I_R ≤ 2.0 µA @ V_R = 20 V

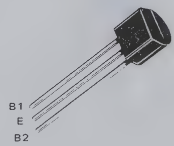
FIGURE 5 – PRR TEST CIRCUIT AND WAVEFORM



MOTOROLA



PN UNIJUNCTION TRANSISTOR

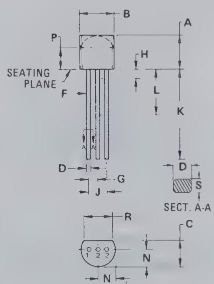


2.3

SILICON UNIJUNCTION TRANSISTOR

. . . designed for use in pulse and timing circuits, sensing circuits and thyristor trigger circuits.

- Low Peak Point Current — 5.0 μA (Max)
- Low Emitter Reverse Current — 12 μA (Max)
- Passivated Surface for Reliability and Uniformity
- TO-18 Lead Form Available Upon Request



STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H		2.54		0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	-
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
RMS Emitter Current	$I_{E(RMS)}$	50	mA
Peak Pulse Emitter Current (2)	i_e	2.0	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
RMS Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	300 3.0	mW mW/°C
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	333	°C/W

(1) The total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry.
(2) Capacitor discharge — 10 μF or less, 30 volts or less.

2.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) (Note 1)	η	0.56	–	0.75	–
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)	r_{BB}	4.7	7.0	9.1	kΩ
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = −55°C to +125°C)	$\alpha_{r_{BB}}$	0.1	–	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) (Note 2)	$V_{EB1(sat)}$	–	3.5	–	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)	$I_{B2(mod)}$		15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	I_{EB2O}	–	0.005	12	μA
Peak Point Emitter Current (V_{B2B1} = 25 V)	I_P	–	1.0	5.0	μA
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) (Note 2)	I_V	4.0	6.0	–	mA
Base-One Peak Pulse Voltage (Note 3, Figure 3)	V_{OB1}	3.0	5.0	–	Volts

Notes

(1) Intrinsic standoff ratio, η, is defined by equation

$$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
$V_{(EB1)}$ = Emitter to Base-One Junction Diode Drop (≈0.5 V @ 10 μA)

(2) Use pulse techniques PW ≈ 300 μs, duty cycle ≤ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings

(3) Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1
UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

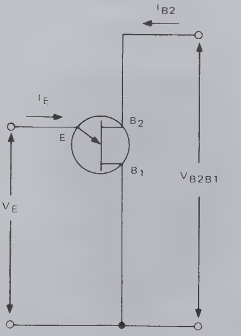


FIGURE 2
STATIC EMITTER CHARACTERISTIC CURVES
(Exaggerated to Show Details)

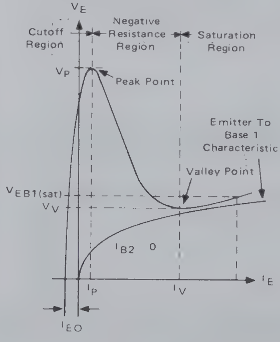
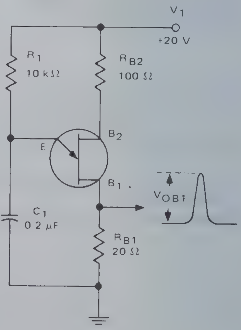
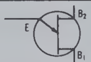


FIGURE 3 – V_{OB1} TEST CIRCUIT
(Typical Relaxation Oscillator)



MOTOROLA

MU4891 thru MU4894



SILICON PLASTIC UNIJUNCTION TRANSISTORS

. . . designed for military and industrial use in pulse, timing, triggering, sensing, and oscillator circuits. The annular process provides low leakage current, fast switching and low peak-point currents as well as outstanding reliability and uniformity.

Recommended usage includes:

- Long-time Delay Circuits - MU4894
- Silicon Controlled Rectifier Triggering Circuits - MU4893
- High-frequency Relaxation-Oscillator Circuits - MU4892
- General-Purpose Unijunction Applications - MU4891

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

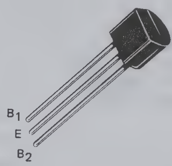
Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D	300	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current**	i_e	1.0**	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Storage Temperature Range	T_{stg}	–65 to +150	°C

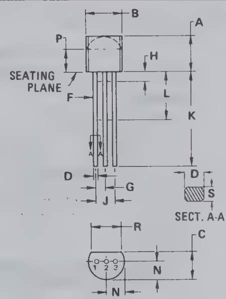
*Derate 3.0 mW/°C increase in ambient temperature. Total power dissipation (available power to Emitter and Base-Two) must be limited by external circuitry. Interbase voltage (V_{B2B1}) limited by power dissipation,

$$V_{B2B1} = \sqrt{R_{BB} \cdot P_D}$$

** Capacitance discharge current must fall to 0.37 Amp within 3.0 ms and PRR ≤ 10 PPS.

PN UNIJUNCTION TRANSISTORS





STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

2.3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio	η				–
(V_{B2B1} = 10 V) Note 1 MU4892		0.51	–	0.69	
MU4891, MU4893		0.55	–	0.82	
MU4894		0.74	–	0.86	
Interbase Resistance	R_{BB}				k ohms
(V_{B2B1} = 3.0 V, I_E = 0) MU4891, MU4892		4.0	7.0	9.1	
MU4893, MU4894		4.0	7.0	12.0	
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = –65°C to +100°C)	αR_{BB}	0.1	–	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) Note 2	$V_{EB1(sat)}$	–	2.5	4.0	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)	$I_{B2(mod)}$	10	15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	I_{EB2O}	–	5.0	10	nA
Peak Point Emitter Current	I_P				µA
(V_{B2B1} = 25 V) MU4891			0.6	5.0	
MU4892, MU4893		–	0.6	2.0	
MU4894		–	0.6	1.0	
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 Ohms) Note 2	I_V				mA
MU4891, MU4893, MU4894		2.0	4.0	–	
MU4892		2.0	3.0	–	
Base-One Peak Pulse Voltage (Note 3, Figure 3)	V_{OB1}				Volts
MU4891, MU4892, MU4894		3.0	5.0	–	
MU4893		6.0	8.0	–	

NOTES

1. Intrinsic standoff ratio.
η, is defined by equation:

$$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
$V_{(EB1)}$ = Emitter to Base-One Junction Diode Drop ($\approx$0.5 V @ 10 µA)

2. Use pulse techniques: PW $\approx$ 300 µs duty cycle $\leq$2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

3. Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

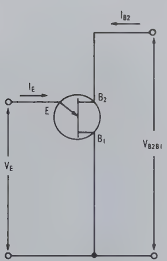


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES

(Exaggerated to Show Details)

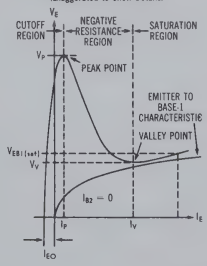
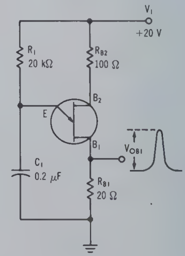


FIGURE 3 — V_{OB1} TEST CIRCUIT

(Typical Relaxation Oscillator)



S2800
series

MOTOROLA

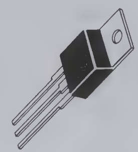
REVERSE BLOCKING TRIODE THYRISTORS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 600 Volts

SILICON CONTROLLED RECTIFIERS

10 AMPERES RMS
100–600 VOLTS



2.3

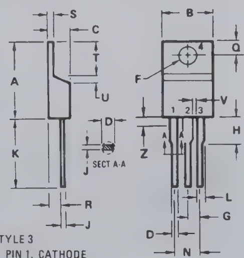
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage (1) Peak Repetitive Off-State Voltage (1)	V_{RRM} V_{DRM}		Volts
S2800A		100	
S2800B		200	
S2800D		400	
S2800M		600	
Non-Repetitive Peak Reverse Voltage Non-Repetitive Off-State Voltage	V_{RSM} V_{DSM}		Volts
S2800A		125	
S2800B		250	
S2800D		500	
S2800M		700	
RMS Forward Current (All Conduction Angles) $T_C = 75^oC$	$I_{T(RMS)}$	10	Amps
Peak Forward Surge Current (1 Cycle, Sine Wave, 60 Hz, $T_C = 80^oC$)	I_{TSM}	100	Amps
Circuit Fusing Considerations (T_J = -65 to +100^{o}C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
Forward Peak Gate Power ($t \leqslant 10\ \mu s$)	P_{GM}	16	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Operating Junction Temperature Range	T_J	-40 to +100	^{o}C
Storage Temperature Range	T_{stg}	-40 to +150	^{o}C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	^{o}C/W

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.



STYLE 3
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220 AB
All JEDEC dimensions and notes apply

2.3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}, $T_C = 100^oC$)	I_{DRM}	–	–	2	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}, $T_C = 100^oC$)	I_{RRM}	–	–	2	mA
Instantaneous On-State Voltage (I_{TM} = 30 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_T	–	1.7	2	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 30 Ohms)	I_{GT}	–	8	15	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 30 Ohms)	V_{GT}	–	0.9	1.5	Volts
Holding Current (Gate Open, V_D = 12 Vdc, I_T = 150 mA)	I_H	–	10	20	mA
Gate Controlled Turn-on Time (V_D = Rated V_{DRM}, I_{TM} = 2 A, I_{GR} = 80 mA)	t_{gt}	–	1.6	–	μs
Circuit Commutated Turn-Off Time ($V_D = V_{DRM}$, I_{TM} = 2 A, Pulse Width = 50 μs, dv/dt = 200 V/μs, di/dt = 10 A/μs, $T_C = 75^oC$)	tq	–	25	–	μs
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Rise, $T_C = 100^oC$)	dv/dt	–	100	–	V/μs

FIGURE 1 — CURRENT DERATING

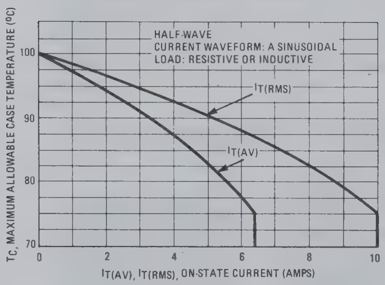
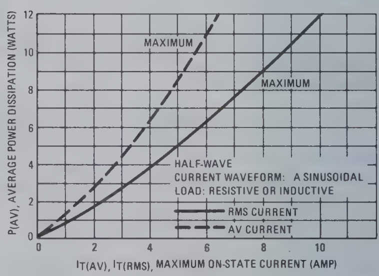


FIGURE 2 — POWER DISSIPATION



MOTOROLA

S6200
S6210
S6220
series

SILICON CONTROLLED RECTIFIERS

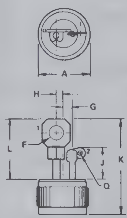
. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

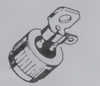
- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 200 Amp
- Low Forward "On" Voltage — 1.2 V (Typ) @ I_{TM} = 20 Amp
- Practical Level Triggering and Holding Characteristics — 10 mA (Typ) @ T_C = 25°C
- Rugged Construction in Either Pressfit, Stud or Isolated Stud Package
- Glass Passivated Junctions for Maximum Reliability

THYRISTORS

20 AMPERES RMS
100 thru 600 VOLTS

S6200 Series



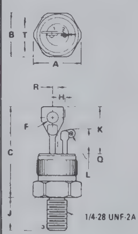


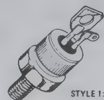
STYLE 1:
1. CATHODE
2 GATE
CASE ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12 83	0 501	0.505
F	–	4.06	–	0 160
G	2.16	2.41	0.085	0.095
H	1.60	2 01	0 063	0.079
J	7.62	8 89	0.300	0.350
K	–	26 67	–	1.050
L	–	17 02	–	0.670
Q	1.40	2.16	0.055	0.085

CASE 310-01

S6210 Series



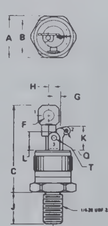


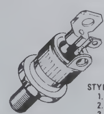
STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15 60	0.604	0 614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1 190
F	3.43	4 06	0 135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0 420	0.455
K	15.75	17 02	0 620	0.670
L	7.62	8.89	0 300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0 505

CASE 263-03

S6220 Series





STYLE 1:
1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2 01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

CASE 311-01

2.3

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Repetitive Peak Off-State Voltage(1) Repetitive Peak Reverse Voltage(1)		V_{DROM} V_{RROM}		Volts
S6200, S6210, S6220	A		100	
S6200, S6210, S6220	B		200	
S6200, S6210, S6220	D		400	
S6200, S6210, S6220	M		600	
Non-Repetitive Peak Off-State Voltage(1) Non-Repetitive Peak Reverse Voltage(1)		V_{DSOM} V_{DROM}		Volts
S6200, S6210, S6220	A		150	
S6200, S6210, S6220	B		250	
S6200, S6210, S6220	D		500	
S6200, S6210, S6220	M		700	
RMS On-State Current (T_C = 75°C)		$I_{T(RMS)}$	20	Amp
Peak Non-Repetitive Surge Current (One Full cycle of surge current at 60 Hz, preceded and followed by rated current, T_C = 75°C)		I_{TSM}	200	Amp
Circuit Fusing Considerations (T_J = –65 to +100°C) (t = 1.0 to 8.3 ms)		I^2t	170	A^2s
Peak Gate Power (10 μs Max)		P_{GM}	40	Watts
Average Gate Power		$P_{G(AV)}$	0.5	Watt
Operating Junction Temperature Range		T_J	–65 to +100	°C
Storage Temperature Range		T_{stg}	–65 to +150	°C
Stud Torque		—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case	S6200	$R_{\theta JC}$	1.2	°C/W
	S6210, S6220		1.4	

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

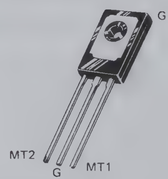
Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Breakover Voltage (Gate Open, T_C = 100°C)	$V_{(BO)O}$				Volts
S6200, S6210, S6220 A		100	–	–	
S6200, S6210, S6220 B		200	–	–	
S6200, S6210, S6220 D		400	–	–	
S6200, S6210, S6220 M		600	–	–	
Peak Blocking Current (Rated V_{DROM} @ T_C = 100°C)	I_{DOM}, I_{RROM}	–	–	2	mA
Peak On-State Voltage (I_T = 100 A Peak)	V_T	–	–	2.4	Volts
Gate Trigger Current, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 30 Ohms	I_{GT}	–	–	15	mA
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 30 Ohms	V_{GT}	–	–	2	Volts
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open	I_{HO}	–	–	20	mA
Gate Controlled Turn-On Time ($V_D = V_{(BO)O}$, I_T = 30 A Peak, I_{GT} = 200 mA, Rise Time = 0.1 μs)	t_{gt}	–	2	–	μs
Critical Rate-of-Rise of Off-State Voltage ($V_D = V_{(BO)O}$, Exponential Voltage Rise, Gate Open, T_C = 100°C)	dv/dt				V/μs
S6200, S6210, S6220 A,D		10	100	–	
S6200, S6210, S6220 B		10	150	–	
S6200, S6210, S6220 M		10	75	–	

SC136 series

MOTOROLA

TRIACS

3 AMPERES RMS
200–600 VOLTS



2.3

BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

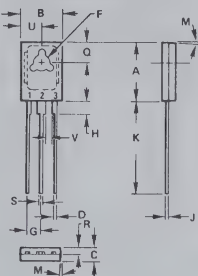
- Low Off-State Leakage Currents
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Rugged Industry Proven Thermopad Construction
- TO-5 Lead Form Available

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_C = 110°C)	V_{DRM}		Volts
SC136 B		200	
SC136 C		300	
SC136 D		400	
SC136 E		500	
SC136 M		600	
RMS On-State Current (T_C = 65°C)	$I_{T(RMS)}$	3.0	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	30	Amp
Circuit Fusing (t = 1 to 8.3 ms)	I^2t	3.6	A^2s
Critical Rate of Rise of On-State Current	di/dt	5.0	A/μs
Peak Gate Power	P_{GM}	5.0	Watts
Average Gate Power	$P_{G(AV)}$	0.1	Watt
Peak Gate Voltage	V_{GM}	5.0	Volts
Operating Junction Temperature Range	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W
Junction to Ambient	$R_{\theta JA}$	75	°C/W



STYLE 7:
PIN 1. MT1
2. GATE
3. MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	-	0.040	-

CASE 77-04
TO-126

***ELECTRICAL CHARACTERISTICS** (T_C = +25°C, either polarity of MT2 to MT1 voltage, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current (V_D = Rated V_{DRM}, Gate Open) T_C = +25°C / T_C = +110°C	I_{DRM}	— / —	— / —	10 / 500	μA
Peak On-State Voltage (I_{TM} = 5A, Pulse Width = 1 ms, Duty Cycle < 2%)	V_{TM}	—	—	1.8	Volts
DC Gate Trigger Current (V_D = 6 Vdc, R_L = 50 Ohms) MT2 (+), G (+); MT2 (−), G (−); MT2 (+), G (−) T_C = 25°C	I_{GT}	—	—	25	mAdc
(V_D = 12 Vdc, R_L = 50 Ohms) MT2 (+), G (+); MT2 (−), G (−), MT2 (+) G (−) T_C = −40°C		—	—	50	
DC Gate Trigger Voltage (V_D = 12 Vdc, R_L = 50 Ohms) MT2 (+), G (+); MT2 (−), G (−); MT2 (+), G (−) T_C = 25°C / T_C = −40°C	V_{GT}	— / —	— / —	2.0 / 3.0	Vdc
(V_D = Rated V_{DRM}, All Modes) T_C = 110°C		0.2	—	—	
Holding Current (V_D = 24 Vdc, R_L = 200 Ohms, Gate Open) T_C = 25°C / T_C = −40°C	I_H	— / —	— / —	50 / 100	mAdc
Latching Current (V_D = 24 Vdc) Trigger Source: 5 V, 50 Ohms, T_C = 25°C MT2 (+), G (+); MT2 (−), G (−); / MT2 (+), G (−)	I_L	— / —	— / —	50 / 100	mAdc
Trigger Source: 10 V, 50 Ohms, T_C = −40°C MT2 (+), G (+); MT2 (−), G (−); / MT2 (+), G (−)		— / —	— / —	100 / 200	
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Gate Open) T_C = 110°C	dv/dt	—	15	—	Volts/μs
Critical Rate-of-Rise of Commutating Voltage (V_D = Rated V_{DRM}, $I_{T(RMS)}$ = 3 A, di/dt = 1.6 A/ms, Gate Open) T_C = 65°C	dv/dt(c)	—	5	—	Volts/μs

NOTE 1. Torque rating applies with use of compression washer (B52200F006). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-290 B)
For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C. For optimum results, an activated flux (oxide removing) is recommended.

FIGURE 1 — RMS CURRENT DERATING

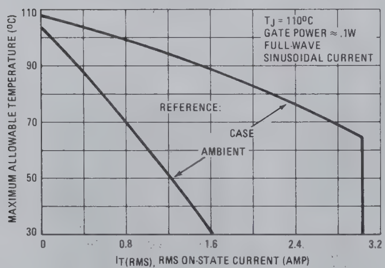
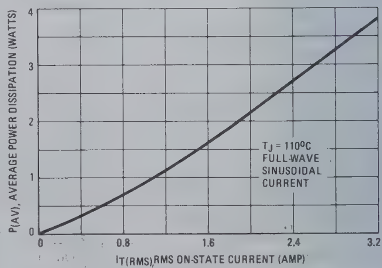


FIGURE 2 — MAXIMUM POWER DISSIPATION



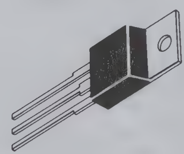
2.3

SC141
SC146

MOTOROLA

TRIACS

6 AND 10 AMPERES RMS
200–600 VOLTS

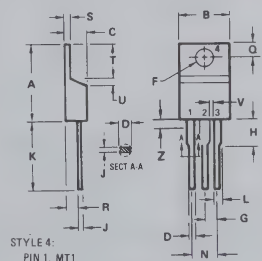


2.3

BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Triggering Specified in Three Quadrants
- Blocking Voltage to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability



STYLE 4:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220 AB
All JEDEC dimensions and notes apply

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage, Gate Open, SC141/SC146 B	V_{DRM}	200	Volts
D		400	
E		500	
M		600	
RMS On-State Current $T_C = 80^oC$ SC141	$I_{T(RMS)}$	6	Amp
SC146		10	
Peak Non-Repetitive Surge Current One Full Cycle, 60 Hz SC141	I_{TSM}	80	Amp
SC146		120	
Circuit Fusing Considerations t = 8.3 ms SC141	I^2t	26.5	A^2s
SC146		60	
Peak Gate Power (Pulse Width = 10 μs)	P_{GM}	10	Watts
Average Gate Power ($T_C = +80^oC$, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current (Pulse Width = 10 μs)	I_{GM}	3.5	Amp
Peak Gate Voltage	V_{GM}	10	Volts
Operating Junction Temperature Range	T_J	-40 to +100	^oC
Storage Temperature Range	T_{stg}	-40 to +125	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case SC141	$R_{\theta JC}$	2.2	$^oC/W$
SC146		1.5	

2.3

ELECTRICAL CHARACTERISTICS (T_C = +25°C, Either Polarity of MT2 - to - MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current	I_{DRM}				mA
V_D = Rated V_{DRM}					
Gate Open-Circuited T_C = +25°C		–	–	0.1	
T_C = +100°C		–	–	0.5	
Peak On-State Voltage	V_{TM}				Volts
Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%.					
SC141 I_{TM} = 8.5 A Peak		–	–	1.83	
SC146 I_{TM} = 14 A Peak		–	–	1.65	
Critical Rate of Rise of Off-State Voltage	dv/dt	–	50	–	Volts/µs
V_D = Rated V_{DRM}, Gate Open-Circuited,					
Exponential Waveform T_C = +100°C					
Critical Rate-of-Rise of Commutating Off-State Voltage (1)	dv/dt(c)				Volts/µs
$I_{T(RMS)}$ = Rated $I_{T(RMS)}$, V_D = Rated V_{DRM}, T_C = +80°C					
Gate Open-Circuited					
SC141 Commutating di/dt = 3.2 A/ms		4	–	–	
SC146 Commutating di/dt = 5.4 A/ms		4	–	–	
DC Gate Trigger Current	I_{GT}				mAdc
V_D = 12 Vdc, Trigger Mode					
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 100 Ohms		–	–	50	
MT2 (+), Gate (–); R_L = 50 Ohms		–	–	50	
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 50 Ohms T_C = –40°C		–	–	80	
MT2 (+), Gate (–); R_L = 25 Ohms; T_C = –40°C		–	–	80	
DC Gate Trigger Voltage	V_{GT}				Vdc
V_D = 12 Vdc, Trigger Mode					
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 100 Ohms		–	–	2.5	
MT2 (+), Gate (–); R_L = 50 Ohms		–	–	2.5	
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 50 Ohms T_C = –40°C		–	–	3.5	
MT2 (+), Gate (–); R_L = 25 Ohms; T_C = –40°C		–	–	3.5	
V_D = Rated V_{DRM}; R_L = 1000 Ohms; All Polarities T_C = +100°C		0.2	–	–	
Holding Current	I_H				mAdc
V_D = 24 Vdc, I_T = 0.5A					
Pulse Width = 1 ms, Duty Cycle ≤ 2%.					
Gate Trigger Source = 7 V, 20 Ohms T_C = +25°C		–	–	50	
T_C = –40°C		–	–	100	
Latching Current	I_L				mAdc
V_D = 24 Vdc					
Gate Trigger Source = 15 V, 100 Ohms, Trigger Mode					
MT2 (+), Gate (+); MT2 (–), Gate (–)		–	–	100	
MT2 (+), Gate (–)		–	–	200	
MT2 (+), Gate (+); MT2 (–), Gate (–); T_C = –40°C		–	–	200	
MT2 (+), Gate (–); T_C = –40°C		–	–	400	

FIGURE 1 — RMS CURRENT DERATING

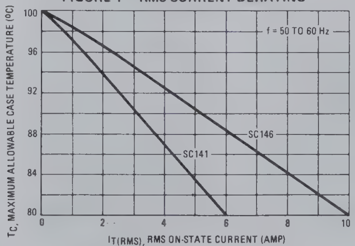
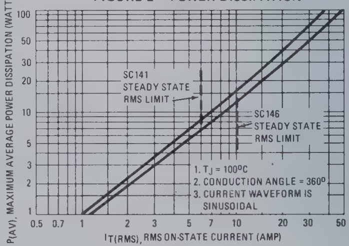


FIGURE 2 — POWER DISSIPATION



MOTOROLA

SC250
SC250( )3
SC251

TRIACS

15 AMPERES RMS
200–600 VOLTS

BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 3 Quadrants

MAXIMUM RATINGS

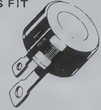
Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage	V_{DRM}		Volts
SC251B, SC250B, SC250B3		200	
SC251D, SC250D, SC250D3		400	
SC251E, SC250E, SC250E3		500	
SC251M, SC250M, SC250M3		600	
RMS On-State Current	$I_{T(RMS)}$	15	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	100	Amp
Circuit Fusing Considerations	I^2t		A^2s
t = 1 ms		20	
t = 8.3 ms		41.5	
Peak Gate Power	P_{GM}	10	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Gate Power (Pulse Width = 10 μs)	I_{GM}	2	Amp
Operating Junction Temperature Range	T_J	-40 to +115	°C
Storage Temperature Range	T_{stg}	-40 to +125	°C
Stud Torque	—	30	in. lb.

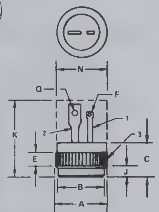
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
SC250, SC251		2	
SC250 ( )3		2.3	

SC251
PRESS FIT

STYLE 3:
TERM. 1. GATE
2. MAIN TERMINAL 1
3. MAIN TERMINAL 2



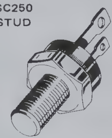


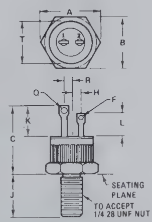
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160

CASE 174-03

SC250
STUD

STYLE 3
TERM. 1 MAIN TERMINAL 1
2 GATE
STUD MAIN TERMINAL 2



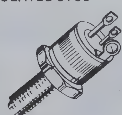


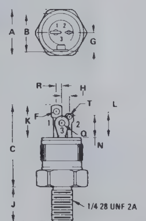
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

CASE 175-02

SC250( )3
ISOLATED STUD

STYLE 2.
PIN 1 MAIN TERMINAL 1
2. GATE
3 MAIN TERMINAL 2
STUD ISOLATED





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C		26.16	–	1.030
F	1.65	4.06	0.065	0.160
G		6.48		0.255
H	2.16	2.41	0.085	0.095
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
R	1.52	1.78	0.060	0.070
T	0.89	2.16	0.035	0.085

CASE 235-02

2.3

2.3

ELECTRICAL CHARACTERISTICS

(T_C = +25°C unless otherwise noted. Values apply for either polarity of Main Terminal 2 Characteristics referenced to Main Terminal 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current V_D = Rated V_{DRM} Gate Open-Circuited T_C = +25°C T_C = +115°C	I_{DRM}	 – –	 – –	 0.1 0.5	mA
Peak On-State Voltage I_{TM} = 21 A, Pulse Width = 1 ms, Duty Cycle ≤ 2%.	V_{TM}	–	–	1.65	Volts
Critical Rate of Rise of Off-State Voltage Rated V_{DRM}, Gate Open-Circuited, Exponential Waveform, T_C = +115°C	dv/dt	100	–	–	Volts/µs
Critical Rate-of-Rise of Commutating Off-State Voltage (1) $I_{T(RMS)}$ = Rated RMS On-State Current, V_D = V_{DRM} Gate Open-Circuited, Commutating di/dt = 8 A/ms SC250, SC251 T_C = +84°C SC250( )3 T_C = +78°C	dv/dt(C)	 4 4	 – –	 – –	Volts/µs
DC Gate Trigger Current V_D = 12 Vdc MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 100 Ohms MT2 (+), Gate (–); R_L - 50 Ohms	I_{GT}	 – –	 – –	 50 50	mAdc
DC Gate Trigger Current V_D = 12 Vdc, T_C = –40°C MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 50 Ohms MT2 (+), Gate (–); R_L = 25 Ohms	I_{GT}	 – –	 – –	 80 80	mAdc
DC Gate Trigger Voltage V_D = 12 Vdc MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 100 Ohms MT2 (+), Gate (–); R_L = 50 Ohms	V_{GT}	 – –	 – –	 2.5 2.5	Vdc
DC Gate Trigger Voltage V_D = 12 Vdc, T_C = –40°C MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 50 Ohms MT2 (+), Gate (–); R_L = 25 Ohms	V_{GT}	 – –	 – –	 3.5 3.5	Vdc
DC Gate Non-Trigger Voltage V_D = Rated V_{DRM}, R_L - 1K Ohms, T_C = 115°C All Trigger Modes	V_{GD}	0.20	–	–	Vdc
Holding Current V_D = 24 Vdc, Peak Initiating Current = 0.5 A, Pulse Width = 0.1 to 10 ms, Gate Trigger Source = 7 V, 20 Ohms T_C = +25°C T_C = –40°C	I_H	 – –	 – –	 50 100	mAdc
Latching Current V_D = 24 Vdc, Gate Trigger Source = 15 V, 100 Ohms, Pulse Width = 50 µs, 5 µs Maximum Rise and Fall Times MT2 (+), Gate (+); MT2 (–), Gate (–); MT2 (+), Gate (–) T_C = 25°C MT2 (+), Gate (+); MT2 (–), Gate (–); MT2 (+), Gate (–) T_C = –40°C	I_L	 – –	 – –	 100 200	mAdc

FIGURE 1 — CURRENT DERATING

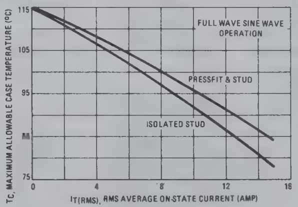
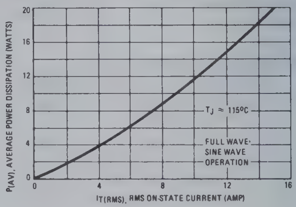


FIGURE 2 — MAXIMUM ON-STATE POWER DISSIPATION



MOTOROLA

SC260
SC260( )3
SC261

TRIACS

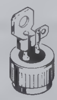
25 AMPERES RMS
200–600 VOLTS

BIDIRECTIONAL TRIODE THYRISTORS

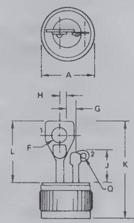
. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 3 Quadrants

SC261



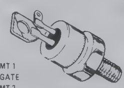
STYLE 2
1 MT 1
2. GATE
CASE. MT 2



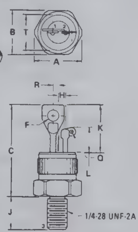
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.52	1.78	0.060	0.070
J	7.62	8.89	0.300	0.350
K	–	26.67	–	1.050
L	–	17 02	–	0.670
Q	1 40	2 16	0.055	0.085

CASE 310-01

SC260



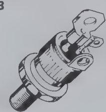
STYLE 2
PIN 1 MT 1
2 GATE
3. MT 2



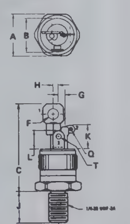
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1 190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

SC260( )3



STYLE 2
1 MT 1
2 GATE.
3 MT 2



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14 00	14 20	0.551	0 559
B	12 73	12 83	0 501	0 505
C		32 51		1 280
F	-	4.06	–	0.160
G	2 16	2.41	0.085	0.095
H	1 60	2.01	0.063	0.079
J	10.67	11 56	0.420	0.455
K	7 62	8.89	0 300	0.350
L	6 48	6 99	0 255	0.275
Q	1 40	2 16	0.055	0.085
T	3 43	3 81	0 135	0 150

CASE 311-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage $T_C = -40^oC$ to $+115^oC$ SC260B, SC260B3, SC261B SC260D, SC260D3, SC261D SC260E, SC260E3, SC261E SC260M, SC260M3, SC261M	V_{DRM}	 200 400 500 600	Volts
RMS On-State Current	$I_{T(RMS)}$	25	Amp
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz)	I_{TSM}	250	Amp
Circuit Fusing Considerations t = 1.0 ms t = 8.3 ms	I^2t	 150 260	A^2s
Peak Gate Power (Pulse Width = 10 μs)	P_{GM}	10	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Gate Current	I_{GM}	2	Amp
Operating Junction Temperature Range	T_J	-40 to +115	^oC
Storage Temperature Range	T_{stg}	-40 to +125	^oC
Stud Torque	–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case SC260, SC261 SC260( )3	$R_{\theta JC}$	 1.8 1.95	$^oC/W$

2.3

ELECTRICAL CHARACTERISTICS

(T_C = +25°C unless otherwise noted. Values apply for either polarity of Main Terminal 2 characteristics referenced to Main Terminal 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current V_D = Rated V_{DRM} = Peak Off-State Voltage, Gate Open-Circuited T_C = +25°C T_C = +115°C	I_{DRM}	 – –	 – –	 0.2 1	mA
Peak On-State Voltage I_{TM} = 35 A Peak, Pulse Width = 1 ms, Duty Cycle ≤ 2%.	V_{TM}	–	–	1.58	Volts
Critical Rate of Rise of Off-State Voltage Rated V_{DRM}, Gate Open-Circuited, Exponential Waveform T_C +115°C	dv/dt	50	–	–	Volts/µs
Critical Rate-of-Rise of Commutating Off-State Voltage $I_{T(RMS)}$ = Rated RMS On-State Current V_{DRM} = Rated Peak Off-State Voltage, Gate Open-Circuited, Commutating di/dt - 13.5 A/ms, T_C = +80°C	dv/dt(c)	5	–	–	Volts/µs
DC Gate Trigger Current V_D = 12 Vdc MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 100 Ohms MT2 (+), Gate (–); R_L = 50 Ohms	I_{GT}	 – –	 – –	 50 50	mAdc
DC Gate Trigger Current V_D = 12 Vdc, T_C = –40°C MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 50 Ohms MT2 (+), Gate (–); R_L = 25 Ohms	I_{GT}	 – –	 – –	 80 80	
DC Gate Trigger Voltage V_D = 12 Vdc MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 100 Ohms MT2 (+), Gate (–); R_L = 50 Ohms	V_{GT}	 – –	 – –	 2.5 2.5	Vdc
DC Gate Trigger Voltage V_D = 12 Vdc, T_C = –40°C MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 50 Ohms MT2 (+), Gate (–); R_L = 25 Ohms	V_{GT}	 – –	 – –	 3.5 3.5	Vdc
DC Gate Non-Trigger Voltage V_D = Rated V_{DRM}, R_L = 1K Ohms, T_C = 115°C All Trigger Modes	V_{GD}	0.25	–	–	Vdc
Holding Current V_D = 24 Vdc, Peak Initiating Current = 0.5A, Pulse Width = 0.1 to 10 ms, Gate Trigger Source = 7 V, 20 Ohms T_C = 25°C T_C = –40°C	I_H	 – –	 – –	 75 100	mAdc
Latching Current V_D = 24 Vdc, Gate Trigger Source = 15 V, 100 Ohms, Pulse Width = 50 µs, 5 µs Maximum Rise and Fall Times MT2 (+), Gate (+); MT2 (–), Gate (–) T_C = 25°C MT2 (+), Gate (–) T_C = 25°C MT2 (+), Gate (+); MT2 (–), Gate (–); T_C = –40°C MT2 (+), Gate (–) T_C = –40°C	I_L	 – – – –	 – – – –	 100 200 200 400	mAdc

FIGURE 1 — CURRENT DERATING

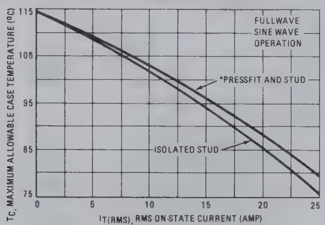
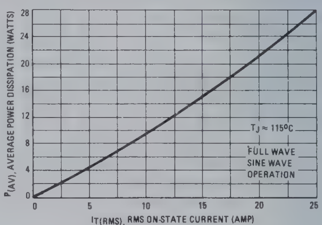


FIGURE 2 — MAXIMUM ON-STATE POWER DISSIPATION



MOTOROLA

T2322
T2323
series

SENSITIVE GATE TRIACS

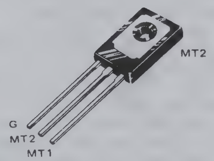
2.5 AMPERES RMS
50-500 VOLTS

2.3

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for ac power switching. The gate sensitivity of these triacs permits the use of economical transistorized or integrated circuit control circuits, and it enhances their use in low-power phase control and load-switching applications.

- Very High Gate Sensitivity
- Low On-State Voltage at High Current Levels
- Glass-Passivated Chip for Stability
- Small, Rugged Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability



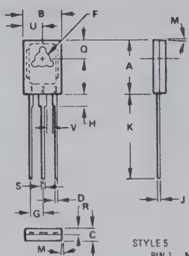
MAXIMUM RATING (Apply for T_J = -40 to 100°C unless otherwise noted)

Rating	Suffix	Symbol	Value	Unit
Peak Repetitive Off-State Voltage T2322, T2323	 F A B C D E	V_{DRM}	 50 100 200 300 400 500	Volts
RMS On-State Current (T_C = 70°C) (Full-cycle sine wave 50 to 60 Hz)		$I_{T(RMS)}$	2.5	Amps
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz)		I_{TSM}	25	Amps
Circuit Fusing ($t \leqslant 8.3$ ms)		I^2t	2.6	A^2s
Peak Gate Power (1.0 μs)		P_{GM}	10	Watts
Average Gate Power (T_C = 60°C + 38.3 ms)		$P_{G(AV)}$	0.15	Watt
Peak Gate Current (1.0 μs)		I_{GM}	0.5	Amp
Operating Junction Temperature Range		T_J	-40 to +110	°C
Storage Temperature Range		T_{stg}	-40 to +150	°C
Mounting Torque (6-32 Screw), Note 2		—	8.0	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

NOTES
1 Ratings apply for open gate conditions Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage
2 Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent) Mounting torque in excess of 6 in lb does not appreciably lower case-to-sink thermal resistance Main terminal 2 and heatsink contact pad are common
For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C, for 10 seconds Consult factory for lead bending options



STYLE 5
PIN 1. MT1
2. MT2
3. GATE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11 05	0 425	0 435
B	7 49	7 75	0 295	0 305
C	2 41	2 67	0 095	0 105
D	0.51	0 66	0 020	0 026
F	2.92	3 18	0 115	0 125
G	2 31	2 46	0 091	0 097
H	1 27	2 41	0 050	0 095
J	0 38	0 64	0 015	0 025
K	15 11	16 64	0 595	0 655
M	3° TYP		3° TYP	
Q	3 76	4 01	0 148	0 158
R	1 14	1 40	0 045	0 055
S	0 64	0 89	0.025	0 035
U	3 68	3.94	0 145	0 155
V	1 02		0 040	

CASE 77-04
TO-126

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Note 1) (V_D = Rated V_{DRM}, T_J = 100°C)	I_{DRM}	—	0.2	0.75	mA
Peak On-State Voltage (I_{TM} = 10 A Peak) T2323 Series T2322 Series	V_{TM}	 — —	 1.7 1.7	 2.6 2 2	Volts
Gate Trigger Current, Continuous dc (All Modes) (V_D = 12 V, R_L = 30 Ω) T2322 Series MT2(+), G(+); MT2(–), G(–) T2323 Series MT2(+), G(–); MT2(–), G(+) T2323 Series	I_{GT}	 — — — —	 — — — —	 10 25 40	mA
Gate Trigger Voltage, Continuous dc (V_D = 12 Vdc, R_L = 30 Ω, T_C = 25°C) (V_D = V_{DROM}, R_L = 125 Ω, T_C = 100°C)	V_{GT}	 — 0.15	 1.0 —	 2.2 —	Volts
Holding Current (V_D = 12 V, I_{TM} = 150 mA, Gate Open)	I_H	—	15	30	mA
Gate Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 10 A pk, I_G = 60 mA)	t_{gt}	—	1.8	2.5	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 100°C)	dv/dt	10	100	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 3.5 A pk, Commutating di/dt = 1.8 A/ms, Gate Unenergized, T_C = 90°C)	dv/dt(c)	1.0	4.0	—	V/μs

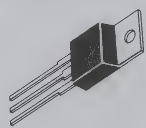
Note 1: Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

T2500

MOTOROLA

TRIACS (THYRISTORS)

6 AMPERES RMS
200—800 VOLTS

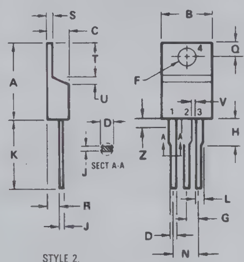


SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability

2.3



STYLE 2.
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221-02
TO-220 AB
All JEDEC dimensions and notes apply

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (1) (T_J = -40 to +100°C) Gate Open T2500 B D M N	V_{DROM}	 200 400 600 800	Volts
On-State Current RMS (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	6	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_C = +80°C)	I_{TSM}	60	Amp
Circuit Fusing Considerations (T_J = -40 to +100°C, t = 1.25 to 10 ms)	I^2t	18	A^2s
Peak Gate Power (T_C = +80°C, Pulse Width = 1 μs)	P_{GM}	16	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.2	Watt
Peak Gate Trigger Current (Pulse Width = 10 μs)	I_{GTM}	4	Amp
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.7	°C/W

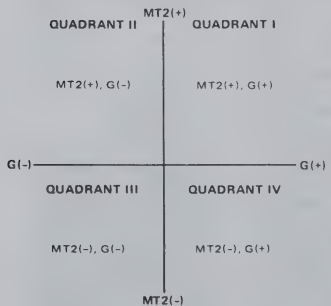
(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current (Either Direction) Rated V_{DROM} @ T_J = 100°C, Gate Open	I_{DROM}	–	–	2	mA
Maximum On-State Voltage (Either Direction) I_T = 30 A Peak	V_{TM}	–	–	2	Volts
Gate Trigger Current, Continuous dc V_D = 12 Vdc, R_L = 12 Ohms V_{MT2} (+), $V_{G(+)}$ V_{MT2} (+), $V_{G(-)}$ V_{MT2} (–), $V_{G(-)}$ V_{MT2} (–), $V_{G(+)}$	I_{GT}	 – – – –	 10 20 15 30	 25 60 25 60	mA
Gate Trigger Voltage, Continuous dc (All Quadrants) V_D = 12 Vdc, R_L = 12 Ohms V_D = V_{DROM}, R_L = 125 Ohms, T_C = 100°C	V_{GT}	 – 0.2	 1.25 –	 2.5 –	Volts
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 150 mA, T_C = 25°C	I_{HO}	–	15	30	mA
Gate Controlled Turn-On Time Rated V_{DROM}, I_T = 10 A, I_{GT} = 160 mA, Rise Time = 0.1 μs	t_{gt}	–	1.6	–	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DROM}, $I_{T(RMS)}$ = 6 A, Commutating di/dt = 3.2 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(C)		10	–	V/μs
Critical Rate of Rise of Off-State Voltage Rated V_{DROM}, Exponential Voltage Rise, Gate Open, T_C = 100°C T2500B T2500D,M,N	dv/dt	 100 75	 – –	 – –	V/μs

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General	
PART NUMBER	MBS4991	MBS4992
V_S	6.0 – 10 V	7.5 9.0 V
I_S	350 μA Max	120 μA Max
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max
Temperature Coefficient	0.02%/°C Typ	

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

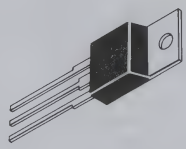
MOTOROLA

T2800
T2802

TRIACS

8 AMPERES RMS
200–600 VOLTS

2.3



BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Blocking Voltage to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- T2800 — Four Quadrant Gating
  T2802 — Two Quadrant Gating

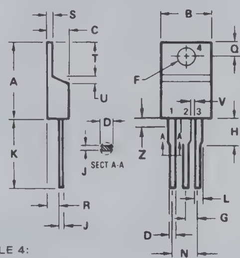
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (1) (T_J = −40 to +100°C) Gate Open	V_{DRM}		Volts
T2800 / T2802 B		200	
C		300	
D		400	
E		500	
M		600	
RMS On-State Current (T_C = +80°C) (Conduction Angle = 360°C)	$I_{T(RMS)}$	8	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = +80°C)	I_{TSM}	100	Amp
Fusing Current (T_J = −40 to +100°C, t = 1.25 to 10 ms)	I^2t	50	A^2s
Peak Gate Power (Pulse Width = 1 μs)	P_{GM}	16	Watts
Average Gate Power	$P_{G(AV)}$	0.35	Watt
Peak Gate Trigger Current (Pulse Width = 1 μs)	I_{GTM}	4	Amp
Operating Junction Temperature Range	T_J	−40 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.



STYLE 4:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220 AB

All JEDEC dimensions and notes apply

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current (Either Direction) Rated V_{DRM} @ T_C = 100°C, Gate Open	I_{DRM}	–	–	2	mA
Peak On-State Voltage (Either Direction) I_T = 30 A Peak	V_{TM}	–	1.7	2	Volts
Gate Trigger Current, Continuous dc V_D = 12 Vdc, R_L = 12 Ohms	I_{GT}				mA
V_{MT2} (+), $V_{G(+)}$ T2800		–	10	25	
T2802		–	25	50	
V_{MT2} (+), $V_{G(-)}$ T2800 Only		–	20	60	
V_{MT2} (–), $V_{G(-)}$ T2800		–	15	25	
T2802		–	25	50	
V_{MT2} (–), $V_{G(+)}$ T2800 Only		–	30	60	
Gate Trigger Voltage, Continuous dc (All Polarities)	V_{GT}				Volts
V_D = 12 Vdc, R_L = 100 Ohms		–	1.25	2.5	
R_L = 125 Ohms, V_D = V_{DRM}, T_C = 100°C		0.2	–	–	
Holding Current (Either Direction)	I_{HO}				mA
V_D = 12 Vdc, Gate Open, T2800		–	15	30	
I_T = 125 mA T2802		–	20	60	
Gate Controlled Turn-On Time Rated V_{DROM}, I_T = 10 A, I_{GT} = 80 mA, Rise Time = 0.1 μs	t_{gt}	–	1.6	–	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, $I_{T(RMS)}$ = 8.0 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(c)	–	10	–	V/μs
Critical Rate of Rise of Off-State Voltage Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C	dv/dt				V/μs
T2800, T2802 B		100	–	–	
C		85	–	–	
D		75	–	–	
E		65	–	–	
M		60	–	–	

FIGURE 1 — CURRENT DERATING

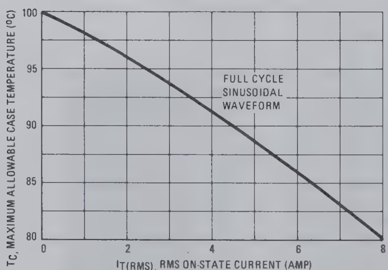
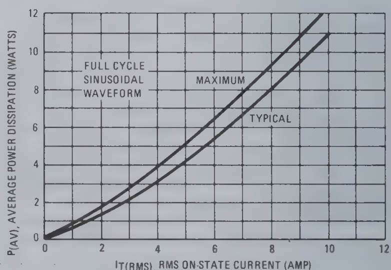


FIGURE 2 — POWER DISSIPATION



MOTOROLA

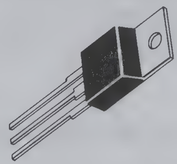
TRIACS

6 AMPERES RMS
200–600 VOLTS

BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Blocking Voltage to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability



2.3

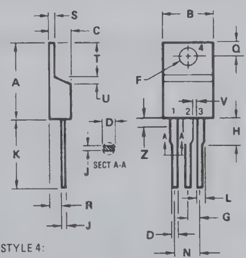
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (1) (T_J = −40 to +100°C) Gate Open T2801 B / C / D / E / M	V_{DRM}	200 / 300 / 400 / 500 / 600	Volts
RMS On-State Current (T_C = +80°C) (Conduction Angle = 360°C)	$I_{T(RMS)}$	6	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	80	Amp
Fusing Current (T_J = −40 to +100°C, t = 1 to 8.3 ms)	I^2t	35	A^2s
Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs)	P_{GM}	16	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.35	Watt
Peak Gate Trigger Current (Pulse Width = 1 μs)	I_{GTM}	4	Amp
Operating Junction Temperature Range	T_J	−40 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.



STYLE 4:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

CASE 221A-02
TO-220 AB

All JEDEC dimensions and notes apply

ELECTRICAL CHARACTERISTICS (T_C = 25°C, Either Polarity of MT2-to-MT1 Voltage, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current Rated V_{DRM}, Gate Open, T_J = 100°C	I_{DRM}	–	–	2	mA
Peak On-State Voltage I_{TM} = 30 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%	V_{TM}	–	2	3	Volts
Gate Trigger Current, Continuous dc (1) V_D = 12 Vdc, R_L = 12 Ohms	I_{GT}	–	25	80	mA
Gate Trigger Voltage, Continuous dc (1) V_D = 12 Vdc, R_L = 12 Ohms V_D = V_{DRM}, R_L = 125 Ohms, T_C = 100°C	V_{GT}	 – 0.2	 1.5 –	 4 –	Volts
Holding Current (Either Direction) V_D = 12 Vdc, Gate Open, Initiating Current = 150 mA	I_H	–	100		mA
Turn-On Time (1) V_D = Rated V_{DRM}, I_T = 10 A, I_{GT} = 80 mA, Rise Time = 0.1 μs	t_{gt}	–	2.2	–	μs
Critical Rate of Rise of Commutation Voltage V_D = Rated V_{DRM}, $I_{T(RMS)}$ = 6.0 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(c)	–	10	–	V/μs
Critical Rate of Rise of Off-State Voltage V_D = V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C T2801 B T2801 C T2801 D T2801 E	dv/dt	 50 40 30 20	 – – – –	 – – – –	V/μs

(1) Applies for MT2 (+), G (+), MT2 (–), G (–).

2.3

FIGURE 1 – CURRENT DERATING

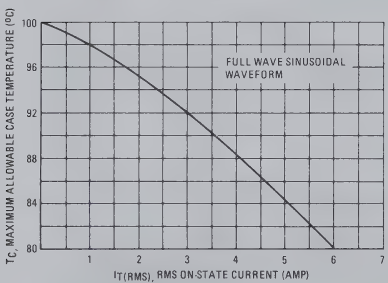
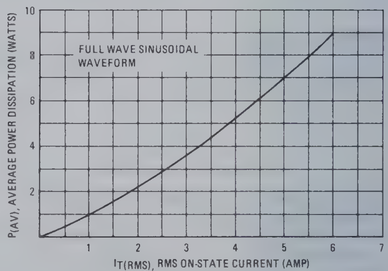


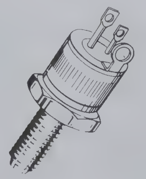
FIGURE 2 – POWER DISSIPATION



MOTOROLA

TRIACS

15 AMPERES RMS
200–600 VOLTS



SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for full wave control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Isolated Stud Package
- Gate Triggering Guaranteed In All 4 Quadrants

MAXIMUM RATINGS

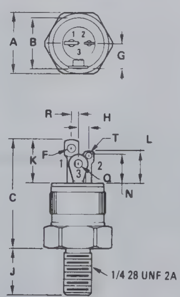
Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (1) (T_J = −65 to +100°C) Gate Open T4120B D M	V_{DRM}	200 400 600	Volts
RMS On-State Current (Conduction Angle = 360°C) T_C = +75°C	$I_{T(RMS)}$	15	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	100	Amp
Circuit Fusing (T_C = −65 to +100°C, t = 1.25 to 10 ms)	I^2t	50	A^2s
Peak Gate Power (Pulse Width = 1.0 μs)	P_{GM}	16	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Gate Trigger Current (Pulse Width = 1 μs)	I_{GTM}	4	Amp
Operating Case Temperature Range	T_C	−65 to +100	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1	°C/W

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

STYLE 2:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2
STUD ISOLATED



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	26.16	–	1.030
F	1.65	4.06	0.065	0.160
G	–	6.48	–	0.255
H	2.16	2.41	0.085	0.095
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
R	1.52	1.78	0.060	0.070
T	0.89	2.16	0.035	0.085

CASE 235-02

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, either polarity of MT2 to MT1 voltage, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current Gate Open Rated V_{DRM} @ T_C = 100°C	I_{DRM}	–	–	2	mA
Peak On-State Voltage I_T = 21 A Peak	V_{TM}	–	1.4	1.8	Volts
Gate Trigger Current, Continuous dc (1) V_D = 12 Vdc, R_L = 30 Ohms	I_{GT}				mA
V_{MT2} (+), V_G (+); V_{MT2} (–), V_G (–)		–	–	50	
V_{MT2} (+), V_G (–); V_{MT2} (–), V_G (+)		–	–	80	
V_{MT2} (+), V_G (+); V_{MT2} (–), V_G (–), T_C = –65°C		–	–	150	
V_{MT2} (+), V_G (–); V_{MT2} (–), V_G (+), T_C = –65°C		–	-	200	
Gate Trigger Voltage, Continuous dc (All Quadrants) V_D = 12 Vdc, R_L = 30 Ohms	V_{GT}				Volts
T_C = 25°C		–	–	2.5	
T_C = –65°C		–	–	4	
V_D = Rated V_{DROM}, R_L = 125 Ohms, T_C = 100°C		0.2	–	–	
Holding Current V_D = 12 Vdc, Gate Open I_T = 500 mA	I_H				mA
T_C = 25°C		–	–	75	
T_C = –65°C		–	–	300	
Gate Controlled Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 25 A Peak, I_{GT} = 160 mA, Rise Time = 0.1 μs	t_{gt}	–	1.6	2.5	μs
Critical Rate-of-Rise of Commutation Voltage Rated V_{DRM}, $I_{T(RMS)}$ = 15 A, Commutating di/dt = 8 A/ms, Gate Unenergized, T_C = 75°C	dv/dt(c)	2	10	–	V/μs
Critical Rate-of-Rise of Off-State Voltage Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C	dv/dt				V/μs
T4120 B		30	150	–	
D		20	100	–	
M		10	75	–	

(1) All Voltage polarity reference to main terminal 1.

FIGURE 1 – CURRENT DERATING

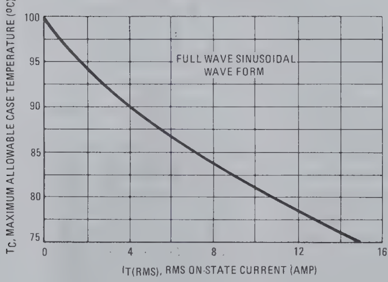
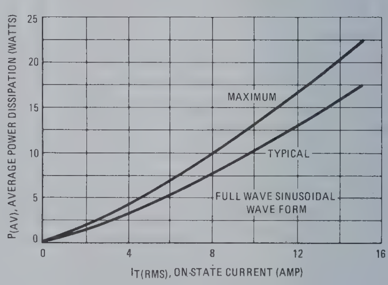


FIGURE 2 – POWER DISSIPATION



MOTOROLA

T6400
T6410
T6420

TRIACS

40 AMPERES RMS
200–800 VOLTS

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

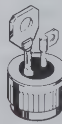
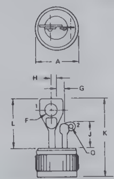
- Glass Passivated Junctions and Center Gate Fire
- Press Fit Stud – T6400
  Stud – T6410
  Isolated Stud – T6420
- Gate Triggering Guaranteed in All 4 Quadrants

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = −65 to +110°C) Gate Open	V_{DRM}		Volts
T6400B, T6410B, T6420B		200	
T6400D, T6410D, T6420D		400	
T6400M, T6410M, T6420M		600	
T6400N, T6410N, T6420N		800	
On-State Current RMS T_C (Pressfit) = 70°C (Conduction Angle = 360°C) T_C (Stud) = 65°C	$I_{T(RMS)}$	40	Amp
Peak Surge Current (Non-Repetitive) (One Full Cycle, 60 Hz)	I_{TSM}	300	Amp
Circuit Fusing (T_J = −65 to +110°C, t = 1.25 to 10 ms)	I^2t	450	A^2s
Peak Gate Power (Pulse Width = 10 μs)	P_{GM}	40	Watts
Average Gate Power	$P_{G(AV)}$	0.75	Watt
Peak Gate Current (Pulse Width = 1 μs)	I_{GTM}	12	Amp
Operating Temperature Range	T_C	−65 to +110	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

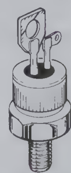
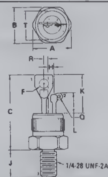
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Pressfit	$R_{\theta JC}$	0.8	°C/W
Stud		0.9	
Isolated Stud		1.0	

STYLE 2
1. MT1
2. GATE
CASE MT2

T6400
PRESS FIT
CASE 310-01

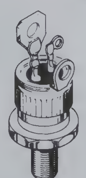
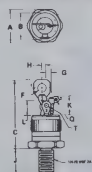
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12 73	12 83	0 501	0 505
F		4 06		0 160
G	2 16	2 41	0.085	0 095
H	1 52	1 78	0.060	0.070
J	7 62	8 89	0 300	0 350
K		26 67	–	1 050
L	-	17 02	–	0 670
Q	1 40	2 16	0.055	0 085

STYLE 2
PIN 1 MT1
2. GATE
3 MT2

T6410
STUD
CASE 263-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14 00	14.20	0.551	0.559
C	26.67	30.23	1 050	1 190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	16.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

STYLE 2.
1. MT1
2. GATE
3. MT2

T6420
ISOLATED STUD
CASE 311-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12 83	0 501	0.506
C	–	32 51		1.280
F	–	4.06		0.160
G	2.16	2.41	0.085	0.095
H	1 60	2.01	0 063	0 079
J	10.67	11.56	0 420	0 455
K	7.62	8.88	0 300	0.350
L	6.48	6.98	0 255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3 81	0.135	0.150

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current (Either Direction) Rated V_{DRM} @ T_J = 110°C, Gate Open	I_{DRM}	–	–	4	mA
Maximum On-State Voltage (Either Direction) I_T = 100 A Peak	V_{TM}	–	1.5	2	Volts
Gate Trigger Current, Continuous dc (1) V_D = 12 Vdc, R_L = 30 Ohms	I_{GT}				mA
V_{MT2} (+), V_G(+)		–	15	50	
V_{MT2} (+), V_G(–)		–	30	80	
V_{MT2} (–), V_G(–)		–	20	50	
V_{MT2} (–), V_G(+)		–	40	80	
V_{MT2} (+), V_G(+); V_{MT2} (–), V_G(–), T_C = –65°C		–	–	125	
V_{MT2} (+), V_G(–); V_{MT2} (–), V_G(+), T_C = –65°C		–	–	240	
Gate Trigger Voltage, Continuous dc	V_{GT}				Volts
V_D = 12 Vdc, R_L = 30 Ohms, T_C = 25°C		–	1.35	2.5	
T_C = –65°C		–	–	3.4	
V_D = Rated V_{DRM}, R_L = 125 Ohms, T_C = 110°C		0.2	–	–	
Holding Current (Either Direction) V_D = 12 Vdc, Gate Open	I_{HO}				mA
Initiating Current = 500 mA T_C = 25°C		–	25	60	
T_C = –65°C		–	–	100	
Gate Controlled Turn-On Time Rated V_{DRM}, I_T = 60 A, I_{GT} = 200 mA, Rise Time = 0.1 μs	t_{gt}	–	1.7	3	μs
Critical Rate of Rise of Commutation Voltage, On-State Conditions: di/dt = 22 A/ms, Gate Unenergized, V_D = Rated V_{DROM}, $I_{T(RMS)}$ = 40 A, T_C (Pressfit) = 70°C T_C (Stud) = 65°C	dv/dt(c)	–	5		V/μs

(1) All voltage polarity reference to main terminal 1.

2.3

FIGURE 1 – ON-STATE POWER DISSIPATION

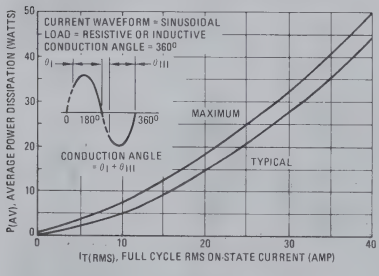
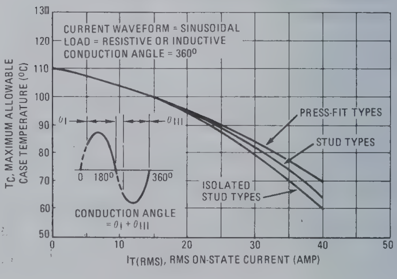


FIGURE 2 – RMS CURRENT DERATING



T6401
T6411
T6421

MOTOROLA

TRIACS

30 AMPERES RMS
200–600 VOLTS

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for full wave control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems.

- Glass Passivated Junctions and Center Gate Geometry
- Press Fit, Stud, Isolated Stud Packages
- Gate Triggering Guaranteed In All 4 Modes

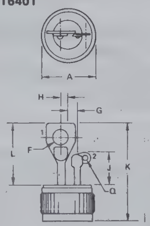
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (T_J = -65 to +100°C) Gate Open T6401B, T6411B, T6421B T6401D, T6411D, T6421D T6401M, T6411M, T6421M	V_{DRM}	 200 400 600	Volts
On-State Current RMS (Conduction Angle = 360°C) $T_C \leq +65°C$	$I_{T(RMS)}$	30	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	300	Amp
Circuit Fusing (T_J = -65 to +100°C, t = 1.25 to 10 ms)	I^2t	450	A^2s
Peak Gate Power (Pulse Width = 1.0 μs)	P_{GM}	40	Watts
Average Gate Power	$P_{G(AV)}$	0.75	Watt
Peak Gate Current Pulse Width ≤ 1 μs)	I_{GM}	2	Amp
Operating Case Temperature Range	T_C	-65 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Pressfit Stud Isolated Stud	$R_{\theta JC}$	0.8 0.9 1.0	°C/W

T6401

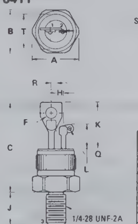


STYLE 2:
1. MT 1
2. GATE
CASE. MT 2

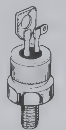
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.52	1.78	0.060	0.070
J	7.62	8 89	0.300	0.350
K		26 67		1.050
L		17 02		0.670
Q	1 40	2 16	0.055	0.085

PRESS FIT
CASE 310-01

T6411



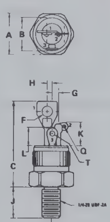
STYLE 2:
PIN 1 MT 1
2 GATE
3. MT 2

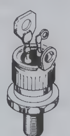


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0 090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0 670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

STUD
CASE 263-03

T6421





STYLE 2.
1. MT 1
2. GATE
3. MT 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0 501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2 16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

ISOLATED STUD
CASE 311-01

2.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current V_D = Rated V_{DRM} @ T_J = 100°C, Gate Open	I_{DRM}	–	–	4	mA
Maximum On-State Voltage (Either Direction) I_{TM} = 100 A Peak	V_{TM}	–	2.1	2.5	Volts
Gate Trigger Current, Continuous dc (1) V_D = 12 Vdc, R_L = 30 Ohms $V_{MT2}(+)$, $V_G(+)$; $V_{MT2}(-)$, $V_G(-)$ $V_{MT2}(+)$, $V_G(-)$; $V_{MT2}(-)$, $V_G(+)$	I_{GT}	 – –	 20 35	 50 80	mA
Gate Trigger Voltage, Continuous dc, All Trigger Modes V_D = 12 Vdc, R_L = 30 Ohms V_D = Rated V_{DRM}, R_L = 125 Ohms, T_C = 100°C	V_{GT}	 – 0.2	 1.35 –	 2.5 –	Volts
Holding Current V_D = 12 Vdc, Gate Open I_T = 150 mA	I_{HO}	–	–	60	mA
Gate Controlled Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 45 A, I_{GT} = 200 mA, Rise Time = 0.1 μs	t_{gt}	–	1.7	3	μs
Critical Rate of Rise of Commutation Voltage, On-State Conditions: di/dt = 16 A/ms, Gate Unenergized, V_D = Rated V_{DRM}, $I_{T(RMS)}$ = 30 A, T_C = Rated Value from Figure 1	dv/dt(c)	3	20	–	V/μs
Critical Rate of Rise of Off-State Voltage V_D = Rated V_{DRM}, Exponential Rise, T_C = 100°C T6401B, T6411B, T6421B T6401D, T6411D, T6421D T6401M, T6411M, T6421M	dv/dt	 40 25 20	 – – –	 – – –	V/μs

FIGURE 1 — CURRENT DERATING

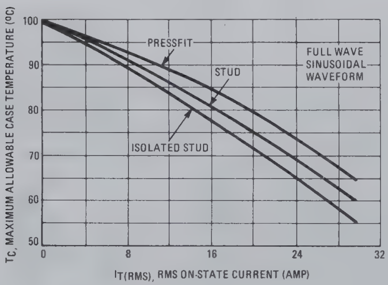
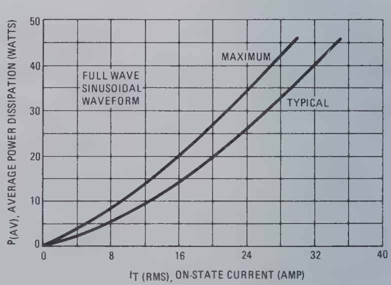


FIGURE 2 — POWER DISSIPATION



TMOS Power MOSFETs

Selector Guide

3.0

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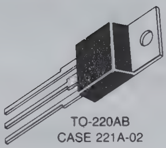
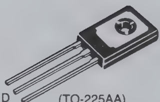
Table 1 — Plastic TMOS Power MOSFETs



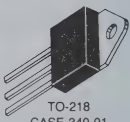
TO-220AB
CASE 221A-02

(MTP and IRF devices in TO-220)



(TO-225AA)
CASE 77-04

(MTA devices are in TO-225AA)



TO-218
CASE 340-01

(MTH devices are in TO-218)

3.0

$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}$ @ I_D (Ohms) Max	Amps	Device	I_D Cont Amps Max	P_D @ T_C = 25°C Watts
1000	10	0.5	MTP1N100	1.0	75
950			MTP1N95		
900	8.0	1.0	MTP2N90	2.0	
850			MTP2N85		
600	12	0.5	MTP1N60	1.0	
	2.5	1.5	MTP3N60	3.0	
	1.2	3.0	MTH6N60	6.0	150
550	12	0.5	MTP1N55	1.0	40
	2.5	1.5	MTP3N55	3.0	75
	1.2	3.0	MTH6N55	6.0	150
500	8.0	0.5	MTP1N50	1.0	50
	6.0	1.0	MTP2P50*	2.0	75
	4.0		MTP2N50		
	2.0	1.5	IRF832	4.0	
	1.5		IRF830	4.5	
		2.0	MTP4N50	4.0	
	0.8	3.5	MTH7N50	7.0	150
450	8.0	0.5	MTP1N45	1.0	50
	6.0	1.0	MTP2P45*	2.0	75
	4.0		MTP2N45		
	2.0	2.5	IRF833	4.0	
	1.5		IRF831	4.5	
		2.0	MTP4N45	4.0	
	0.8	3.5	MTH7N45	7.0	150
400	5.0	1.0	MTP2N40	2.0	50
	3.3	1.5	MTP3N40	3.0	75
	1.5	3.0	IRF732	4.5	
	1.0		IRF730	5.5	
		2.5	MTP5N40	5.0	
	0.55	4.0	MTH8N40	8.0	150
350	5.0	1.0	MTP2N35	2.0	50
	3.3	1.5	MTP3N35	3.0	75
	1.5	3.0	IRF733	4.5	
	1.0		IRF731	5.5	
		2.5	MTP5N35	5.0	
	0.55	4.0	MTH8N35	8.0	150
250	0.50	5.0	MTP10N25	10	100
	2.0	1.0	MTP2N25	2.0	50

*Indicates P-Channel

Table 1 — Plastic TMOS Power MOSFETs TO-220AB, TO-225AA and TO-218AC (continued)

CASE 221A-02, CASE 77-04 CASE 340-01

$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}$ @ I_D (Ohms) Max	Amps	Device	I_DCont Amps Max	P_D @ T_C = 25°C Watts
200	2.4	1.25	IRF612	2.0	20
	1.8	1.0	MTP2N20		50
	1.5	1.25	IRF610	2.5	20
	1.2	2.0	MTA4N20	4.0	30
		2.5	IRF622		40
	1.0	2.5	MTP5N20	5.0	75
	0.8		IRF620	5.0	40
	0.7	3.5	MTP7N20	7.0	75
	0.6	5.0	IRF632	8.0	
	0.4		IRF630	9.0	
		4.0	MTP8N20	8.0	
	0.35	6.0	MTP12N20	12	100
	0.22	10	IRF642	16	125
	0.18	10	IRF640	18	
	0.16	7.5	MTH15N20	15	150
180	1.8	1.0	MTP2N18	2.0	50
	1.2	2.0	MTA4N18	4.0	30
	1.0	2.5	MTP5N18	5.0	75
	0.7	3.5	MTP7N18	7.0	
	0.4	4.0	MTP8N18	8.0	
	0.35	6.0	MTP12N18	12	100
	0.16	7.5	MTH15N18	15	150
150	2.4	1.25	IRF613	2.0	20
	1.5		IRF611	2.5	
	1.3	1.5	MTP3N15	3.0	50
	1.2	2.5	IRF623	4.0	40
	0.9		MTA5N15	5.0	30
	0.8		IRF621	4.0	40
	0.7	3.5	MTP7N15	7.0	75
	0.6	5.0	IRF633	8.0	
	0.5	4.0	MTP8N15	8.0	
	0.4	5.0	IRF631	9.0	
	0.3	5.0	MTP10N15	10	
	0.25	7.5	MTP15N15	15	100
	0.22	10	IRF643	16	125
	0.18		IRF641	18	
	0.12		MTH20N15	20	150
120	1.3	1.5	MTP3N12	3.0	50
	1.2	2.5	MTA5N12	5.0	30
	0.7	3.5	MTP7N12	7.0	75
	0.5	4.0	MTP8N12	8.0	
	0.3	5.0	MTP10N12	10	
	0.25	7.5	MTP15N12	15	100
	0.12	10	MTH20N12	20	150
100	0.8	2.0	MTP4N10	4.0	50
			IRF512	3.5	20
	0.6		IRF510	4.0	
		3.0	MTA6N10	6.0	30
	0.5	4.0	MTP8N10	8.0	75
	0.4		MTP8P10*		
			IRF522	7.0	40
	0.33	5.0	MTP10N10	10	75
	0.3	4.0	IRF520	8.0	40
	0.25	8.0	IRF532	12	75
	0.18		IRF530	14	
		6.0	MTP12N10	12	
	0.15	10	MTP20N10	20	100
	0.11	15	IRF542	24	125
	0.085		IRF540	27	
	0.070	12.5	MTH25N10	25	150

*Indicates P-Channel

3.0

Table 1 — Plastic TMOS Power MOSFETs TO-220AB, TO-225AA and TO-218AC (continued)

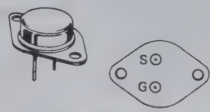
CASE 221A-02, CASE 77-04 CASE 340-01

$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}$ @ I_D (Ohms) Max	Amps	Device	I_DCont Amps Max	P_D @ T_C = 25°C Watts
80	0.8	2.0	MTP4N08	4.0	50
	0.6	3.0	MTA6N08	6.0	30
	0.5	4.0	MTP8N08	8.0	75
	0.4		MTP8P08*		
	0.33	5.0	MTP10N08	10	
	0.18	6.0	MTP12N08	12	
	0.15	10	MTP20N08	20	100
	0.07	12.5	MTH25N08	25	150
60	0.8	2.0	IRF513	3.5	20
	0.6		IRF511	4.0	
		2.5	MTP5N06	5.0	50
	0.4	3.5	MTA7N06	7.0	30
		4.0	IRF523		40
	0.3		IRF521	8.0	
	0.28	5.0	MTP10N06	10	75
	0.25	8.0	IRF533	12	
	0.20	6.0	MTP12N06		
	0.18	8.0	IRF531	14	
	0.16	7.5	MTP15N06	15	
	0.11	15	IRF543	24	125
	0.085		IRF541	27	
	0.08	12.5	MTP25N06	25	100
	0.055	17.5	MTH35N06	35	150
50	0.8	2.5	MTP5N05	5.0	50
	0.4	3.5	MTA7N05	7.0	30
	0.28	5.0	MTP10N05	10	75
	0.20	6.0	MTP12N05	12	
	0.16	7.5	MTP15N05	15	
	0.10	6.0	BUZ10	12	
	0.08	12.5	MTP25N05	25	100
	0.055	17.5	MTH35N05	35	150

*Indicates P-Channel

Table 2 — Metal TMOS Power MOSFETs TO-204 (Formerly TO-3)

CASE 1-04 and CASE 1-05



Drain connected to case

$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}$ @ I_D (Ohms) Max	Amps	Device	I_D Cont Amps Max	P_D @ T_C = 25°C Watts
1000	10	0.5	MTM1N100	1.0	75
950			MTM1N95		
900	8.0	1.0	MTM2N90	2.0	
850			MTM2N85		
600	2.5	1.5	MTM3N60	3.0	
	1.2	3.0	MTM6N60	6.0	150
550	2.5	1.5	MTM3N55	3.0	75
	1.2	3.0	MTM6N55	6.0	150
500	6.0	1.0	MTM2P50*	2.0	75
	4.0		MTM2N50		
	2.0	2.5	IRF432	4.0	
	1.5		IRF430	4.5	
		2.0	MTM4N50	4.0	
		3.0	2N6762	4.5	
	0.8	3.5	MTM7N50	7.0	150
	0.4	7.5	MTM15N50	15	250
450	6.0	1.0	MTM2P45*	2.0	75
	4.0		MTM2N45		
	2.0	2.5	IRF433, 2N6761	4.0	
	1.5		IRF431	4.5	
		2.0	MTM4N45	4.0	
	0.8	3.5	MTM7N45	7.0	150
	0.40	7.5	MTM15N45	15	250
400	3.3	1.5	MTM3N40	3.0	75
	1.5	3.0	IRF332	4.5	
	1.0		IRF330	5.5	
		2.5	MTM5N40	5.0	
		3.5	2N6760	5.5	
	0.55	4.0	MTM8N40	8.0	150
	0.30	7.5	MTM15N40	15	250
350	3.3	1.5	MTM3N35	3.0	75
	1.5	3.0	IRF333, 2N6759	4.5	
	1.0		IRF331	5.5	
		2.5	MTM5N35	5.0	
	0.55	4.0	MTM8N35	8.0	150
	0.30	7.5	MTM15N35	15	250
250	0.50	5.0	MTM10N25	10	100
200	1.2	2.5	IRF222	4.0	40
	1.0		MTM5N20	5.0	75
	0.8		IRF220		
	0.7	3.5	MTM7N20	7.0	
	0.6	5.0	IRF232	8.0	
	0.4		IRF230	9.0	
		6.0	2N6758		
		4.0	MTM8N20	8.0	
	0.35	6.0	MTM12N20	12	100
	0.22	10	IRF242	16	125
	0.18		IRF240	18	
	0.16	7.5	MTM15N20	15	150
	0.12	16	IRF252	25	
	0.085		IRF250	30	
	0.08	20	MTM40N20	40	250
180	1.0	2.5	MTM5N18	5.0	75
	0.70	3.5	MTM7N18	7.0	
	0.40	4.0	MTM8N18	8.0	
	0.35	6.0	MTM12N18	12	100
	0.16	7.5	MTM15N18	15	150
	0.08	20	MTM40N18	40	250

*Indicates P-Channel

3.0

Table 2 — Metal TMOS Power MOSFETs TO-204 (Formerly TO-3) (continued)

CASE 1-04 and CASE 1-05

$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}$ @ I_D (Ohms) Max	Amps	Device	I_D Cont Amps Max	P_D @ T_C = 25°C Watts
150	1.2	2.5	IRF223	4.0	40
	0.8		IRF221	5.0	
	0.7	3.5	MTM7N15	7.0	75
	0.6	5.0	2N6757	8.0	
			IRF233		
	0.5	4.0	MTM8N15		
	0.4	5.0	IRF231	9.0	
	0.3		MTM10N15	10	
	0.25	7.5	MTM15N15	15	150
	0.22	10	IRF243	16	125
	0.18		IRF241	18	
	0.12		MTM20N15	20	150
		16	IRF253	25	
	0.085		IRF251	30	
	0.06	22.5	MTM45N15	45	250
120	0.70	3.5	MTM7N12	7.0	75
	0.50	4.0	MTM8N12	8.0	
	0.30	5.0	MTM10N12	10	
	0.25	7.5	MTM15N12	15	150
	0.12	10	MTM20N12	20	
	0.06	22.5	MTM45N12	45	250
100	0.5	4.0	MTM8N10	8.0	75
	0.4		MTM8P10*		
			IRF122	7.0	40
	0.33	5.0	MTM10N10	10	
	0.3	4.0	IRF120	8.0	40
	0.25	8.0	IRF132	12	75
	0.18		IRF130	14	
		6.0	MTM12N10	12	
		9.0	2N6756	14	
	0.15	10	MTM20N10	20	100
	0.11	15	IRF142	24	125
	0.085		IRF140	27	
	0.08	20	IRF152	33	150
	0.07	12.5	MTM25N10	25	
	0.055	20	IRF150	40	
	0.04	27.5	MTM55N10	55	250
80	0.50	4.0	MTM8N08	8.0	75
	0.40		MTM8P08*		
	0.33	5.0	MTM10N08	10	
	0.18	6.0	MTM12N08	12	
	0.15	10	MTM20N08	20	100
	0.07	12.5	MTM25N08	25	150
	0.04	27.5	MTM55N08	55	250
60	0.4	4.0	IRF123	7.0	40
	0.3		IRF121	8.0	
	0.28	5.0	MTM10N06	10	75
	0.25	8.0	IRF133, 2N6755	12	
	0.20	6.0	MTM12N05		
	0.18	8.0	IRF131	14	
	0.16	7.5	MTM15N06	15	
	0.11	15	IRF143	24	125
	0.85		IRF141	27	
	0.08	12.5	MTM25N06	25	100
		20	IRF153	33	150
	0.055	17.5	MTM35N06	35	
		20	IRF151	40	
	0.028	30	MTM60N06	60	250
50	0.28	5.0	MTM10N05	10	75
	0.20	6.0	MTM12N06	12	
	0.16	7.5	MTM15N05	15	
	0.08	12.5	MTM25N05	25	100
	0.055	17.5	MTM35N05	35	150
	0.028	30	MTM60N06	60	250

*Indicates P-Channel

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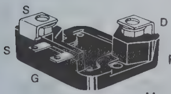
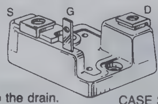
Table 3 — Energy Management Series TMOS Power MOSFETs



$P_D = 500W$

CASE 346-01

Mounting base is connected to the drain.



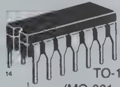
$P_D = 250W$

CASE 353-01

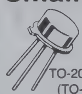
V_{DSS} (Volts)	$r_{DS(on)}$ @ I_D (Ohms)	(Amp)	Device	I_D(Cont) (Amps)	P_D @ T_C = 25°C (Watts)
200	0.048	30	MTE60N20	60	250
	0.024	60	MTE120N20	120	500
180	0.048	30	MTE60N18	60	250
	0.024	60	MTE120N18	120	500
150	0.038	32.5	MTE65N15	65	250
	0.020	65	MTE130N15	130	500
120	0.038	32.5	MTE65N12	65	250
	0.020	65	MTE130N12	130	500
100	0.028	37.5	MTE75N10	75	250
	0.012	75	MTE150N10	150	500
80	0.028	37.5	MTE75N08	75	250
	0.012	75	MTE150N08	150	500
60	0.018	50	MTE100N06	100	250
	0.009	100	MTE200N06	200	500
50	0.018	50	MTE100N05	100	250
	0.009	100	MTE200N05	200	500

3.0

Table 4 — TMOS Small-Signal MOSFETs

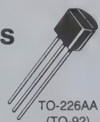


TO-116 (MO-001 AA)

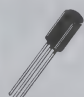


TO-205AD (TO-39)

TO-206AA (TO-18)



TO-226AA (TO-92)



TO-226AE

$V_{(BR)DSS}$ Volts Min	$r_{DS(on)}$ @ I_D (Ohms) Max	Amps	Device	I_DCont Amps Max	P_D @ T_C = 25°C Watts	Package
200	14	0.2	BS107	0.25	0.6	TO-226AA (TO-92)
	6.0	0.1	MPF9200	0.40		
			MFE9200		1.8	TO-206AA (TO-18)
	5.0	0.2	BS170	0.50	0.6	TO-226AA (TO-92)
90	5.0	1.0	VN90AB	2.0	6.25	TO-205AD
	4.5		VN99AB			(TO-39)
	4.0		MPF6661		2.5	TO-226AE
			2N6661		6.25	TO-205AD (TO-39)
	2.0		MPF990		2.5	TO-226AE
			MFE990		6.25	TO-205AD (TO-39)
			MFQ990C		4.0	TO-116
60	5.0	0.5	MPF910/MPF10LM	0.5	2.5	TO-226AE
			MFE910		6.25	TO-205AD
		0.3	VN67AB			(TO-39)
	3.0	1.0	MPF6660	2.0	2.5	TO-226AE
			2N6660		6.25	TO-205AD (TO-39)
	1.7		MPF960		2.5	TO-226AE
			MFE960		6.25	TO-205AD (TO-39)
			MFQ960C		4.0	TO-116
35	2.5		VN35AB		6.25	TO-205AD (TO-39)
	1.4		MPF930		2.5	TO-226AB
			MFE930		6.25	TO-205AD (TO-39)
			MFQ930C		4.0	TO-116

Table 5 — TMOS Product Matrix

I_D (AMP) / $V_{(BR)DSS}$ Volts	≤1	2–2.9	3–3.9	4–5	5–6	7	8	9–10	12–13	14–19	20–24	25–29	30–40	50–75	100–200
1000 950	MTM/MTP 1N100/95		MTM 3N10/95	MTM 4N100/95											
900 850		MTM/MTP 2N90/85		MTM 4N90/85	MTM 5N90/85										
600 550	MTP 1N60/55	MTM/MTP 2N60/55	MTM/MTP 3N60/55		MTM/MTH 6N60/55		MTM 8N60/55				MTE 20N60/55		MTE 40N60/55		
500 450	MTP 1N50/45	MTM/MTP 2N50/45 MTM/MTP 2P50/45		MTM/MTP 4N50/45 2N6761 2N6762 IRF430-33 IRF830-33		MTM/MTH 7N50/45	IRF440 IRF441 IRF740 IRF741	MTM/MTH 10N50/45	IRF450 IRF451	MTM15N 50/45		MTE 25N50/45		MTE 50N50/45	
400 350		MTP 2N40/35	MTM/MTP 3N40/45	2N6759	MTM/MTP 5N40/35 2N6760 IRF330-33 IRF730-33		MTM/MTH 8N40/35		MTM/MTH 12N40/35	MTM 15N40/35 IRF350 IRF351			MTE 30N40/35	MTE 60N40/35	
250 180	MFE9200 MPF9200 BS170 BS107	MTP 2N20/18 MTP 2N25 IRF610-12		IRF222 IRF622 MTA 4N18/20 IRF220 IRF620	MTM/MTP 5N20/18	MTM/MTP 7N20/18	MTM/MTP 8N20/18 IRF232 IRF632	MTM/MTP 10N25 2N6758 IRF230 IRF630	MTM/MTP 12N20/18	IRF240,640 MTM 15N20/18 IRF242,642 MTH 15N20/18		IRF252	IRF250 MTM 40N20/18 MTH 30N20/18	MTE 60N20/18	MTE 120N20/18
150 120		IRF611-13	MTP 3N15/12	IRF223,623 MTA 5N12/15 IRF221 IRF621	IRF221 IRF621	MTM/MTP 7N15/12	IRF233 IRF633 2N6757 MTM/MTP 8N12/15	MTM/MTP 10N15/12 IRF231 IRF631 2N6757		MTM/MTP 15N15/12 IRF241,641 IRF243,643	MTM/MTH 20N15/12	IRF253	IRF251 MTM 45N15/12 MTH 35N15/20	MTE 65N15/12	MTE 130N15/12
100 80		2N6661 MPF6661 MPF990 MFE990 MFQ990C	IRF512	MTP 4N10/08 IRF510	MTA 6N08/10	IRF122 IRF522	MTM/MTP 8N10/08 MTM/MTP 8P10/08 IRF120 IRF520	MTM/MTP 10N10/08	MTM/MTP 12N10/08 IRF132 IRF532	2N6756 IRF130 IRF530	MTM/MTP 20N10/08 IRF142 IRF542	MTM 25N10/08 MTH 25N10/08 IRF140 IRF540	IRF150,152 MTH40N 10/08	MTE 75N10/08 MTM 55N10/08	150N10/08
60 50	MFE910 MPF910	2N6660 MPF6660 MFE960 MPF960 MFQ960	IRF513	IRF511	MTP 5N06/05	IRF123 IRF523 MTA 7N05/06	IRF121 IRF521	MTM/MTP 10N06/05	MTM/MTP 12N06/05 2N6755 IRF133 IRF533 BUZ10	MTM/MTP 15N06/05 IRF131 IRF531	IRF143 IRF543	MTM/MTP 25N06/05 IRF141 IRF541	MTM/MTH 35N06/05 IRF151 IRF153 MTH 40N06/05	MTM 60N06/05	MTE 100N06/05 MTE 200N06/05

MTM Prefix — TO-204
MTP Prefix — TO-220AB
MTH Prefix — TO-218AC
MTA Prefix — TO-225AA

MFE Prefix — TO-205AD (TO-39)
MPF Prefix — TO-226AA (TO-92)
MFQ Prefix — TO-116
MTE Prefix — Case 346 or 353

IRF100 thru 400 Series — TO-204
IRF500 thru 800 Series — TO-220AB

■ Devices in the shaded area will be introduced in 1984.

Rectifiers

Selector Guide

Motorola is the worlds' leading supplier of ectifiers, including those for use in switching oower supplies. Wafer fabrication technology ıas constantly improved, leading to the product offering outlined in this selector guide. Todays' Motorola rectifiers embody the same precision echnology as the most advanced IC's, and are apable of passing stringent environmental esting, including under the hood of an utomobile.

In addition rectifier product trends are oward higher operating temperature to mproved quality, faster switching times, plastic ackages (translate lower cost) and use of dual ectifier modules.

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4.0

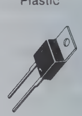
RECTIFIERS

Schottky Rectifiers

SWITCHMODE Schottky Power Rectifiers with the high speed and low forward voltage drop characteristic of Schottky's metal/silicon junctions are produced with ruggedness and temperature performance comparable to silicon-junction rectifiers. Ideal for use in low voltage, high frequency power supplies and as very fast clamping diodes, these devices feature switching times less than 10 ns, and are offered in current ranges from 0.5 to 300 amperes, and reverse voltages to 45 volts.

In some current ranges, devices are available with junction temperature specifications of 125° C, 150° C, 175° C. Devices with higher T_J ratings can have significantly lower leakage currents, but higher forward-voltage specifications. These parameter tradeoffs should be considered when selecting devices for applications that can be satisfied by more than one device type number. Detailed specifications are available on the individual data sheets.

4.0

	I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)					
	0.5	**1.0**	**3.0**	**5.0**	**7.5**	**10**
	299-02 (DO-204AH) Glass	59-04 Plastic	267 Plastic	60 Metal	221B-01 (TO-220AC) Plastic	
V_{RRM} (Volts)						
20		1N5817	1N5820	1N5823		
30	MBR030	1N5818	1N5821	1N5824		
35					MBR735	MBR1035
40	MBR040	1N5819	1N5822	1N5825		
45					MBR745	MBR1045
I_{FSM} (Amps)	5.0	25	80	500	150	150
†T_C @ Rated I_O (°C)					105	135
†T_L @ Rated I_O (°C)	75	90	95	80		
T_J (Max) (°C)	150	125	125	125	150	150
Max V_F @ $I_{FM} = I_O$	*0.65 T_L = 25°C	*0.60 T_L = 25°C	*0.525 T_L = 25°C	*0.38 T_C = 25°C	0.57 @ 7.5 A T_C = 125°C	0.72 @ 20 A T_C = 125°C

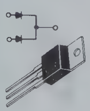
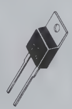
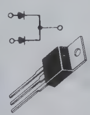
▢ TX versions available.
* Values are for the 40-Volt units. The lower voltage parts provide lower limits.
** I_O is total device output.
† Must be derated for reverse power dissipation. See Data Sheet.

SCHOTTKY RECTIFIERS (contiunued)

There are many other standard features in Motorola Schottky rectifiers that give added performance and reliability.

1. GUARDRINGS are included in all Schottky die for reverse voltage stress protection from high rates of dv/dt to virtually eliminate the need for snubber networks. The guardring also operates like a zener and avalanches when subjected to voltage transients.
2. MOLYBDENUM DISCS on both sides of the die minimize fatigue from power cycling in all metal product. The plastic TO-220 devices have a special solder formulation for the same purpose.

3. QUALITY CONTROL monitors all critical fabrication operations and performs selected stress tests to assure constant processes.

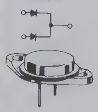
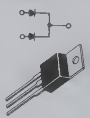
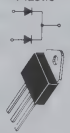
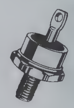
I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)					
15		16	20	25	
221A-02 (TO-220AB) Plastic  Dual Diode**	56-02 (DO-4) Metal 	221B-01 (TO-220AC) Plastic 	221A-02 (TO-220AB) Plastic  Dual Diode**	56-02 (DO-4) Metal 	
	1N5826			1N5829	
	1N5827			1N5830	1N6095
MBR1535CT		MBR1635	MBR2035CT		
	1N5828			1N5831	1N6096
MBR1545CT		MBR1645	MBR2045CT		
150	500	300	150	800	400
105	85	125	135	85	70
150	125	150	150	125	125
0.70 @ 15 A T_C = 125°C	*0.50 T_C = 25°C	0.60 @ 16 A T_C = 125°C	0.72 @ 20 A T_C = 125°C	*0.48 T_C = 25°C	0.86 @ 78.5 A T_C = 70°C

▢ TX versions available.
* Values are for the 40-Volt units. The lower voltage parts provide lower limits.
** I_O is total device output.

4.0

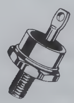
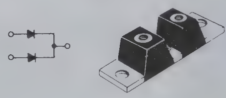
SCHOTTKY RECTIFIERS (contiunued)

4.0

V_{RRM} (Volts)	I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)					
	30			35	40	50
	11-03 (TO-3) Metal  Dual Diode** (40 Mil Pins)	221A-02 (TO-220AB) Plastic  Dual Diode**	340-01 (TO-218AC) Plastic  Dual Diode**	56-02 (DO-4) Metal 	257 (DO-5) Metal 	
20					1N5832	
30					1N5833	1N6097
35	MBR3035CT	MBR2535CT	MBR3035PT	MBR3535		
40					1N5834	1N6098
45	SD241 MBR3045CT	MBR2545CT	MBR3045PT	SD41 MBR3545		
I_{FSM} (Amps)	400	300	400	600	800	800
†T_C @ Rated I_O (°C)	105	125	105	90	75	70
†T_L @ Rated I_O (°C)						
T_J (Max) (°C)	150	150	150	150	125	125
Max V_F @ $I_{FM} = I_O$	0.72 T_C = 125°C	0.73 @ 30 A T_C = 125°C	0.72 @ 30 A T_C = 125°C	0.70 @ 78.5 A T_C = 25°C	*0.59 T_C = 25°C	0.86 @ 157 A T_C = 70°C

▩ TX versions available.
* Values are for the 40-Volt units. The lower voltage parts provide lower limits.
** I_O is total device output.
† Must be derated for reverse power dissipation. See Data Sheet.

SCHOTTKY RECTIFIERS (contiunued)

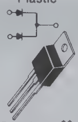
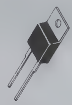
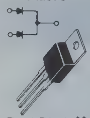
I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)						
60	65	75	80	120	200	300
257 (DO-5) Metal 				357B-01 Plastic POWERTAP  Dual Diode**		
MBR6035	MBR6535	MBR7535	MBR8035	MBR12035CT	MBR20035CT	MBR30035CT
				1N6458	1N6460	
SD51 MBR6045	MBR6545	MBR7545	MBR8045	MBR12045CT 1N6457	MBR20045CT 1N6459	MBR30045CT
800	800	1000	1000	1500	1500	2500
90	120	90	120	140	140	140
150	175	150	175	175	175	175
0.80 @ 157 A T_C = 125°C	0.62 @ 65 A T_C = 150°C	0.90 @ 220 A T_C = 125°C	0.59 @ 80 A T_C = 150°C	0.68 @ 120 A T_C = 125°C	0.68 @ 200 A T_C = 125°C	0.615 @ 200 A T_C = 125°C

** I_O is total device output.

4.0

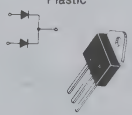
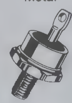
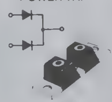
Ultrafast Recovery Rectifiers

EXPANDING the SWITCHMODE Rectifier family are these ultrafast devices with reverse recovery times of 25 to 100 nanoseconds. They complement the broad Schottky offering for use in the higher voltage outputs and internal circuitry of switching power supplies as operating frequencies increase from 20 kHz to 250 kHz. Additional package styles and operating current levels are planned.

	I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)					
	1.0	4.0	6.0	8.0	15	16
V_{RRM} (Volts)	59-03 (DO-41) Plastic 	267-01 Plastic 	221A-02 (TO-220AB) Plastic  Dual Diode**	221B-01 (TO-220AC) Plastic 		221A-02 (TO-220AB) Plastic  Dual Diode**
50	MUR105	MUR405	MUR605CT	MUR805	MUR1505	MUR1605CT
100	MUR110	MUR410	MUR610CT	MUR810	MUR1510	MUR1610CT
150	MUR115	MUR415	MUR615CT	MUR815	MUR1515	MUR1615CT
200	MUR120		MUR620CT	MUR820	MUR1520	MUR1620CT
400				MUR840	MUR1540	
500				MUR850	MUR1550	
600				MUR860	MUR1560	
I_{FSM} (Amps)	35	125	75	100	200	100
T_A @ Rated I_O (°C)	50	80				
T_C @ Rated I_O (°C)			130	150	150	150
T_J (Max) (°C)	175	175	175	175	175	175
t_{rr} ns	35	35	35	35/60	35/60	35

** I_O per leg is half.
Reverse Polarity (Anode-To-Case) indicated with an "R" Suffix.

ULTRAFAST RECOVERY RECTIFIERS (continued)

I_O AVERAGE RECTIFIED FORWARD CURRENT (Amperes)				
25	30		50	100
245 (DO-4) Metal 	340-01 (TO-218AC) Plastic  Dual Diode**		257 (DO-5) Metal 	357B-01 Plastic POWER TAP  Dual Diode**
MUR2505	R710XPT	MUR3005PT	MUR5005	MUR10005CT
MUR2510	R711XPT	MUR3010PT	MUR5010	MUR10010CT
MUR2515		MUR3015PT	MUR5015	MUR10015CT
MUR2520	R712XPT	MUR3020PT	MUR5020	MUR10020CT
	R714XPT			

500	150	400	600	400
145	100	150	125	150
175	150	175	175	175
50	100	35	50	50

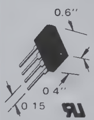
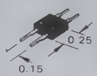
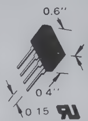
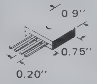
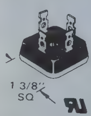
** I_O per leg is half.
Reverse Polarity (Anode-To-Case) indicated with an "R" Suffix.

4.0

Rectifier Bridges

Motorola SUPERBRIDGES offer cost effectiveness and reliability in single phase applications. Chip/leadframe techniques are used for lower-current types, while the higher current assemblies combine pretested "button" rectifier cells for low assembly cost and high yields. Performance of four individual diodes is achieved at the cost of only two, with reliability of the whole assembly comparable to that of a single unit. The higher current assemblies feature versatile slip-on/solder/wire wrap terminals.

4.0

	I_O, DC OUTPUT CURRENT (Amperes)					
	1.0	**1.5**	**2.0**	**4.0/8.0**	**25**	**35**
V_{RRM} (Volts)	312-02 	109-03 	312-02 	117A-02 Note 1 	309A-03 	309A-02 
50	3N246 MDA100A	MDA920A2	3N253 MDA200	MDA970A1	MDA2500	MDA3500
100	3N247 MDA101A	MDA920A3	3N254 MDA201	MDA970A2	MDA2501	MDA3501
200	3N248 MDA102A	MDA920A4	3N255 MDA202	MDA970A3	MDA2502	MDA3502
400	3N249 MDA104A	MDA920A6	3N256 MDA204	MDA970A5	MDA2504	MDA3504
600	3N250 MDA106A	MDA920A7	3N257 MDA206		MDA2506	MDA3506
800	3N251 MDA108A	MDA920A8	3N258 MDA208	CF		MDA3508
1000	3N252 MDA110A	MDA920A9	3N259 MDA210	CF		MDA3510
I_{FSM} (Amps)	30	45	60	100	400	400
T_A @ Rated I_O (°C)	75	50	55	25 @ 4 A		
T_C @ Rated I_O (°C)				55 @ 8 A	55	55
T_J (Max) (°C)	150	175	175	150	175	175

CF: Consult Factory.

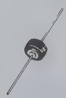
UL RECOGNIZED E61980

Dimensions given are nominal

Note 1. The MDA970A series replaces the MDA970 in the new Case 117A-02, which has minor changes over the old Case 117.

Fast Recovery Rectifiers

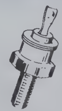
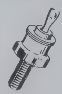
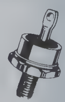
...available for designs requiring a power rectifier having maximum switching times ranging from 200 ns to 750 ns. These devices are offered in current ranges of 1.0 to 50 amperes and in voltages to 1000 volts.

	I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)					
	1.0		60	3.0		5.0
V_{RRM} (Volts)	59-04 Plastic 		60 Metal 	267-01 Plastic 		194-04 Plastic 
50	†1N4933	MR810	MR830	MR850	MR910	MR820
100	†1N4934	MR811	MR831	MR851	MR911	MR821
200	†1N4935	MR812	MR832	MR852	MR912	MR822
400	†1N4936	MR814	MR834	MR854	MR914	MR824
600	†1N4937	MR816	MR836	MR856	MR916	MR826
800		MR817			MR917	
1000		MR818			MR918	
I_{FSM} (Amps)	30	30	100	100	100	300
T_A @ Rated I_O (°C)	75	75		*90	*90	*55
T_C @ Rated I_O (°C)		100	100			
T_J (Max) (°C)	150	150	150	175	175	175
t_{rr} (μs)	0.2	0.75	0.2	0.2	0.75	0.2

* Must be derated for reverse power dissipation. See Data Sheet.
† Package Size: 0.120″ Max Diameter by 0.260″ Max Length.

FAST RECOVERY RECTIFIERS (continued)

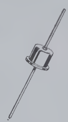
4.0

V_{RRM} (Volts)	I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)						
	6.0	12	20	24	30	40	50
	245 (DO-4) Metal Note 1 		42A (DO-5) Metal 	339 Plastic Note 1 	42A (DO-5) Metal Note 2 	257 (DO-5) Metal Note 2 	
50	1N3879	1N3889	1N3899	MR2400F	1N3909	MR860	MR870
100	1N3880	1N3890	1N3900	MR2401F	1N3910	MR861	MR871
200	1N3881	1N3891	1N3901	MR2402F	1N3911	MR862	MR872
400	1N3883	1N3893	1N3903	MR2404F	1N3913	MR864	MR874
600	MR1366	MR1376	MR1386	MR2406F	MR1396	MR866	MR876
800							
1000							
I_{FSM} (Amps)	150	200	250	300	300	350	400
T_A @ Rated I_O (°C)							
T_C @ Rated I_O (°C)	100	100	100	125	100	100	100
T_J (Max) (°C)	150	150	150	175	150	160	160
t_{rr} ns	0.2	0.2	0.2	0.2	0.2	0.2	0.2

▢ TX versions available.
Note 1. Meets mounting configuration of TO-220 outline.
Note 2. Braided lead top terminal configuration available; consult your Sales Representative.
** I_O is total device output.

General-Purpose Rectifiers

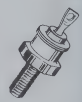
Motorola offers a wide variety of low-cost devices, packaged to meet diverse mounting requirements. Avalanche capability is available in the axial lead 1.5,3 and 6 amp packages shown below to provide protection from transients.

	I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)					
	1.0	1.5		3.0		6.0
V_{RRM} (Volts)	59-04 (DO-15) Plastic 		60 Metal 	267 Plastic 		194-04 Plastic 
50	†1N4001	**1N5391	1N4719	**MR500	1N5400	**MR750
100	†1N4002	**1N5392	1N4720	**MR501	1N5401	**MR751
200	†1N4003	1N5393 *MR5059	1N4721	**MR502	1N5402	**MR752
400	†1N4004	1N5395 *MR5060	1N4722	**MR504	1N5404	**MR754
600	†1N4005	1N5397 *MR5061	1N4723	**MR506	1N5406	**MR756
800	†1N4006	1N5398	1N4724	MR508		MR758
1000	†1N4007	1N5399	1N4725	MR510		MR760
I_{FSM} (Amps)	30	50	300	100	200	400
T_A @ Rated I_O (°C)	75	$T_L = 70$	75	95	$T_L = 105$	60
T_C @ Rated I_O (°C)						
T_J (Max) (°C)	175	175	175	175	175	175

† Package Size: 0.120″ Max Diameter by 0.260″ Max Length.
* 1N5059 series equivalent Avalanche Rectifiers.
** Avalanche versions available, consult factory.

4.0

GENERAL-PURPOSE RECTIFIERS (continued)

V_{RRM} (Volts)	I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)						
	12	24	25	30		40	50
	245 (DO-4) Metal 	339 Plastic Note 1 	193-03 Plastic Note 2 	43-02 (DO-21) Metal 		42A (DO-5) Metal 	43-04 Metal 
50	MR1120 1N1199,A,B	MR2400	MR2500	1N3491	1N3659	1N1183A	MR5005
100	MR1121 1N1200,A,B	MR2401	MR2501	1N3492	1N3660	1N1184A	MR5010
200	MR1122 1N1202,A,B	MR2402	MR2502	1N3493	1N3661	1N1186A	MR5020
400	MR1124 1N1204,A,B	MR2404	MR2504	1N3495	1N3663	1N1188A	MR5040
600	MR1126 1N1206,A,B	MR2406	MR2506	MR328	Note 3	1N1190A	Note 3
800	MR1128 1N3988		MR2508	MR330	Note 3	Note 3	Note 3
1000	MR1130 1N3990		MR2510	MR331	Note 3	Note 3	Note 3
I_{FSM} (Amps)	300	400	400	300	400	800	600
T_A @ Rated I_O (°C)							
T_C @ Rated I_O (°C)	150	125	150	130	100	150	150
T_J (Max) (°C)	190	175	175	175	175	190	195

Note 1. Meets mounting configuration of TO-220 outline.
Note 2. Request Data Sheet for Mounting Information.
Note 3. Available on special order.

Regulator and Reference Diodes

Selector Guide

Motorola's standard Zeners and Avalanche Regulator diodes comprise the largest inventoried line in the industry. Continuous development of improved manufacturing techniques have resulted in computerized diffusion and test, as well as critical process controls learned from surface-sensitive MOS fabrication. Resultant high yields lower factory costs. Check the following features for application to your specific requirements:

- Wide selection of package materials and styles:
  - Plastic (Surmetic) for low cost, mechanical ruggedness
  - Glass for highest reliability, lowest cost
  - Metal for highest power
- Power ratings from 0.25 to 50 Watts
- Breakdown voltages from 1.8 to 200 V in approximately 10% steps
- Available tolerances from 10% (low cost) to a tight as 1% (critical applications) with off-the-shelf delivery
- Special selection of electrical characteristics available at low cost due to high-volume lines (check your Motorola sales representative for special quotations)
- JAN/JANTX(V) availability.
- Special glass now used in DO-35 type packages is compatible with low temperature alloy processes, yielding sharper breakdown and low leakage.

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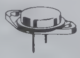
Zener and Avalanche Regulator Diodes

General-Purpose Regulator Diodes

Nominal Zener Voltage	250 mW Low Level Cathode = Polarity Mark	250 mW Low Noise Cathode = Polarity Mark	400 mW Low Noise Low Leakage Cathode = Polarity Mark	500 mW Cathode = Polarity Mark			1 Watt Cathode = Polarity Mark	1 Watt Cathode to Case	1.5 Watt Cathode = Polarity Mark
(Note 1)	(Notes 2,3)	(Notes 2,3,5)	(Notes 2,4,5)	(Notes 2,5)	(Notes 2,6)	(Notes 1,2,13)	(Notes 2,7)	(Notes 2,8)	(Notes 2,9)
		Case 299-02		 Glass DO-204AH (DO-35)			 Glass Case 59 (DO-41)	 Metal Case 52 (DO-13)	 Surmetic 30 Case 59 (DO-41)
1.8	1N4678	1N4614							
2.0	1N4679	1N4615							
2.2	1N4680	1N4616							
2.4	1N4681	1N4617		1N4370	1N5221	1N5985A			
2.7	1N4682	1N4618		1N4371	1N5223	1N5986A			
3.0	1N4683	1N4619		1N4372	1N5225	1N5987A			
3.3	1N4684	1N4620	1N5518A	1N746	1N5226	1N5988A	1N4728	1N3821	1N5913A
3.6	1N4685	1N4621	1N5519A	1N747	1N5227	1N5989A	1N4729	1N3822	1N5914A
3.9	1N4686	1N4622	1N5520A	1N748	1N5228	1N5990A	1N4730	1N3823	1N5915A
4.3	1N4687	1N4623	1N5521A	1N749	1N5229	1N5991A	1N4731	1N3824	1N5916A
4.7	1N4688	1N4624	1N5522A	1N750	1N5230	1N5992A	1N4732	1N3825	1N5917A
5.1	1N4689	1N4625	1N5523A	1N751	1N5231	1N5993A	1N4733	1N3826	1N5918A
5.6	1N4690	1N4626	1N5524A	1N752	1N5232	1N5594A	1N4734	1N3827	1N5919A
6.2	1N4691	1N4627	1N5525A	1N753	1N5234	1N5995A	1N4735	1N3828	1N5920A
6.8	1N4692	1N4099	1N5526A	1N754 1N957A	1N5235	1N5996A	1N4736	1N3829 1N3016A	1N5921A
7.5	1N4693	1N4100	1N5527A	1N755 1N958A	1N5236	1N5997A	1N4737	1N3830 1N3017A	1N5922A
8.2	1N4694	1N4101	1N5528A	1N756 1N959A	1N5237	1N5998A	1N4738	1N3018A	1N5923A
8.7	1N4695	1N4102			1N5238				
9.1	1N4696	1N4103	1N5529A	1N757 1N960A	1N5239	1N5999A	1N4739	1N3019A	1N5924A
10	1N4697	1N4104	1N5530A	1N758 1N961A	1N5240	1N6000A	1N4740	1N3020A	1N5925A
11	1N4698	1N4105	1N5531A	1N962A	1N5241	1N6001A	1N4741	1N3021A	1N5926A
12	1N4699	1N4106	1N5532A	1N759 1N963A	1N5242	1N6002A	1N4742	1N3022A	1N5927A
13	1N4700	1N4107	1N5533A	1N964A	1N5243	1N6003A	1N4743	1N3023A	1N5928A
14	1N4701	1N4108	1N5534A		1N5244				
15	1N4702	1N4109	1N5535A	1N965A	1N5245	1N6004A	1N4744	1N3024A	1N5929A
16	1N4703	1N4110	1N5536A	1N966A	1N5246	1N6005A	1N4745	1N3025A	1N5930A
17	1N4704	1N4111	1N5537A		1N5247				
18	1N4705	1N4112	1N5538A	1N967A	1N5248	1N6006A	1N4746	1N3026A	1N5931A
19	1N4706	1N4113	1N5539A		1N5249				
20	1N4707	1N4114	1N5540A	1N968A	1N5250	1N6007A	1N4747	1N3027A	1N5932A
22	1N4708	1N4115	1N5541A	1N969A	1N5251	1N6008A	1N4748	1N3028A	1N5933A
24	1N4709	1N4116	1N5542A	1N970A	1N5252	1N6009A	1N4749	1N3029A	1N5934A
25	1N4710	1N4117	1N5543A		1N5253				
27	1N4711	1N4118		1N971A	1N5254	1N6010A	1N4750	1N3030A	1N5935A
28	1N4712	1N4119	1N5544A		1N5255				
30	1N4713	1N4120	1N5545A	1N972A	1N5256	1N6011A	1N4751	1N3031A	1N5936A
33	1N4714	1N4121	1N5546A	1N973A	1N5257	1N6012A	1N4752	1N3032A	1N5937A
36	1N4715	1N4122		1N974A	1N5258	1N6013A	1N4753	1N3033A	1N5938A
39	1N4716	1N4123		1N975A	1N5259	1N6014A	1N4754	1N3034A	1N5939A
43	1N4717	1N4124		1N976A	1N5260	1N6015A	1N4755	1N3035A	1N5940A
47		1N4125		1N977A	1N5261	1N6016A	1N4756	1N3036A	1N5941A
51		1N4126		1N978A	1N5262	1N6017A	1N4757	1N3037A	1N5942A
56		1N4127		1N979A	1N5263	1N6018A	1N4758	1N3038A	1N5943A
60		1N4128			1N5264				
62		1N4129		1N980A	1N5265	1N6019A	1N4759	1N3039A	1N5944A
68		1N4130		1N981A	1N5266	1N6020A	1N4760	1N3040A	1N5945A
75		1N4131		1N982A	1N5267	1N6021A	1N4761	1N3041A	1N5946A
82		1N4132		1N983A	1N5268	1N6022A	1N4762	1N3042A	1N5947A
87		1N4133			1N5269				
91		1N4134		1N984A	1N5270	1N6023A	1N4763	1N3043A	1N5948A
100		1N4135		1N985A	1N5271	1N6024A	1N4764	1N3044A	1N5949A
110				1N986A	1N5272	1N6025A	♦1M110ZS10	1N3045A	1N5950A
120				†1N987A	1N5273#		♦1M120ZS10	1N3046A	1N5951A
130				†1N988A	1N5274#		♦1M130ZS10	1N3047A	1N5952A
140					1N5275#				
150				†1N989A	1N5276#		♦1M150ZS10	1N3048A	1N5953A
160				†1N990A	1N5277#		♦1M160ZS10	1N3049A	1N5954A
170					1N5278#		♦1M170ZS10		
180				†1N991A	1N5279#		♦1M180ZS10	1N3050A	1N5955A
200				†1N992A	1N5281#		♦1M200ZS10	1N3051A	1N5956A

▒ JAN/JANTX(V) available, ±5% only.
†1N987-1N992 supplied in DO-7 glass package.
#1N5273-1N5281 supplied in Surmetic DO-7 plastic package.
♦ 1M110ZS10 Series supplied in Surmetic (Plastic) DO-41 package.

5.0

1.5 Watt Cathode to Case	5 Watt Cathode = Polarity Mark	10 Watt Cathode to Case = 1N3993 Series Anode to Case = 1N2970 Series	50 Watt Anode to Case	
(Note 2,10)	(Notes 2,11)	(Notes 2,10,12)	(Notes 2,10,12)	(Notes 2,10,12)
 Metal Case 55	 Surmetic 40 Case 17	 Metal Case 56 (DO-4)	 Metal Case 54 (TO-3)	 Metal Case 58 (DO-5 Type)
	1N5333A			
	1N5334A			
	1N5335A	1N3993&R	1N4557A&RA	1N4549A&RA
	1N5336A	1N3994&R	1N4558A&RA	1N4550A&RA
	1N5337A	1N3995&R	1N4559A&RA	1N4551A&RA
	1N5338A	1N3996&R	1N4560A&RA	1N4552A&RA
	1N5339A	1N3997&R	1N4561A&RA	1N4553A&RA
	1N5341A	1N3998&R	1N4562A&RA	1N4554A&RA
1N3785A	1N5342A	1N3999&R	1N4563A&RA	1N4555A&RA
		1N2970A&RA	1N2804A&RA	1N3305A&RA
1N3786A	1N5343A	1N4000&R	1N4564A&RA	1N4556A&RA
		1N2971A&RA	1N2805A&RA	1N3306A&RA
1N3787A	1N5344A	1N2972A&RA	1N2806A&RA	1N3307A&RA
	1N5345A			
1N3788A	1N5346A	1N2973A&RA	1N2807A&RA	1N3308A&RA
1N3789A	1N5347A	1N2974A&RA	1N2808A&RA	1N3309A&RA
1N3790A	1N5348A	1N2975A&RA	1N2809A&RA	1N3310A&RA
1N3791A	1N5349A	1N2976A&RA	1N2810A&RA	1N3311A&RA
1N3792A	1N5350A	1N2977A&RA	1N2811A&RA	1N3312A&RA
	1N5351A	1N2878A&RA	1N2812A&RA	1N3313A&RA
1N3793A	1N5352A	1N2979A&RA	1N2813A&RA	1N3314A&RA
1N3794A	1N5353A	1N2980A&RA	1N2814A&RA	1N3315A&RA
	1N5354A		1N2815A&RA	1N3316A&RA
1N3795A	1N5355A	1N2982A&RA	1N2816A&RA	1N3317A&RA
	1N5356A	1N2983A&RA	1N2817A&RA	1N3318A&RA
1N3796A	1N5357A	1N2984A&RA	1N2818A&RA	1N3319A&RA
1N3797A	1N5358A	1N2985A&RA	1N2819A&RA	1N3320A&RA
1N3798A	1N5359A	1N2986A&RA	1N2820A&RA	1N3321A&RA
	1N5360A		1N2821A&RA	1N3222A&RA
1N3799A	1N5361A	1N2988A&RA	1N2822A&RA	1N3223A&RA
	1N5362A			
1N3800A	1N5363A	1N2989A&RA	1N2823A&RA	1N3224A&RA
1N3801A	1N5364A	1N2990A&RA	1N2824A&RA	1N3225A&RA
1N3802A	1N5365A	1N2991A&RA	1N2825A&RA	1N3226A&RA
1N3803A	1N5366A	1N2992A&RA	1N2826A&RA	1N3227A&RA
1N3804A	1N5367A	1N2993A&RA	1N2827A&RA	1N3228A&RA
1N3805A	1N5368A	1N2996A&RA	1N2829A&RA	1N3330A&RA
1N3806A	1N5369A	1N2997A&RA	1N2831A&RA	1N3332A&RA
1N3807A	1N5370A	1N2999A&RA	1N2832A&RA	1N3334A&RA
	1N5371A			
1N3808A	1N5372A	1N3000A&RA	1N2833A&RA	1N3335A&RA
1N3809A	1N5373A	1N3001A&RA	1N2834A&RA	1N3336A&RA
1N3810A	1N5374A	1N3002A&RA	1N2835A&RA	1N3337A&RA
1N3811A	1N5375A	1N3003A&RA	1N2836A&RA	1N3338A&RA
	1N5376A			
1N3812A	1N5377A	1N3004A&RA	1N2837A&RA	1N3339A&RA
1N3813A	1N5378A	1N3005A&RA	1N2838A&RA	1N3340A&RA
1N3814A	1N5379A	1N3007A&RA	1N2840A&RA	1N3342A&RA
1N3815A	1N5380A	1N3008A&RA	1N2841A&RA	1N3343A&RA
1N3816A	1N5381A	1N3009A&RA	1N2842A&RA	1N3344A&RA
				1N3345A&RA
1N3817A	1N5383A	1N3011A&RA	1N2843A&RA	1N3346A&RA
1N3818A	1N5384A	1N3012A&RA	1N2844A&RA	1N3347A&RA
	1N5385A			
1N3819A	1N5386A	1N3014A&RA	1N2845A&RA	1N3349A&RA
1N3820A	1N5388A	1N3015A&RA	1N2846A&RA	1N3350A&RA

NOTES

1. The Zener Voltage is measured at approximately 1/4 the rated power, with the following exceptions: the 1N4678–4717 is measured with I_{ZT} = 50 μAdc; the 1N4614/1N4099 is measured with I_{ZT} = 250 μAdc; the 1N4370/1N746 and the 1N5221–5242 are measured with I_{ZT} = 20 mAdc; the 1N5985A–6012A is measured with I_{ZT} = 5 mA; 1N6013A–6023A is measured with I_{ZT} = 2 mA; 1N6024–6025 is measured with I_{ZT} = 1 mA.
2. Contact your Motorola representative for information on intermediate voltages and tighter tolerances.

Tolerances

3. No suffix = ±5%
4. A suffix = ±10% — with guaranteed limits on V_Z, V_F, and I_R only
   B suffix = ±5%
   C suffix = ±2%
   D suffix = ±1%
5. 1N4370/1N746 series: No suffix = ±10%, A suffix = ±5%
   1N957 series: A suffix = ±10%, B suffix = ±5%

Military parts in 1N4370/746/962 series and standard 1N987–1N992 supplied in DO-7. Military parts in 1N4370/746/962 are also available in the cost effective DO-204AH (DO-35) package as the -1 version. This version can be ordered by inserting a 1 between the part number and the JAN, JTX or JTXV suffix, ie 1N746A1JAN. MIL-STD 19500/117 and 127 state the -1 version is a direct substitute for the non -1 version The -1 versions appear on MIL-STD 701 as the preferred parts for new designs. Military parts in 1N4614, 1N4099 and 1N5518A series supplied in DO-7.

6. No suffix = ±10% with guaranteed limits on V_Z, V_F and I_R only.
   A suffix = ±10%
   B suffix = ±5%
7. No suffix = ±10%
   A suffix = ±5%
8. 1N3821 series: No suffix = ±10%, A suffix = ±5%
   1N3016 series: A suffix = ±10%, B suffix = ±5%
9. A suffix = ±10% C suffix = ±2%
   B suffix = ±5% D suffix = ±1%
10. A suffix = ±10%
    B suffix = ±5%
    Exception:
    1N3993–1N4000: No suffix = ±10%, A suffix = ±5%
11. A suffix = ±10%
    B suffix = ±5%
12. RA and RB = Reverse Polarity Types Available
13. A suffix = ±10%
    B suffix = ±5%

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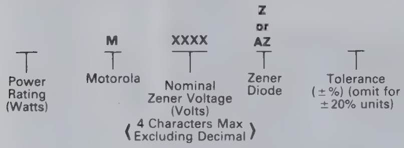
Selected Zener Diode Options

In cases where standard specifications do not meet application requirements, an appropriate device can be selected and ordered from the following options. This coding system is provided as a means of communicating a specific requirement to Motorola. Certain voltages, tolerances and packages may not be available. Contact your Motorola sales representative for availability, price, and minimum order quantities.

NON-STANDARD ZENER DIODES SPECIAL VOLTAGE AND TOLERANCE RATINGS

JEDEC "1N" type numbers denote a specific Zener voltage, power rating, and tolerance. For example, JEDEC type 1N4728 is a standard 1 watt diode, rated at 3.3 volts ± 10%. A suffix "A" on this type number indicates a ± 5% voltage tolerance.

Special Motorola devices, with a choice of voltages and tolerances, are also available. The following diagram explains the Motorola coding system:



For example, the code for a special 10 watt Zener diode with a voltage of 41 volts and a tolerance of ± 1% would be: 10M41Z1.

Following is a list of other standard Motorola symbols for special Zener device orders (X's indicate nominal Zener voltage):

BASIC MOTOROLA TYPE	**ELECTRICALLY SIMILAR SERIES	DEVICE DESCRIPTION
1 4MXXAZXX	1 4M2.4AZ10 series	250 mW, Glass, DO-35
1 4MXXXZXX	1.4M6.8Z10 series	250 mW, Glass, DO-35
.4MXXAZXX	1N4370 & 1N746 series	400 mW 500 mW, Glass, DO-7
4MXXXZXX	1N957 series	400 mW 500 mW, Glass, DO-7
5MXXAZXX	1N4370 & 1N746 series	400 mW 500 mW, Glass, DO-35
5MXXXZXX	1N957 series	400 mW 500 mW, Glass, DO-35
1MXXAZXX	1N3821 series	1 Watt, Metal, DO-13
1MXXXZXX	1N3016 series	1 Watt, Metal, DO-13
1MXXXZGXX	1N4728 series	1 Watt, Glass, DO-41
1MXXXZSXX	1N4728 series	1 Watt, Surmetic-30, DO-41
1.5MXXXZXX	1N3785 series	1.5 Watt Metal Can
5MXXXZSXX	1N5333 series	5 Watt Surmetic-40
10MXXAZXX	1N3993 series	10 Watt, Stud, DO-4
10MXXXZXX	1N2970 series	10 Watt, Stud, DO-4
50MXXAZXX	1N4557 series	50 Watt, TO-3
50MXXXZXX	1N2804 series	50 Watt, TO-3
50MXXAZSXX	1N4549 series	50 Watt, Stud, DO-5
50MXXXZSXX	1N3305 series	50 Watt, Stud, DO-5
MZG35-YYZ	1N5985 series	500 mW, Glass, DO-35
MZG41-YYZ	1N5913 series	1.5 Watt, Surmetic-30

** Electrical parameters shall be tested per the similar series listed. Test currents for non-standard voltages will be linearly interpoled between the test currents for standard parts on either side. For reverse polarity devices (10 W and 50 W) insert an "R" before tolerance.

1N5518 thru 1N5546 — This series may be ordered in ±2% and ±1% tolerance by adding the following suffix:

C = ±2% D = ±1%

For example the 1N5518D would be the same as the 1N5518B except V_Z = 3.3 ±1%.

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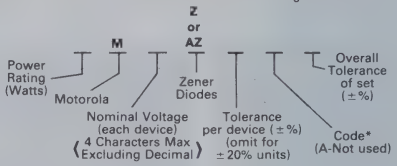
MATCHED SETS OF ZENER DIODES

Zener diodes can also be obtained in sets consisting of two or more matched devices. The method for specifying such matched sets is similar to the one described for specifying units with a special voltage and/or tolerance except that two extra suffixes are added to the code number described above.

These units are marked with code letters to identify the matched sets and in addition, each unit in a set is marked with the same serial number which is different for each set being ordered.



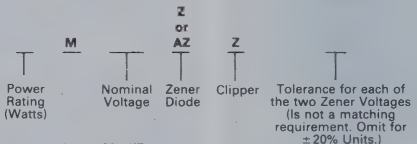
*Code:

B — Two devices in series
C — Three devices in series
D — Four devices in series
E — Five devices in series
F — Six devices in series
G — Seven devices in series
H — Eight devices in series
X — Two devices; one standard polarity, the other reverse polarity. (10 and 50 watts only)

i.e., 10M51Z5B1 is for two 10 watt zeners, each of 51 volts, ± 5%, matched to a total voltage of 102 volts ± 1%.

ZENER CLIPPERS

Special clipper diodes with opposing Zener junctions built into the device are available by using the following nomenclature:



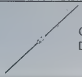
i.e., 10M20ZZ10

This nomenclature is applicable to all packages and power ratings as restricted in the above paragraphs.

Special Purpose Regulators

Field-Effect Current Regulator Diodes

High impedance diodes whose "constant current source" characteristic complements the "constant voltage" of the zener line. Currents are available from 0.22 to 4.7 mA, with usable voltage range from a minimum limit of 1.0 to 2.5 V, up to a voltage compliance of 100 V, for the 1N5283 series, or 70 V, for the MCL1300 series.



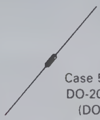
Glass
Case 51-02
DO-204AA
(DO-7)

Reg. Current I_P @V_T = 25 V mA Nom	Device Type	Knee Imp Z_K @V_K = 6.0 V MΩ Min	Limiting Voltage @I_L = 0.8 I_P Volts Max
0.22	1N5283	2.75	1.00
0.24	1N5284	2.35	1.00
0.27	1N5285	1.95	1.00
0.30	1N5286	1.60	1.00
0.33	1N5287	1.35	1.00
0.39	1N5288	1.00	1.05
0.43	1N5289	0.870	1.05
0.47	1N5290	0.750	1.05
0.56	1N5291	0.560	1.10
0.62	1N5292	0.470	1.13
0.68	1N5293	0.400	1.15
0.75	1N5294	0.335	1.20
0.82	1N5295	0.290	1.25
0.91	1N5296	0.240	1.29
1.00	1N5297	0.205	1.35
1.10	1N5298	0.180	1.40
1.20	1N5299	0.155	1.45
1.30	1N5300	0.135	1.50
1.40	1N5301	0.115	1.55
1.50	1N5302	0.105	1.60
1.60	1N5303	0.092	1.65
1.80	1N5304	0.074	1.75
2.00	1N5305	0.061	1.85
2.20	1N5306	0.052	1.95
2.40	1N5307	0.044	2.00
2.70	1N5308	0.035	2.15
3.00	1N5309	0.029	2.25
3.30	1N5310	0.024	3.35
3.60	1N5311	0.020	2.50
3.90	1N5312	0.017	2.60
4.30	1N5313	0.014	2.75
4.70	1N5314	0.012	2.90
0.5±.03	MCL1300	0.500	1.00
1.0±0.6	MCL1301	0.200	1.50
2.0±0.6	MCL1302	0.100	2.00
3.0±0.6	MCL1303	0.050	2.00
4.0±0.6	MCL1304	0.025	2.50

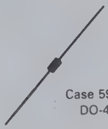
☐ JAN/JANTX (V) availability

Low-Voltage Regulators

High-conductance silicon diodes designed as stable forward-reference sources for transistor amplifier biasing and similar applications. Available in high reliability glass construction or economic plastic packaging.



Case 51-02
DO-204AA
(DO-7)
Surmetic 20



Case 59-03
DO-41

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted).

Forward Reference Voltage		I_F Test Current	Leakage Current I_R @ V_R		Device Type	Case
Min	Max	mA	μA	Volts		
0.63	0.71	10	10	5.0	MZ2360	59 Surmetic
1.24	1.38	10	10	5.0	MZ2361	51 Surmetic

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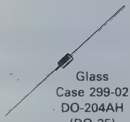
Temperature Compensated Reference Devices

For applications where output voltage must remain within narrow limits during changes in input voltage, load resistance and temperature. Motorola guarantees all References Devices to fall within the specified maximum voltage variations, ΔV_Z, at the specifically indicated test temperatures and test current (JEDEC Standard #5). Temperature Coefficient is also specified but should be considered as a reference only—not a maximum rating.

Devices in this table are hermetically sealed structures. Includes JAN, JANTX AND JTXV devices.

Glass
Case 51-02
DO-204AA
(DO-7)



Glass
Case 299-02
DO-204AH
(DO-35)

V_Z Volts	Test Current mAdc	Test Temp Points	AVERAGE TEMPERATURE COEFFICIENT OVER THE OPERATING RANGE										Case
			0.01 %/°C		0.005 %/°C		0.002 %/°C		0.001 %/°C		0.0005 %/°C		
			Device Type	ΔV_Z Max Volts	Device Type	ΔV_Z Max Volts	Device Type	ΔV_Z Max Volts	Device Type	ΔV_Z Max Volts	Device Type	ΔV_Z Max Volts	
6.2	7.5	A	1N821	0 096	1N823	0.048	1N825	0 019	1N827	0 009	1N829	0 005	299-02
6.2	7.5	A	1N821A	0 096	1N823A	0.048	1N825A	0.019	1N827A	0 009	1N829A	0 005	
6.4	0.5	B	1N4565	0 018	1N4566	0.024	1N4567	0.010	1N4568	0 005	1N4569	0.002	DO-204AH (DO-35)
	0.5	A	1N4565A	0.099	1N4566A	0.050	1N4567A	0.020	1N4568A	0.010	1N4569A	0 005	
	1.0	B	1N4570	0.048	1N4571	0 024	1N4572	0 010	1N4573	0.005	1N4574	0 002	
	1.0	A	1N4570A	0 099	1N4571A	0 050	1N4572A	0 020	1N4573A	0 010	1N4574A	0 005	
	2.0	B	1N4575	0.048	1N4576	0.024	1N4577	0.010	1N4578	0 005	1N4579	0 002	
	2.0	A	1N4575A	0 099	1N4576A	0.025	1N4577A	0.020	1N4578A	0.010	1N4579A	0 005	
	4 0	B	1N4580	0.048	1N4581	0.024	1N4582	0.010	1N4583	0 005	1N4584	0 002	
	4 0	A	1N4580A	0 099	1N4581A	0.050	1N4582A	0.020	1N4583A	0.010	1N4584A	0 005	
8.4	10	A	1N3154	0 130	1N3155	0 065	1N3156	0 026	1N3157	0 013			
	10	C	1N3154A	0.072	1N3155A	0.085	1N3156A	0.034	1N3157A	0.017			51-02
	0.5	B	1N4775	0.064	1N4776	0.032	1N4777	0.013	1N4778	0 006	1N4779	0 003	DO-204AA (DO-7)
	0.5	A	1N4775A	0.132	1N4776A	0 066	1N4777A	0.026	1N4778A	0.013	1N4779A	0.007	
8.5	1.0	B	1N4780	0 064	1N4781	0.032	1N4782	0.013	1N4783	0.006	1N4784	0 003	
	1.0	A	1N4780A	0 132	1N4781A	0 066	1N4782A	0 026	1N4783A	0.013	1N4784A	0 007	
	7.5	B	1N935	0 067	1N936	0.033	1N937	0 013	1N938	0 006	1N939	0 003	
9.0	7.5	A	1N935A	0 139	1N936A	0.069	1N937A	0 027	1N938A	0 013	1N939A	0 007	
	7.5	C	1N935B	0.184	1N936B	0 092	1N937B	0 037	1N938B	0 018	1N939B	0 009	
	7.5	B	1N941	0 088	1N942	0 044	1N943	0.018	1N944	0 009	1N945	0 004	51-02
11.7	7.5	A	1N941A	0 081	1N942A	0 090	1N943A	0.036	1N944A	0.018	1N945A	0 009	DO-204AA
	7.5	C	1N941B	0.239	1N942B	0.120	1N943B	0.047	1N944B	0 024	1N945B	0.012	(DO-7)

Test Temperature Points	
A	-55, 0, +25, +75, +100
B	0, +25, +75
C	-55, 0, +25, +75, +100, +150
D	0, +25, +70
E	55, 0, +25, +75, +125
F	-55, 0, +75, +125, +185
G	+25, +75, +100

(1) Non-suffix — Z_{ZT} = 15, "A" Suffix — Z_{ZT} 10

JAN/JANTX(V) available, +5% only, Military part in the 1N821 and 1N4565 series and supplied in the DO-7 package

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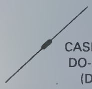
Precision Reference Diodes

Designed, manufactured and tested for ultra-high stability of voltage with time and temperature change. Use of special measurement equipment and voltage standards provide calibration directly traceable to the National Bureau of Standards.

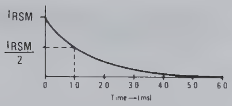


CASE 51-02
DO-204AA
(DO-7)

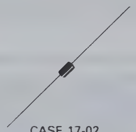
Reference Voltage Volts	Test Current mA	Temperature Stability		CERTIFIED VOLTAGE TIME STABILITY OVER 1000 HOURS OF OPERATION (Parts/Million Change)							
				5 PPM/1000 HR		<10 PPM/1000HR		<20 PPM/1000 HR		40 PPM/1000 HR	
		ΔV_Z (mV)	OP Temp Range °C	Device Type	Change µV Max	Device Type	Change µV Max	Device Type	Change µV Max	Device Type	Change µV Max
6.2 ± 5%	7.5	2 5	25 75,100	MZ605	30	MZ610	60	MZ620	120	MZ640	240

Transient Suppressors

Transient suppressors designed for applications requiring protection of voltage sensitive electronic devices in danger of destruction by high energy voltage transients. Select from standard factory available types or design the suppressor to meet specific needs by paralleling cells. For specific options, i.e., non-standard voltages, higher power capacity, and package configurations, consult factory.



Surge Current Characteristics



CASE 17-02

PEAK POWER DISSIPATION @ 1.0 ms = 600 WATTS

Breakdown Voltage $V_{(BR)}$ Volts Nom	Breakdown Voltage @I_T mA	Device Type	I_{RSM} Maximum Reverse Surge Current Amp	V_{RSM} Maximum Reverse Voltage @ I_{RSM} Volts	Case
6.8	10	P6KE6.8	56	10.8	17-02
7.5	10	P6KE7.5	51	11.7	↓
8.2	10	P6KE8.2	48	12.5	
9.1	1.0	P6KE9.1	44	13.8	
10	1.0	P6KE10	40	15	
11	1.0	P6KE11	37	16.2	
12	1.0	P6KE12	35	17.3	
13	1.0	P6KE13	32	19	
15	1.0	P6KE15	27	22	
16	1.0	P6KE16	26	23.5	
18	1.0	P6KE18	23	26.5	
20	1.0	P6KE20	21	29.1	
22	1.0	P6KE22	19	31.9	
24	1.0	P6KE24	17	34.7	
27	1.0	P6KE27	15	39.1	
30	1.0	P6KE30	14	43.5	
33	1.0	P6KE33	12.6	47.7	
36	1.0	P6KE36	11.6	52	
39	1.0	P6KE39	10.6	56.4	
43	1.0	P6KE43	9.6	61.9	
47	1.0	P6KE47	8.9	67.8	
51	1.0	P6KE51	8.2	73.5	
56	1.0	P6KE56	7.4	80.5	
62	1.0	P6KE62	6.8	89	
68	1.0	P6KE68	6.1	98	
75	1.0	P6KE75	5.5	108	
82	1.0	P6KE82	5.1	118	
91	1.0	P6KE91	4.8	131	
100	1.0	P6KE100	4.2	144	
110	1.0	P6KE110	3.8	158	
120	1.0	P6KE120	3.5	173	
130	1.0	P6KE130	3.2	187	
150	1.0	P6KE150	2.8	215	
160	1.0	P6KE160	2.6	230	
170	1.0	P6KE170	2.5	244	
180	1.0	P6KE180	2.3	258	
200	1.0	P6KE200	2.1	287	↓

Breakdown Voltage for Standard is ±10% Tolerance; ±5% version is available by adding "A", i.e., P6KE6.8A. Clipper (back to back) versions are available by ordering with a "C" or "CA" suffix, i.e., P6KE6.8C or P6KE6.8CA.

TRANSIENT SUPPRESSORS (continued)

CASE 41-11

PEAK POWER DISSIPATION @ 1.0 ms = 1500 WATTS

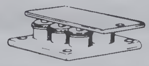
Breakdown Voltage						
$V_{(BR)}$ Volts Nom	@I_T mA	Device Type		I_{RSM} Maximum Reverse Surge Current Amp	V_{RSM} Maximum Reverse Voltage @ I_{RSM} Volts	Case
6.0	1.0	1N5908		120	8.5	41-11
6.8	10	1N6267	1.5KE6.8	139	10.8	
7.5	10	1N6268	1.5KE7.5	128	11.7	
8.2	10	1N6269	1.5KE8.2	120	12.5	
9.1	1.0	1N6270	1.5KE9.1	109	13.8	
10	1.0	1N6271	1.5KE10	100	15.0	
11	1.0	1N6272	1.5KE11	93	16.2	
12	1.0	1N6273	1.5KE12	87	17.3	
13	1.0	1N6274	1.5KE13	79	19.0	
15	1.0	1N6275	1.5KE15	68	22.0	
16	1.0	1N6276	1.5KE16	64	23.5	
18	1.0	1N6277	1.5KE18	56.5	26.5	
20	1.0	1N6278	1.5KE20	51.5	29.1	
22	1.0	1N6279	1.5KE22	47.0	31.9	
24	1.0	1N6280	1.5KE24	43.0	34.7	
27	1.0	1N6281	1.5KE27	38.5	39.1	
30	1.0	1N6282	1.5KE30	34.5	43.5	
33	1.0	1N6283	1.5KE33	31.5	47.7	
36	1.0	1N6284	1.5KE36	29.0	52	
39	1.0	1N6285	1.5KE39	26.5	56.4	
43	1.0	1N6286	1.5KE43	24	61.9	
47	1.0	1N6287	1.5KE47	22.2	67.8	
51	1.0	1N6288	1.5KE51	20.4	73.5	
56	1.0	1N6289	1.5KE56	18.6	80.5	
62	1.0	1N6290	1.5KE62	16.9	89	
68	1.0	1N6291	1.5KE68	15.3	98	
75	1.0	1N6292	1.5KE75	13.9	108	
82	1.0	1N6293	1.5KE82	12.7	118	
91	1.0	1N6294	1.5KE91	11.4	131	
100	1.0	1N6295	1.5KE100	10.4	144	
110	1.0	1N6296	1.5KE110	9.5	158	
120	1.0	1N6297	1.5KE120	8.7	173	
130	1.0	1N6298	1.5KE130	8.0	187	
150	1.0	1N6299	1.5KE150	7.0	215	
160	1.0	1N6300	1.5KE160	6.5	230	
170	1.0	1N6301	1.5KE170	6.2	244	
180	1.0	1N6302	1.5KE180	5.8	258	
200	1.0	1N6303	1.5KE200	5.2	287	
220	1.0		1.5KE220	4.3	344	
250	1.0		1.5KE250	5.0	360	

Breakdown Voltage for Standard is ±10% Tolerance; ±5% version is available by adding "A", i.e., 1N6267A, 1.5KE6.8A. Clipper (back to back) versions are available by ordering the 1.5KE series with a "C" or "CA" suffix, i.e., 1.5KE6.8C or 1.5KE6.8CA.

(continued on next page)

TRANSIENT SUPPRESSORS (continued)

CASE 41-11



CASE 119-01

PEAK POWER DISSIPATION @ 1.0 ms = 1500 WATTS

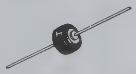
V_{RWM} Working Peak Reverse Voltage (Blocking or Stand-Off Voltage)	Device Type	Clipper (Back To Back) Version	I_{RSM} Maximum Reverse Surge Current Amp	V_{RSM} Maximum Reverse Voltage @ I_{RSM} Volts	Case
5.0	1N6373 / ICTE-5 / MPTE-5	ICTE-5C	160	9.4	41-11
8.0	1N6374 / ICTE-8 / MPTE-8	1N6382	100	15	
10	1N6375 / ICTE-10 / MPTE-10	1N6383	90	16 7	
12	1N6376 / ICTE-12 / MPTE-12	1N6384	70	21.2	
15	1N6377 / ICTE-15 / MPTE-15	1N6385	60	25	
18	1N6378 / ICTE-18 / MPTE-18	1N6386	50	30	
22	1N6379 / ICTE-22 / MPTE-22	1N6387	40	37.5	
36	1N6380 / ICTE-36 / MPTE-36	1N6388	23	65.2	
45	1N6381 / ICTE-45 / MPTE-45	1N6389	19	78 9	

PEAK POWER DISSIPATION @ 1.0 ms = 8000 WATTS

V_R Operating Voltage Nom Vdc	$V_{(RMS)}$	Device Type	I_R Reverse Current µA	ΔV_Z Breakdown Voltage Min Volts	@ I_{ZT} mA	V_C Clamping Voltage Max Volts	@ I_{PP} Amp	V_F Forward Voltage Volts	@ I_F Amp	Case
14	10	MPZ5-16A	50	16	0.4	24	200	1.5	10	119-01
14	10	MPZ5-16B		16	0.4	20	200			
28	20	MPZ5-32A		32	0.2	50	100			
28	20	MPZ5-32B		32	0.2	45	100			
28	20	MPZ5-32C		32	0.2	40	100			
165	117	MPZ5-180A		180	0.03	250	20			
165	117	MPZ5-180B		180	0.03	225	20			
165	117	MPZ5-180C		180	0.03	205	20			

Automotive Transient Suppressors

Automotive Transient Suppressors are designed for protection against over-voltage conditions in the auto electrical system including the "LOAD DUMP" phenomenom that occurs when the battery open circuits while the car is running.

AUTOMOTIVE TRANSIENT SUPPRESSOR		
V_{RRM} (Volts)	194-01 	
23	MR2525L	MR2520L
I_O (Amp)	6	6
$V_{(BR)}$ (Volts)	24-32	24-32
I_{RSM}* (Amp)	110	68
T_C @ Rated I_O (°C)	150	150
T (°C)	175	175

* Time Constant = ms,
Duty Cycle ≤1.0%, T_C = 25°C.

5.0

Lead Tape Packaging Standards for Axial-Lead Components

1.0 SCOPE — This document covers packaging requirements the following axial - lead components for use in automatic testing and assembly equipment: Motorola Case 51 (DO-7), Case 52 (DO-13), Case 59 (DO-41), Case 267, Case 299 (DO-35), Case 59-04 and Case 17. Packaging, as covered in this document, shall consist of axial-lead components mounted by their leads on pressure-sensitive tape, wound onto a reel.

2.0 PURPOSE — This document establishes Motorola standard practices for lead-tape packaging of axial-lead components and meets the requirements of EIA Standard RS-296-D "Lead-taping of components on axial lead configuration for automatic insertion", level 1.

3.0 REQUIREMENTS

3.1 Component Leads

3.1.1 — Component leads shall not be bent beyond dimension E from their nominal position. See Figure 2.

3.1.2 — The "C" dimension shall be governed by the overall length of the reel packaged component. The distance between flanges shall be 0.059 inch to 0.315 inch greater than the overall component length. See Figure 2 and 3.

3.1.3 — Cumulative dimension "A" tolerance shall not exceed 0.059 over 5 in consecutive components.

ORIENTATION — All polarized components must be oriented in one direction. The cathode lead tape shall be blue, and the anode tape shall be white. See Figure 1.

3.3 Reeling

3.3.1 — Components on any reel shall not represent more than two date codes when date code indentification is required.

3.3.2 — Components leads shall be positioned perpendicularly between pairs of 0.250 inch tape. See Figure 2.

3.3.3 — A minimum 12 inch leader of tape shall be provided before the first and last component on the reel.

3.3.4 — 50 lb. Kraft paper is wound between layers of components as far as necessary for component protection. Width of paper is 0.062 inch to 0.750 inch less than "C" dimension of reel. See Figure 3.

3.3.5 — Components shall be centered between tapes such that the difference between D1 and D2 does not exceed 0.055

3.3.6 — Staple shall not be used for splicing. No more than 4 layers of tape shall be used in any splice area and no tape shall be offset from another by more than 0.031 inch noncumulative. Tape splices shall overlap at least 6 inches for butt joints and at least 3 inches for lap joints, and shall not be weaker than unspliced tape.

3.3.7 — Quantity per reel shall be as indicated in Table 1. Orders for tape and reeled product will only be processed and shipped in full reel increments. Scheduled orders must be in releases of full reel increments or multiples thereof. High volume orders and releases (item numbers 6 through 10 excepted) may be reeled on 14.00 inch reels at Motorola's option, therefore making the quantity per reel twice that shown for the 10.50 inch reels.

3.3.8 — A maximum of 0.25% of the components per reel quantity may be missing without consecutive missing per level 1 of RS-296-D.

3.3.9 — The single face roll pad shall be placed around the finished reel and taped securely. Each reel shall then be placed in an appropriate container.

3.4 MARKING — Minimum reel and carton marking shall consist of the following: See Figure 3.

Part number
Purchase order number
Quantity
Date of reeling (when aplicable)
Manufacturer's name
Electrical value (when applicable)
Date codes (when applicable; see note 3.3.1)
Tape (when applicable)

4.0 — Requirements differing from this Motorola standard shall be negotiated with the factory.

The packages indicated in the following table are suitable for lead tape packaging. The table indicates the specific devices (rectifiers and/or zeners) that can be obtained from Motorola in reel packaging, and provides the appropriate packaging specification.

TABLE 1—PACKAGING DETAILS (ALL DIMENSIONS IN INCHES)

Case Type	Product Catagory	Quantity Per Reel (Item 3.3.7)	Component Spacing A	Tape Spacing B	Reel Dimensions C	Reel Dimensions D (max)	Max Off Alignment E	Item Number
Case 51 (DO-7)	Zeners	3000	0.200 ± 0.020	2.062 ± .059	3.00	10.50	0.047	1
Case 299 (DO-35)	Zeners	3000	0.200 ± 0.020	2.062 ± .059	3.00	10.50	↓	2
Case 17	Zeners	2000	0.200 ± 0.015	2.062 ± .059	3.00	10.50		3
Case 59-03 (DO-41)	Zeners	3000	0.200 ± 0.015	2.062 ± .059	3.00	10.50		4
Case 59-01 (DO-41)	Zeners	3000	0.200 ± 0.015	2.062 ± .059	3.00	10.50		5
Case 59-04	Rectifiers	5000	0.200 ± 0.020	2.062 ± .059	3.00	14.00		6
Case 52 (DO-13)	Zeners	1500	0.400 ± 0.020	2.500 ± .059	3.81	14.00		7
Case 267	Rectifiers	1500	0.400 ± 0.020	2.062 ± .059	3.00	14.00		8
Case 41-11	Zeners	1500	0.400 ± 0.020	2.500 ± .059	3.81	14.00		9
Case 194-01	Rectifiers	720	0.500 ± 0.020	1.875 ± .059	3.00	14.00		10
Case 194-05	Rectifiers	810	0.400 ± 0.020	1.875 ± .059	3.00	14.00		11

FIGURE 1 - REEL PACKING

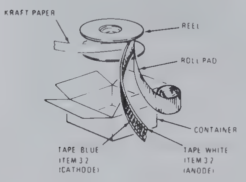


FIGURE 2 COMPONENT SPACING

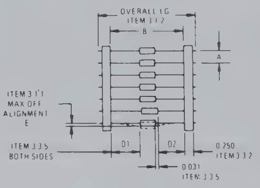
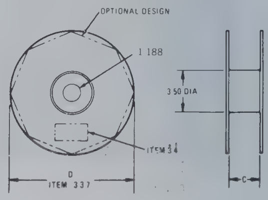


FIGURE 3 - REEL DIMENSIONS



5.0

OUTLINE DIMENSIONS LEADFORM OPTIONS MOUNTING HARDWARE & TECHNIQUES

Contents

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Thyristor Outline Dimensions	6-4
Power Transistor Leadform Options	6-7
Power Transistor Mounting Hardware	6-11
Thyristor Mounting Hardware	6-25
Power Semiconductors Mounting Techniques	6-26

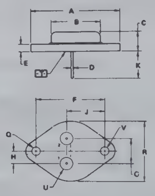
6.0

Power Transistor Package Outline Dimensions

CASE 1-05
TO-204AA

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN



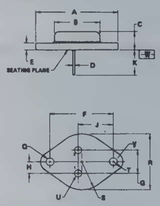
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. -T- IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
⌖ | ø 0.13 (0.005) Ⓜ | T | V Ⓜ
FOR LEADS
⌖ | ø 0.13 (0.005) Ⓜ | T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

CASE 1-04
TO-204AA

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

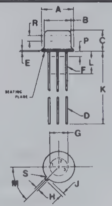


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
⌖ | ø 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ | ø 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

CASE 31-03
TO-205AA

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

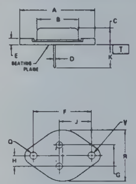


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.711	0.864	0.028	0.034
J	0.734	1.14	0.029	0.045
K	38.10	44.45	1.500	1.750
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	—		—	
P	–	1.27	–	0.050
R	2.54	–	0.100	–
S	–	0.25	–	0.010

NOTES:
1. LEAD POSITIONAL TOLERANCE
⌖ | ø 0.36 (0.014) Ⓜ | A | C Ⓜ | B Ⓜ
2. F DIA. SHALL BE HELD BETWEEN L MINUS P DIM. D DIA. SHALL APPLY BETWEEN K MINUS L DIM. LEAD DIAMETER IS NOT CONTROLLED WITHIN P LENGTH NOR BEYOND K DIMENSION
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973
4. CONTROLLING DIMENSION INCH

CASE 11-01
TO-204AA

STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

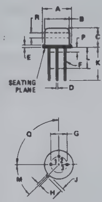
NOTES
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS
2. POSITIONAL TOLERANCE FOR HOLE Q
⌖ | ø 0.25 (0.010) Ⓜ | T | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS
⌖ | ø 0.30 (0.012) Ⓜ | T | V Ⓜ | Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973

CASE 79-02
TO-205AD

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

STYLE 1
PIN 1 EMITTER
2 BASE
3 COLLECTOR

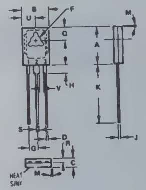


CASE 77-04
TO-126

STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 5
1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–



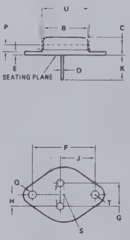
NOTES.
2. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. TO DIM. "A" & "B" AT MAXIMUM MATERIAL CONDITION.

CASE 80-02
TO-213AA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

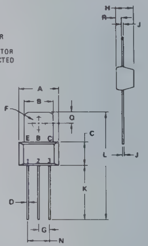
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR



CASE 152-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

STYLE 1
PIN 1 EMITTER
2 BASE
3 COLLECTOR
(COLLECTOR CONNECTED TO TAB)



NOTE
1. LEADS WITHIN 0.15 mm (0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

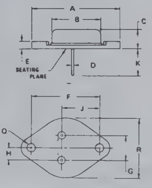
6.0

CASE 197-01
TO-204AE (Type) (TO-3)
Except Pin Diameter

STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

STYLE 2
PIN 1 EMITTER
2 BASE
CASE COLLECTOR

STYLE 3
PIN 1 GATE
2 SOURCE
CASE DRAIN



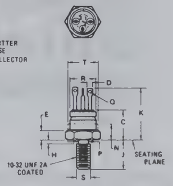
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.0[illegible]	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 160-03
TO-210AA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	10.77	11.10	0.424	0.437
C	8.13	11.89	0.320	0.468
E	2.29	3.81	0.090	0.150
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	10.16	11.56	0.400	0.455
K	14.48	19.38	0.570	0.763
L	2.29	2.79	0.090	0.110
N	–	6.35	–	0.250
P	4.14	4.80	0.163	0.189
Q	1.02	1.65	0.040	0.065
R	8.08	9.65	0.318	0.380
S	4.212	4.310	0.1658	0.1697
T	9.65	11.10	0.380	0.437

All JEDEC dimensions and notes apply
Collector isolated from case.

STYLE 1
PIN 1 EMITTER
2 BASE
3 COLLECTOR

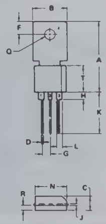


CASE 306-04
TO-202AC

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

STYLE 1
PIN 1 EMITTER
2 BASE
3 COLLECTOR
4 COLLECTOR

STYLE 3
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

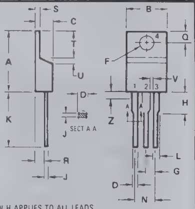


CASE 221A-02
TO-220AB

STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

STYLE 5
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14 60	15 75	0 575	0 620
B	9 65	10 29	0 380	0 405
C	4 06	4 82	0 160	0 190
D	0 64	0 89	0 025	0 035
F	3 61	3 73	0 142	0 147
G	2 41	2 67	0 095	0 105
H	2 79	3 93	0 110	0 155
J	0 36	0 56	0 014	0 022
K	12 70	14 27	0.500	0 562
L	1 14	1 39	0 045	0 055
N	4 83	5 33	0 190	0 210
Q	2 54	3 04	0 100	0 120
R	2 04	2 79	0 080	0.110
S	1 14	1 39	0 045	0 055
T	5.97	6 48	0.235	0 255
U	0 00	1 27	0 000	0.050
V	1.14	–	0 045	–
Z	–	2.03	–	0.080

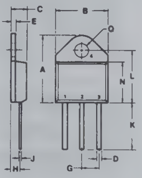


NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3
3 DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4 DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
5 CONTROLLING DIMENSION INCH

CASE 340-01
TO-218AC

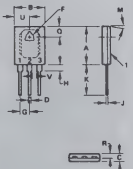
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20 32	21 08	0 800	0 830
B	15 49	15 90	0 610	0 626
C	4 19	5 08	0 165	0 200
D	1 02	1 65	0 040	0 065
E	1 35	1 65	0 053	0 065
G	5 21	5 72	0 205	0 225
H	2 41	3 20	0 095	0 126
J	0 38	0 64	0 015	0 025
K	12 70	15 49	0 500	0 610
L	15 88	16 51	0 625	0 650
N	12 19	12 70	0 480	0 500
Q	4 04	4 22	0 159	0 166

STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR



CASE 90-05
TO-225AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

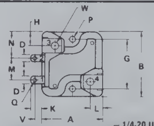


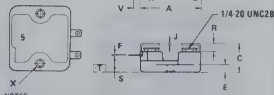
NOTES
1 DIM "Q" UNCONTROLLED IN ZONE "H"
2 DIM "F" DIA THRU
3 HEAT SINK CONTACT AREA (BOTTOM)
4 LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION

CASE 346-01
MO-040AA

STYLE 1
PIN 1 BASE
2 EMITTER
3 EMITTER
4 COLLECTOR
5 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	53.09	53.84	2 090	2.120
B	55 37	56.39	2 180	2 220
C	–	26.67	–	1.050
D	6 10	6.60	0.240	0 260
E	6.60	7 11	0.260	0.280
F	0 71	0 81	0.028	0 032
G	43.31 BSC		1.705 BSC	
H	12.57	12.82	0.495	0 505
J	1.52	1 62	0.060	0.064
K	9 50	9.75	0 374	0.384
L	10.21	10 46	0.402	0 412
M	18 92	19.18	0.745	0 755
N	23.67	23.93	0.932	0.942
P	5 08	5.21	0.200	0.205
Q	3.53	3 78	0 139	0 149
R	6 76	7.26	0.266	0.286
S	14.73	15.24	0.580	0.600
V	5 33	5.84	0.210	0.230
W	6.40	6.65	0.252	0 262
X	7.37	7.87	0.290	0.310





NOTES
1 DIMENSION A AND B ARE DATUMS
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
⊕ ∅ 0 36 (0 014) Ⓜ T A Ⓜ B Ⓜ
4 DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

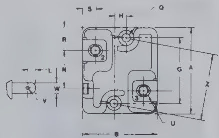
STYLE 2
PIN 1 GATE
2 SOURCE
3 SOURCE
4 DRAIN
5 DRAIN

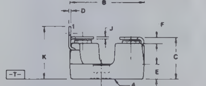
CASE 353-01

STYLE 1
PIN 1 BASE
2 EMITTER
3 COLLECTOR
4 COLLECTOR

STYLE 2
PIN 1 GATE
2 SOURCE
3 DRAIN
4 DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	39.11	40.13	1.540	1 580
B	33.93	34 95	1.336	1.376
C	-	20.32		0 800
D	0.68	0.83	0 027	0.033
E	8.30	8.81	0.327	0 347
F	–	4 44	–	0 175
G	29.67 BSC		1.168 BSC	
H	5 03 BSC		0.200 BSC	
J	0.93	1 09	0.037	0 043
K	—	25 40	–	1 000
L	2.92	3.30	0 115	0.130
N	17 14	17 39	0 675	0 685
Q	3.73	3.88	0 147	0 153
R	10.41	10.79	0.410	0.425
S	5.84	6.35	0.230	0.250
U	M5 .8 (METRIC THRD)			
V	1.27	1.52	0.050	0.060
W	4 69	4.85	0.185	0 191
X	30.15 BSC		1.187 BSC	





NOTES
1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM SURFACE AND SEATING PLANE
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES
⊕ ∅ 0 25 (0 010) Ⓜ T A Ⓜ P Ⓜ
3 DIMENSIONING AND TOLERANCING PER ANSI Y14 5 1982
4 CONTROLLING DIMENSION INCH EXCEPT FOR METRICALLY THREADED INSERTS
5 MOUNTING HOLE CENTERS (DIMENSION X) SAME AS TO 204 (TO 3) FAMILY

6.0

THYRISTOR OUTLINE DIMENSIONS

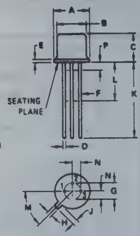
Case 22-03
TO-206AA (TO-18)
Styles 5, 6, 9

STYLE 5:
PIN 1. EMITTER
2. BASE 1
3. BASE 2

STYLE 6:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4 32	5.33	0 170	0.210
D	0.406	0 533	0.016	0.021
E	–	0 762	–	0 030
F	0 406	0 483	0 016	0 019
G	2 54 BSC		0 100 BSC	
H	0 914	1 17	0 036	0 046
J	0 711	1 22	0 028	0 048
K	12 70	–	0 500	–
L	6 35	–	0 250	–
M	45° BSC		45° BSC	
N	1 27 BSC		0 050 BSC	
P	–	1.27	–	0.050

STYLE 9:
PIN 1. ANODE 2
2. ANODE 1
3. GATE
(CONNECTED TO CASE)

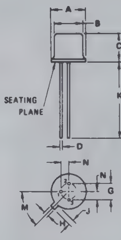


All JEDEC notes and dimensions apply.

Case 22A-01
Style 1

STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	



Case 29-02
TO-226AA (TO-92)
Style 9, 10, 12, 16

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0 210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0 165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.67	0.080	0.105
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

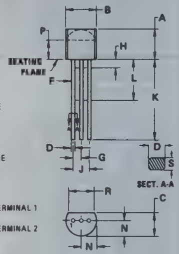
STYLE 9
PIN 1. BASE 1
2. EMITTER
3 BASE 2

STYLE 10:
PIN 1. CATHODE
2 GATE
3. ANODE

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

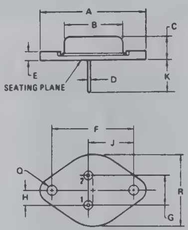
STYLE 16.
PIN 1. ANODE
2. GATE
3. CATHODE



All JEDEC dimensions and notes apply

Case 54-05
Style 2

STYLE 2: (THY)
PIN 1. GATE
2. CATHODE
CASE: ANODE

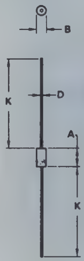


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.12	–	1.540
B	–	20.70	–	0.815
C	–	7.92	–	0.312
D	1.22	1.30	0.048	0.051
E	2.84	3.05	0.112	0.120
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.54	16.79	0.651	0.661
K	8.13	10.67	0.320	0.420
Q	3.84	4.09	0.151	0.161
R	–	26.16	–	1.030

Case 59-04
Style 1

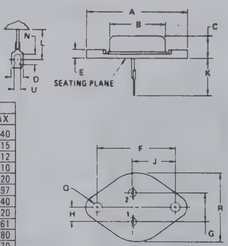
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.60	0 235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

NOTES.
1. ALL RULES AND NOTES ASSOCIATED WITH JEDEC DO-41 OUTLINE SHALL APPLY.
2. POLARITY DENOTED BY CATHODE BAND.
3. LEAD DIAMETER NOT CONTROLLED WITHIN "F" DIMENSION.



Case 61-03
Style 1

STYLE 1:
PIN 1. GATE
2. CATHODE
CASE: ANODE

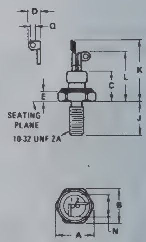


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.23	39.12	1.505	1.540
B	20.32	20.70	0.800	0.815
C	6.99	7.92	0.275	0.312
D	4.83	5.33	0.190	0.210
E	2.84	3.05	0.112	0.120
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.54	16.79	0.651	0.661
K	16.51	17.27	0.650	0.680
N	3.30	4.32	0.130	0.170
Q	3.84	4.09	0.151	0.161
R	24.64	26.16	0.970	1.030
U	2.29	2.79	0.090	0.110

Case 63-02
TO-64
Style 1

STYLE 1.
PIN 1. CATHODE
2. GATE
STUD – ANODE

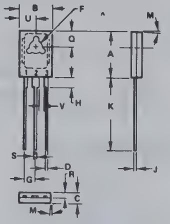
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.57	12.83	0 495	0.505
B	10.77	11 10	0.424	0.437
C	–	10.80	–	0.425
D	3.94	4.70	0.155	0 185
E	–	3.56	–	0 140
J	10.16	11 51	0.400	0 453
K	–	21.72	–	0.855
L	–	17.78	–	0.700
N	–	7.11	–	0.280
Q	1.02	1.91	0 040	0 075



6.0

Case 77-04
Styles 2, 5, 7

STYLE 2
PIN 1. CATHODE
2. ANODE
3. GATE



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

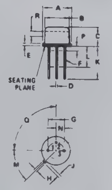
STYLE 5
PIN 1. MT1
2. MT2
3. GATE

STYLE 7
PIN 1 MT 1
2 GATE
3. MT 2

Case 79-02
TO-39
Style 3

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P		1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

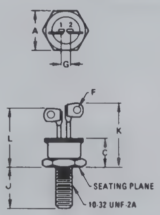
STYLE 3.
PIN 1. CATHODE
2. GATE
3. ANODE



All JEDEC dimensions and notes apply.

Case 86-01
Style 1

STYLE 1:
PIN 1. GATE
2. CATHODE
STUD: ANODE



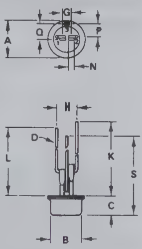
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	11.10	–	0.437
C	–	7.87	–	0.310
F	1.78 TYP		0.070 TYP	
G	2.29	2.79	0.090	0.110
J	10.72	11.48	0.422	0.452
K	–	16.76	–	0.660
L	–	15.49	–	0.610

NOTE.
1. DIM "G" MEASURED AT CAN.

Case 87L-02
Style 1

STYLE 1:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 2:
PIN 1. GATE
2. MAIN TERMINAL 1
3. MAIN TERMINAL 2



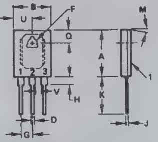
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	10.92	–	0.430
B	–	8 89	–	0.350
C	–	5.97	–	0.235
D	0.76	0.86	0.030	0.034
G	2.29	2.79	0.090	0 110
H	8.89	9.39	0.350	0.370
K	33.53	–	1 320	–
L	31.50 TYP		1.240 TYP	
N	1.65	1.91	0.065	0.075
P	3.43	3.68	0.135	0.145
Q	4.57	5.08	0.180	0.200
S	30.48	–	1.200	–

NOTES:
1. DIM "G" MEASURED AT CAN.
2. LEAD NO. 3 ±7.5° DISPLACEMENT

Case 90-05
Styles 1, 4

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

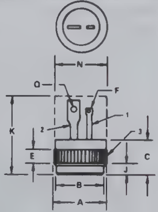


STYLE 1:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 4:
PIN 1. MT1
2. MT2
3. GATE
MT = MAIN TERMINAL

Case 174-04
Styles 1, 3

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	2.16	0.035	0.085
H	3.75	4.41	0.148	0.174
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160



STYLE 1:
TERM. 1. GATE
2. CATHODE
3. ANODE

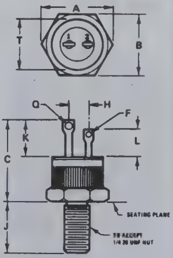
STYLE 3:
TERM. 1. GATE
2. MAIN TERMINAL 1
3. MAIN TERMINAL 2

Case 175-03
Styles 1, 3

STYLE 1:
TERM 1 CATHODE
2. GATE
STUD: ANODE

STYLE 2.
TERM. 1. ANODE
2. GATE
STUD: CATHODE

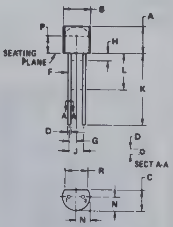
STYLE 3:
TERM. 1. MAIN TERMINAL 1
2. GATE
STUD MAIN TERMINAL 2



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	3.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	3.75	4.41	0.148	0.174
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.416
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
T	12.70	12.83	0.500	0.505

Case 182-02
TO-226AC (TO-92)
Style 3

STYLE 3:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

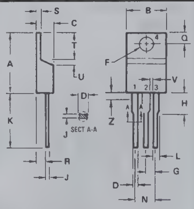
All JEDEC dimensions and notes apply

6.0

Case 221A-02
TO-220AB
Styles 3, 4

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2 MAIN TERMINAL 2
3. GATE
4 MAIN TERMINAL 2



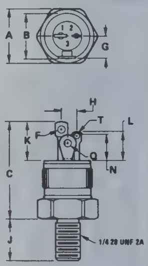
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0 142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0 045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	-	0.045	-
Z	-	2.03	-	0.080

NOTES
1 DIMENSION H APPLIES TO ALL LEADS
2 DIMENSION L APPLIES TO LEADS 1 AND 3
3 DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4 DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
5 CONTROLLING DIMENSION INCH

Case 235-03
Styles 1, 2

STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE
STUD. ISOLATED

STYLE 2:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2
STUD. ISOLATED

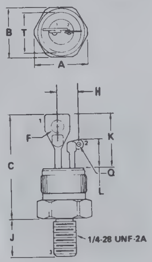


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	26.16	–	1.030
F	1.65	4.06	0.065	0.160
G	–	6.48	–	0.255
H	3.75	4.41	0.148	0 174
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
T	0.89	2.16	0 035	0.085

Case 263-04
Styles 1, 2

STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

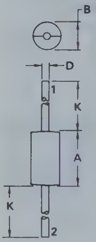
STYLE 2:
PIN 1. MT 1
2. GATE
3. MT 2



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	2.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	–	6.73	–	0.265
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
T	12.73	12.83	0.501	0.505

Case 267-01
Style 1

STYLE 1:
PIN 1. MT 1
2. MT 2

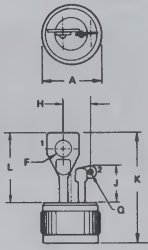


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

Case 310-02
Styles 1, 2

STYLE 1:
1. CATHODE
2. GATE
CASE. ANODE

STYLE 2:
1. MT 1
2. GATE
CASE. MT 2

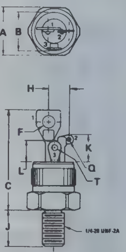


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.73	12.83	0.501	0.505
F	–	4.06	–	0.160
H	–	6.73	–	0.265
J	7.62	8.89	0.300	0.350
K	–	26.67	–	1.050
L	–	17.02	–	0.670
Q	1.40	2.16	0.055	0.085

Case 311-02
Styles 1, 2

STYLE 1:
1. CATHODE
2. GATE
3. ANODE

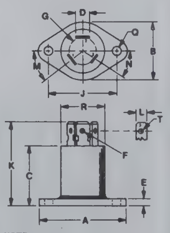
STYLE 2:
1. MT 1
2. GATE
3. MT 2



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
H	–	6.73	–	0.265
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

Case 326-01
Style 2

STYLE 2
1. MT 1
2. MT 2
3. GATE

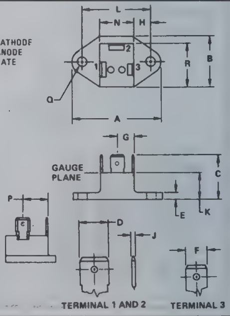


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	26.67	–	1.050
C	–	27.30	–	1.075
D	6.22	6.48	0.245	0.255
E	3.02	3.33	0.119	0.131
F	1.52	2.03	0.060	0.080
G	12.19	12.70	0.480	0.500
J	29.90	30.40	1.177	1.197
K	35.56	37.08	1.400	1.460
L	4.57	4.95	0.180	0.195
M	35°	40°	35°	40°
N	30°	35°	30°	35°
Q	3.81	4.09	0.150	0.161
R	19.81	22.35	0.780	0.880
T	1.02	1.52	0.040	0.060

NOTE:
1. DIMENSIONS D AND F APPLY TO TERMINAL 1 AND 2.

Case 342-01
Style 1

STYLE 1:
TERM. 1. CATHODE
2. ANODE
3. GATE



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.62	1.510	1.560
B	21.85	24.38	0.860	0.960
C	22.86	25.40	0.900	1.000
D	6.28	6.42	0.247	0.253
E	2.80	4.06	0.110	0.160
F	4.68	4.82	0.184	0.190
G	6.86	8.12	0.270	0.320
H	7.24	8.00	0.285	0.315
J	0.79	0.83	0.031	0.033
K	14.48	15.49	0.570	0.610
L	29.85	30.35	1.175	1.195
N	14.48	15.49	0.570	0.610
P	10.67	12.19	0.420	0.480
Q	3.81	4.19	0.150	0.165
R	17.78	19.30	0.700	0.760

NOTES:
1. TERMINAL DIMENSIONS SHALL BE MEASURED AT GAUGE PLANE.
2. DIMENSION J; 3 PLACES.

LEADFORM OPTIONS FOR MOTOROLA PLASTIC POWER TRANSISTORS

ORDERING INFORMATION

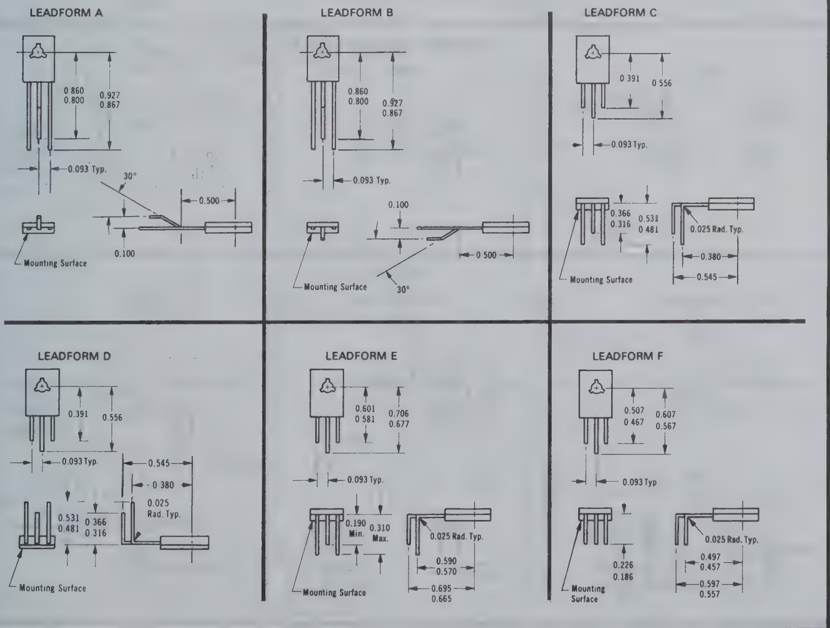
TO-225AA (Case 77), TO-225AB (Case 90), TO-220AB (Case 221A)

Devices may be leadformed by first converting to a special "SJE" number. The factory must be given the designation of the package and the applicable leadform suffix letter. The factory must be consulted.

TO-202 (Duowatt) Case 152 (Uniwatt)

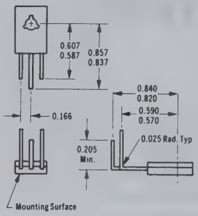
Any device in these packages may be leadformed by designating the proper suffix number after the device type called out.
Example—To leadform an MPS-U01 into the TO-5 configuration, designate it as: MPS-U01-05.

TO-225AA LEADFORMS

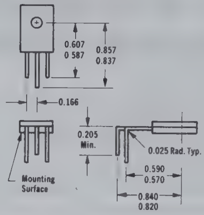


TO-225AB LEADFORMS

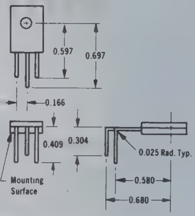
LEADFORM A



LEADFORM B

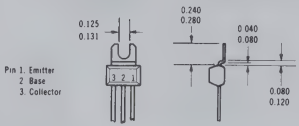


LEADFORM C

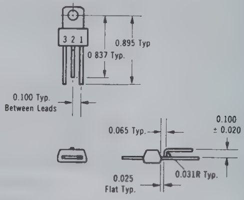


CASE 152 - UNIWATT

CASE 152 - 1

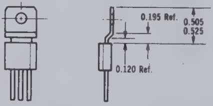


CASE 152 - 5
(TO - 5 Type)

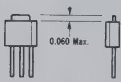


TO202 - DUOWATT

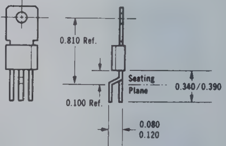
TO202 - 1



TO202 - 2

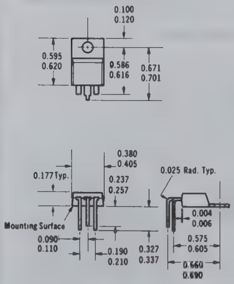


TO202 - 5
(TO - 5 Type)

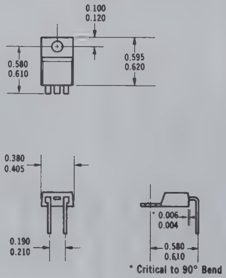


TO220

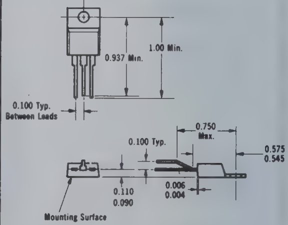
TO220 - A



TO220 - B
(JEDEC TO220 - AA)
(TO66 Type)



TO220 - C



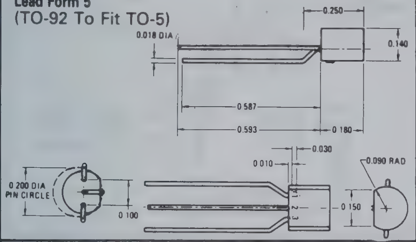
6.0

THYRISTOR LEADFORM OPTIONS

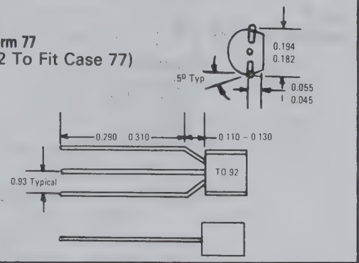
Plastic packaged semiconductors may be leadformed to a variety of configurations for insertion into sockets and boards designed for metal can devices. The following are standard thyristor and trigger leadforms offered by Motorola.

To order leadformed product, determine the form desired, and specify case number and applicable leadform number. A special device title will be assigned by the factory to process your order. Certain standard devices already incorporate a leadform, and may be purchased without consulting the factory.

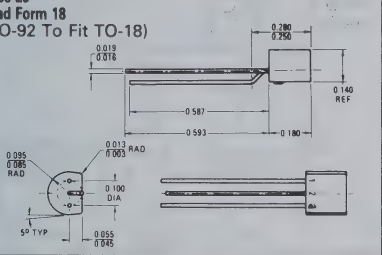
Case 29
Lead Form 5
(TO-92 To Fit TO-5)



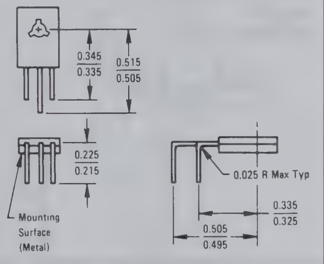
Case 29
Lead Form 77
(TO-92 To Fit Case 77)



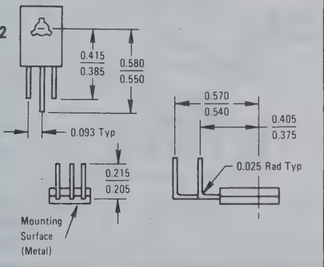
Case 29
Lead Form 18
(TO-92 To Fit TO-18)



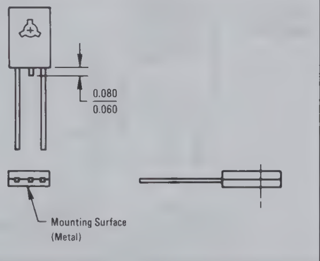
Case 77
Lead Form 1



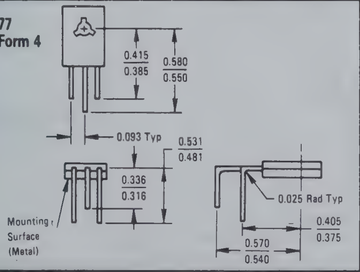
Case 77
Lead Form 2



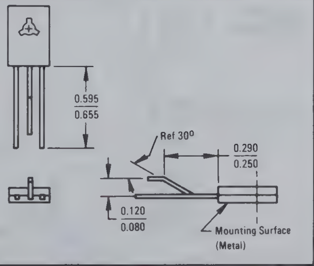
Case 77
Lead Form 3



Case 77
Lead Form 4

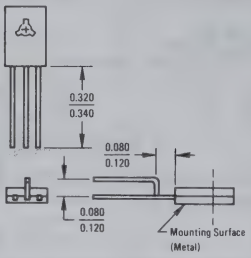


Case 77
Lead Form 5

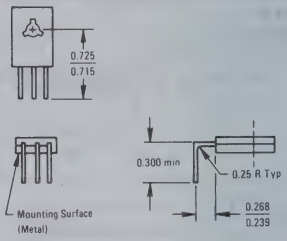


6.0

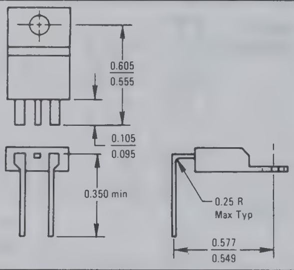
Case 77
Lead Forms 11 and 21



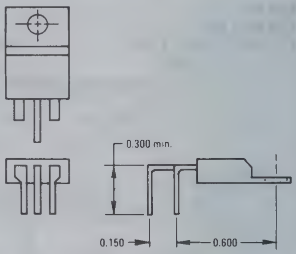
Case 90
Lead Form 1



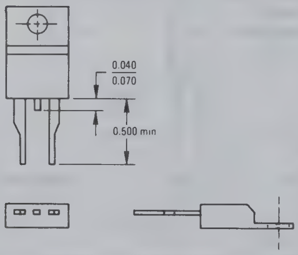
Case 221
Lead Form 2



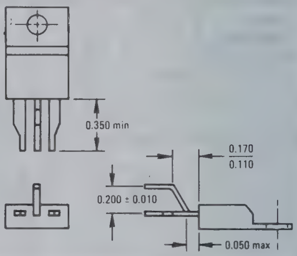
Case 22
Lead Form 3



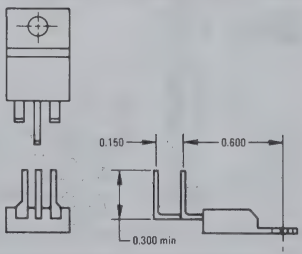
Case 221
Lead Form 4



Case 221
Lead Form 5



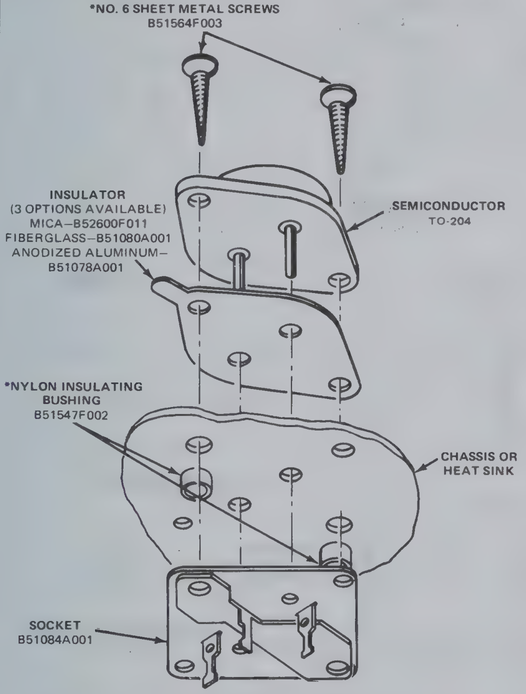
Case 221
Lead Form 6



6.0

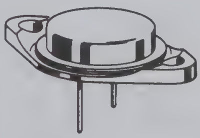
POWER TRANSISTOR MOUNTING HARDWARE

MOUNTING HARDWARE
TO-204
(Formerly TO-3)



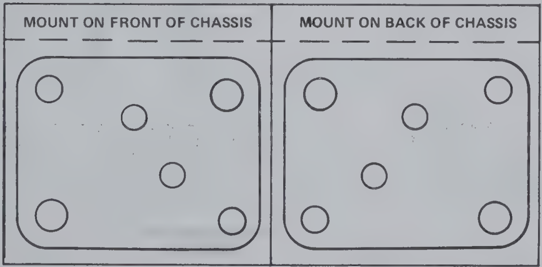
*Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

This hardware is applicable to the following packages.



CASE 1 (TO-204)
CASE 3
CASE 11A
CASE 11 (TO-204)
CASE 12
CASE 54
CASE 197

DRAWINGS NOT TO SCALE

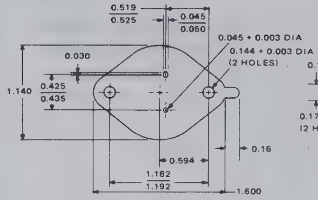


FRONT TEMPLATE
B51087A001

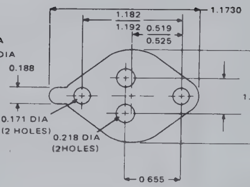
BACK TEMPLATE
B51087A002

6.0

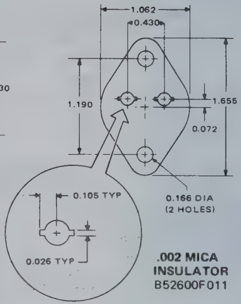
MOUNTING HARDWARE TO-204



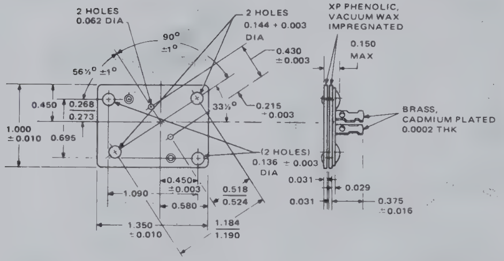
0.003 TEFLON-COATED FIBERGLASS INSULATOR
B51080A001



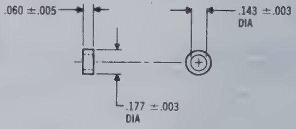
.020 ALUMINUM INSULATOR
B51078A001



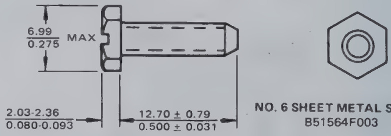
.002 MICA INSULATOR
B52600F011



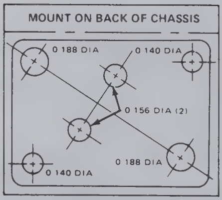
TRANSISTOR SOCKET
B51084A001



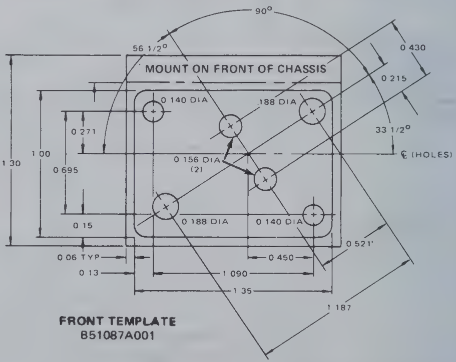
NYLON INSULATING BUSHING
B51547F002



NO. 6 SHEET METAL SCREW
B51564F003



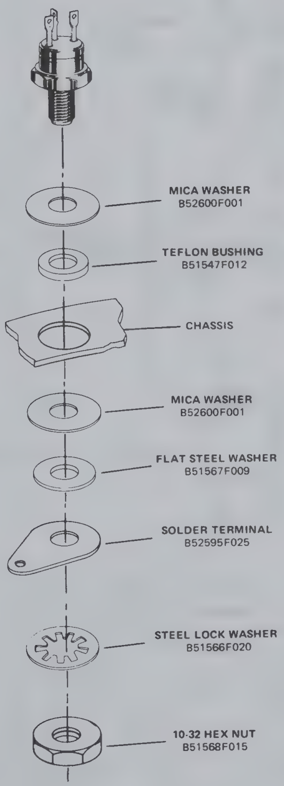
BACK TEMPLATE
B51087A002



FRONT TEMPLATE
B51087A001

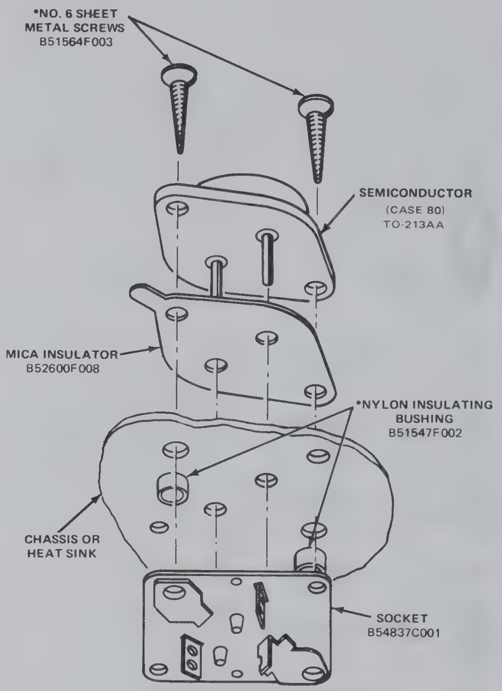
6.0

MOUNTING HARDWARE TO-210AA
(Formerly TO-59)

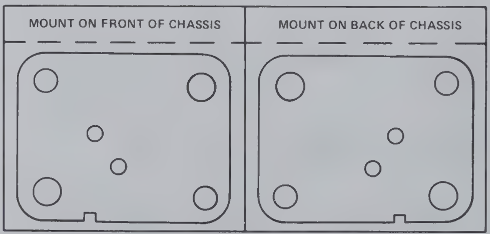


MOUNTING HARDWARE TO-213AA

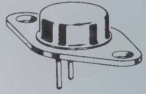
(Formerly TO-66)

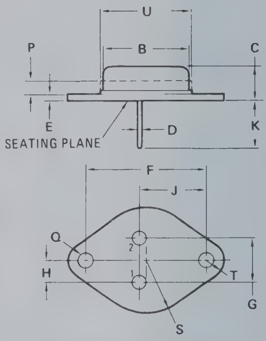


*Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.



FRONT TEMPLATE B54879C001 (DRAWINGS NOT TO SCALE) BACK TEMPLATE B54879C002





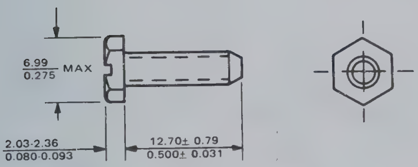
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

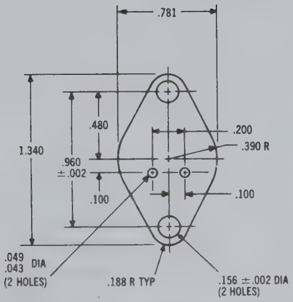
CASE 80
TO-213AA

6.0

MOUNTING HARDWARE TO-213AA

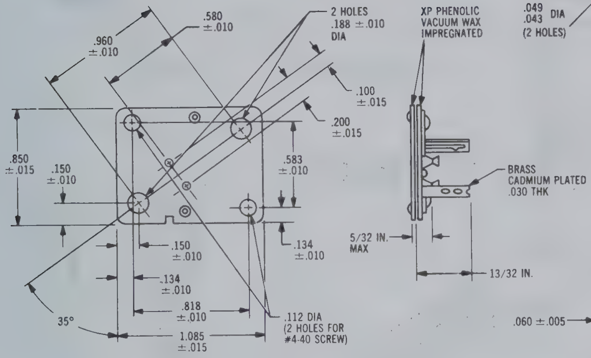


NO. 6 SHEET METAL SCREW
B51564F003

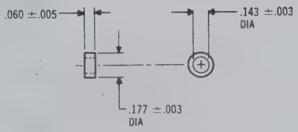


0.005 MICA INSULATOR
B52600F008

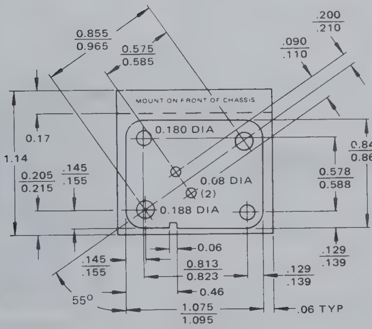
0.003 MICA INSULATOR
B52600F009



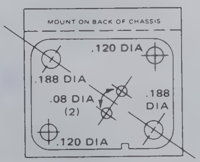
TRANSISTOR SOCKET
B54837C001



NYLON INSULATING BUSHING
B51547F002

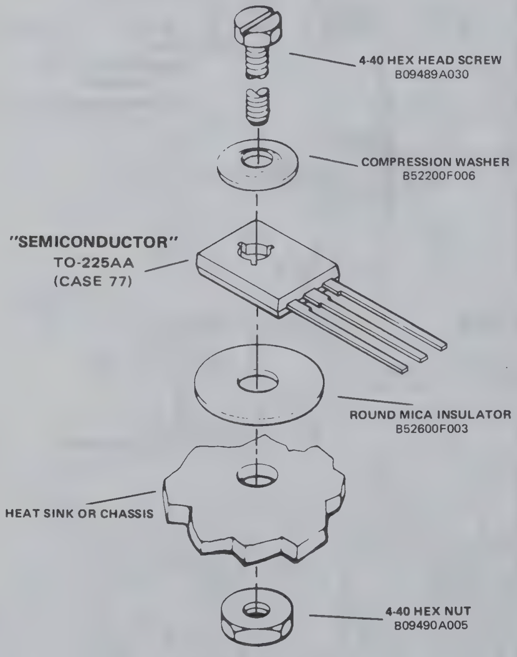


FRONT TEMPLATE
B54879C001

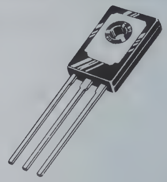


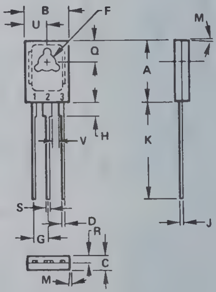
BACK TEMPLATE
B54879C002

MOUNTING HARDWARE TO-225AA
(Formerly TO-126)



TORQUE REQUIREMENTS
0.68N-m (6IN-LBS.) MAX.





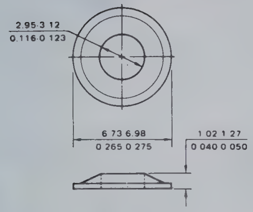
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
(TO-225AA)

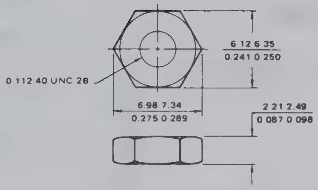
6.0

MOUNTING HARDWARE TO-225AA

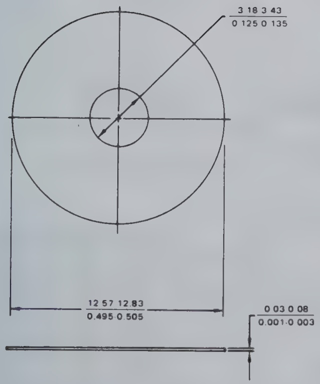
(DIMENSIONS – MILLIMETERS / INCH)



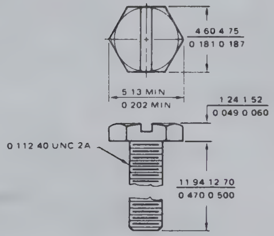
STEEL COMPRESSION WASHER
B52200F006



4-40 HEX NUT
CARBON STEEL,
CADMIUM PLATED
B09490A005



ROUND MICA INSULATOR
B52600F003



4-40 HEX HEAD SCREW
CARBON STEEL,
CADMIUM PLATED
B09489A003

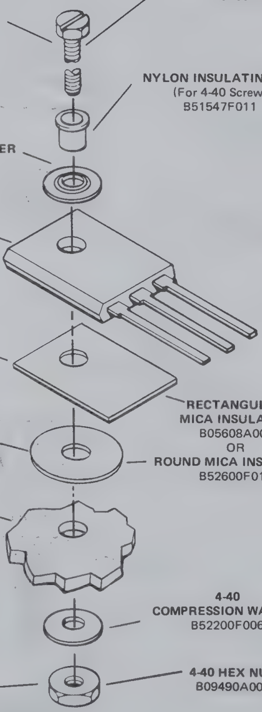
6.0

MOUNTING HARDWARE TO-225AB CASE 90

(Formerly TO-127)

Part numbers in this column for **INSULATED MOUNTING**

Part numbers in this column for ***HIGH VOLTAGE INSULATED MOUNTING**

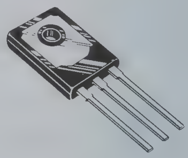


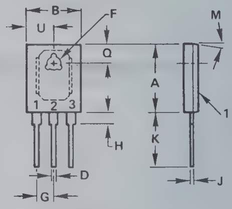
TORQUE REQUIREMENTS

Insulated 0.68 N-m (8 IN. LBS.) MAX

High Voltage Insulated 0.90 N-m (6 IN. LBS.) MAX

*High voltage mounting requirements depend on use environment. User is encouraged to make his own evaluation.





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255

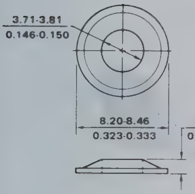
CASE 90
(TO-225AB)

6.0

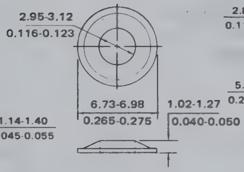
MOUNTING HARDWARE TO-225AB CASE 90

OUTLINE DIMENSIONS

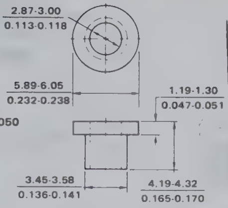
DIMENSIONS – $\frac{\text{MILLIMETER}}{\text{INCH}}$



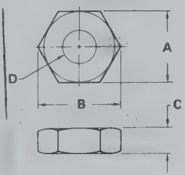
STEEL COMPRESSION WASHER
B52200F004



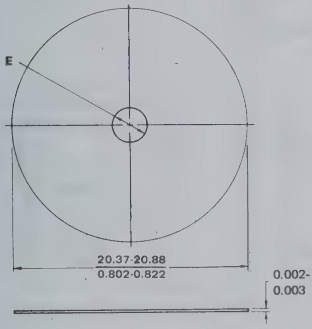
STEEL COMPRESSION WASHER
B52200F006



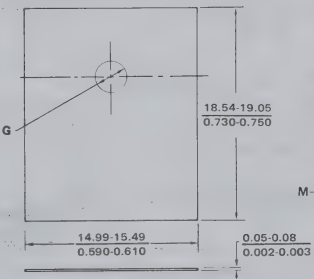
NYLON INSULATING BUSHING
B51547F011



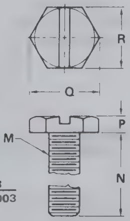
HEX NUT
CARBON STEEL
CADMIUM PLATED



ROUND MICA INSULATOR
(See table below.)



RECTANGULAR MICA INSULATOR
(See table below.)



HEX HEAD SCREW
CARBON STEEL,
CADMIUM PLATED

DIMENSIONS – MILLIMETER (INCH)

ROUND MICA INSULATOR

PART NO.	DIM E
B52600F013	3.56-3.81 (0.140-0.150)
B52600F015	2.87-2.97 (0.113-0.117)

RECTANGULAR MICA INSULATOR

PART NO.	DIM G
B05608A001	3.68-3.94 (0.145-0.155)
B05608A002	2.87-3.00 (0.113-0.118)

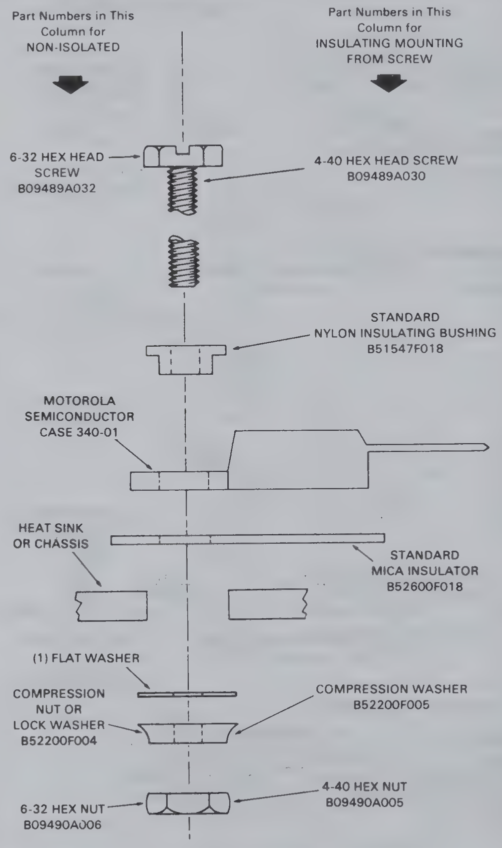
HEX NUT

TYPE	PART NO.	DIM A	DIM B	DIM C	DIM D
4-40	B09490A005	6.12-6.35 (0.241-0.250)	6.98-7.34 (0.275-0.289)	2.21-2.49 (0.087-0.098)	2.84 NOM (0.112 NOM)
6-32	B09490A006	7.67-7.92 (0.302-0.312)	8.74-9.17 (0.344-0.361)	2.59-2.90 (0.102-0.114)	3.50 NOM (0.138 NOM)

HEX HEAD SCREW

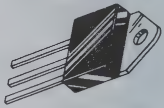
TYPE	PART NO.	DIM M	DIM N	DIM P	DIM Q	DIM R
4.40	B09489A030	2.84-40 (0.112-40)	11.94-12.70 (0.470-0.500)	1.24-1.52 (0.049-0.060)	5.13 MIN (0.202 MIN)	4.60-4.75 (0.181-0.187)
6.32	B09484A032	3.5-32 (0.138-32)	11.94-12.70 (0.470-0.500)	2.03-2.36 (0.080-0.093)	6.91 MIN (0.272 MIN)	6.20-6.35 (0.244-0.250)

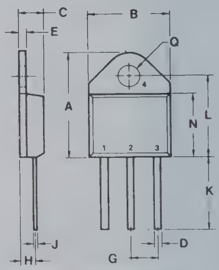
MOUNTING HARDWARE TO-218AC



TORQUE REQUIREMENTS
0 68 NM (6 in./lbs.) max.
Recommended Torque: 0.57 Nm/5 in./lbs. - 5.5 kg/cm.

(1) USE WITH LOCK WASHER





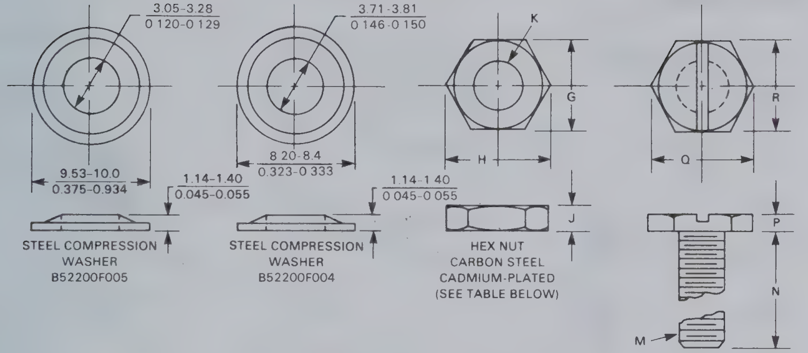
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

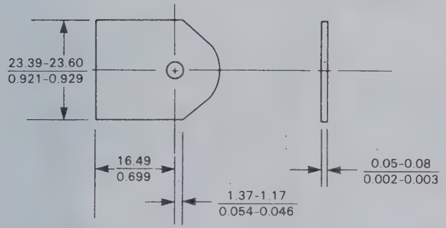
CASE 340-01
(TO-218AC)

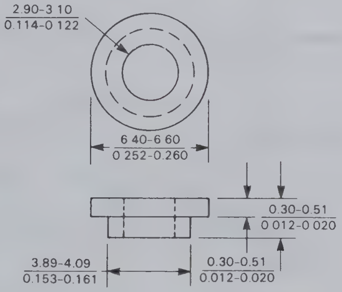
6.0

MOUNTING HARDWARE TO-218AC

(Dimensions - Millimeter/Inch)







MICA INSULATOR B52600F018	NYLON INSULATING BUSHING B51547F018

HEX NUT

TYPE	PART NO.	DIM G	DIM H	DIM J	DIM E
4-40	B09490A005	6.12-6.35 (0.241-0.250)	6.98-7.34 (0.275-0.289)	2.21-2.49 (0.087-0.098)	2.84 NOM (0.112) NOM
6-32	B09490A006	7.67-7.92 (0.302-0.312)	8.74-9.17 (0.344-0.361)	2.59-2.91 (0.102-0.114)	3.50 NOM (0.138) NOM

HEX HEAD SCREW

TYPE	PART NO.	DIM M	DIM N	DIM P	DIM Q	DIM R
4-40	B09489A030	2.84-40 (0.112-40)	11.94-12.70 (0.470-0.500)	1.24-1.52 (0.049-0.060)	5.13 MIN (0.202 MIN)	4.60-4.75 (0.181-0.187)
6-32	B09489A032	3.5-32 (0.138-32)	11.94-12.70 (0.470-0.500)	2.03-2.36 (0.080-0.093)	6.91 MIN (0.272 MIN)	6.20-6.35 (0.244-0.250)

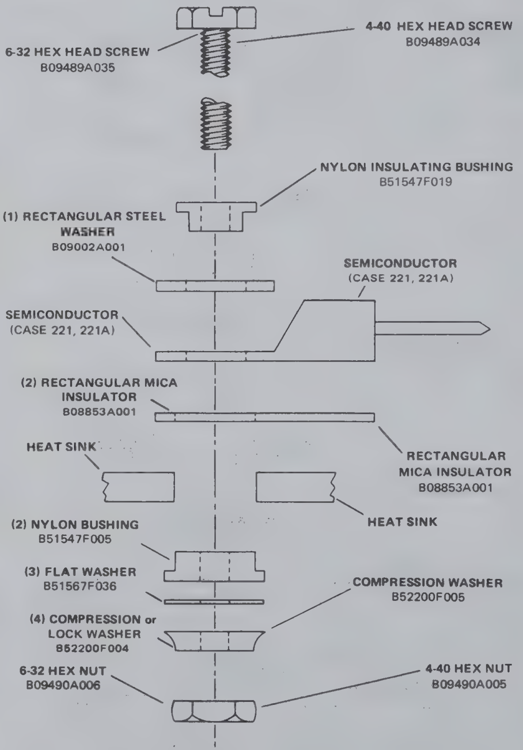
MOUNTING HARDWARE TO-220AB

PREFERRED ARRANGEMENT
for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential.
6-32 Hardware is Used.

Choose from Parts Listed Below.

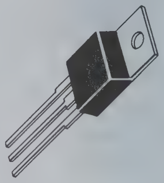
ALTERNATE ARRANGEMENT
for Isolated Mounting when Screw must be at Heat-Sink Potential.
4-40 Hardware is Used.

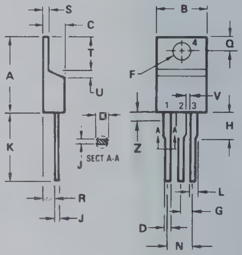
Use Parts Listed Below.



(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing and lock washer are used.
(4) Compression washer preferred when plastic insulating material is used.

TORQUE REQUIREMENTS
Insulated 0.68 N-M (6 in-lbs) max
Noninsulated 0.9 N-M (8 in-lbs) max





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	–	0.045	–
Z	–	2.03	–	0.080

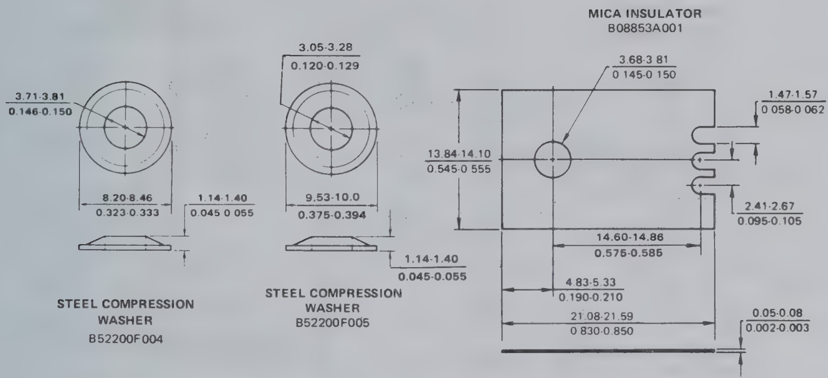
CASE 221A-02
TO-220AB

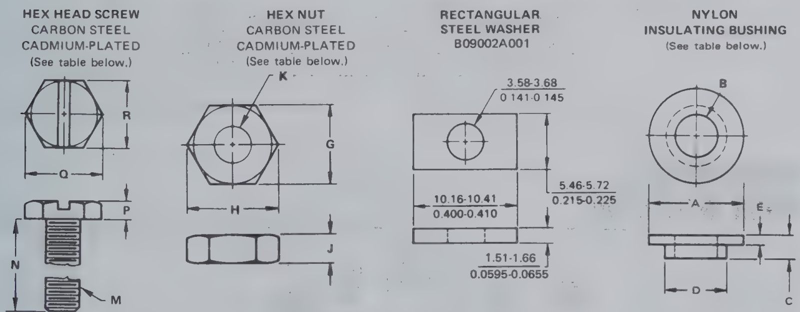
All JEDEC dimensions and notes apply

6.0

MOUNTING HARDWARE TO-220AB

(DIMENSION — MILLIMETER / INCH)





DIMENSIONS — MILLIMETER (INCH)

NYLON BUSHING

PART NO.	DIM A	DIM B	DIM C	DIM D	DIM E
B51547F005	9.40-9.65 (0.370-0.380)	3.84-4.09 (0.151-0.161)	2.16-2.41 (0.085-0.095	6.10-6.35 (0.240-0.250)	1.02-1.27 (0.040-0.050)
B51547F019	5.59-6.10 (0.220-0.240)	3.05-3.15 (0.120-0.124)	1.73-1.91 (0.068-0.075)	3.61-3.68 (0.142-0.145)	0.51-0.64 (0.020.0.025)

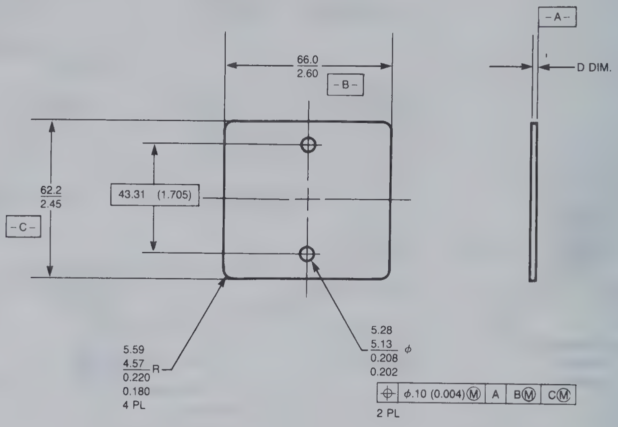
HEX NUT

TYPE	PART NO.	DIM G	DIM H	DIM J	DIM K
4-40	B09490A005	6.12-6.35 (0.241-0.250)	6.98-7.34 (0.275-0.289)	2.21-2.49 (0.087-0.098)	2.84 NOM (0.112 NOM)
6-32	B09490A006	7.67-7.92 (0.302-0.312)	8.74-9.17 (0.344-0.361)	2.59-2.90 (0.102-0.114)	3.50 NOM (0.138 NOM)

HEX HEAD SCREW

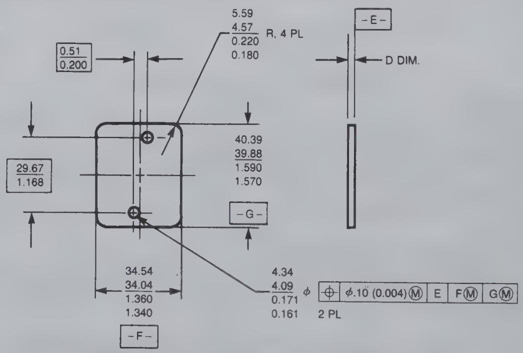
TYPE	PART NO.	DIM M	DIM N	DIM P	DIM Q	DIM R
4-40	B09489A034	0.112-40	1.57 (0.62)	1.24-1.52 (0.049-0.060)	5.13 MIN (0.202 MIN)	4.60-4.75 (0.181-0.187)
6-32	B09489A035	0.138-32	1.57 (0.62)	2.03-2.36 (0.080-0.093)	6.91 MIN (0.272 MIN)	6.20-6.35 (0.244-0.250)

MOUNTING HARDWARE
CASE 346-01 (MO-040AA)
MICA INSULATOR



MOTOROLA PART NO.	"D" DIMENSION
14CSB12387B002	0.10 – 0.15 mm (0.004 – 0.006 in.)
14CSB12387B001	0.05 – 0.10 mm (0.002 – 0.004 in.)

CASE 353-01
MICA INSULATOR



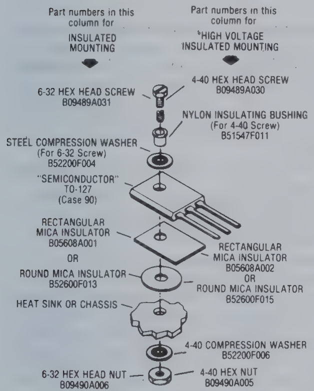
MOTOROLA PART NO.	"D" DIMENSION
14CSB12387B004	0.13 – 0.18 mm (0.005 – 0.007 in.)
14CSB12387B003	0.05 – 0.10 mm (0.002 – 0.004 in.)

6.0

THYRISTOR MOUNTING HARDWARE

Information on recommended mounting techniques and hardware is available in data sheets listed for each package type, including part numbers for hardware items which may be purchased from Motorola.

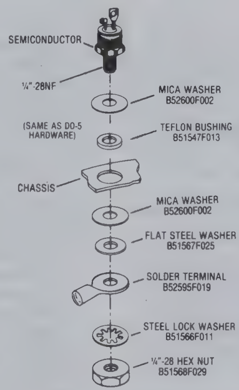
CASE 90
TO-225AB
(Formerly TO-127)



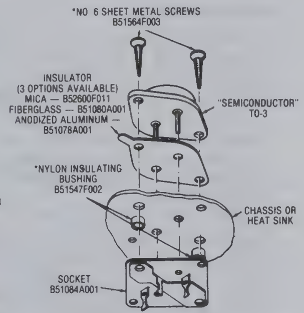
TORQUE REQUIREMENTS
Insulated 0.68 N-m (6 IN. LBS.) MAX
High Voltage Insulated 0.90 N-m (8 IN. LBS.) MAX

*High voltage mounting requirements depend on use environment. User is encouraged to make his own evaluation.

CASE 263

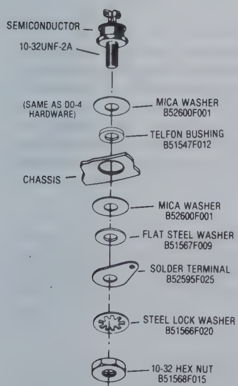


CASE 54
TO-204 Type
(Formerly TO-3)



*Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

CASE 86



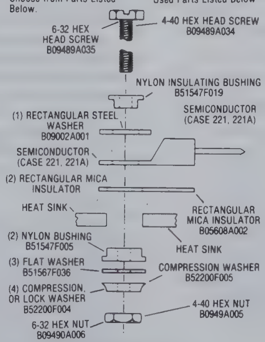
CASE 221-02
TO-220AB

1) Preferred Arrangement for Isolated or Nonisolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used.

Choose from Parts Listed Below.

b) Alternate Arrangement for Isolated Mounting when Screw must be at Heat-Sink Potential. 4-40 Hardware is Used.

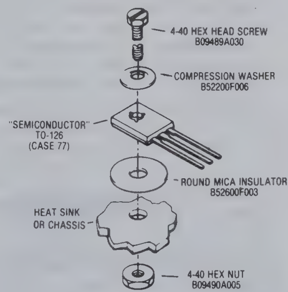
Used Parts Listed Below



TORQUE REQUIREMENTS
Insulated 0.68 N-m (6 IN. LBS.) MAX
Noninsulated 0.9 N-m (8 IN. LBS.) MAX

(1) Used with thin chassis and/or large hole
(2) Used when isolation is required
(3) Required when nylon bushing and lock washer are used.
(4) Compression washer preferred when plastic insulating material is used.

CASE 77
TO-225AA
(Formerly TO-126)



TORQUE REQUIREMENTS
0.68 N-m (6 IN. LBS.) MAX

6.0

MOUNTING TECHNIQUES FOR POWER SEMICONDUCTORS

INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, semiconductor-industry field history indicates that the failure rate of most silicon semiconductors decreases approximately by one half for a decrease in junction temperature from 160°C to 135°C.*

Many failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from mounting securely to a warped surface. With the widespread use of various plastic-packaged semiconductors, the dimension of mechanical damage becomes very significant.

Figure 1 shows an example of doing nearly everything wrong. In this instance, the device to be victimized is in the TO-220 package. The leads are bent to fit into a socket—an operation which, if not properly done, can crack the package, break the bonding wires, or crack the die. The package is fastened with a sheet-metal screw through a 1/4"-hole containing a fiber-insulating sleeve. The force used to tighten the screw pulls the package into the hole, causing enough distortion to crack the die. Even if the die were not cracked, the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heat sink surface and some burrs around the hole are present, many—but unfortunately not all—poor mounting practices are covered.

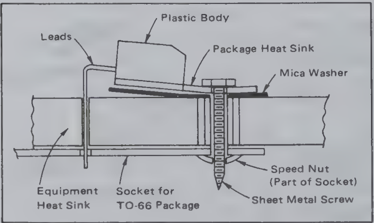


FIGURE 1 — Extreme Case of Improperly Mounting A Semiconductor (Distortion Exaggerated)

*See MIL–Handbook–217B, Section 2.2

In many situations the case of the semiconductor must be isolated electrically from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are being handled. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures necessitate attention to the following areas:

1. Mounting surface preparation,
2. Application of thermal compounds,
3. Installation of the insulator,
4. Fastening of the assembly, and
5. Lead bending and soldering.

In this note, the procedures are discussed in general terms. Specific details for each class of packages are given in the figures and in Table 1. Appendix A contains a brief review of thermal resistance concepts, and Appendix B lists sources of supply for accessories. Motorola supplies hardware for all power packages. It is detailed on separate data sheets for each package type.

MOUNTING SURFACE PREPARATION

In general, the heat-sink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heat-sink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e., Δh/TIR, is satisfactory in most cases if less than 4 mils per inch, which is normal for extruded aluminum—although disc type devices usually require 1 mil per inch.

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory;* a finer finish is costly to achieve and does not significantly lower contact resistance. Most commercially available cast or extruded

*Tests run by Thermalloy (Catalog #74-INS-3, page 14) using a copper TO-204 type package with a typical 32-microinch finish, showed that finishes between 16 and 64 μ-in caused less than ± 2.5% difference in interface thermal resistance.

6.0

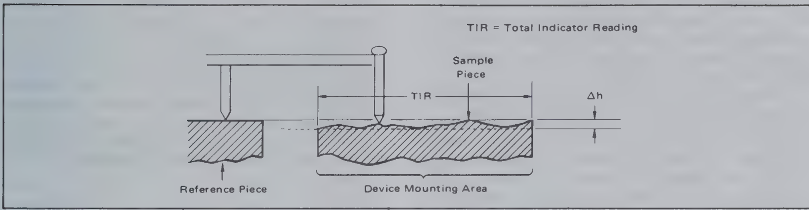


FIGURE 2 – Surface Flatness

heat sinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger packages having mounting holes removed from the semiconductor die location, such as a TO-204 type, may successfully be used with larger holes to accommodate an insulating bushing, but Thermopad plastic packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heat sink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heat-sink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heat sink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heat sinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heat sinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. The edges should be broken to remove burrs which cause poor contact between device and heat sink and may puncture isolation material.

Many aluminum heat sinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heat sinks. For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heat sink, anodized or painted surfaces may be more effective than other insulating materials which tend to creep (i.e., they flow), thereby reducing contact pressure.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Unless used immediately after machining, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse. Thermal grease should be immediately applied thereafter and the semiconductor attached as the grease readily collects dust and metal particles.

THERMAL COMPOUNDS

To improve contacts, thermal joint compounds or greases are used to fill air voids between all mating surfaces. Values of thermal resistivity vary from 0.10 degrees Celsius-inches per watt for copper film to 1200°C-in/W for air, whereas satisfactory joint compounds will have a resistivity of approximately 60°C-in/W. Therefore, the voids, scratches, and imperfections which are filled with a joint compound, will have a thermal resistance of about 1/20th of the original value which makes a significant reduction in the overall interface thermal resistance.

Joint compounds are a formulation of fine zinc particles in a silicon oil which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Experience will indicate whether the quantity is sufficient, as excess will appear around the edges of the contact area. To prevent accumulation of airborne particulate matter, excess

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compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the assembly.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table I. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator and is therefore highly desirable despite the handling problems created by its affinity for foreign matter. Some sources of supply for joint compounds are shown in Appendix B.

Some users and heat-sink manufacturers prefer not to use compounds. This necessitates use of a heat sink with lower thermal resistance which imposes additional cost, but which may be inconsequential when low power is being handled. Others design on the basis of not using grease, but apply it as an added safety factor, so that if improperly applied, operating temperatures will not exceed the design values.

TABLE 1
Approximate Values for Interface Thermal Resistance and Other Package Data
(See Table II for Case Number to JEDEC Outline Cross-Reference)

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heat sink. (See Note 4.)

Package Type and Data					Interface Thermal Resistance ($^{o}C/W$)					
JEDEC Outline	Description	Recommended Mounting Hole and Drill Size	Machine Screw Size[2]	Torque In-Lb	Metal-to-Metal Dry	Metal-to-Metal Lubed	With Insulator Dry	With Insulator Lubed	With Insulator Type	See Note
Case 152*	Uniwatt	0.113, #33	4-40	6	5.0	3.8	7.4	5.4	2 mil Mica	3
DO-4	10-32 Stud 7/16″ Hex	0.188, #12	10-32	20	0.3	0.2	1.6	0.8	3 mil Mica	
DO-5	1/4-28 Stud 11/16″ Hex	0.250, #1	1/4-28	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO-21	Pressfit, 1/2″	See Figure 8	—	—	0.15	0.10	—	—	—	
TO-3	Diamond Flange	0.140, #28	6-32	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO-66	Diamond Flange	0.140, #28	6-32	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO-83 TO-94	1/2″ 20 Stud 1-1/16″ Hex	0.5, 0.5 —	1/2-20	130	—	0.1	—	—	—	
TO-126	Thermopad 1/4″ x 3/8″	0.113, #33	4-40	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO-127	Thermopad 1/2″ x 5/8″	0.140, #28	6-32	8	1.6	0.8	2.6	1.8	2 mil Mica	
TO-202AC	Duowatt	0.140, #28	6-32	8	1.3	0.9	4.8	2.0	2 mil Mica	3
TO-220AB	Thermowatt	0.140, #28	6-32	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

*Motorola Case Number

NOTE 1. See Figures 3 and 4 for additional data on TO-204 type and TO-220 packages.

NOTE 2. Screw not insulated.

NOTE 3. Case thermocouple soldered to top of tab.

NOTE 4. **Measurement of Interface Thermal Resistance.** Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semi, a thermocouple on the heat sink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are in poor agreement.

Consider the TO-220 package shown in the accompanying figure. The mounting pressure at one end causes the other end—where the die is located—to lift off the mounting surface slightly. To improve contact, Motorola TO-220 packages are slightly concave and use of a spreader bar under the screw lessens the lifting, but some is inevitable with a single-ended package.

The thermocouple locations are shown:

a. The Motorola location is directly under the die reached through a hole in the heat sink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b. The EIA location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the EIA location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction-to-sink thermal resistance is constant for a given setup, junction-to-case values decrease and case-to-sink values increase as the case thermocouple readings become warmer.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semi package and the heat sink, tightening the screw will not bow the package;

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Table 1, Note 5 (continued)

instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heat sink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location could be close to the temperature at the EIA location as the lateral heat flow is generally small.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the semi is making contact to the heat sink, since heat sinks are measured from the point of semi contact to the ambient. Once the special heat sink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO-220 package mounted to a heat sink without thermal grease and no insulator. This error is small when compared to the heat dissipators often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant, and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heat sink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ-inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use and yields reproducible results. At this printing, however, sufficient data to compare results to other methods is not available.

The only way to get accurate measurements of the interface resistance is to also test for junction-to-case thermal resistance at the same time. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

JEDEC TO-220 Package mounted to heat sink showing various thermocouple locations and lifting caused by pressure at one end.

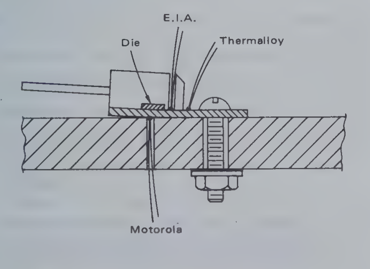

TABLE 2

Cross Reference Chart

Motorola Case Number to JEDEC Outline Number and Table 1 Reference

Motorola Number	Former JEDEC Number	JEDEC Number	Reference in Table 1
1	TO-3	TO-204AA	TO-3
3	TO-3[1]	–	TO-3
9	TO-61	TO-210AC	DO-5
11	TO-3	TO-204AA	TO-3
11A	TO-3[1]	–	TO-3
12	TO-3[1]	–	TO-3
36	TO-60	TO-210AB	DO-4
42A	DO-5	DO-203AB	DO-5
44	DO-4	DO-203AA	DO-4
54	TO-3[1]	–	TO-3
56	DO-4	DO-203AA	DO-4
58	DO-5	DO-203AB	DO-5
77	TO-126	TO-225AA	TO-126
80	TO-66	TO-213AA	TO-66
86	TO-208[1]	–	DO-4
86L	TO-298[1]	–	DO-4
90	TO-127	TO-225AB	TO-127
145C	TO-232[1]	–	DO-4
152	TO-202[1]	–	Case 152
160-03	TO-59	TO-210AA	DO-4
167	DO-203	–	DO-4
157	DO-203[1]	–	DO-5
197	TO-3	TO-204AE	TO-3
219	TO-94	TO-209AC	TO-83
221,A	TO-220AB	TO-220AB	TO-220AB
235	TO-208[1]	–	DO-5
238	TO-208[1]	–	DO-5
245	DO-4	DO-203AA	DO-4
246	TO-83	TO-208AD	TO-83
257-01	DO-5	DO-204AB	DO-5
263	TO-208[1]	–	DO-5
283	DO-4	DO-203AA	DO-4
285	TO-209[1]	–	TO-83
288	TO-208[1]	–	TO-83
289	TO-209[1]	–	DO-5
291	TO-94	TO-209AC	TO-83
306	TO-202AC	TO-202AC	TO-202AC

NOTE 1. Would fit within this family outline if registered with JEDEC.

INSULATION CONSIDERATIONS

Since it is most expedient to manufacture power semiconductors with collectors or anodes electrically common to the case, the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, it is best to isolate the entire heat sink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heat sink. Where heat sink isolation is not possible, because of safety reasons or in instances where a chassis serves as a heat sink or where a heat sink is common to several devices, insulators are used to isolate the individual components from the heat sink.

When an insulator is used, thermal grease assumes greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a markedly uneven surface. Reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torque applied to TO-204 type and TO-220 packages, are shown in Figure 3 for bare surfaces and Figure 4 for greased surfaces. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case). When high power is handled, beryllium oxide is unquestionably the best choice. Thermafilm is Thermalloy's tradename for a polyimide material which is also commonly known as Kapton*; this material is fairly popular for low power applications because it is low cost, withstands high temperatures and is easily handled, in contrast to mica which chips and flakes easily.

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly so that having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the breakdown voltage of the insulation system. Because of these factors, which are not amenable to analysis, hi-pot testing should be done on prototypes and a large margin of safety employed. In some situations, it may be necessary to substitute "empty" packages for the semiconductors to avoid shorting them or to prevent the semiconductors from limiting the voltage applied during the hi-pot test.

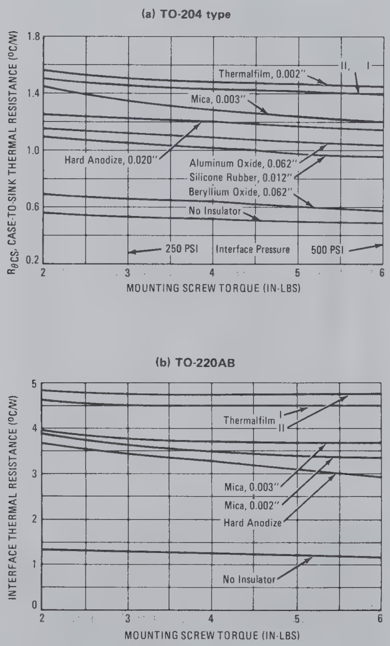

FIGURE 3 — Interface Thermal Resistance Without Thermal Grease as a Function of Mounting Screw Torque Using Various Insulating Materials

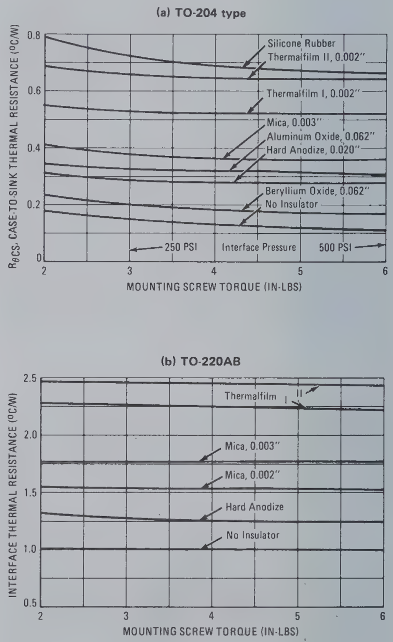

FIGURE 4 — Interface Thermal Resistance Using Thermal Grease as a Function of Mounting Screw Torque Using Various Insulating Materials

*® DuPont

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Washers

A very useful piece of hardware is the bell-type compression washer. As shown in Figure 5, it has the ability to maintain a fairly constant pressure over a wide range of physical deflection—generally 20% to 80%—thereby maintaining an optimum force on the package. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package or insulating washer caused by temperature changes. Bell type washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme.

Motorola washers designed for use with the Thermopad package maintain the proper force when properly secured. They are used with the large face contacting the packages.

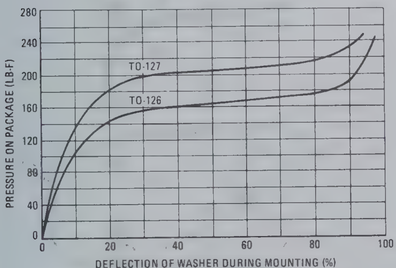

FIGURE 5 — Characteristics of the Bell Compression Washers Designed for Use with Thermopad Semiconductors

Machine Screws

Machine screws and nuts form a trouble-free fastener system for all types of packages which have mounting holes. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of any of the Thermopad plastic package types as the screw heads are not sufficiently flat to provide properly distributed force.

Self-Tapping Screws

Under some conditions, sheet-metal screws are acceptable. However, during the tapping process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; a very unsatisfactory surface results. When used, a speed-nut must be used to secure a standard screw, or the type of screw must be used which roll-forms machine screw threads.

Eyelets

Successful mounting can also be accomplished with hollow eyelets provided an adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Rivets

When a metal flange-mount package is being mounted directly to a heat sink, rivets can be used. Rivets are not a recommended fastener for any of the plastic packages except for the tab-mount type. Aluminum rivets are preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

Insulators and Plastic Hardware

Because of its relatively low cost and low thermal resistance, mica is still widely used to insulate semiconductor packages from heat sinks despite its tendency to chip and flake. It has a further advantage in that it does not creep or flow so that the mounting pressure will not reduce with time in use. Plastic materials, particularly Teflon*, will flow. When plastic materials form parts of the fastening system, a compression washer is a valuable addition which assures that the assembly will not loosen with time.

FASTENING TECHNIQUES

Each of the various types of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heat sinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Manufacturers which provide heat sinks for general use and other associated hardware are listed in Appendix B. Manufacturer's catalogs should be consulted to obtain more detailed information. Motorola also has mounting hardware available for a number of different packages. Consult the Hardware Data Sheet for dimensions of the components and part numbers.

Specific fastening techniques are discussed in the remainder of this note for the following categories of semiconductor package.

1. Stud mount: DO-4, DO-5, DO-9, DO-30, TO-59, TO-60/63, TO-83, TO-93/94, etc.
2. Flange mount: DO-43, DO-44, TO-204 type, TO-37, TO-41, TO-53, TO-66, etc.
3. Pressfit: DO-21, DO-24, TO-203
4. Disc: DO-200 and TO-200 Families
5. Thermopad®: TO-126/7
6. Thermowatt®: TO-220 Family
7. Tab Mount (Duowatt® and Uniwatt®): TO-202 Family
8. RF Stripline: TO-119/121, TO-128/9, TO-216

*Trademark E. I. DuPont

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Stud Mount

Mounting errors with stud-mounted parts are generally confined to application of excessive torque or tapping the stud into a threaded heat-sink hole. Both these practices may cause a warpage of the hex base which may crack the semiconductor die. The best fastening method is to use a nut and washer; the details are shown in Figure 6.

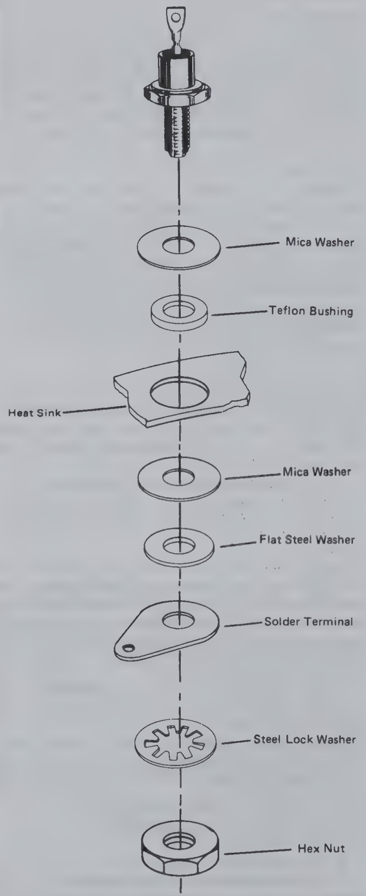

FIGURE 6 – Mounting Details For Stud-Mounted Semiconductors

Flange Mount

Few known mounting difficulties exist with this type of package. The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. A typical mounting installation is shown in Figure 7. Machine screws, self-tapping screws, eyelets, or rivets may be used to secure the package.

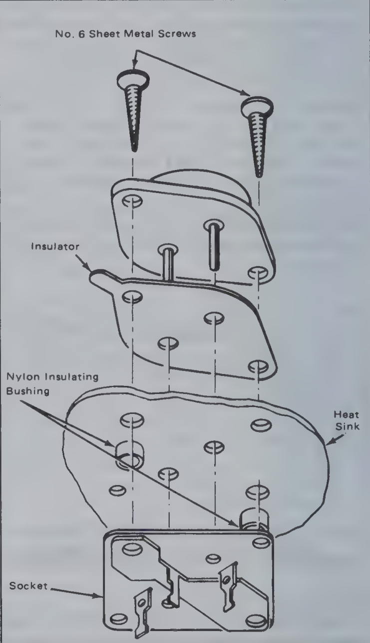

FIGURE 7 – Mounting Details for Flat-Base Mounted Semiconductors (TO-3 Shown).

When not using a socket, machine screws tightened to their torque limits will produce lowest thermal resistance.

Press Fit

For most applications, the press-fit case should be mounted according to the instructions shown in Figure 8. A special fixture meeting the necessary requirements is a must.

Disc

Disc type devices also require special handling. The details are shown in Figure 9.

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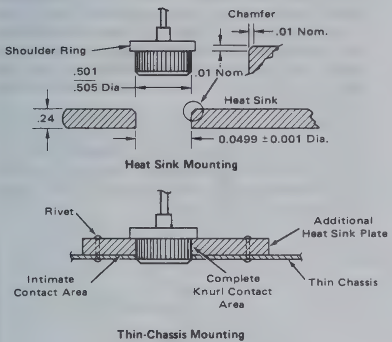
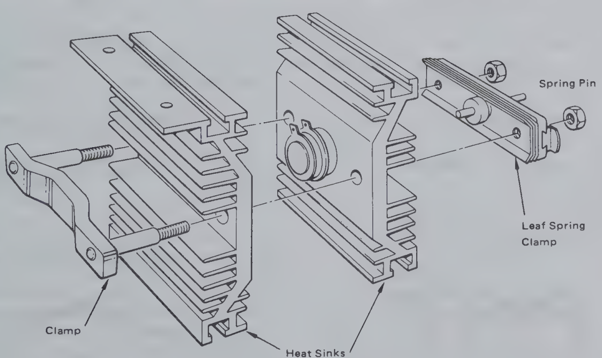


The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the case during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heat-sink material. Recommended hardnesses are: copper—less than 50 on the Rockwell F scale; aluminum—less than 65 on the Brinell scale. A heat sink as thin as 1/8" may be used, but the interface thermal resistance will increase in direct proportion to the contact area. A thin chassis requires the addition of a backup plate.

FIGURE 8 — Mounting Details for Press-Fit Semiconductors



A self-leveling type mounting clamp is recommended to assure parallelism and even distribution of pressure on each contact area. A swivel type clamp or a narrow leaf spring in contact with the heat dissipator provides acceptable performance.

The clamping force should be applied smoothly, evenly, and perpendicularly to the semiconductor package to prevent deformation of the device or the heat-dissipator mounting surfaces during installation. The spring used should provide a mounting force within the range recommended by the semiconductor manufacturer; clamping forces usually range from 800 to 2000 pounds force depending upon the type number.

Installation of an assembly of disc-type semiconductors mounted between two heat dissipators should be done in a manner to permit one heat dissipator to move with respect to the other. Movement will avoid stresses being developed due to thermal expansion, which could damage the semiconductor.

Similarly, when two or more devices are to be operated electrically in parallel, one of the heat dissipators used may be common to all devices. Individual heat dissipators must be provided against the other mounting surfaces of the semiconductors so that the mounting force applied in each case will be independently adjustable.

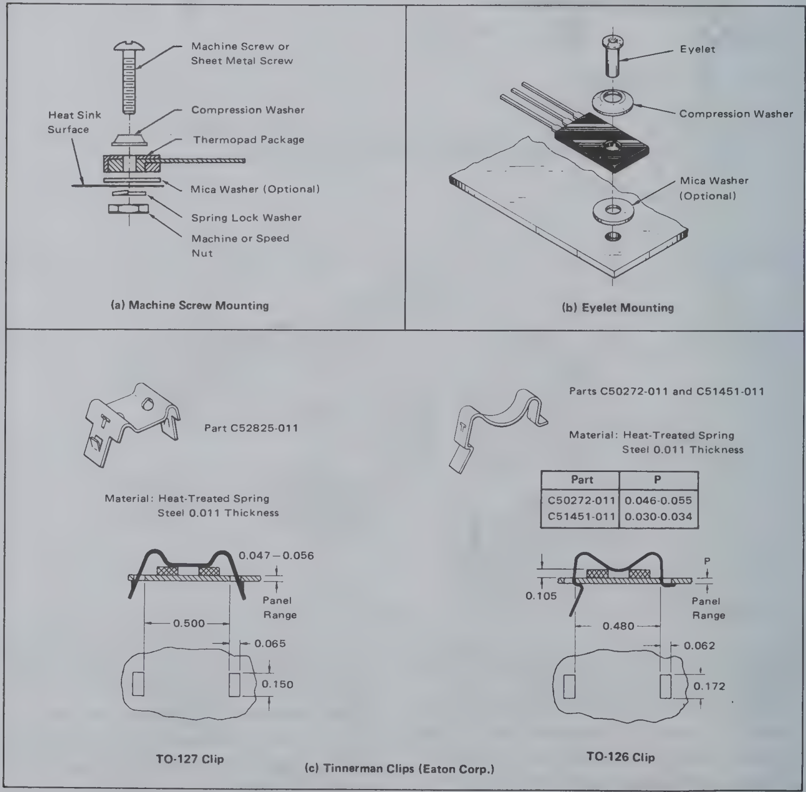
FIGURE 9 — Mounting Details for Disc-Type Semiconductors

Thermopad

The Motorola Thermopad® plastic power packages have been designed to feature minimum size with no compromise in thermal resistance. This is accomplished by die-bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting, i.e., plastic is molded enveloping the chip but leaving the mounting hole open. The benefits of this construction are obtained at the expense of a requirement that strict attention be paid to the mounting procedure. Success in mounting Thermopad devices depends largely upon using a compression washer which provides a controllable pressure across a large bearing surface. Having a small hole with no chamfer and a flat, burr-free, well-finished heat sink are also important requirements.

Several types of fasteners may be used to secure the Thermopad package; machine screws, eyelets, or clips are preferred. With screws or eyelets, a bell compression washer should be used which applies the proper force to the package over a fairly wide range of deflection. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of the recommended washers are shown in Figure 5.

Figure 10 shows details of mounting TO-126 or TO-127 devices. Use of the clip requires that caution be exercised to insure that adequate mounting force is applied. When electrical isolation is required, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.



Part	P
C50272-011	0.046-0.055
C51451-011	0.030-0.034

FIGURE 10 — Recommended Mounting Arrangements for TO-126 and TO-127 Thermopad Packages

The case 199 Thermopad is not more tolerant of mounting conditions than Case 77 or 90 parts even though the fastener does not bear on the plastic. The screw must not contact the semiconductor base plate as screw heads are not flat enough to apply pressure evenly and may cause warpage of the base plate resulting in die fracture. Procedures for mounting the Case 199 are shown in Figure 11.

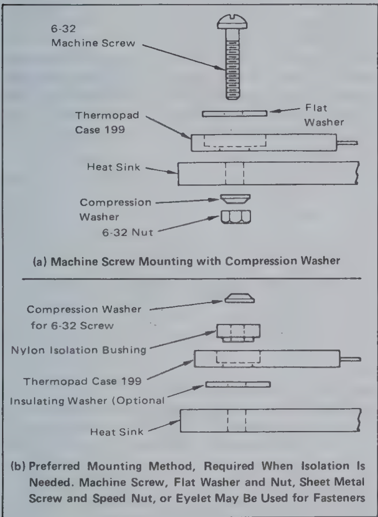


FIGURE 11 — Various Mounting Schemes For the Case 199 Thermopad

(a) shows direct contact with heat sink.
(b) shows technique when isolation is required.

Manual Assembly Should Be Used.

Thermowatt®

The popular TO-220 Thermowatt® package also requires attention to mounting details. Figure 12 shows suggested mounting arrangements and hardware. The rectangular washer shown in Figure 12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is suggested when using a 6-32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

In situations where the Thermowatt package is making direct contact with the heat sink, an eyelet may be used, provided sharp blows or impact shock is avoided.

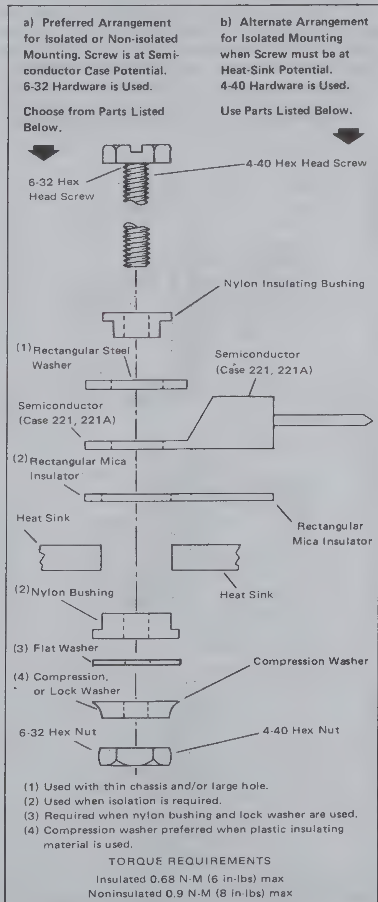


FIGURE 12 — Mounting Arrangements for Thermowatt Packages

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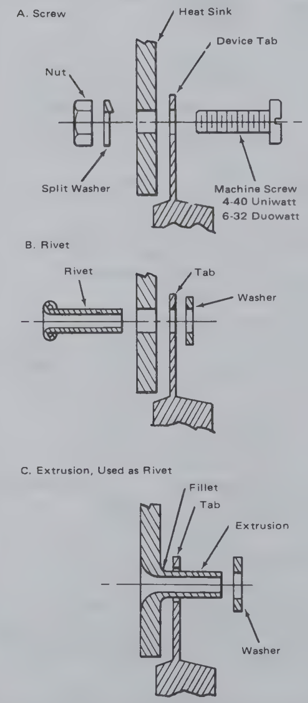
Tab Mount

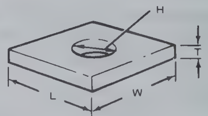
Although the Duowatt® and Uniwatt® packages are designed primarily for use in low-power applications where heat sinks are not required, they can be used to dissipate up to 10 watts if properly mounted to a heat sink. These packages are relatively rugged, since the mounting hole is not close to the die; mounting stresses, therefore, are not easily transmitted to the die.

Figure 13 shows some possible mounting arrangements. An axial load of 300 lbs-force produces minimum contact thermal resistance. This is achieved at 6 in-lbs when a 4-40 machine screw is used. A sheet-metal screw and speed-nut can be substituted for the machine screw and nut, but torque readings are uncertain. The riveting technique should produce 300 lbs-force, using a gradually increasing pressure such as provided by an arbor press.

The extrusion requires a punch press to manufacture; however, it is potentially the least expensive technique. Note that the radius of the fillet must be small enough to allow the tab to lie flat on the heat sink. To utilize an existing chassis and board arrangement on heat sinking, it may be necessary to have the device lie flat on the chassis. In this case, the chassis mounting blocks shown in Figure 13d might be utilized. A possible application is shown in Figure 13e, where a complementary transistor pair is used. Insulated screws and mica insulating washers under the blocks must be used to prevent shorting of the collector circuits of the two transistors. Alternately, an insulated bushing and a #3 screw could be used to secure the packages.

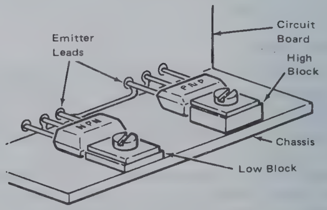
To avoid the use of mounting blocks, a tab-forming option is available. Alternately, some equipment manufacturers have constructed heat sinks with a flat, raised island to permit the package to be flat. Users should not attempt to bend the tab as a cracked die is the probable result.





D. Chassis Mounting Block Details

	Block Dimensions				
	H	W	L	T	
				Low Block	High Block
Duowatt	0.140	0.4	0.5	0.07	0.12
Uniwatt	0.113	0.3	0.3	0.06	0.12



E. Chassis Mount Block, Mounting Details

Use Nylon Screws and Mica Insulating Washer to Prevent Shorting the Tabs to the Chassis, and Thus to Each Other.

FIGURE 13 – Methods of Mounting Duowatt and Uniwatt Transistors to a Heat Sink

R.F. Stripline

Besides the usual precautions regarding surface flatness and torque, the stripline package (see Figure 14a) requires attention to the following:

1. The device should never be mounted in such a manner as to place ceramic-to-metal joints in tension.
2. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.
3. When the device is mounted in a printed circuit board with the copper stud or flange and BeO portion of the header passing through a hole in the circuit board, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.
4. Some clearance must be allowed between the leads and the circuit board when the device is properly secured to the heat sink.
5. The device should be properly secured into the heat sinks before the device leads are attached into the circuit.
6. The leads must not be used to prevent device rotation on stud type devices during stud torque application. A wrench flat is provided for this purpose.

Most of the considerations listed above are designed to prevent tension at the metal-ceramic interfaces on the SOE package. Improper mechanical design can lead to application of stresses to these joints resulting in device destruction. Three joints are considered: the cap to the BeO disc, the leads to the disc, and the stud or flange to the disc.

The joint between the ceramic cap and the BeO ceramic disc is composed of a material which loses strength above 175°C. While the strength of the material returns upon cooling, any force applied to the cap at high temperature may result in failure of the cap to ceramic joint.

Figure 14b shows a cross-section of a printed circuit board and heat-sink assembly for mounting a stud type stripline device. H is the distance from the top surface of the printed circuit board to the D-flat heat-sink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the package, there is no possibility of tensile forces in the copper stud – BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurances are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead-soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heat-sink surface will occur as the differences between H and the package dimension becomes larger, this may result in device failure as power is applied.

Figure 14c shows a typical mounting technique for flange-type stripline transistors. Again, H is defined as the distance from the top of the printed circuit board to the heat-sink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur. Because of the ability of the copper flange to bend under the types of loads encountered when the mounting screws are tightened, permanent deformation of the flange may result. Corrective action after the flange has been bent will not necessarily insure proper thermal contact with the heat sink.

The flange surface as supplied with Motorola transistors is either flat or slightly convex. It is important that the mating heat-sink surface also be flat or slightly convex to provide the best contact when the device is properly secured.

Since the flange may be permanently deformed during mounting, the device should not be dismounted and remounted in another position, without checking the flatness. The flange may be resurfaced using emery cloth mounted on a large, flat block. While this removes the gold- or nickel-plating, the thin layer of copper oxide which rapidly forms causes an insignificant increase in thermal resistance, although corrosion may occur.

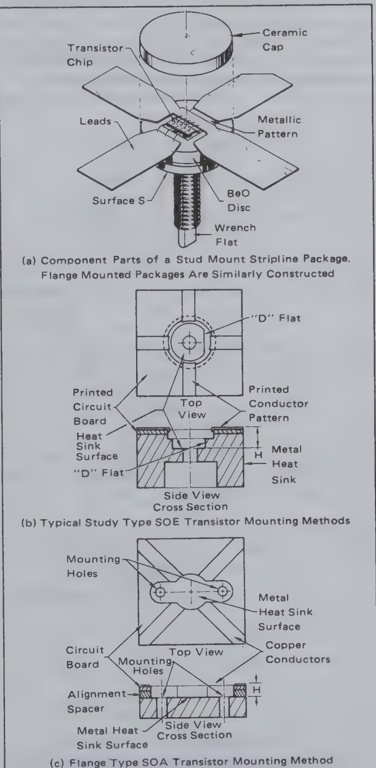


FIGURE 14 — Mounting Details for SOE Transistors

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FREE AIR AND SOCKET MOUNTING

In applications where average power dissipation is of the order of a watt or so, power semiconductors may be mounted with little or no heat-sinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked glass-to-metal seals around the leads. The plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heat sink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance.

In many situations, because its leads are fairly heavy, the TO-127 package has supported a small heat sink; however, no definitive data is available. When using a small heat sink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 15. The arrangement of part (a) could be used with any plastic package, but the scheme of part (b) is more practical with Case 77 or Case 90 Thermopad devices. With the other package types, mounting the transistor on top of the heat sink is more practical.

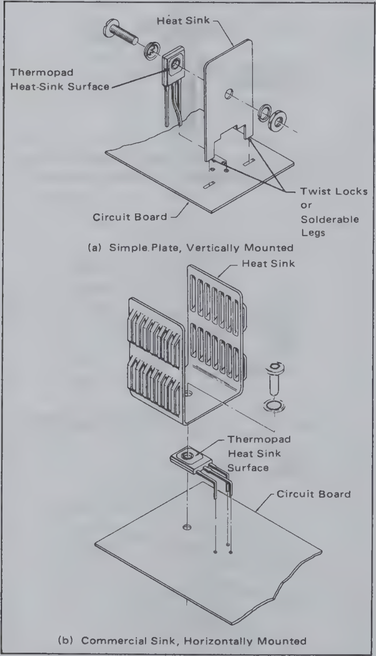

FIGURE 15 — Methods of Using Small Heat Sinks With Plastic Semiconductor Packages

In certain situations, in particular where semiconductor testing is required, sockets are desirable. Manufacturers have provided sockets for all the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details.

HANDLING PINS, LEADS, AND TABS

The pins and lugs of metal-packaged devices are not designed for any bending or stress. If abused, the glass-to-metal seals could crack. Wires may be attached using sockets, crimp connectors, or solder, provided the data-sheet ratings are observed.

The leads and tabs of the plastic packages are more flexible and can be reshaped, although this is not a recommended procedure for users to do. In some cases, a heat sink can be chosen which makes lead-bending unnecessary. Numerous lead- and tab-forming options are available from Motorola. Preformed leads remove the risk of device damage caused by bending from the users.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantitites of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A lead-bend radius greater than 1/16 inch is advisable for TO-126, 1/10 inch for TO-127 and Case 199, and 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. An acceptable lead-forming method that provides this relief is to incorporate an S-bend into the lead. Wire-wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices.

Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline may cause the encapsulant to swell, possibly damaging the

transistor die. Likewise, chlorinated Freon solvents are unsuitable, since they may cause the outer package to dissolve and swell.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if the packages are free-standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN-569.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area or thyristor di/dt limits, as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #32AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where T_J = junction temperature (^{o}C)
T_C = case temperature (^{o}C)
$R_{\theta JC}$ = thermal resistance junction-to-case as specified on the data sheet ($^{o}C/W$)
P_D = power dissipated in the device (W).

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

APPENDIX A

THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T \qquad (1)$$

where q = rate of heat transfer or power dissipation (P_D),
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \qquad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that ΔT could be thought of as a voltage; thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \qquad (3)$$

where T_J = junction temperature,
P_D = power dissipation,
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heat sink),
$R_{\theta SA}$ = heat sink thermal resistance (heat sink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

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The value for the interface thermal resistance, $R_{\theta CS}$, is affected by the mounting procedure and may be significant compared to the other thermal-resistance terms.

The thermal resistance of the heat sink is not constant; it decreases as ambient temperature increases and is affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. In some applications such as in RF power amplifiers and short-pulse applications, the concept may be invalid because of localized heating in the semiconductor chip.

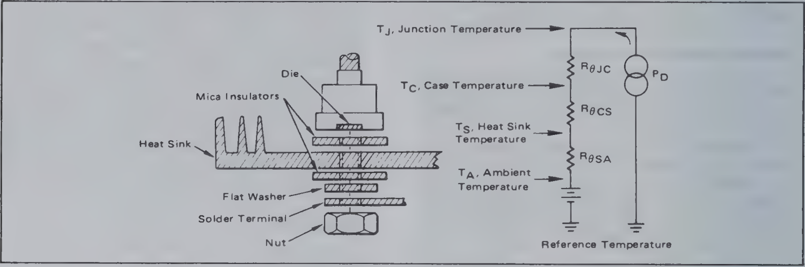

FIGURE A1 — Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

APPENDIX B
SOURCES OF ACCESSORIES

		Insulators						Heat Sinks					
Manufacturer	Joint Compound	BeO	AlO_2	Anodize	Mica	Plastic Film	Silicone Rubber	Stud	Flange	Disc	Thermowatt	Uni/Duo Watt	RF Stripline
Aavid Eng.	Ther-o-link 1000	–	–	–	–	–	–	X	X	–	X	–	–
AHAM	–	–	–	–	–	–	–	X	X	–	X	–	–
Astrodyne	#829	–	–	–	–	–	–	X	X	X	X	X	–
Delbert Blinn	–	X	–	X	X	X	X	X	X	–	–	–	–
IERC	Thermate	–	–	–	–	–	–	X	X	–	X	X	X
Staver	–	–	–	–	–	–	–	X	X	–	X	X	X
Thermalloy	Thermacote	X	X	X	–	X	–	X	X	X	X	X	X
Tor	TJC	X	–	X	X	X	–	X	X	–	X	–	–
Tran-tec	XL500	X	–	–	–	X	X	X	X	X	X	X	X
Wakefield Eng.	Type 120	X	–	X	–	–	–	X	X	X	X	X	–
Wei Corp.	–	–	–	–	–	–	–	X	X	–	–	–	–

Other sources for Joint Compounds: Dow Corning, Type 340
Emerson & Cuming, Eccoshield — SO (Electrically Conducting)
Emerson & Cuming, Eccotherm — TC-4 (Electrically Insulating)

APPENDIX B
SUPPLIERS ADDRESSES

Aavid Engineering, Inc., 30 Cook Court, Laconia, New Hampshire 03246 (603) 524-4443

AHAM Heat Sinks, 27901 Front Street, Rancho, California 92390 (714) 676-4151

Astrodyne, Inc., 353 Middlesex Avenue, Wilmington, Massachusetts 01887 (617) 272-3850

Delbert Blinn Company, P.O. Box 2007, Pomona, California 91766 (714) 623-1257

Dow Corning, Savage Road Building, Midland, Michigan 48640 (517) 636-8000

Eaton Corporation, Engineered Fasteners Division, Tinnerman Plant, P.O. Box 6688, Cleveland, Ohio 44101 (216) 523-5327

Emerson & Cuming, Inc., Dielectric Materials Division, 869 Washington Street, Canton, Massachusetts 02021 (617) 828-3300

International Electronics Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849-2481

The Staver Company, Inc., 41-51 North Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666-8000

Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243-4321

Tor Corporation, 14715 Arminta Street, Van Nuys, California 91402 (213) 786-6524

Tran-tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564-2748

Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245-5900

Wei Corporation, 1405 South Village Way, Santa Ana, California 92705 (614) 834-9333

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Application Notes
&
Supplemental Literature

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SUPPLEMENTAL LITERATURE

The following documents may provide additional information for your circuit designs. Copies may be obtained from Motorola Semiconductor Products Inc., Literature Distribution Center, P.O. Box 20924, Phoenix, AZ 85036.

POWER SUPPLY CIRCUIT DESIGN

AN-719 A New Approach to Switching Regulators

This article describes a 24-Volt, 3-Ampere switching mode supply. It operates at 20 kHz from a 120 Vac line with an overall efficiency of 70%. New techniques are used to shape the load line. The control portion uses a quad comparator and an opto coupler and features short circuit protection.

AN-725 A Low-Cost 80 V-1.5 A Color TV Power Supply

A full-wave SCR power supply is proposed for application in line operated color television receivers. Economy of design is maintained while providing good regulation against line, load and temperature changes.

AN-737A Switched Mode Power Supplies—Highlighting a 5-V, 40-A Inverter Design

This application note identifies the features of various regulator circuits that are in use today in AC to DC power supplies. The note also illustrates how these circuits may be used as complementary building blocks in a system design. Primary emphasis is on switched mode regulators beause they fill the present need for energy and space savings.

A complete 5-V, 40-A line operated inverter supply is described in detail including design procedures for the magnetic components. The inverter itself is a "state-of-the-art" design which features CMOS logic, high voltage power transistors, Schottky rectifiers and an opto-electronic coupler. It operates with a full load efficiency of 80% at a frequency of 20kHz.

AN-752 An 80-Watt Switching Regulator for CATV and Industrial Applications

This application note describes a 24-Volt, 3-Ampere switching, regulated power supply that operates above 18 kHz from a 40-to 60-Volt, 60-Hz square wave source (CATV power line from a ferroresonant transformer) or a dc standby source with input output isolation. The control circuit consists of a dual operational amplifier and a linear integrated circuit timer which are used to vary the on time of a new high-speed power transistor. The circuit provides good efficiency, good regulation, low output ripple and incorporates input and output voltage over shutdown protection.

AN-767 A Line Operated, Regulated 5V/50A Switching Power Supply

This application note describes a regulated 220V ac to 5 Vdc converter using high voltage switching transistors and Schottky barrier rectifiers. The control functions are all performed by integrated circuits.

AN-786 Power Darlington Load Line Considerations

Power Darlington load lines are discussed in the light of a typical application of a Switchmode Darlington power transistor. Darlington advantages are reviewed and the test circuit is introduced. Load line analysis revealed a reverse bias SOA problem and just enough snubbing was used to insure reliability without unduly sacrificing efficiency.

AN-803 The Effect of Emitter-Base Avalanching on High-Voltage Power Switching Transistors

Reverse biasing the base of a power transistor during turn-off decreases its turn-off switching losses. This application note investigates the effect of increasing the bias into avalanche on the life, switching speeds and inductive turn-off stresses on several types of high-voltage switching power transistors.

AN-828 The Effects of Base Drive Consditions on RBSOA

This application note describes the turn-off stresses placed on high voltage power transistors when used in clamped inductive load switching applications. The effects of off-boas voltage $V_{BE(off)}$, reverse base current I_{B2}, forward base current I_{B1} and temperature on the RBSOA capability and switching speeds are illustrated. Also described is the non-destruct RBSOA test circuit used in generating this data.

AN-845 New Power Bipolars compare favorably with FETs for Switching Efficiency

Power MOSFETs are recognized as being extremely fast switching devices, but are they more efficient than bipolars in all or many high voltage switching applications? The answer is — it depends. Efficiency is a measure of dissipation, which, in switchmode circuits, consists primarily of switching losses, both turn-off and turn-on, and saturation losses. Since switching losses are a function of the switching frequency and saturation losses are relatively constant, there reaches a point in the frequency spectrum

where one loss predominates over the other. Thus, in low frequency applications, devices with low saturation or ON voltage would show lower losses as measured by the device case temperature and at high frequencies, the fast switchers would run cooler.

AN-861 Power Transistor Safe Operating Area—Special Considerations for Motor Drives

Motor drives present a unique set of safe operating area conditions to power output transistors. Starting with the basics of forward and reverse safe operating area, considerations unique to motor drives are discussed.

EB-66A A Symmetry Correcting Circuit for Use with the MC3420

EB-66 shows a method of implementing an external symmetry-correction circuit with the MC3420 Switchmode Regulator Control IC to insure balanced operation of the power transformer in push-pull inverter configurations.

MC3420/3520 Switchmode Regulator Control Circuit

The MC3520/3420 is an inverter control unit which provides all the control circuitry for PWM push-pull, bridge and series type Switchmode power supplies.

TL494/495 Switchmode Pulse Width Modulation Control Circuits

The TL494 and TL495 combine the best features of existing PWM control circuits and add other on-chip functions. These devices provide, on a single monolithic chip, all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

AUDIO CONTROL CIRCUIT DESIGN

AN-240 SCR Power Control Fundamentals

Relationships of control angle to peak voltage, average voltage, RMS voltage and power are presented in chart form. Time constants for relaxation oscillators are discussed for both DC and AC supplies. These basic form the heart of SCR control.

AN-483B 20 and 30 Watt Power Amplifiers Using Darlington Output Transistors

Use of monolithic power Darlington output transistors can greatly simplify the design of highfidelity amplifiers. Described herein is a 20-Watt amplifier which uses only three transistors, and a 30-Watt amplifier which uses four.

AN-484A Medium-Power Audio Amplifiers

This note describes a basic circuit design approach for audio complementary power amplifiers. Procedures are detailed for the selection of input, driver and output transistors. Both simple and Darlington transistor systems are included. Biasing, thermal considerations, overload protection and power supply information is given extensive treatment.

Design examples, including all circuit values, performance data and and suggested P.C. board layouts, are given for simple tranasistor amplfiers at the 3, 5, 7, 10, 15, 20, 25, and 35 Watt levels. Also included are three amplfiers using Darlington output transistors at the 15, 20, and 25 Watt levels.

AN-485 High-Power Audio Amplifiers with Short-Circuit Protection

This application note describes a recommended circuit approach for high-performance audio amplifiers in the 35-Watt to 100-Watt RMS power range. Circuitry is included which enables the amplifier to operate safely continuously under any load condition including a short.

AN-755 Solid-State Relays for AC Power Control

Solid-State Relays (SSRs) using both SCRs and Triacs are examined in detail. The advantages and disadvantages of SSRs compared with electromechanical relays are discussed. Inductive loads are reviewed and snubbing suggestions made. Parts lists are given for SSRs for voltages of 120 and 240 V rms and currents from 5 to 113 A rms. Also described are circuits to give ac and CMOS compatibility.

AN-766 A Variable Frequency Control for 3Ø Induction Motors

This application note describes a variable variable voltage drive system for three-phase induction motor controls. A survey of possible system configurations and a detailed description of a semi-converter/transistor inverter quasi-square wave drive system are included.

POWER TRANSISTORS

AN-569 Transient Thermal Resistance — General Data and Its Use

Data illustrating the thermal response of a number of semiconductor die and package combinations are given. Its use, employing the concepts of transient thermal resistance and superposition, permit the circuit designer to predict semiconductor junction temperature at any point in time during application of a complex power pulse train.

AN-778 Mounting Techniques for Power Semiconductors

For reliable operation, semiconductors must be properly mounted. Discussed are aspects of preparing the mounting surface, using thermal compounds, insulation techniques, fastening techniques, handling of leads and pins, and evaluation methods for the thermal system.

AN-785 Reverse Bias Safe Operating Area

The rating of high voltage, high speed switching transistors for safe turn-off operations is examined. Clamped inductive turn-off measurements are used to generate a switching RBSOA—reverse bias safe operating area—which can be used in conjunction with load line analysis to assure proper transistor operation. The effects of inductance, temperature, base turn-off conditions and forward base drive on RBSOA are included in the discussion.

EN-101 Verifying Collector Voltage Ratings

Methods of verifying the various voltage ratings given on transistor data sheets are described. Practical test circuits are given and testing problems are discussed. A detailed discussion of the avalanche breakdown mechanism and the significance of various voltage ratings is also included.

AN-828 The Effects of Base Drive Conditions on RBSOA

This application note describes the turn-off stresses placed on high voltage power transistors when used in clamped inductive load switching applications. The effects of off-bias voltage $V_{BE(off)}$, reverse base current I_{B2}, forward base current I_{BE} and temperature on the RBSOA capability and switching speeds are illustrated. Also described is the non-destruct RBSOA test circuit used in generating this data.

AN-845 New Power Bipolars Compare Favorably with FETs for Switching Efficiency

This application note discusses whether Power MOSFETs are more efficient than Bipolars in all or many high voltage switching applications.

AN-873 Understanding Power Transistor Dynamic Behavior—dv/dt Effects on Switching RBSOA—

Power transistor dynamic behavior can be affected to a large extent by dv/dt limitations. A look at the internal workings of the transistor readily shows how these limitations arise. A simple circuit model is developed which reproduces the behavior of power transistors in dv/dt limited modes of operation. Experience with the model gives some guidelines for minimizing dv/dt limitations in practical circuits.

AN-875 Power Transistor Safe Operating Area—Special Considerations for Switching Power Supplies

The purpose of this application note is to take a look at some of the more subtle aspects of how stress imposed by the power supply relates to transistor safe operating area and differentiate those stresses that the transistor can handle from those it cannot. In order to provide a proper foundation, special considerations are preceded with a review of forward bias safe operating area.

AR-119 Dynamic Saturation Voltage — A Designer's Comparison

AR-120 Speeding Up The Very High Voltage Transistor

POWER MOSFETs

TDT-101A

This note describes a circuit for a 60 W, 100 kHz FET switcher with four output voltages, operating from 120 Vac.

TDT-102

This TDT defines how the Motorola MMH0026 Dual MOS Clock Driver and MC14050CP Hex Inverter can serve the drive requirements of TMOS Power MOSFETs.

TDT-103

This design tip discusses some drive considerations of Power MOSFETs which are different from Bipolar Transistors.

TDT-104

This TDT discusses paralleling Power MOSFETs in a very fast, highvoltage, high current switch.

TDT-105

This TDT reviews a typical Designer's data sheet. The Motorola Designer's Data Sheet provides all vital parameters necessary for the engineer who is designing tomorrow's switching circuits.

THYRISTORS

AN-268 Pulse Triggering of Radar Modulator SCR's

Factors involved in dynamic gate triggering are examined and relations of gate triggering characteristics to variations of total current amplifications with gate current are shown.

AN-290B Mounting Procedure for, and Thermal Aspects of, Thermopad Plastic Power Devices.

This application note provides information concerning the handling and mounting of Thermopad Plastic packages, as well as information on some thermal aspects.

AN-293 Theory and Characteristics of the Unijunction Transistor

This note discusses the theory of operation, the important characteristics and the behavior of the unijunction transistor under several operating conditions. In addition, a comparison is made between the different fabrication methods used to construct the UJT. Included is a table explaining UJT nomenclature.

AN-295 Supressing RFI in Thyristor Circuits

Measures taken to supress RFI are shown. Design considerations and examples are explored as well as some solutions to the RFI problem.

AN-466 Circuit Applications for the Triac

This note discusses the basic theory of operation of the triac with control methods and circuit applications. Among the applications included are basic switches, lamp dimmers, motor controls, a heater control, a flasher, a regulator, protective circuits and zero-point switching.

AN-482 Electronic Speed Control of Appliance Motors

This application note discusses the possibilities of controlling several types of induction motors, universal motors and permanent-magnet motors, and includes circuit designs for each. By matching the motor to its electronic control, the designer can obtain a simple and efficient system.

AN-509 True RMS Voltage Regulators

This note describes ac voltage regulators that are ideal for use with electronic and electrical equipment such as lamps and heaters that are highly sensitive to supply voltage. These regulators maintain constant RMS voltage levels for input or load changes.

AN-527 Theory, Characteristics and Applications of the Programmable Unijunction Transistor

This note discusses the characteristics of a programmable unijunction transistor (PUT) and offers comparisons with the Annular unijunction. Also included are several circuits showing the versatility of the PUT.

AN-569 Transient Thermal Resistance—General Data and Its Use

Data illustrating the thermal response of a number of semiconductor die and package combinations are given. Its use, employing the concepts of transient thermal resistance and superposition, permit the circuit designer to predict semiconductor junction temperature at any point in time during application of a complex power pulse train.

AN-780A Applications of the MOC3011 Triac Driver

This note describes methods of applying the MOC3011 optically coupled triac driver to provide simple and effective interfaces from logic or microprocessor systems to ac power systems.

AN-843 A Review of Transients and their Means of Suppression

This note addresses the problem of transient overvoltages which most electronic equipment designs must deal with. Effective transient suppression requires that the impulse energy is dissipated in the added suppressor at a low enough voltage so the capabilities of the circuit or device will not be exceeded.

AN-849 Guide to Thyristor Applications

In this note, significant thyristor characteristics, the basis of their rating, and their relationship to circuit design are discussed.

AN-862 Interfacing Digital Circuits to Thyristor Controlled AC Loads

This note describes the interfacing of triacs with integrated circuit drivers (e.g., logic gates) for the control of ac power loads.

EB-30 Sensitive Gate SCRs — Don't Forget the Gate-Cathode Resistor

In applications of sensitive gate SCRs the gate-cathode resistor, R_{GK} is an important factor. Its value affects, in varying degrees, such parameters as I_{GT}, V_{DRM}, dV/dt, I_H, leakage current, and noise immunity. This bulletin discusses these relationships and gives typical data on the performance of devices in the 2N6236 (4 A) family. Similar relationships can be expected for the 2N5060 (800 mA) family.

EB-103 The MOS SCR, A New Thyristor Technology

With the introduction of the Motorola developed MOS SCR, the circuit designer is now offered a device which has the advantages of the high input impedance and fast turn-on of a power MOSFET and the regenerative, latching action of a thyristor. It is easily driven by low power logic — CMOS in this case — but the driver can be an IC or circuit with pull-down (sinking) capability.

AN-784A Transient Power Capability of Zener Diodes

Because of the sensitivity of semiconductor components to voltage transients in excess of their ratings, circuits are often designed to inhibit voltage surges in order to protect equipment from catastrophic failure. This note discusses the power capability of zener diodes for transient suppression.

7.0

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1.0 **Power Transistors**
1.1 **Index and Cross Reference**
1.2 **Selector Guide**
1.3 **Data Sheets**

2.0 **Thyristors**
2.1 **Index and Cross Reference**
2.2 **Selector Guide**
2.3 **Data Sheets**

3.0 **TMOS Power MOSFET**
Selector Guide

4.0 **Rectifiers**
Selector Guide

5.0 **Regulator and Reference Diodes**
Selector Guide

6.0 **Outline Dimensions/Leadform Options/Mounting Hardware & Techniques**

7.0 **Application Literature**

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